SP1000G series datasheet and user manual

1GSPS logic analyzer and pattern generator

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Contents

SP1000G Series overview

SP1000G series logic analyzers and pattern generators offer in depth analysis of logic signals and protocols with 1GSPS (1ns) timing resolution. External reference clocking (IN and OUT), trigger input and output as well as adjustable threshold and output voltage level make SP1000G series a uniquely powerful laboratory equipment. SP1000G series offer **up to** 54 channels that can be individually configured as input, push-pull outputs or open drain output.

Please refer to ordering information for the exact number of available channels and embedded memory.

Typical applications

SP1000G series logic analyzers and pattern generators are perfectly adapted for demanding applications, where it is required to capture logic signals with the maximum time resolution of 1ns on all channels. As a matter of fact, SP1000G series allow the usage of the maximum number of available channels without any reduction in sampling frequency (for example, SP1054 can capture signals on all 54 channels with 1ns resolution). Typical applications are:

- Automated or manual Semiconductor testing
- Electronic circuits testing and validation
- Embedded systems debugging
- Scientific Research
- Serial protocols analysis, like I2C, SPI, UART or 1-Wire (non exhaustive list)
- ADC diagnostic

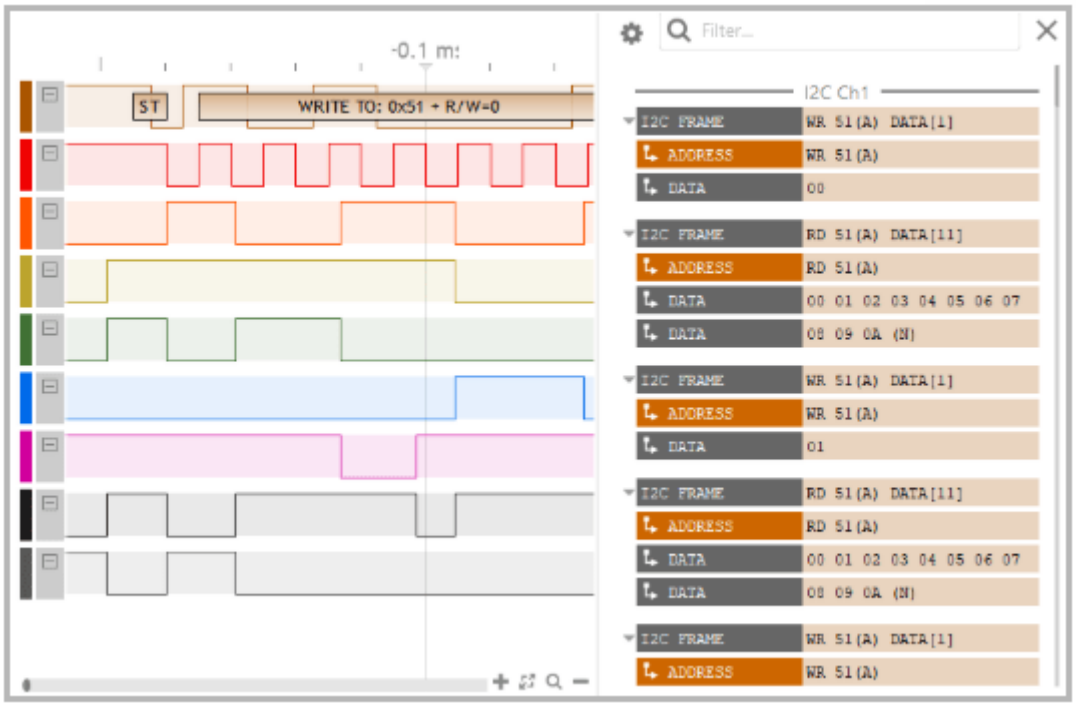

Figure 1: Example of logic signals captured and analyzed by SP1018G logic analyzer

Product highlights

- Schmitt trigger input stages with adjustable thresholds (each group of 9 channels can have a different input threshold).
- 1 GSPS capture rate (adjustable down to 4 MSPS)
- Embedded buffer memory (4Gb, 8Gb or 12Gb depending on model).
- USB3 super-speed interface.
- Samples compression (only events consume memory and USB bandwidth).
- Various trigger options (Edge, pulse width, pattern, protocol).
- Two independent trigger engines that can be combined to create cascaded trigger sequences.
- 250 MSPS pattern generator rate (maximum output frequency is 125MHz).
- 1 continuous clock output per group of 9 channels.
- 1 External sampling clock input (state mode) per group of 9 channels, up to 250MHz.
- Over-voltage protection on all inputs and outputs.
- Precise trigger-In and trigger-Out signals on SMA ports
- 10MHz Reference clock-in and clock-out on SMA ports.

Warning

Read **safety information** section carefully before using this instrument.

SP1000G system architecture

A functional SP1000G measurement system consists of several main components that are presented in the image below.

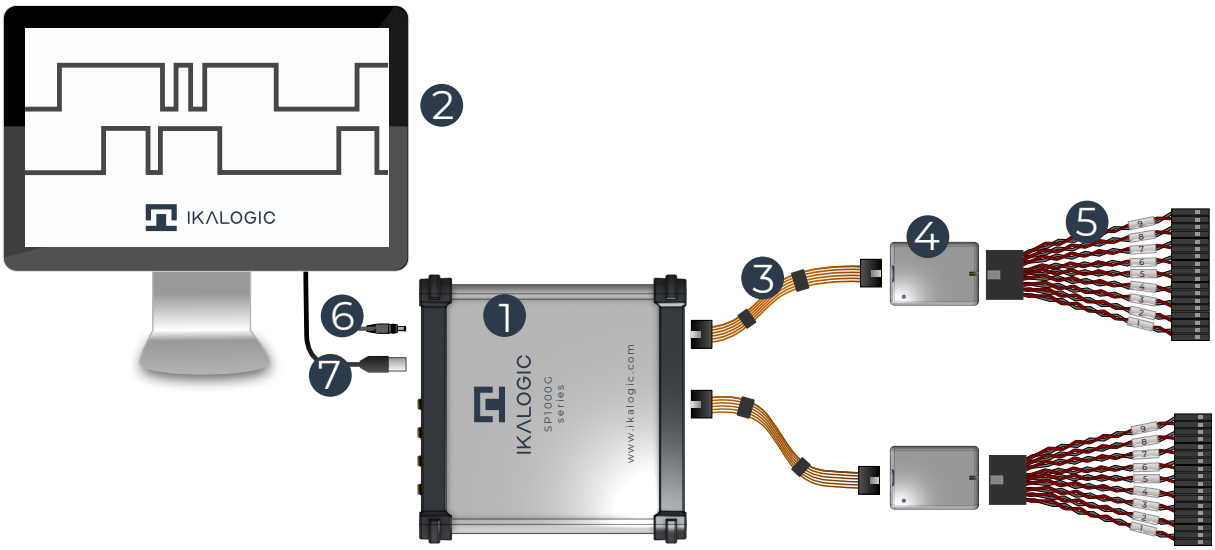

Figure 2: SP1000G system architecture

The main labeled components are:

1. SP1000G main host unit that contains the main memory buffer and the processing power to capture and compress signals before sending them over USB.
2. Computer running ScanaStudio software (Windows / Mac / Linux) that controls the main host unit and display captured signals.
3. Probes to host harness (60 cm): Flexible, high speed (10Gbps) LVDS cable, allowing the probes to be freely positioned near the device under test
4. 9 channels active probe set: High impedance 9 probes set. an SP1000G systems can contain several of those probes.
5. Probes terminations (signal capture points): Special 0.1 inch pair of terminations (signal + ground) including a resistor placed near the free end of the probe for improved signal integrity and to minimize the loading of measured signal.
6. 12VDC power supply
7. USB3 Cable

Main characteristics

Operating conditions

Room Temperature	10°C to 35°C
Relative humidity	< 80% non condensing
Altitude	< 2000m

Timing and measurements[1]

Sampling rate (MAX.)	1000 MSPS
Internal timebase	Yes, 10MHz feeds internal PLL
External timebase input	Yes, via SMA connector
External timebase output	Yes, via SMA connector
External clock timebase (Typical)	10MHz (max 25 ppm [2])
External state mode clock Max rate	250 MHz
Logic Inputs digital bandwidth	250 MHz
Trigger output	Yes, via SMA connector
External trigger input	Yes, via SMA connector

Active probes set specifications (input mode) [3]

Number of channels per probes set	9
Input impedance (Input mode)	10 KΩ|| 5 pF (preliminary)
Threshold circuits	1
Adjustable capture threshold	0V to 3.0V with 10mV resolution
Adjustable pattern generator voltage	0V to 5.0V with 10mV resolution
Compatible logic level	0.9V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V

[1] DDR-3 sampling memory is used to buffer samples before streaming to host computer.
[2] External timebase is tested up to 25ppm stability. System operation is not guaranteed beyond this limit.
[3] An SP1000G device have several probes set, each probe set providing 9 channels. Check ordering information to see how many probes set are available for a specific SP1000G device.

Absolute max voltage on digital inputs (Continuous or Transient)	± 10 V

Power requirements

Input power connector	5mm / 2.1mm DC Jack (positive center)
Input current (SP1000G)	3 A
Input voltage	12V V ± 1 V
Protection	Overvoltage (up to 25V), overcurrent, back-powering.

Note: A suitable 220V/110V to 12V power supply is provided with each product.

SP1000G Interfaces

As described in the architecture chapter, SP1000G device is composed of two main elements, the host device containing all the acquisition hardware (FPGA, memory buffer, USB interfaces) and the active probes sets containing all signal conditioning, ESD protection, Input/Output buffers and level shifting. Each active probe connects to the host device using a flexible harness of high speed twinax cables, ensuring perfectly predictable propagation delay and timing alignment between all channels.

SP1000G host device interfaces

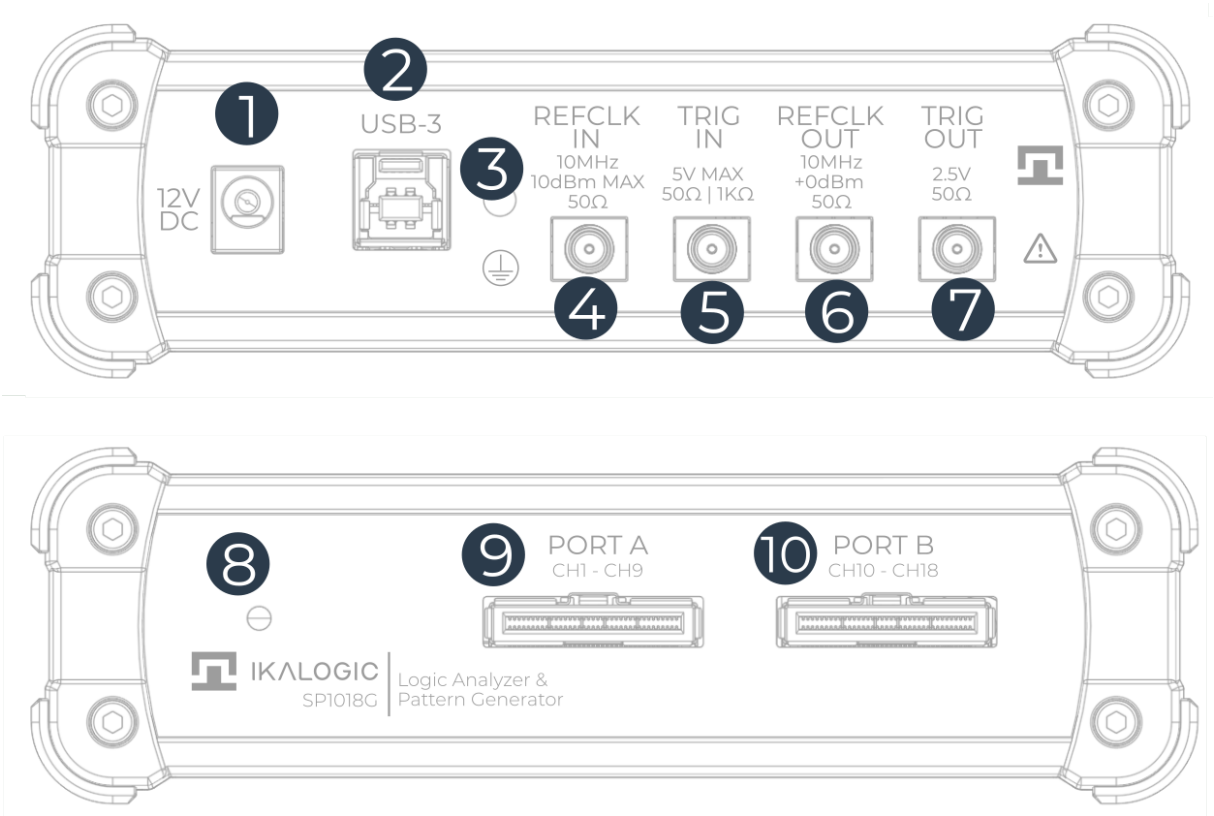

Figure 3: SP1000G Logic Analyzer and pattern generator interfaces

1. 12V DC power input
2. USB3 port (Type B)
3. 3 Earth connection (M3 thread size)
4. 10MHz Reference clock input (optional) - 50 Ohm impedance
5. Trigger input - 50 Ohm impedance
6. Reference clock output
7. Trigger clock output
8. Status LED
9. Port A (connection to 9-channels active probe set)
10. Port B (connection to 9-channels active probe set)

SP1018G, SP1036G and SP1054G

All SP1000G series logic analyzers have similar architectures. The main difference is the number of active probes that can be connected. As an example, below is the front view of an SP1054G device,

showing the connectors for the maximum 6 probes that can be connected to it.

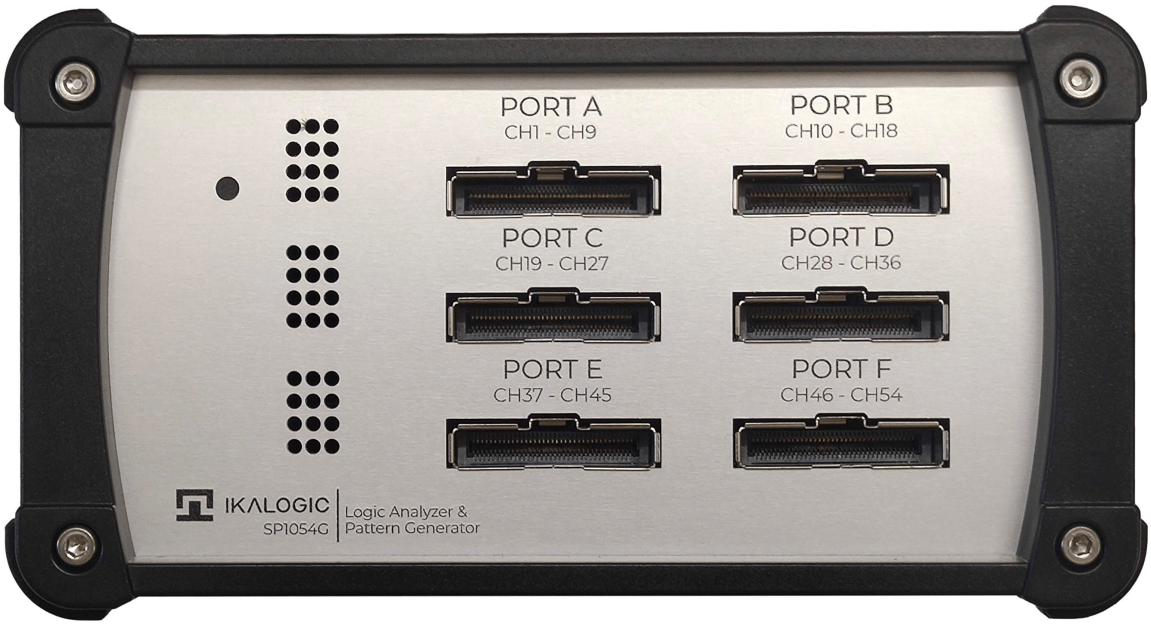

Figure 4: SP1054G Logic Analyzer and pattern genrator front view

Active probe set interfaces

Figure 5: SP1000G Series Active probe interfaces

1. Connection to host device
2. Status LED

3. Connection to device under test (9 measurement channels + individual GND connections per channel)

Principle of operation

SP1000G Series logic analyzers connect to a computer via a USB-3 cable. A free software - called ScanaStudio - is used to configure the device, display captured signals, build patterns and control the pattern generator. The software can also be used to further analyze the captured samples by decoding protocols like I2C, SPI or UART. A versatile scripting system allows sophisticated features and add-ons.

It is highly recommended to download the software to familirize with all its various features. A demonstration mode allows the user to simulate full device operation without connecting a physical SP1000G device to the computer.

Embedded memory vs streaming

USB based logic analyzers (ones that don't have a display and rely on a computer for that matter) usually operate according to one of two schemes:

- Using an **embedded memory** to store captured samples. Samples are later downloaded at a slower speed via the USB interface. This has the advantage of not being limited by USB transfer rate, but has the disadvantage of limited embedded memory.
- **Streaming** captured samples over the USB connection, at the maximum possible speed. While this offers the advantage of a virtually unlimited memory (only limited by host computer's memory), it has the disadvantage of limiting the sampling rate to USB's throughput.

SP1000G combines the advantages of both streaming and embedded memory techniques, while implementing novel compression algorithms, to optimize the usage of memory and bandwidth. Samples are analyzed and compressed before being stored in an embedded DDR-3 memory (4Gb, 8Gb, or 12Gb depending on the model). At the same time, a superspeed USB-3 interface transfers the data to the computer, effectively emptying the embedded memory and making more room for new samples. This results in a logic analyzer that can capture hours of logic signals activity on all channels at 1 GSPS, overcoming any bandwidth limitations related to the user's computer or USB interface.

Clocking architecture

SP1000G offers versatile clocking system to adapt to various measurement setups. The diagram below shows a simplified overview of the clocking architecture.

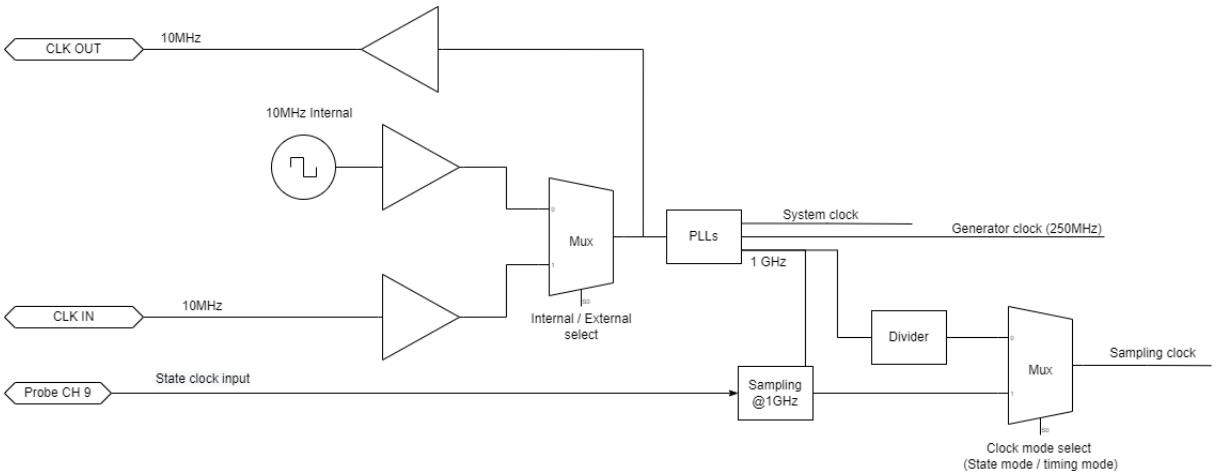

Figure 6: SP1000G simplified clocking architecture block diagram

Timebase

SP1000G Series offer a variety of clocking strategies and options. SP1000G can use as a timebase:

- Internal 10MHz clock (default operation)
- External 10MHz clock

In both cases, the 10MHz timebase is fed to an internal low jitter PLL that generates sampling frequency (for both capture and generator).

Additionally, SP1000G will constantly output a 10MHz timebase on SMA connector.

Please see interfaces chapter for more information about the specific SMA ports for connecting external clocks.

State mode

SP1000G allows the 9th channel of each active probe (group of 9 channels) to be used as a state mode clock input. (For example, the SP1018G, which has 18 channels, have two state mode clock inputs). Only one state mode input can be used in the same time.

Continuous output clock

SP1000G can be used to generate arbitrary pattern. Those patterns can be loaded and generated as chunks, with interruptions between two chunks. Those interruptions can be problematic for clock signals (in case they are feeding a PLL, a micro-controller, or other sensitive application). For that

particular reason, each active probe set in SP1000G offer a continuous output clock option. This special channel can either be used as any other channel, or it can be used to output a continuous clock. By saying continuous, it is implied that the clock is not interrupted between chunks.

Versatile trigger system

SP1000G offers a variety of triggering options, ranging from simple edge trigger, to complex protocol based triggering. An external trigger input can be fed to the device. Additionally, SP1000G can generate a trigger output pulse to synchronize other instruments.

SP1000G trigger system is composed of two well proven FlexiTrig®trigger engines, each FlexiTrig engine can be used in one of those modes:

- Edge trigger
- Pulse trigger (with minimum and maximum pulse width)
- Timed logic sequence
- Protocol based trigger (e.g. I2C bus address or serial UART character)
- External trigger source

Furthermore, the two trigger engines (called A and B hereafter) can be cascaded in one of the following modes:

- A then B (Wait until A triggers then arm B trigger engine)
- B then A
- A and B (Trigger engines A and B must trigger, but in any order)
- A or B (whoever triggers first)

Finally, an external trigger output is always active, in all modes and generates a trigger pulse whenever a trigger condition is met and a capture starts. Signal specifications for External trigger input and output are detailed in the following section.

External trigger OUT specifications

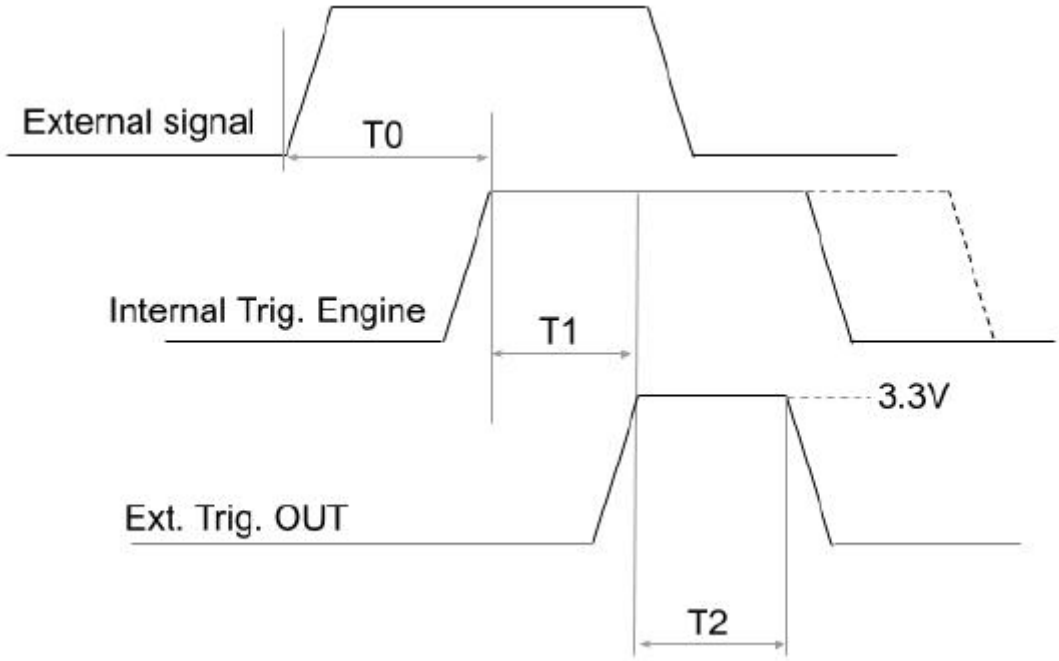

Figure 7: External trigger OUT timings

There is an internal data path delay before external signals reach internal trigger engine and go through internal state machines (T0). When trigger event occurs, a 10ms pulse is generated on the Trig Out port (T2 = 10ms). This port has a 50 Ωseries impedance allowing easy interfacing to 50 Ωinput devices. This can be used to synchronise the capture with other equipment like an oscilloscope. Polarity of the trigger can be set in software (rising or falling edge). There is also a delay (T1) between internal trigger detection and Trig Out assertion on SMA port. Therefore, the total time for an external event to generate a Trigger OUT pulse is T0+T1.

The timings below have been measured at 1GHz sampling rate:

Parameter	Value
T0	150 ns $\pm$ 1ns
T1	20 ns $\pm$ 4ns
T2	10ms $\pm$ 4ns

External trigger IN specifications

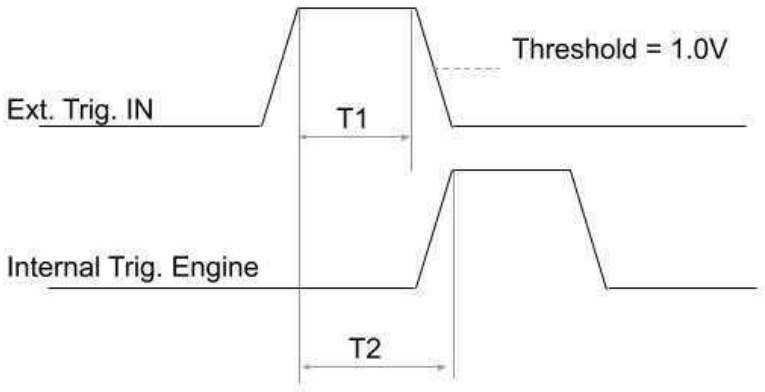

Figure 8: External trigger input specification

The Trig In port allows to start acquisition on an external event generated by another instrument. The minimum pulse width (T1) is 2ns . Polarity can be set in software, as well as the logic-high threshold (1.0V by default, adjustable from 0.0V to 2.5V). The input impedance is also software selectable (100k Ωor 50 Ω). T2, the time between external trigger in active edge and internal trigger engine assertion is 150ns (measured when sampling rate is set 1GHz).

Active probes

Actives probes are used to interface the device under test and main SP1000G host device. The active probes are independent units that can be detached from the system and replaced. It's important to note that the active probe defines the exact input/out characteristics, as well as the bandwidth limit of the digital signals being sampled.

SP1000G series come with several active probes (standard active probes) depending on the model:

- SP1018G: 2 actives probes sets (18 channels)
- SP1036G: 4 actives probes sets (36 channels)
- SP1054G: 6 actives probes sets (54 channels)

Custom probes for specific applications can be designed upon request (e.g. Active probes with RS485, CAN, LIN or other industrial interfaces).

Equivalent schematic of 1 channel (standard active probe)

The standard active probe has full capture and generation capabilities. The following bloc diagram shows a simplified architecture for 1 channel.

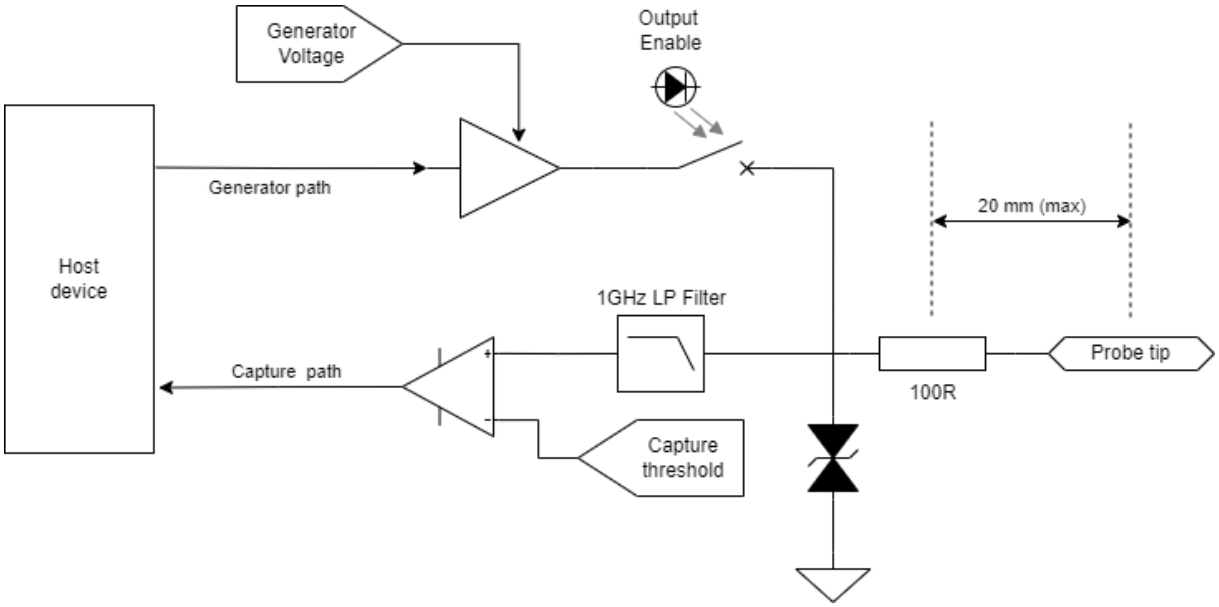

Figure 9: active probe simplified diagram

What's in the box

SP1000G series is shipped with the following items:

1. SP1000G host device
2. USB 3 cable
3. Power supply
4. SMA anti-dust covers

5. Active probe sets
6. Probes terminations
7. Probe to host-device harness.

The number of probes set and probes terminations depend on the device.

Unpacking and first usage

We recommend the user to start by identifying all the different components that are provided. To turn ON the SP1000G device, connect it to to a power source using the provided power supply and to a free USB-3 port of your computer using the provided USB cable[4]. The LED should glow according to the table in the “Status LEDs behavior” section. To switch off the device, simply disconnect the power and USB cables.

Host status LEDs behavior

Status led can be in one of 3 states:

Status LED	Meaning
Red fix	Device is booting (this should last approx 15 seconds after being powered up)
Green fix	Device ready.
Fushia	Waiting for trigger.
Blue blinking	Capturing signals.
Red blinking	Device hardware fault.

Active probe LED behavior

Status LED	Meaning
Green fix	Probe powered up.
Green blinking	Logic activity detected on one ore more channels.

[4] Do not connect SP1000G device to anything else than a computer’s USB port. Never connect the SP1000G device to a USB charging adaptor.

Status LED	Meaning
Red blinking	Hardware fault.

Software Quick Start guide

Start by downloading the latest version of ScanaStudio software www.ikalogic.com and following instructions to install both software and provided drivers. It is recommended to restart your computer after the software and drivers have been installed.

Once the software is installed, run it, and create a new workspace by selecting SP10xxG as the device type. (replacing xx with the correct model depending on your device).

Note: if at this point the device is not recognized by your computer, the ScanaStudio workspace is created as a demo workspace, please follow these steps:

- Ensure the device is connected to a functionnal USB-3 port. A USB-2 port is not supported.
- Try switching to another machine if one is available.
- If all of the above fails, please contact Ikalogic support.

Capturing your first signal

To capture your first logic signals, please follow these steps:

1. Connect the device via USB-3 and to provided power plug.
2. Launch ScanaStudio and create a workspace.
3. Connect the probes to your signals source.
4. Ensure at least oneground probe is connected to the ground of your system being tested.
5. Hit the start button in ScanaStudio and wait until signals are captured and displayed on the screen.

You can adjust the capture duration by adjusting the number of samples in the device configuration tab.

Mechanical data

All SP1000G series host devices casing are manufactured from extruded aluminum, able to withstand heavy duty usage in various harsh environments.

Host device model SP1018G

Weight: 500 gm ± 10 gm

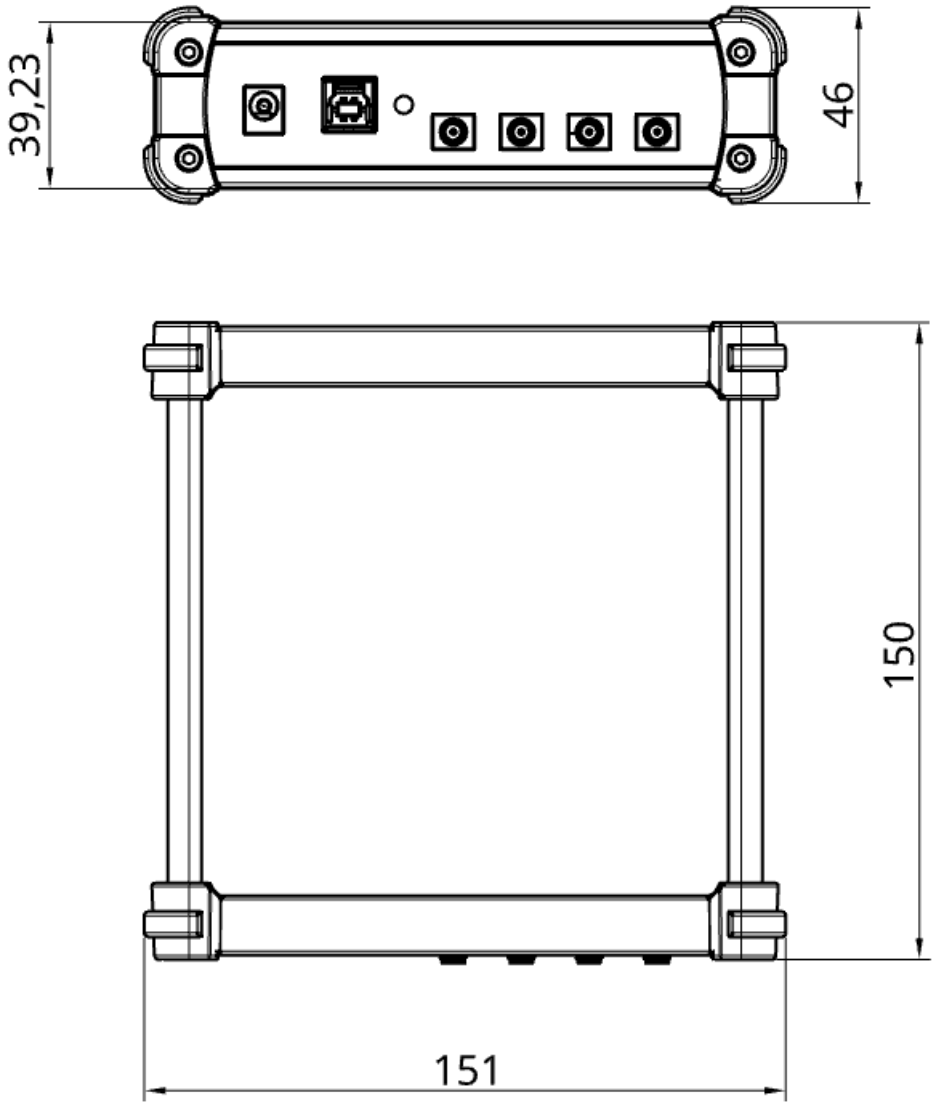

Figure 10: SP1018G Host device dimensions (mm)

Host device models SP1036G and SP1054G

Weight for SP1036G : 680 gm ± 10 gm Weight for SP1054G : 790 gm ± 10 gm

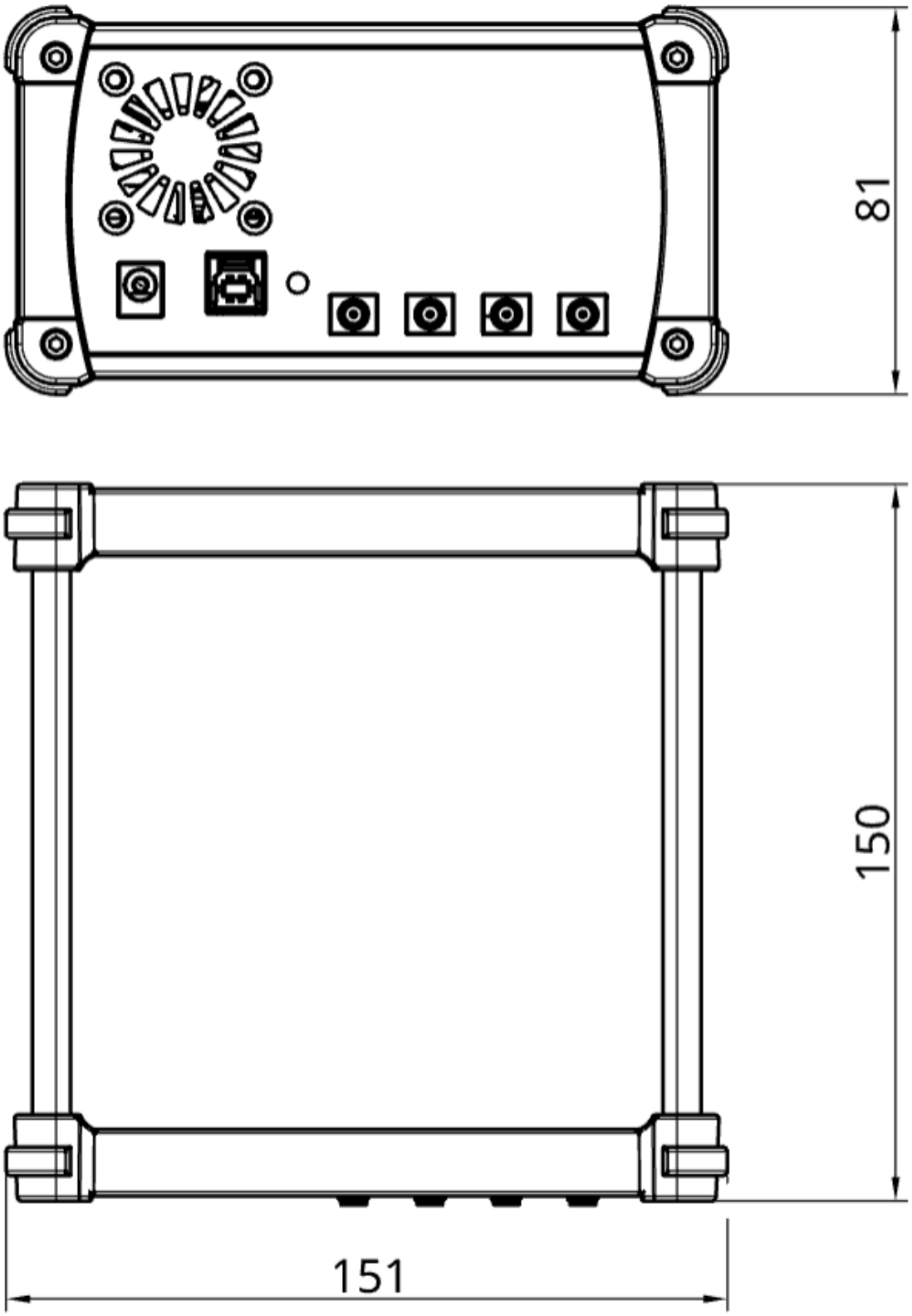

Figure 11: SP1036G and SP1054G dimensions (mm)

Active probe set

Weight: 40 gm ± 1 gm

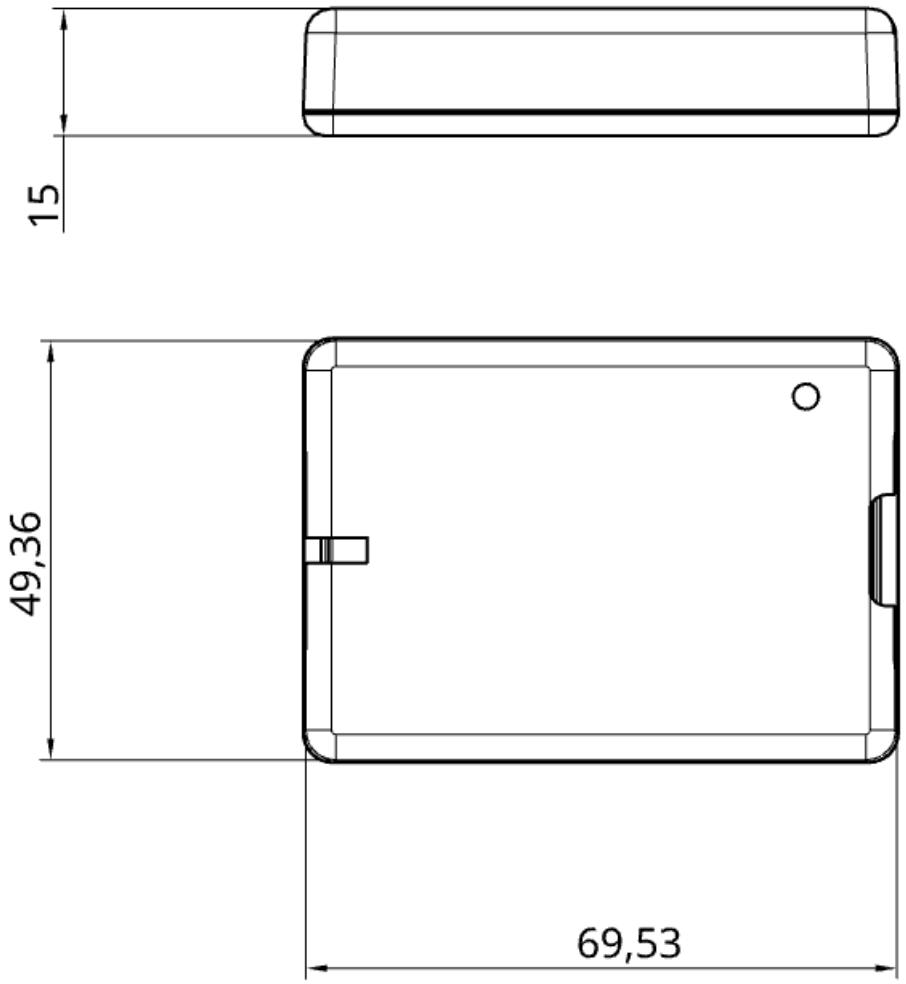

Figure 12: Active probe set dimensions (mm)

Probes terminations

Probes termination cables are made of 24AWG flexible wire pairs (GND + signal).

All GND wires are black colored, and signal wires are red colored. Every signal wire has a white marking tube with the channel number (e.g. “1”) and a colored sticker on the probe tip.

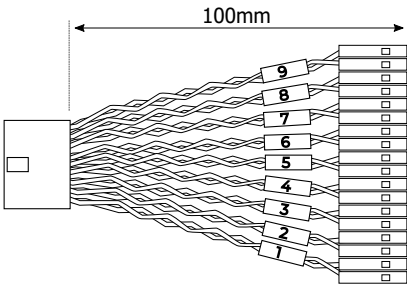

Figure 13: SP1000G probes terminations dimensions (mm)

Software technical requirements

Download ScanaStudio software on www.ikalogic.com so you can use your device on your favorite platform. SP1000G and ScanaStudio were tested to supports the following platforms:

- Windows 7/8/10
- Mac OS support expected in March 2023
- Ubuntu support expected in March 2023

Ordering information

All devices in SP1000G series offer similar functionalities, the only difference between different versions in the SP1000G family is the number of channels and embedded memory buffer.

Product reference	Number of active probes sets	Total number of Channels	Total Embedded memory (Gb)
SP1018G	2	18	4
SP1036G	4	36	8
SP1054G	6	54	12

For purchasing, please check for nearest distributor on www.ikalogic.com or contact us for any inquiry at contact@ikalogic.com.

Accessories, maintenance and customer support

Accessories and maintenance services (probes replacement) are available on our website: www.ikalogic.com or by contacting customer support (support@ikalogic.com).

Certifications and regulations

This device complies with the following applicable European Directives: Electromagnetic Compatibility (EMC) Directive 2004/108/EC, Low-Voltage Directive 2006/95/EC, IEC 61326-2.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

CAN ICES-3 (B) / NMB-3 (B)

RoHS Compliant 2011/65/EC. This device does not contain any of the substances in excess of the maximum concentration values (“MCVs”) defined in the EU RoHS Directive.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Safety information

This product complies with safety standards IEC NF/EN 61010-1: 2010, IEC NF/EN 61010-2-030 and UL 61010-1: 2015 To prevent possible electrical shock, fire, personal injury, or damage to the product, read all safety information before you use the product. The following international symbols are used on the product and in this manual.

Symbols definitions

Figure 14: Risk of Danger. Important information. See Manual.

Figure 15: WEEE logo. This product complies with the WEEE Directive (2002/96/EC) marking requirements. The affixed label indicates that you must not discard this electrical/electronic product in domestic household waste. Product Category: With reference to the equipment types in the WEEE Directive Annex I, this product is classed as category 9 Do not dispose of this product as unsorted municipal waste.

Figure 16: CE Logo. Conforms to European Union directives.

Important safety notes

Warning, to avoid electrical shock or fire:

- Carefully read all instructions.
- Use the product only as specified, otherwise the protection supplied by the product can be compromised.

- Do not use the product if it operates incorrectly.
- Before use, inspect device casing, probes, test leads and accessories for mechanical damage and replace if damaged.
- Never attempt to repair a defective device. Contact after-sale service.
- Do not use the product or its accessories in case of any damage.
- Remove all probes, test leads and accessories that are not in use.
- Never use the device for measuring mains circuits.
- Never use the device for measuring circuits which are not isolated from mains.
- Do not touch electrical wires with bare hands.
- Keep away from children's sight or from animals.
- Do not expose to water, heat or moisture.
- The device's ground connection through the USB cable is for measurement purposes only. The logic analyzer does not have a protective safety ground.
- Ensure there is no significant voltage between device ground and the point to which you intend to connect it.
- Do not apply more than the rated voltage (±25V), between the terminals or between each terminal and ground.
- Do not apply input voltages above the rating of the instrument (±25V).
- Measure a known voltage first to make sure that the product operates correctly.
- Do not work alone.
- Comply with local and national safety codes. Use personal protective equipment (approved rubber gloves, face protection, and flame resistant clothes) to prevent shock.
- Do not use the device in wet or damp conditions, or around explosive gas or vapor.
- Do not operate the product with covers removed or the case open. Hazardous voltage exposure is possible.
- Do not use in a system in which the failure of the product might result in personal injury.

Limited warranty & limitation of liability

Each Ikalogic product is warranted to be free from defects in material and workmanship under normal use and service. The warranty period is three years for the test tool and two year for its accessories. This warranty extends only to the original buyer or end-user customer of an Ikalogic authorized reseller, and does not apply to fuses, disposable batteries or to any product which, in Ikalogic's opinion, has been misused, altered, neglected or damaged by accident or abnormal conditions of operation or handling.

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EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IKALOGIC SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES OR LOSSES, INCLUDING LOSS OF DATA, WHETHER ARISING FROM BREACH OF WARRANTY OR BASED ON CONTRACT, TORT, RELIANCE OR ANY OTHER THEORY. Since some countries or states do not allow limitation of the term of an implied warranty, or exclusion or limitation of incidental or consequential damages, the limitations and exclusions of this warranty may not apply to every buyer. If any provision of this Warranty is held invalid or unenforceable by a court of competent jurisdiction, such holding will not affect the validity or enforceability of any other provision.

Document Revisions

22-Jan-2023	Updated information about SP1036G and SP1054G
10-March-2022	Initial release of this document.

The information in this document is subject to change without notice.