

Universal Evaluation Board for Triple, High Speed Op Amps Offered in 14-Lead TSSOP Packages

FEATURES

- Enables quick breadboarding/prototyping**
- User-defined circuit configuration**
- Edge-mounted SMA connector provisions**
- Easy connection to test equipment and other circuits**
- RoHS compliant**

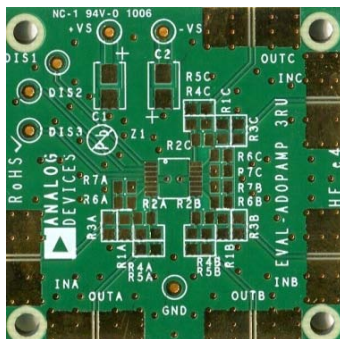
GENERAL DESCRIPTION

The Analog Devices, Inc., EB-O14RU-3Z universal evaluation board is designed to help users evaluate triple, high speed op amps offered in 14-lead TSSOP packages. The EB-O14RU-3Z is a bare board (that is, there are no components soldered to the board) that enables users to quickly prototype a variety of triple op amp circuits, which minimizes risk and reduces time to market. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side of the bare evaluation board.

The 2-layer evaluation board accepts SMA edge-mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry. The ground plane, component placement, and supply bypassing are designed to minimize parasitic inductance and capacitance.

Figure 3 shows the evaluation board schematic. The PCB assembly drawings are shown in Figure 4 and Figure 5. The layout patterns for the PCB are shown in Figure 6 and Figure 7.

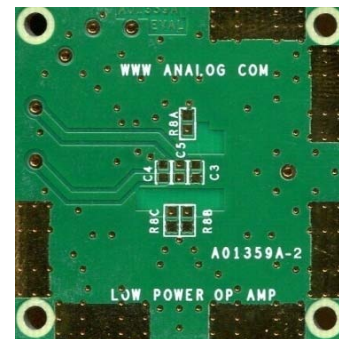
EVALUATION BOARD, COMPONENT SIDE AND CIRCUIT SIDE



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 1. Component Side of Evaluation Board

081522-001



NOTES
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 2. Circuit Side of Evaluation Board

081522-002

TABLE OF CONTENTS

| | | | |
|---|---|--|---|
| Features | 1 | Evaluation Board Schematic, Assembly Drawings, and Layout Patterns..... | 3 |
| General Description | 1 | Ordering Information..... | 5 |
| Evaluation Board, Component Side and Circuit Side | 1 | Bill of Materials..... | 5 |
| Revision History | 2 | | |

REVISION HISTORY

4/10—Revision 0: Initial Version

EVALUATION BOARD SCHEMATIC, ASSEMBLY DRAWINGS, AND LAYOUT PATTERNS

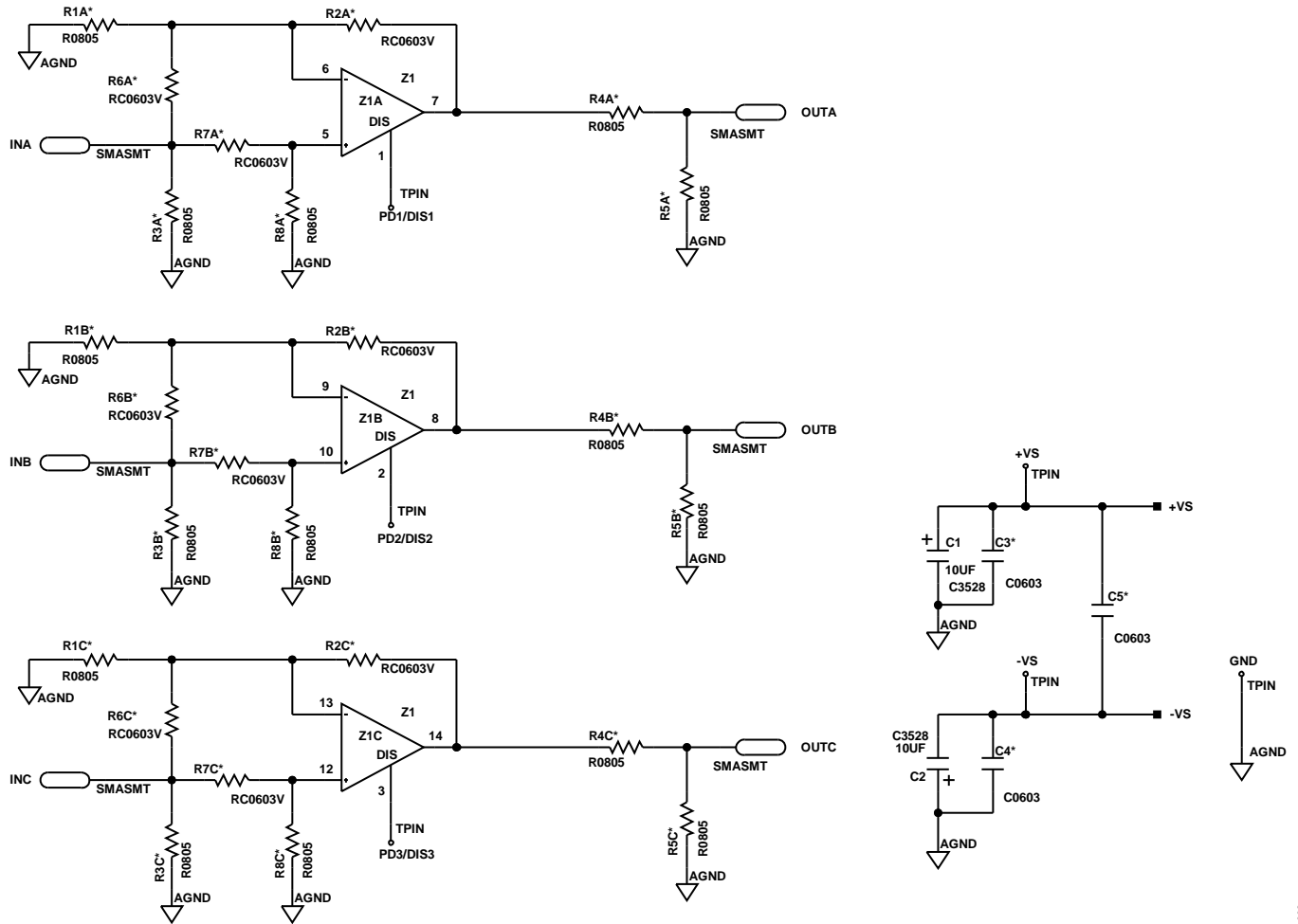


Figure 3. Universal Evaluation Board Schematic

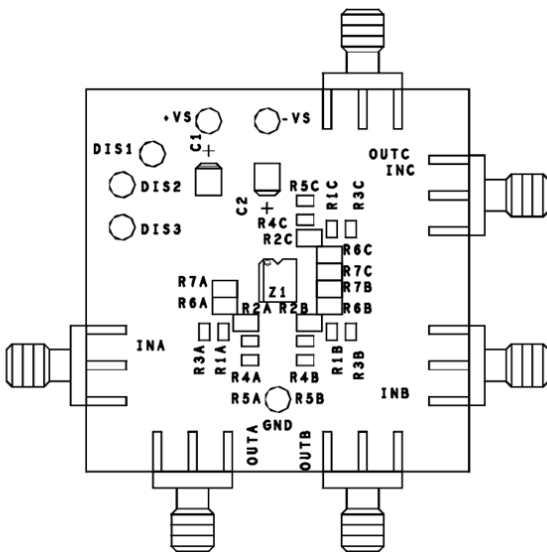


Figure 4. Component Side Assembly Drawing

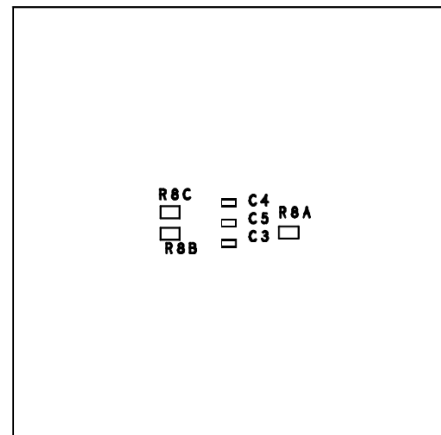


Figure 5. Circuit Side Assembly Drawing

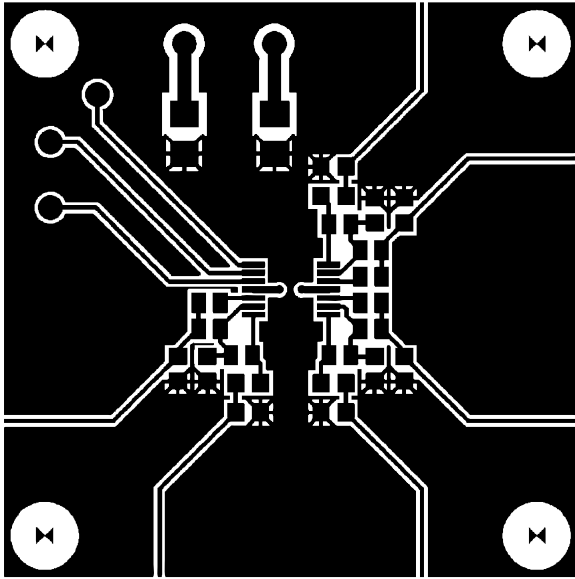


Figure 6. Component Side Layout Pattern

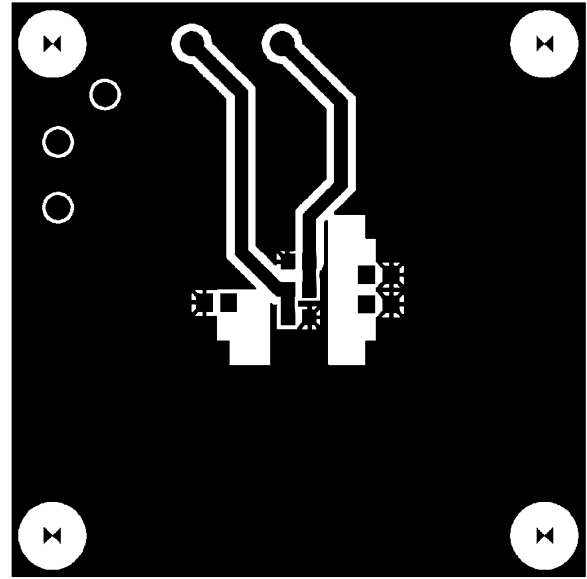


Figure 7. Circuit Side Layout Pattern

ORDERING INFORMATION**BILL OF MATERIALS**

Table 1.

| Quantity | Reference Designator | Description | Package |
|----------|--|-------------------------|---------------|
| 6 | +VS, -VS, PD1/DIS1, PD2/DIS2, PD3/DIS3, GND | Connectors | TP1 |
| 2 | C1, C2 | 10 μ F | 3528 |
| 3 | C3, C4, C5 | Capacitor, user defined | C0603 |
| 6 | INA, INB, INC, OUTA, OUTB, OUTC | SMA SMT | SMA SMT |
| 15 | R1A, R1B, R1C, R3A, R3B, R3C, R4A, R4B, R4C, R5A, R5B, R5C, R8A, R8B, R8C | Resistor, user defined | R0805 |
| 9 | R2A, R2B, R2C, R6A, R6B, R6C, R7A, R7B, R7C | Resistor, user defined | R0603 |
| 1 | DUT | Amplifier | 14-lead TSSOP |

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**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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