ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE834 & NTE834SM
Integrated Circuit
Low Power Low Offset Voltage Comparator

Description:

The NTE834 and NTE834SM are precision voltage comparators designed to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also has a unique characteristic in that the input common−mode voltage range includes GND, even though operated from a single power supply voltage.

Features:

- Wide Single Supply Voltage Range: 2V to 36V
- Very Low Supply Current Drain: 0.8mA Typ
- Low Input Biasing Current: 25nA
- Low Offset Voltage: ±3mV
- Low Input Offset Current: ±5nA
- Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems
- Available in Standard 14−Lead DIP (NTE834) and Surface Mount SOIC−14 (NTE834SM)

Applications:

- Limit Comparators
- Simple Analog to Digital Converters
- Pulse, Squarewave, and Time Delay Generators

Absolute Maximum Ratings:

Supply Voltage, V^+ . . . . . 36V or ±18V
Differential Input Voltage . . . . . ±36V
Input Voltage . . . . . −0.3V to +36V
Power Dissipation (Note 1), P_D 775mW
Derate above +25°C . . . . . 6.2mW/°C
Output Short−Circuit to GND (Note 2) . . . . . Continuous
Input Current (V_{IN} < −0.3V, Note 3) 50mA
Operating Temperature Range, T_{opr} . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (Soldering, 10 seconds), T_L . . . . . +300°C

Electrical Characteristics: (V^+ = 5V, −55°C ≤ T_A ≤ +125°C, unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	T_A = +25°C, Note 6	−	±2.0	±5.0	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = +25°C, Note 4	−	25	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = +25°C	−	±5.0	±50	nA
Input Common−Mode Voltage Range	T_A = +25°C, Note 5	0	−	V^+ −1.5	V
Supply Current	R_L = ∞ on all Comparators, T_A = +25°C	−	0.8	2.0	mA
Voltage Gain	R_L ≥ 15kΩ, V^+ = 15V (To Support Large V_O Swing), T_A = +25°C	−	200	−	V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C	−	300	−	ns
Response Time	V_{RL} = 5V, R_L = 5.1kΩ, T_A = +25°C	−	1.3	−	μs
Output Sink Current	$V_{IN(-)}$ ≥ 1V, $V_{IN(+)}$ = 0, V_O ≤ 1.5V, T_A = +25°C	6.0	16	−	mA
Saturation Voltage	$V_{IN(-)}$ ≥ 1V, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA, T_A = +25°C	−	250	400	mV
Output Leakage Current	$V_{IN(+)}$ ≥ 1V, $V_{IN(-)}$ = 0, V_O = 5V, T_A = +25°C	−	0.1	−	nA
Input Offset Voltage	Note 6	−	−	9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$	−	−	±150	nA
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range	−	−	400	nA
Input Common Mode Voltage Range		0	−	V^+ −2.0	V
Saturation Voltage	$V_{IN(-)}$ ≥ 1V, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA	−	−	700	mV
Output Leakage Current	$V_{IN(+)}$ ≥ 1V, $V_{IN(-)}$ = 0, V_O = 30V	−	−	1.0	μA
Differential Input Voltage	All V_{IN}'s ≥ 0V (or V−, if used)	−	−	36	V

Note 1 For operating at high temperatures, these devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered to a printed circuit board, operating in ambient still air. The low bias dissipation and the "ON−OFF" characteristic of the outputs keeps the chip dissipation very low (P_D ≤ 100mW), provided the output transistors are allowed to saturate.

Note 2 Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V^+.

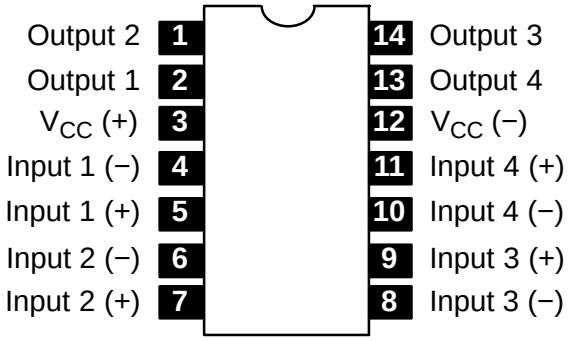
Note 3 This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector−base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps.

Note 4 The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference to input lines.

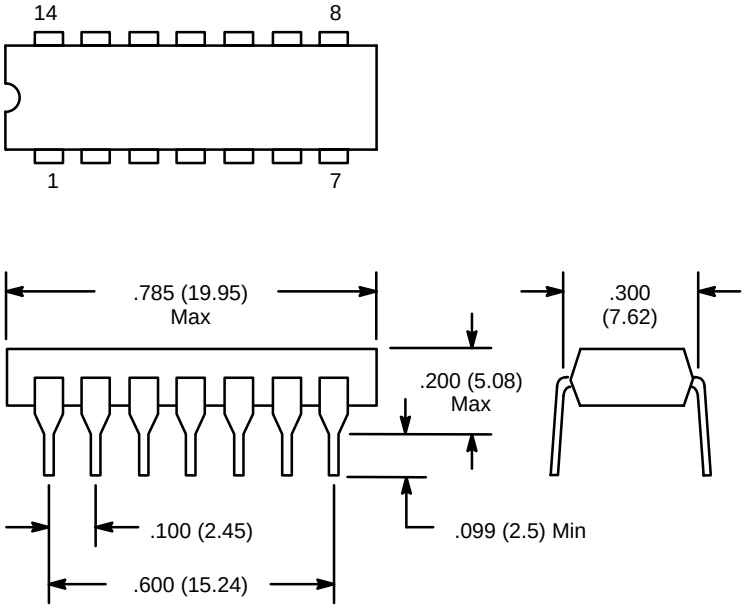
Note 5 The input common−mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common−mode voltage range is V^+ −1.5V, but either or both inputs can go to +30V without damage.

Note 6. At output switch point, $V_O \cong$ 1.4V, R_S = 0Ω with V^+ from 5V; and over the full input common−mode range (0V to V+ − 1.5V).

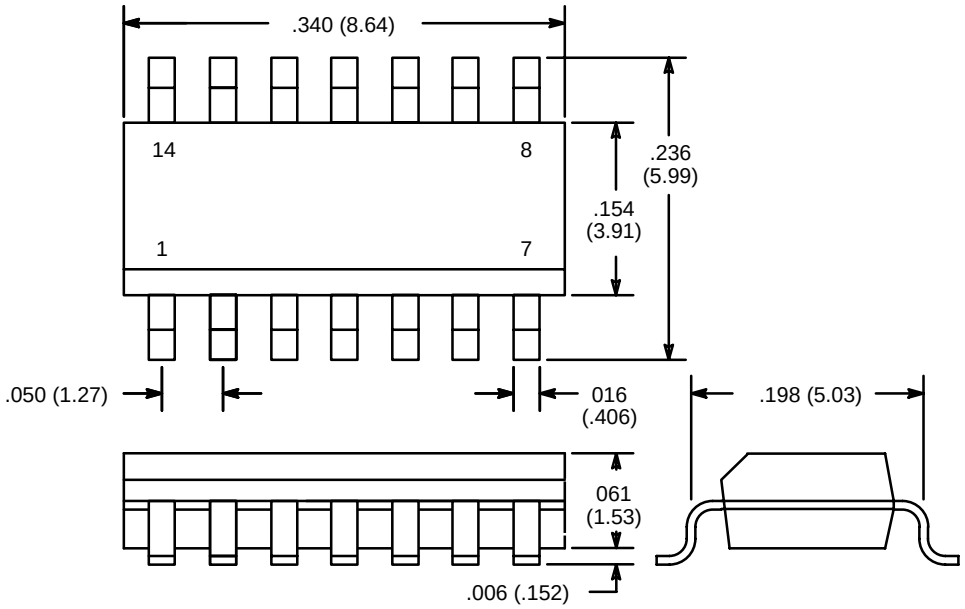
Pin Connection Diagram



NTE834 (14−Lead DIP)



NTE834SM (SOIC−14)



NOTE: Pin1 on Beveled Edge