ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE56051 & NTE56052
TRIAC, 8A Low Logic Level

Description:

The NTE56051 and NTE56052 are glass passivated, Low Logic Level TRIACs in a TO220 type package designed for use in general purpose bidirectional switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits, and other low power gate trigger circuits.

Absolute Maximum Ratings:

Repetitive Peak Off–Sate Voltage (Note 1), V_{DRM}
- NTE56051 . . . . . 500V
- NTE56052 . . . . . 600V

RMS On–State Current (Full Sine Wave, $T_{MB} \le 102°C$), $I_T(RMS)$ 8A

Non–Repetitive Peak On–State Current, I_{TSM}
(Full Sine Wave, T_J = +125°C prior to Surge, with Reapplied V_{DRM}max)
- t = 20ms 55A
- t = 16.7ms 60A

I^2t for Fusing (t = 10ms), I^2t . . . . . $15A^2sec$

Repetitive Rate–of–Rise of On–State Current after Triggering, dI_T/dt
(I_{TM} = 12A, I_G = 0.2A, dI_G/dt = 0.2A/μs)
- MT_2 (+), G (+) 50A/μs
- MT_2 (+), G (–) 50A/μs
- MT_2 (–), G (–) 50A/μs
- MT_2 (–), G (+) 10A/μs

Peak Gate Current, I_{GM} 2A

Peak Gate Voltage, V_{GM} 5V

Peak Gate Power, P_{GM} 5W

Average Gate Power (Over Any 20ms Period), $P_{G(AV)}$ 500mW

Operating Junction Temperature, T_J . . . . . +125°C

Storage Temperature Range, T_{stg} . . . . . –40° to +150°C

Thermal Resistance, Junction–to–Mounting Base, R_{thJMB}
- Full Cycle 2.0K/W
- Half Cycle 2.4K/W

Typical Thermal Resistance, Junction–to–Ambient, R_{thJA} 60K/W

Note 1. Although not recommended, off–state voltages up to 800V may be applied without damage, but the TRIAC may switch to the on–State. The rate–of–rise of current should not exceed 6A/μs.

Electrical Characteristics: (T_J = +25°C unless otherwise specfied)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static Characteristics						
Gate Trigger Current MT_2 (+), G (+)	I_{GT}	V_D = 12V, I_T = 0.1A	–	2.5	5	mA
MT_2 (+), G (–)			–	3.5	5	mA
MT_2 (–), G (–)			–	3.5	5	mA
MT_2 (–), G (+)			–	6.5	10	mA
Latching Current MT_2 (+), G (+)	I_L	V_D = 12V, I_T = 0.1A	–	1.6	15	mA
MT_2 (+), G (–)			–	8.5	20	mA
MT_2 (–), G (–)			–	1.2	15	mA
MT_2 (–), G (+)			–	2.5	20	mA
Holding Current	I_H	V_D = 12V, I_T = 0.1A	–	1.5	10	mA
On–State Voltage	V_T	I_T = 5A	–	1.4	1.7	V
Gate Trigger Voltage	V_{GT}	V_D = 12V, I_T = 0.1A	–	0.7	1.5	V
		V_D = 400V, I_T = 0.1A, T_J = +125°C	0.25	0.4	–	V
Off–State Leakage Current	I_D	$V_D = V_{DRM}$max, T_J = +125°C	–	0.1	0.5	mA
Dynamic Characteristics						
Critical Rate–of–Rise of Off–State Voltage	dV_D/dt	V_{DM} = 67% V_{DRM}max, T_J = +125°C, Exponential Waveform, R_{GK} = 1kΩ	–	5	–	V/µs
Gate Controlled Turn–On Time	t_{gt}	I_{TM} = 12A, $V_D = V_{DRM}$max, I_G = 0.1A, dI_G/dt = 5A/µs	–	2	–	µs