User Guide
EVB-ATEK951P4-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	28.07.2021	Initial Version	
1.1	10.01.2022	Format and Content Fixed	
1.2	16.04.2022	Format and Content Fixed	

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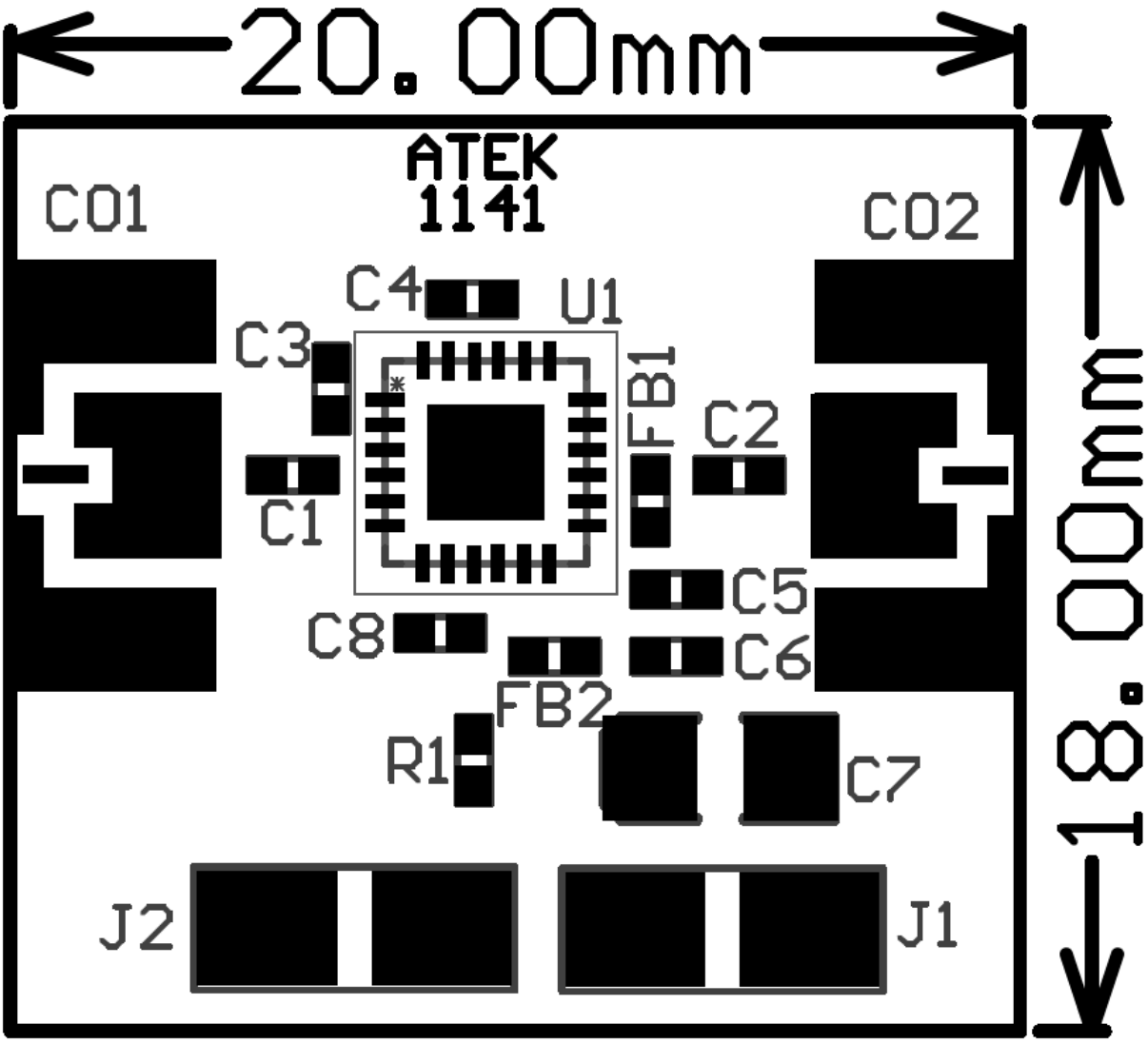
1 GENERAL INFORMATION



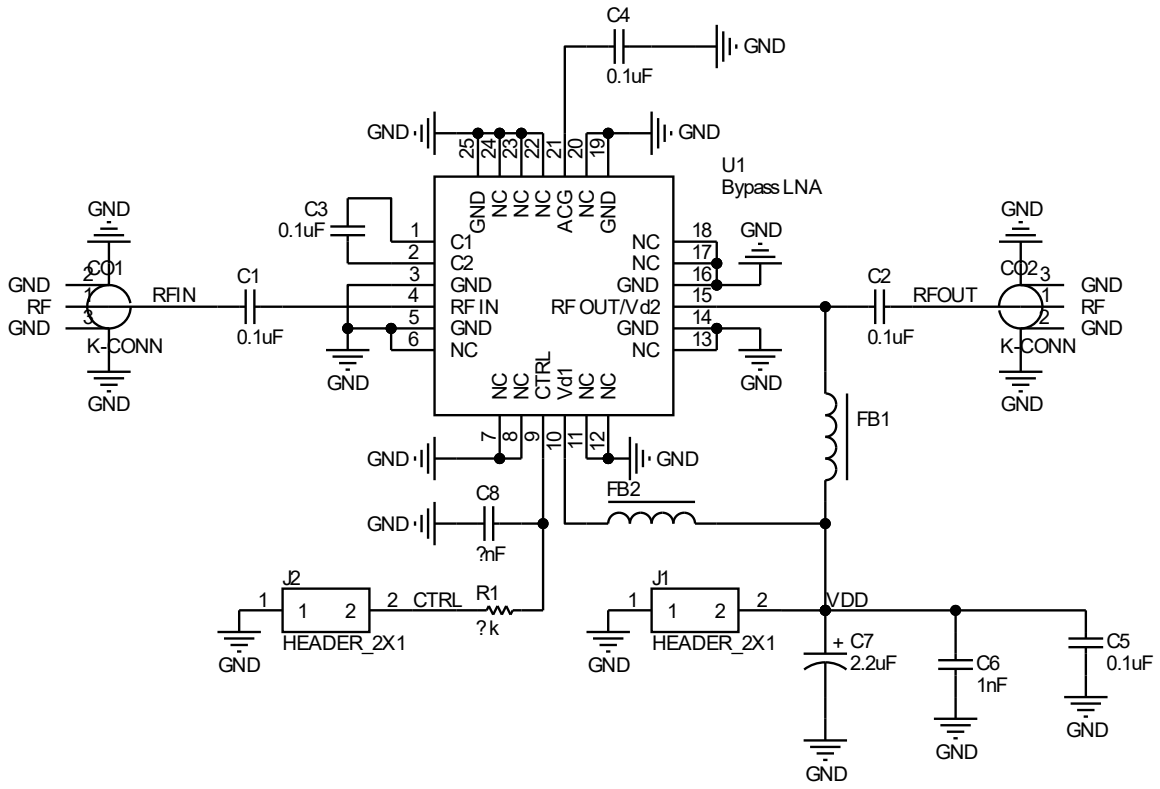
PIN Name	Definition	Comment
CO1	RF IN	SMA Connector
CO2	RF OUT	SMA Connector
J1 Right	GND	2.54mm Header
J1 Left	VDD	2.54mm Header
J2 Right	Control Voltage	2.54mm Header
J2 Left	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



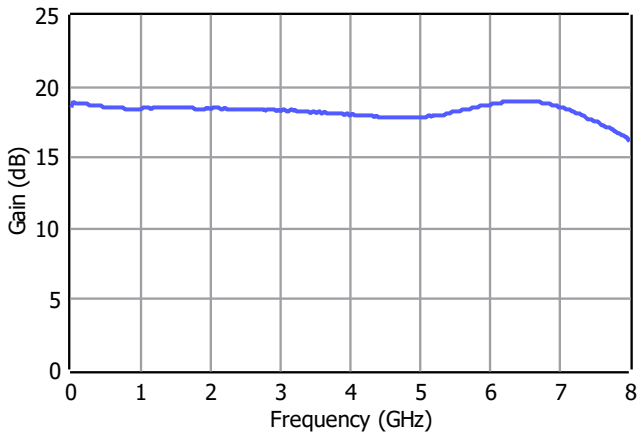
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C2, C3	0402	3	100nF	
C4	0402	1	DNP	
C5	0402	1	100nF	
C6	0402	1	1nF	
C7	CASEA	1	2.2uF	
C8	0402	1	DNP	
CO1, CO2	SMA Connector	2	SMA Connector	
FB1, FB2	0402	2	Ferrite Bead	
J1, J2	2x1 Header	2	2x1 Header	
R1	0402	1	0R	
U1	ATEKQ4424	1	Bypass LNA	ATEK951P4

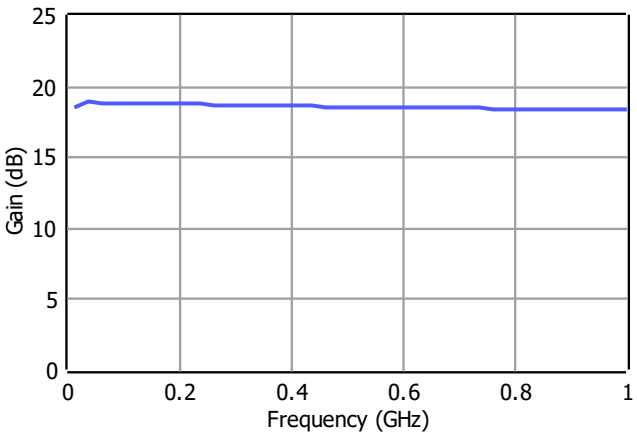
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: Vdd = 5 V, T = 25 C, CW. For details, please refer to the datasheet.

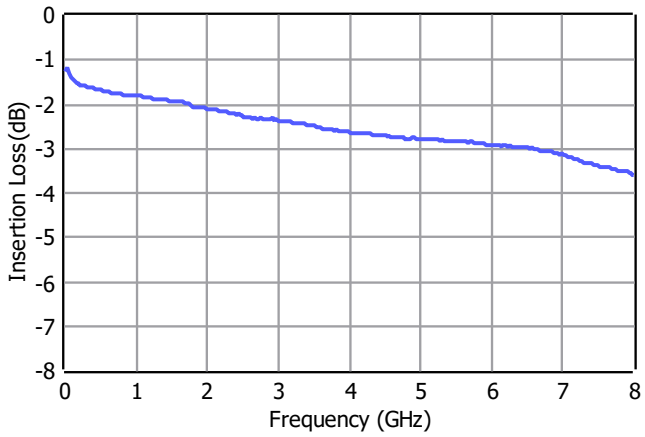
Gain Wideband, LNA State



Gain Low Frequency, LNA State



Insertion Loss WideBand, Bypass State



Insertion Loss Low Frequency, Bypass State