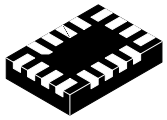
DATA/AUDIO Low-Voltage Dual DPDT Analog Switch

FSA2466



UQFN16 1.8x2.6, 0.4P
CASE 523BF

Description

The FSA2466 is a dual Double−Pole, Double−Throw (DPDT) analog switch. The FSA2466 operates from a single 1.65 V to 4.45 V supply and features an ultra−low on resistance of 2 Ω at a +2.7 V supply and T_A = 25°C. This device is fabricated with sub−micron CMOS technology to achieve fast switching speeds and is designed for break−before−make operation.

FSA2466 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This allows mobile handset applications direct interface with the baseband processor general−purpose I/Os.

Features

Switch Type	DPDT (2x)
Input Type	Data / Audio Switch
Input Signal Range	0 to V_{CC}
V_{CC}	1.65 to 4.45 V
R_{ON}	2.5 Ω at 2.7 V
R_{FLAT}	0.8 Ω at 2.7 V
ESD	8 kV HBM
Bandwidth	245 MHz
C_{ON} at 240 MHz	16 pF
C_{OFF} at 240 MHz	6.0 pF
Features	Low I_{CTT}
Package	16−Lead UMLP 1.80 x 2.60 x 0.55 mm, 0.40 mm pitch
Top Mark	KA
Ordering Information	FSA2466UMX

Applications

- MP3 Portable Media Players
- Cellular Phones, Smartphones

MARKING DIAGRAM

KA = Specific Device Code
&K = 2−Digits Lot Run Traceability Code
&2 = 2−Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

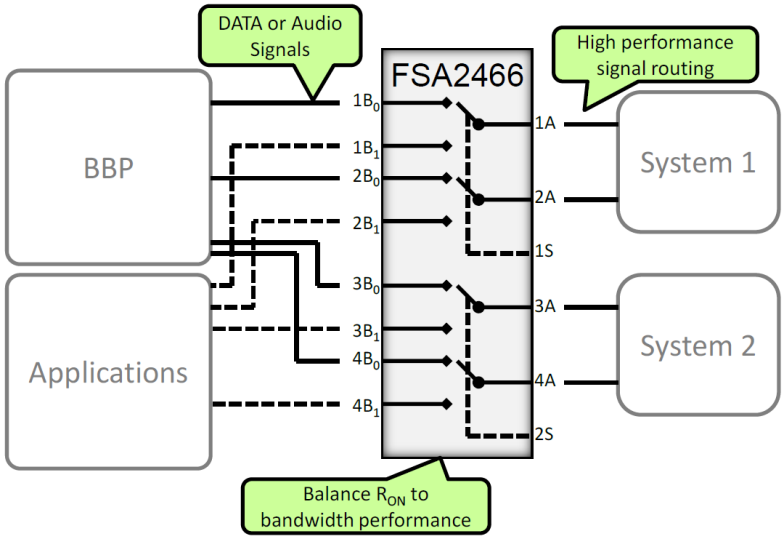


Figure 1. Typical Mobile Phone Application

ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Shipping†
FSA2466UMX	KA	−40 to 85°C	16−Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8 x 2.6 mm	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Pin Configuration

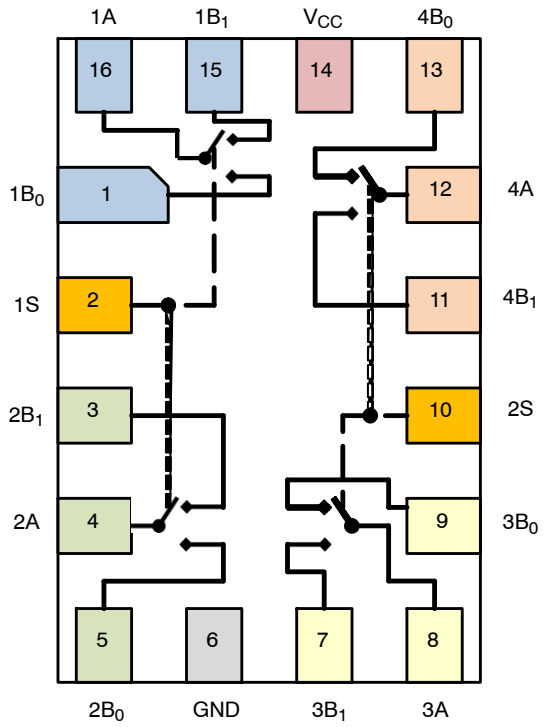


Figure 2. FSA2466UMX (Top View)

PIN DESCRIPTIONS

Pin #	Name	Type	Description		
1	$1B_0$	I/O	Data / Audio Port		
2	1S	Input	Control Input for Data & Common Ports 1 & 2	0	$1B_0$ = 1A & $2B_0$ = 2A
				1	$1B_1$ = 1A & $2B_1$ = 2A
3	$2B_1$	I/O	Data / Audio Port		
4	2A	I/O	Data / Audio Common Port		
5	$2B_0$	I/O	Data / Audio Port		
6	GND	GND			
7	$3B_1$	I/O	Data / Audio Port		
8	3A	I/O	Data / Audio Common Port		
9	$3B_0$	I/O	Data / Audio Port		
10	2S	Input	Control Input for Data & Common Ports 3 & 4	0	$3B_0$ = 3A & $4B_0$ = 4A
				1	$3B_1$ = 3A & $4B_1$ = 4A
11	$4B_1$	I/O	Data / Audio Port		
12	4A	I/O	Data / Audio Common Port		
13	$4B_0$	I/O	Data / Audio Port		
14	V_{CC}	Supply	Voltage supply		
15	$1B_1$	I/O	Data / Audio Port		
16	1A	I/O	Data / Audio Common Port		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.50	5.25	V
V_S	Switch Voltage		−0.5	V_{CC} + 0.3	V
V_{IN}	Input Voltage		−0.5	5.0	V
I_{IK}	Input Diode Current		−50		mA
I_{SW}	Switch Current			350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1 ms Duration, <10% Duty Cycle)			500	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature			+150	°C
T_L	Lead Temperature, Soldering 10 seconds			+260	°C
ESD	Human Body Model, JESD22−A114	I/O to GND		8	kV
		Power to GND		8	
		All Other Pins		8	
	Charged Device Model, JEDEC: JESD22−C101			2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage (Note 1)	1.65	4.45	V
V_{IN}	Control Input Voltage (Note 2)	0	V_{CC}	V
V_S	Switch Input Voltage	0	V_{CC}	V
TA	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. For 4.45 V operation, SEL frequency (pins 1S & 2S) should not exceed 100 Hz and 100 ns edge rate.
2. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC} (V)	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		4.30				1.4		V
			2.70 to 3.60				1.3		
			2.30 to 2.70				1.1		
			1.65 to 1.95				0.9		
V_{IL}	Input Voltage Low		4.30					0.7	V
			2.70 to 3.60					0.5	
			2.30 to 2.70					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage	V_{IN} = 0 V to V_{CC}	1.65 to 4.30				−0.5	0.5	μA
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Port nB0 and nB1	nA=0.3 V, V_{CC}−0.3V	1.95 to 4.30	−10		10	−50	50	nA
		nB0 or nB1=0.3 V, V_{CC}−0.3V or Floating							
$I_{A(ON)}$	On Leakage Current of Port A	nA = 0.3 V, V_{CC}−0.3V	1.95 to 4.30	−10		10	−50	50	nA
		nB0 or nB1 = 0.3 V, V_{CC}−0.3V or Floating							
R_{ON}	Switch On Resistance (Note 3)	I_{OUT}=100 mA	4.30		1.6			2.0	Ω
		I_{OUT}=100 mA, nB0 or nB1=0 V, 0.7 V, 1.2 V, V_{CC}	2.70		2.0			2.5	
			2.30		2.2			2.7	
		I_{OUT}=100mA, nB0 or nB1=0.7 V	1.80		4.3			6.0	
ΔR_{ON}	On Resistance Matching Between Channels (Note 4)	I_{OUT}=100 mA, nB0 or nB1=0.8 V	2.70		0.04			0.20	Ω
		I_{OUT}=100 mA, nB0 or nB1=0.7 V	2.30		0.03			0.30	
$R_{FLAT(ON)}$	On Resistance Flatness (Note 5)	I_{OUT}=100 mA, nB0 or nB1 = 0V → V_{CC}	2.70		0.60			0.8	Ω
			2.30		0.75			0.9	
I_{CC}	Quiescent Supply Current	V_{IN}=0 V to V_{CC}, I_{OUT}=0 V	4.30	−100		100	−500	500	nA
I_{CCT}	Increase in I_{CC} Current per Control Voltage	V_{IN}=1.8 V	4.30		7	12		15	μA
		V_{IN}=2.6 V	4.30		3	6		7	

3. On resistance is determined by the voltage drop between the A and B pins at the indicated current through the switch.
4. $\Delta R_{ON}=R_{ON\ max} - R_{ON\ min}$ measured at identical V_{CC}, temperature, and voltage.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC ELECTRICAL CHARACTERISTICS

(Typical values are are at T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Condition	V_{CC}	T_A = +25°C			T_A = −40 to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn−On Time	nB_0 or nB_1=1.5 V, R_L=50 Ω, C_L=35 pF	3.6 to 4.3			50		60	ns	Figure 3
			2.7 to 3.6			65		75		
			2.3 to 2.7			80		90		
t_{OFF}	Turn−Off Time	nB_0 or nB_1=1.5 V, R_L=50 Ω, C_L=35 pF	3.6 to 4.3			32		40	ns	Figure 3
			2.7 to 3.6			42		50		
			2.3 to 2.7			52		60		
t_{BBM}	Break−Before−Make Time (Note 6)	nB_0 or nB_1=1.5 V, R_L=50 Ω, C_L=35 pF	3.6 to 4.3		15				ns	Figure 4
			2.7 to 3.6		15					
			2.3 to 2.7		15					
Q	Charge Injection	C_L=100 pF, V_{GEN}=0 V, R_{GEN}=0 Ω	3.6 to 4.3		8				pC	Figure 6
		C_L=100 pF, V_{GEN}=0 V, R_{GEN}=0 Ω	2.7 to 3.6		6					
		C_L=100 pF, V_{GEN}=0 V, R_{GEN}=0 Ω	2.3 to 2.7		3					
OIRR	Off Isolation	f=100 KHz, R_L=50 Ω, C_L=5 pF	3.6 to 4.3		−90				dB	Figure 5
			2.7 to 3.6		−90					
			2.3 to 2.7		−90					
Xtalk	Crosstalk	f=100 KHz, R_L=50 Ω, C_L=5 pF	3.6 to 4.3		−90				dB	Figure 5
			2.7 to 3.6		−90					
			2.3 to 2.7		−90					
BW	−3dB Bandwidth	R_L=50 Ω	2.3 to 4.3		245				MHz	Figure 8
THD	Total Harmonic Distortion	R_L=32 Ω, V_{IN}=2V_{PP}, f=20 to 20 kHz	3.6 to 4.3		0.21				%	Figure 9
			2.7 to 3.6		0.17					
			2.3. to 2.7		0.26					
		R_L=600 Ω, V_{IN}=2 V_{PP}, f=20 to 20 kHz	3.6 to 4.3		0.01					
			2.7 to 3.6		0.008					
			2.3. to 2.7		0.012					

6. Guaranteed by characterization, not production tested.

CAPACITANCE

Symbol	Parameter	Condition	V_{CC}	T_A = +25°C Typical	Unit	Figure
C_{IN}	Control Pin Input Capacitance	f = 1 MHz	0	1.3	pF	Figure 3
C_{OFF}	B Port Off Capacitance	f = 1 MHz	3.3	6.0	pF	Figure 3
		f = 240 MHz	3.3	6.0		
C_{ON}	A Port On Capacitance	f = 1 MHz	3.3	21.0	pF	Figure 3
		f = 240 MHz	3.3	16.0		

AC Loadings and Waveforms

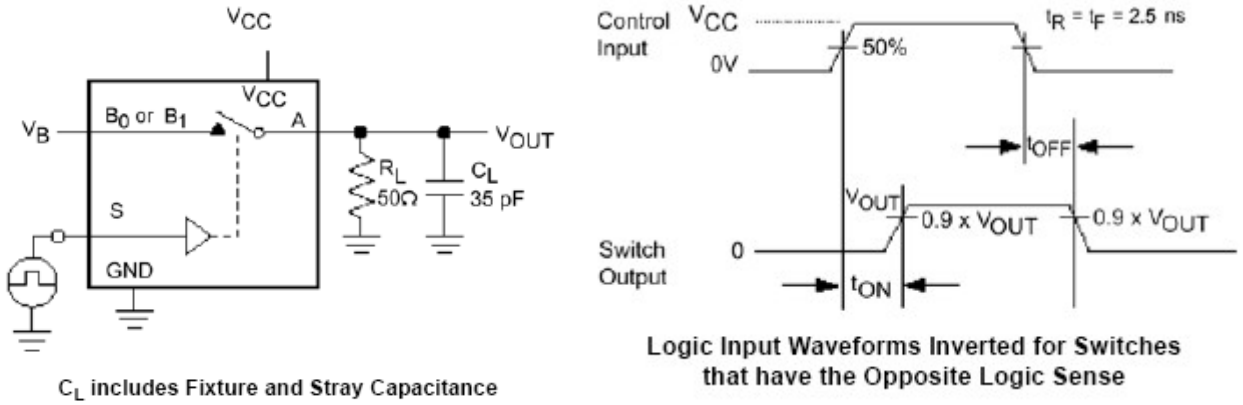


Figure 3. Turn−On / Turn−Off Timing

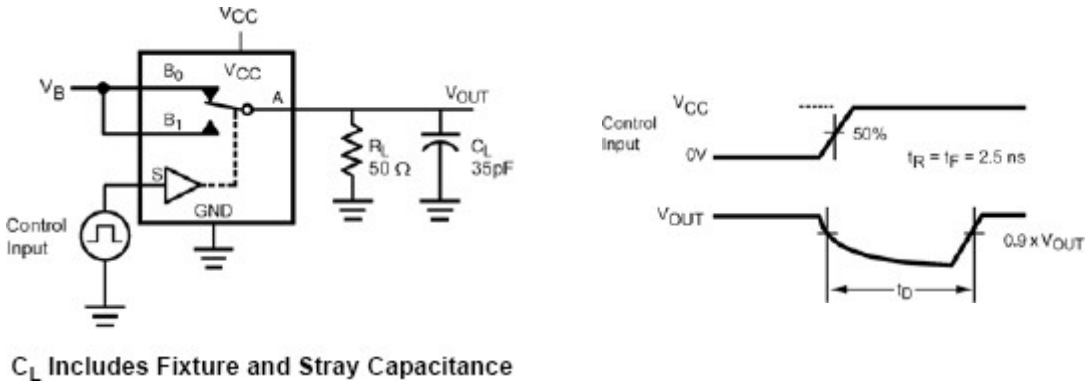


Figure 4. Break−Before−Make Timing

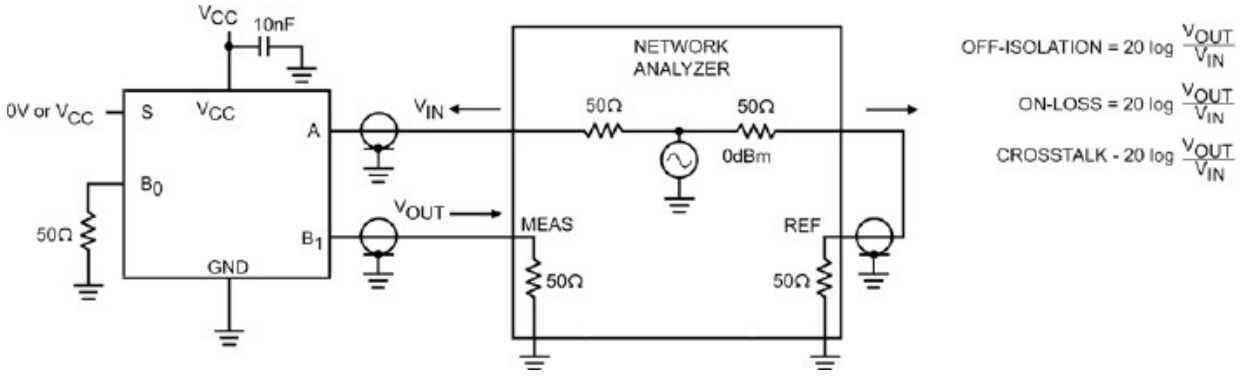


Figure 5. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)

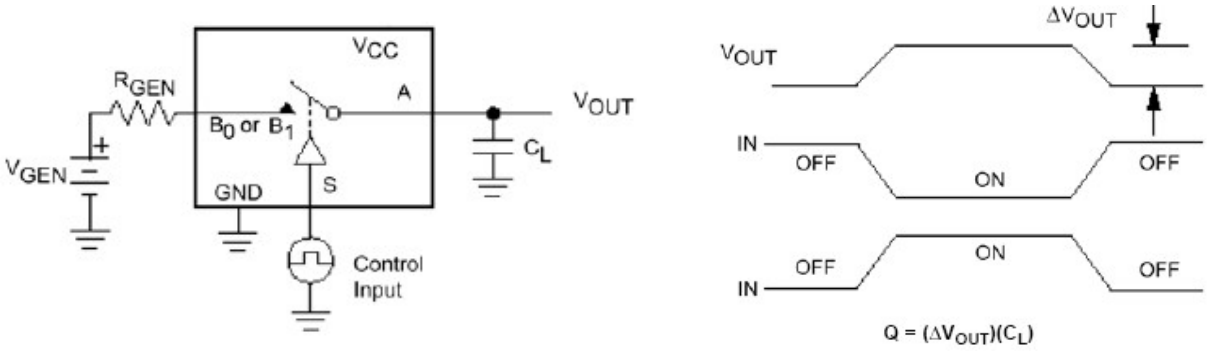


Figure 6. Charge Injection

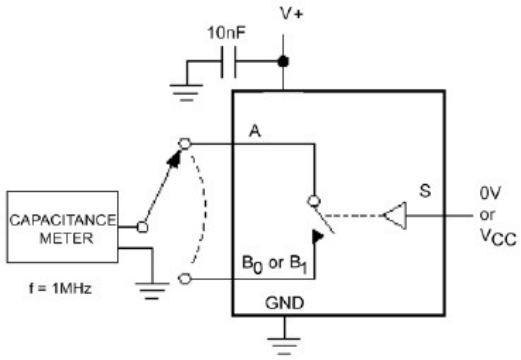


Figure 7. On / Off Capacitance Measurement Setup

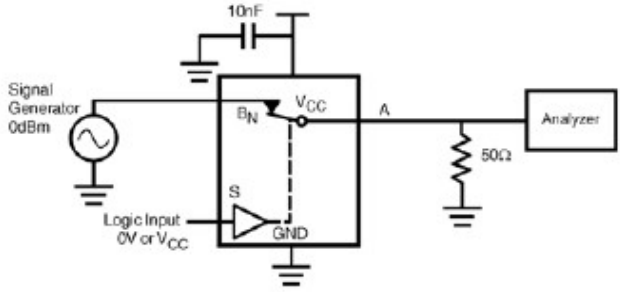


Figure 8. Bandwidth

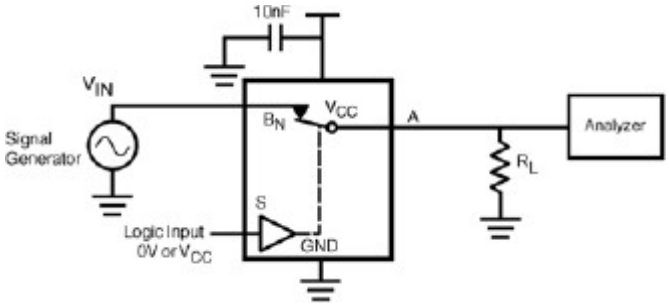
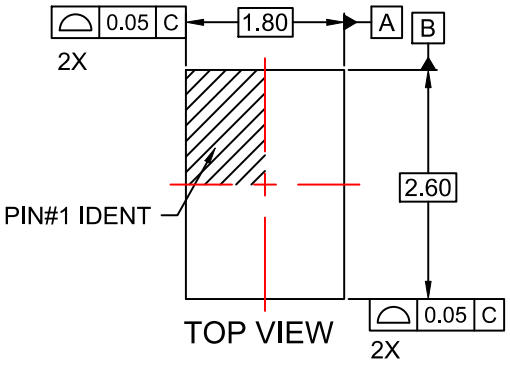


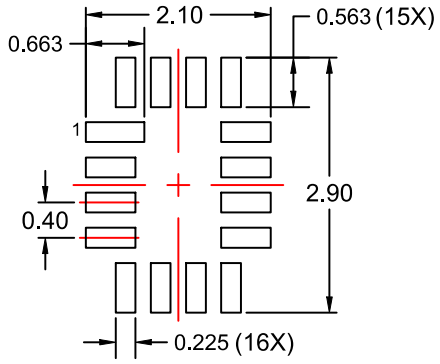
Figure 9. Harmonic Distortion

UQFN16 1.8x2.6, 0.4P
CASE 523BF
ISSUE O

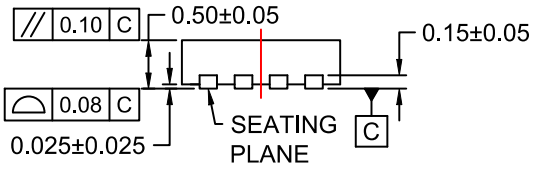
DATE 31 OCT 2016



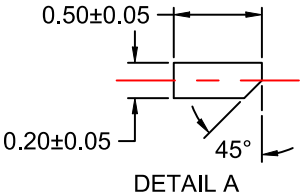
TOP VIEW



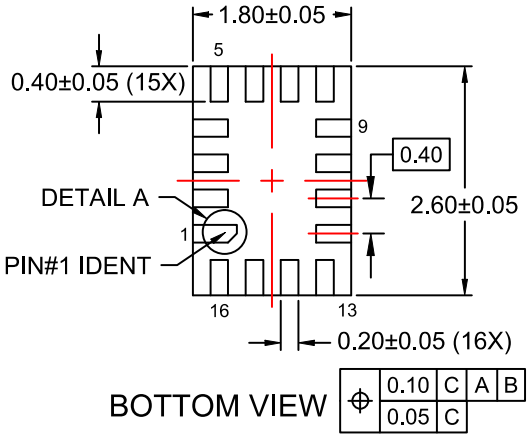
RECOMMENDED
LAND PATTERN



SIDE VIEW

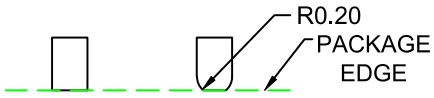


DETAIL A
SCALE : 2X



BOTTOM VIEW

LEAD SHAPE AT PACKAGE EDGE



LEAD
OPTION 1
SCALE : 2X

LEAD
OPTION 2
SCALE : 2X

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

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