Am25LS14A

8-Bit Serial/Parallel Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 50MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- IMOX™ process with ECL internal

GENERAL DESCRIPTION

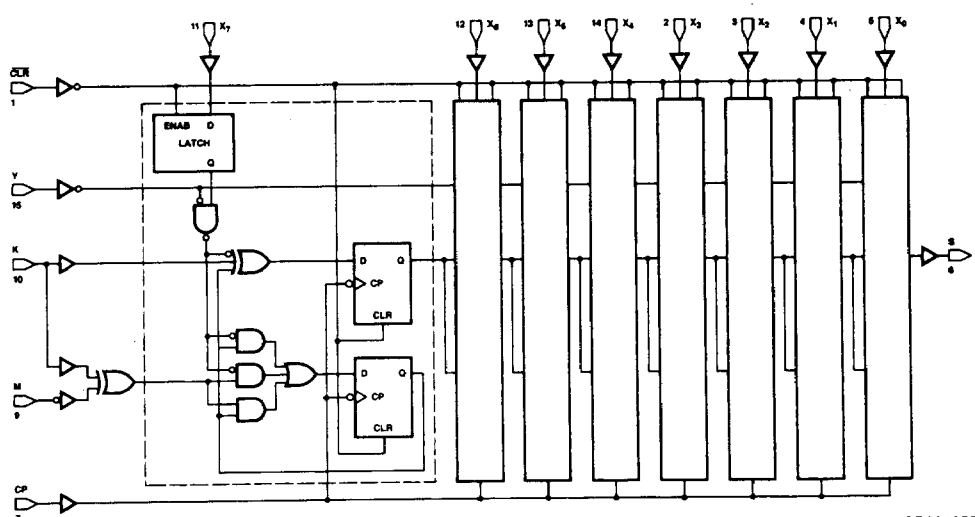
The Am25LS14A is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream – least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14A must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

BLOCK DIAGRAM



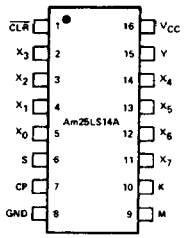
BD001650

IMOX is a trademark of Advanced Micro Devices.

01767C

Refer to Page 13-1 for Essential Information on Military Devices

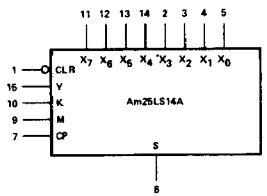
CONNECTION DIAGRAM
Top View



CD001800

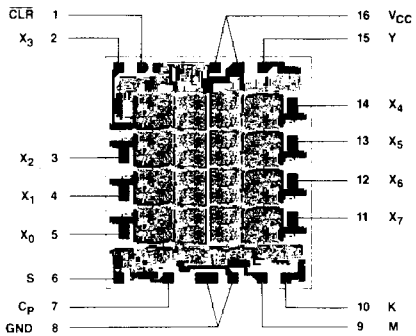
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000660

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.084" x 0.095"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS14A **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 16-pin CERDIP
  - F– 16-pin flatpak
  - P– 16-pin plastic DIP
  - X– Dice
- **Am25LS14A** — Device type 8-Bit Multiplier

Valid Combinations	
Am25LS14A	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

Pin No.	Name	I/O	Description
	X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7	I	The eight data inputs for the multiplicand (X) data.
15	Y	I	The serial input for the multiplier (Y) data—least significant bit first.
6	S	O	The serial output for the product of X • Y—least significant bit first.
7	CP	I	Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.
1	CLR	I	Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.
10	K	I	The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.
9	M	I	The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	
CLR	CP	K	M	X_I	Y	Y_{-1}	S	FUNCTION
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

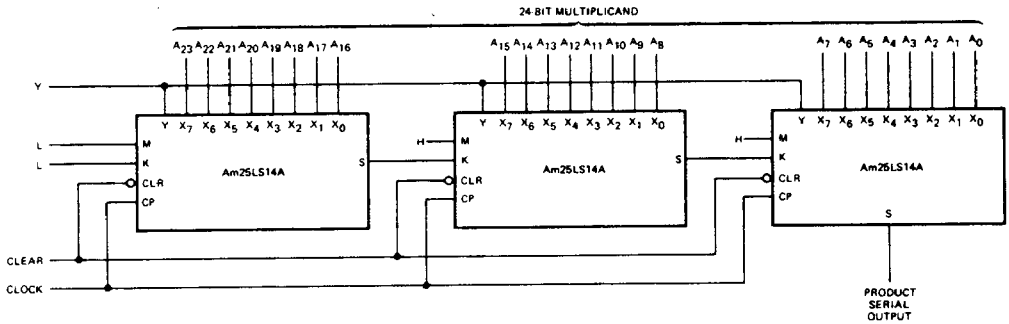
H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.
L LOW, applying to a LOW voltage level.
I Input.
O Output.
Negative Current Current flowing out of the device.
Positive Current Current flowing into the device.
I_{IL} LOW-level input current with a specified LOW-level voltage applied.
I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.
I_{OL} LOW-level output current.
I_{OH} HIGH-level output current.
I_{SC} Output short-circuit source current.
I_{CC} The supply current drawn by the device from the V_{CC} power supply.
V_{IL} Logic LOW input voltage.
V_{IH} Logic HIGH input voltage.
V_{OL} LOW-level output voltage with I_{OL} applied.
V_{OH} HIGH-level output voltage with I_{OH} applied.

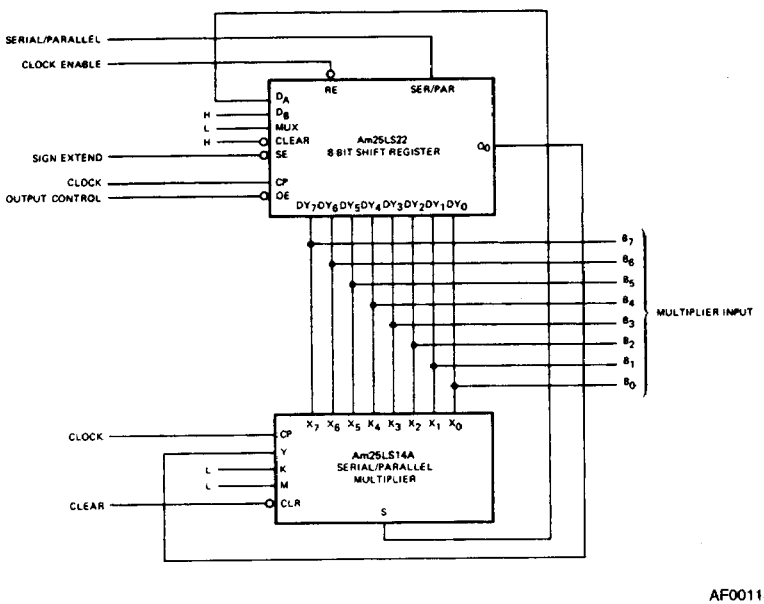
APPLICATIONS

See also Digital Signal Processing Applications Section for more information.



AF001120

Basic 24-Bit Serial/Parallel Connection



AF001130

8-Bit by 8-Bit Multiplier, Bus Organized, with 8-Bit Truncated Product

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ..... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4	Volts
			I_{OL} = 12mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			−0.48	mA
			K, $\overline{CLR}$			−1.2	
			CP			−1.6	
			Y			−3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20	μA
			K, $\overline{CLR}$			30	
			CP			40	
			Y			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			45	65	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Duration of the short circuit test should not exceed one second.

01767C

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Output	C_L = 15pF R_L = 2.0kΩ		8	14	ns
t_{PHL}				10	18	
t_{PHL}	Clear to Output			9	17	ns
t_s	Y to Clock		15			ns
t_h			0			
t_s	K to Clock		15			ns
t_h			0			
t_s	X_i to Clear		13			ns
t_h			0			
t_{pw}	Clock (HIGH)		10			ns
	Clock (LOW)		10			
t_{pw}	Clear Pulse Width		10			ns
t_s	Clear Recovery Time (Inactive State)		5			ns
f_{max} (Note 1)	Maximum Clock Frequency		50	60		MHz

Note 1: Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	Am25LS COMMERCIAL		Am25LS MILITARY		Units
			Min	Max	Min	Max	
t_{PLH}	Clock to Output	C_L = 50pF R_L = 2.0kΩ		18		20	ns
t_{PHL}				22		25	
t_{PHL}	Clear to Output			22		25	ns
t_s	Y to Clock		22		25		ns
t_h			0		0		
t_s	K to Clock		20		22		ns
t_h			0		0		
t_s	X_i to Clear		20		22		ns
t_h			0		0		
t_{pw}	Clock (HIGH)		10		10		ns
	Clock (LOW)		10		10		
t_{pw}	Clear Pulse Width		10		10		ns
t_s	Clear Recovery Time (Inactive State)		5		5		ns
f_{max} (Note 1)	Maximum Clock Frequency		50		50		MHz

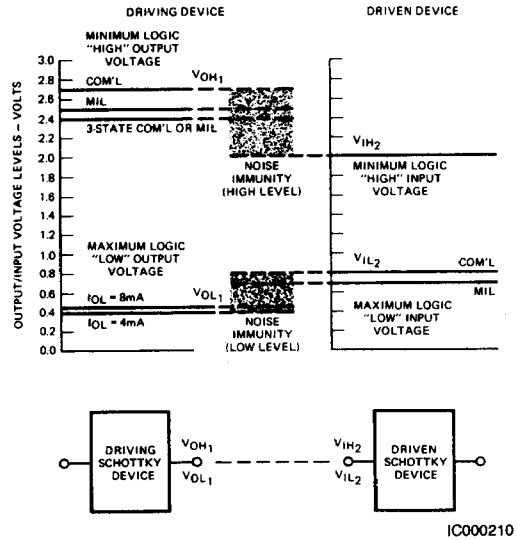
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

9

01767C

Refer to Page 13-1 for Essential Information on Military Devices

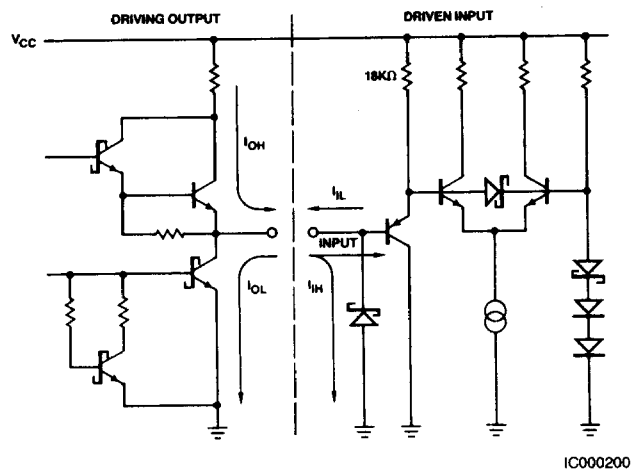
LOW CURRENT SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000210

Note: Refer to Electrical Characteristics for measure currents.

INPUT/OUTPUT INTERFACE CONDITIONS



IC000200

Note: Actual current flow direction shown.