ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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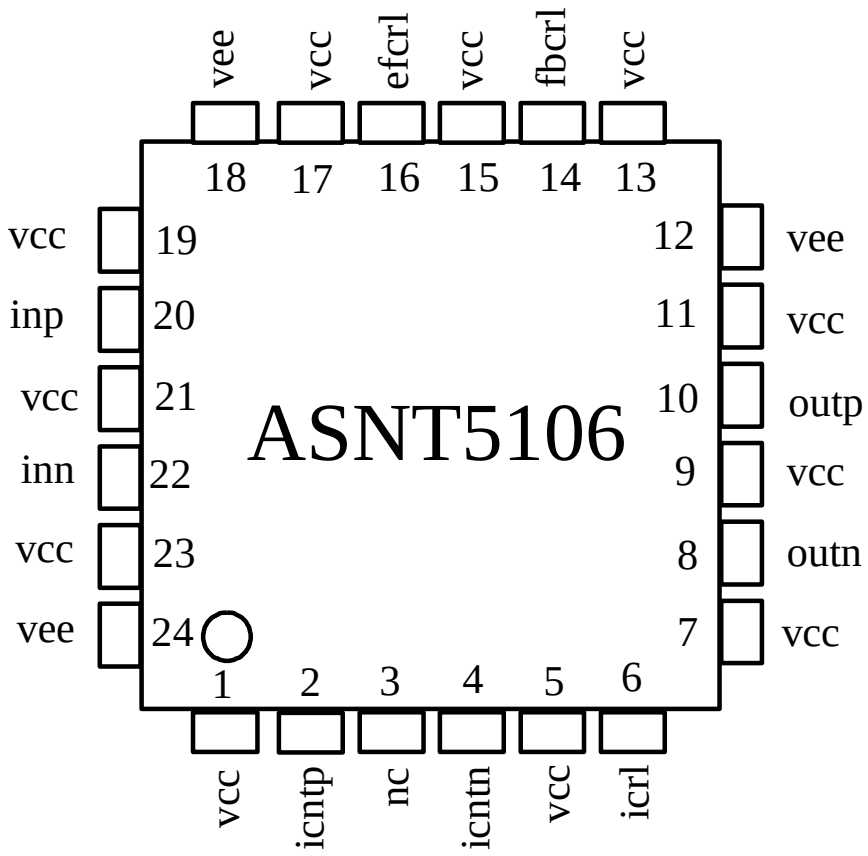
ASNT5106-PQC
DC-28*Gbps*/18*GHz* Signal Phase Shifter

- Broadband tunable data/clock phase shifter
- Manual control of power consumption / operational speed
- 1*GHz* of bandwidth for the phase adjustment tuning port
- Automatic temperature and process corner delay compensation with manual override
- Duty cycle distortion compensation with adjustable gain
- Manual internal peaking control
- Fully differential CML input interface
- Fully differential CML output interface
- Single +3.3*V* or -3.3*V* power supply
- Fabricated in SiGe for high performance, yield, and reliability
- Standard MLF/QFN 24-pin package



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DESCRIPTION

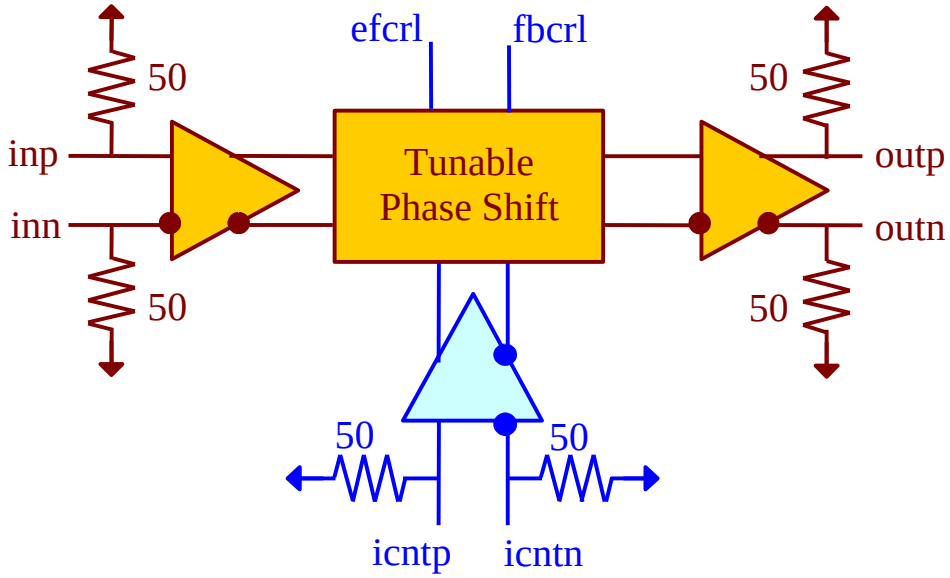

Fig. 1. Functional Block Diagram

ASNT5106-PQC is a data/clock variable delay line with an advanced control system fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its broadband input signal inp/inn. The delay is controlled through a wide-band differential tuning port icntp/icntn. The chip incorporates an automatic common-mode offset cancellation circuit that operates with either clock signals or data signals with balanced patterns. In case of non-balanced data patterns, the circuit should be disabled through a control port fbcrl. The single-ended control port efcrl can be used to manipulate internal peaking in the delay block in order to adjust the part's frequency response and thus improve output eye diagrams for various data rates and operating conditions.

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

The part's power consumption can be adjusted between its minimum (default) and maximum values using a single-ended analog control port icrl. It should be noted that higher power leads to higher operational speed of the part.

Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment.

Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. This part's delay control system was designed to minimize output jitter and increase the control function linearity. To achieve the goals, the control system is split so that each delay stage has its own control buffer. Only three stages

operate in interpolation mode at any delay position, and all the other stages are fully switched either to the short path or to the long path.

The measured diagram of phase delay versus the difference between icntp and icntn for nominal conditions is shown in Fig. 2.

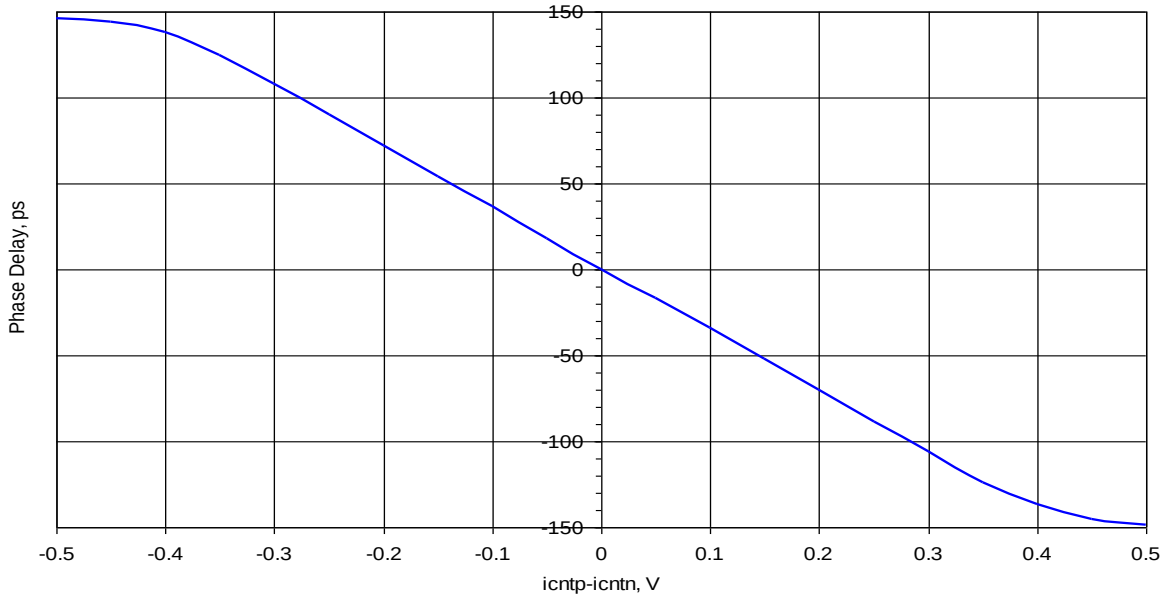

Fig. 2. Delay Control Diagram

Feedback Gain Control Port

This part has two duty cycle correction feedback loops. In case of feedback malfunction, currents inside feedback amplifiers can be manually adjusted or completely shut down through a single-ended tuning port fbcrl. The simulated dependence of feedback reference current on the control voltage is shown in Fig. 3. Higher feedback amplifier currents result in higher feedback gain and lower stability. If the port is left not connected, it defaults to an internal level of vcc-0.66*V*, the feedback current is half its maximum value and the phase shifter is in normal operating mode.

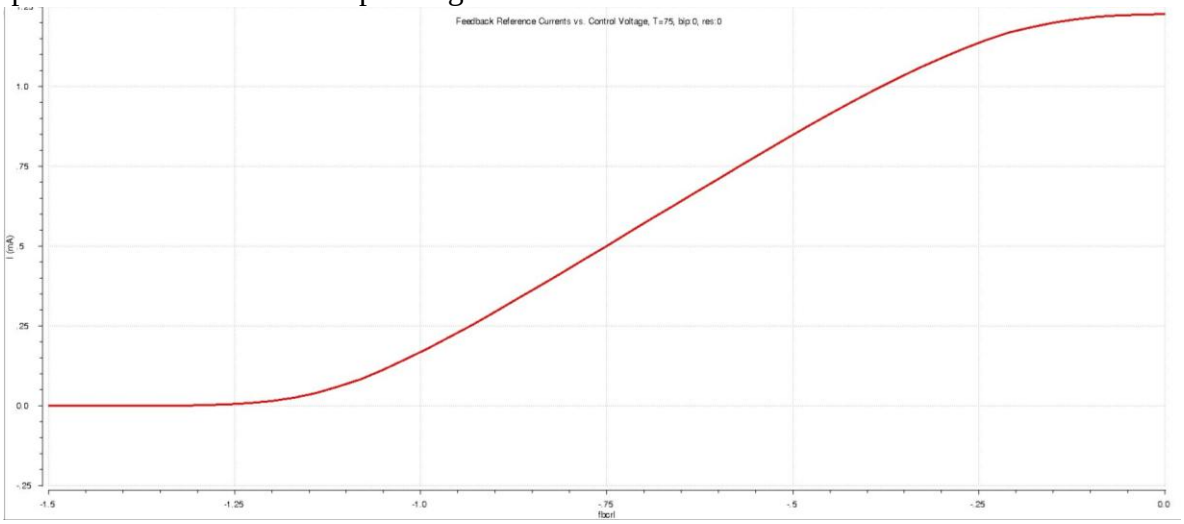

Fig. 3 Simulated Internal Feedback Current vs. Control Voltage

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Internal Peaking Control Port

Depending on the data rate and operational conditions, the output eye diagram may get distorted because of jitter caused by parasitic internal peaking. Internal peaking can be adjusted by varying currents of internal emitter followers through a single-ended port efcrl. The simulated dependence of reference current of internal emitter followers on the control voltage is shown in Fig. 4. If this port is left not connected, it defaults to an internal level of vcc-0.66*V* and emitter follower currents are half of their maximum values and the circuit is in normal operating mode.

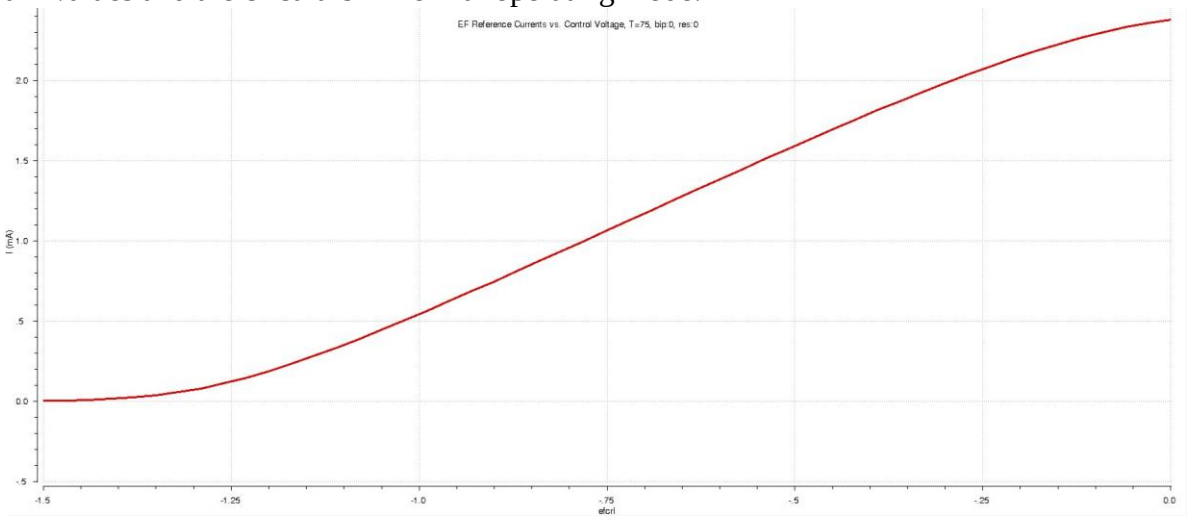

Fig. 4. Simulated Internal EF Reference Current vs. Control Voltage

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground), or a positive supply (vee = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

The part's power consumption can be adjusted between its minimum and maximum values using a single-ended analog control port icrl. Higher voltages at the control input correspond to higher power consumption. With the non-connected control port, the part defaults to minimum power consumption. It should be noted that higher power consumption leads to higher operational speed of the part as detailed in ELECTRICAL CHARACTERISTICS.

All the characteristics detailed below assume vcc = 0.0*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
inp	20	CML input	Differential high-speed signal inputs with internal SE 50*Ohm* termination to vcc
inn	22		
icntp	2	input	Differential control input with internal SE 50*Ohm* terminations to vcc
icntn	4	input	
icrl	6	input	SE DC analog control input with internal 11.5*KOhm* termination to vee
fbcrl	14	input	SE DC control input terminated to internal resistive divider between vee and vcc
efcrl	16	input	
outp	10	CML output	Differential high-speed signal outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	8		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V* or 0)	1, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23
vee	Negative power supply. (0*V* or -3.3*V*)	12, 18, 24
nc	Not connected	3

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	327		440	*mA*	Adjustable
Power consumption	1080		1450	*mW*	Adjustable
Junction temperature	-25	50	125	*°C*	
HS Input Data/Clock (inp/inn)					
Data Rate	DC		28	*Gbps*	
Frequency	DC		16	*GHz*	At minimum power consumption
	DC		18	*GHz*	At maximum power consumption
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data/Clock (outp/outn)					
Data Rate	DC		28	*Gbps*	
Frequency	DC		16	*GHz*	At minimum power consumption
	DC		18	*GHz*	At maximum power consumption
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.44		*V*	With external 50*Ohm* DC termination.
Rise/Fall times	11		13	*ps*	20%-80%
Output Jitter		3.5		*ps*	For PRBS input, peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal
Output-to-Input Delay					
Phase shift	0		290	*ps*	For the full range of phadj control signal
Phase shift stability	-10		10	*ps*	0-125*°C* junction temperature
Absolute delay stability	-25		25	*ps*	0-125*°C* junction temperature
Tuning port (icntp/icntn)					
Bandwidth	DC		1000	*MHz*	
Control voltage range	vcc-1000		vcc	*mV*	Default voltage is vcc
Tuning port (icrl)					
Control voltage range	vee		vcc	*mV*	Default voltage is vee
Tuning port (fbcrl)					
Control voltage range	vcc-1300		vcc	*mV*	Default voltage is vcc-0.66*V*
Tuning port (efcrl)					
Control voltage range	vcc-1300		vcc	*mV*	Default voltage is vcc-0.66*V*

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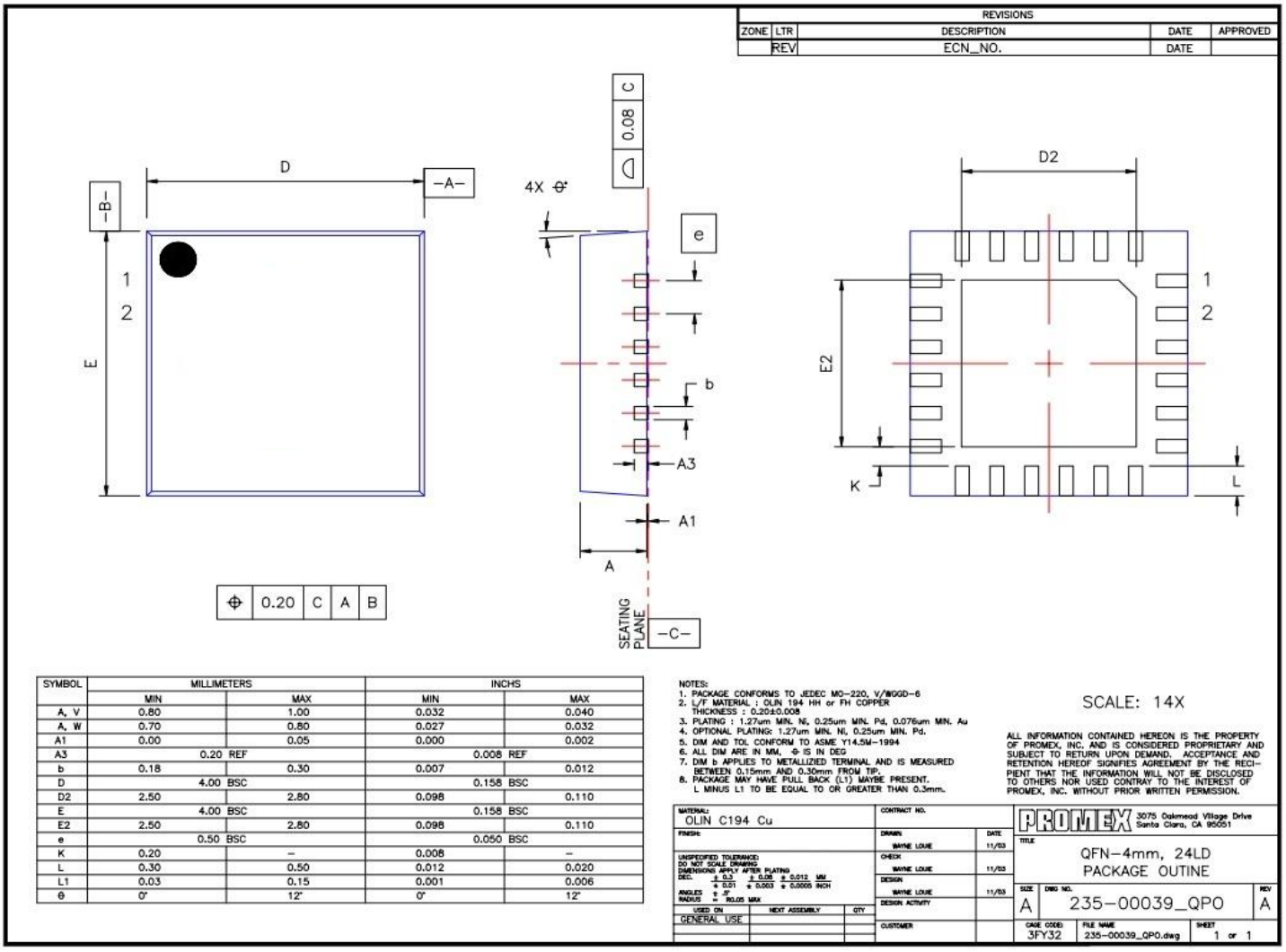
PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 5. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

NOTES:
1. PACKAGE CONFORMS TO JEDEC MO-220, V/WGGD-6
2. L/F MATERIAL : OLIN 194 HH or FH COPPER THICKNESS : 0.20±0.008
3. PLATING : 1.27um MIN. Ni, 0.25um MIN. Pd, 0.076um MIN. Au
4. OPTIONAL PLATING: 1.27um MIN. Ni, 0.25um MIN. Pd.
5. DIM AND TOL CONFORM TO ASME Y14.5M-1994
6. ALL DIM ARE IN MM, θ IS IN DEG
7. DIM b APPLIES TO METALLIZIED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TIP.
8. PACKAGE MAY HAVE PULL BACK (L1) MAYBE PRESENT. L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.3mm.

Fig. 5. QFN 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5106-PQC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
1.3.2	01-2020	Updated Package Information
1.2.2	07-2019	Updated Letterhead
1.2.1	01-2018	Added measured delay control diagram
1.1.1	09-2017	Package information correction
1.0.1	09-2017	Initial release