LMC6572/LMC6574 Dual and Quad Low Voltage (2.7V and 3V) Operational Amplifier

Check for Samples: LMC6572, LMC6574

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Guaranteed 2.7V and 3V Performance**
- **Rail-to-Rail Output Swing (Within 5 mV of Supply Rail, 100 kΩ Load)**
- **Ultra-Low Supply Current: 40 µA/Amplifier**
- **Low Cost**
- **Ultra-Low Input Current: 20 fA**
- **High Voltage Gain @ V_S=2.7V, R_L=100 kΩ: 120 dB**
- **Specified for 100 kΩ and 5 kΩ Loads**
- **Available in VSSOP Package**

APPLICATIONS

- **Transducer Amplifier**
- **Portable or Remote Equipment**
- **Battery-Operated Instruments**
- **Data Acquisition Systems**
- **Medical Instrumentation**
- **Improved Replacement for TLV2322 and TLV2324**

DESCRIPTION

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.

3V amplifier performance is backed by 2.7V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.

The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of open-loop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7V supply.

These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground.

This device is built with Texas Instruments' advanced Double-Poly Silicon-Gate CMOS process.

LMC6572 is also available in VSSOP package which is almost half the size of a SOIC-8 device.

Connection Diagram

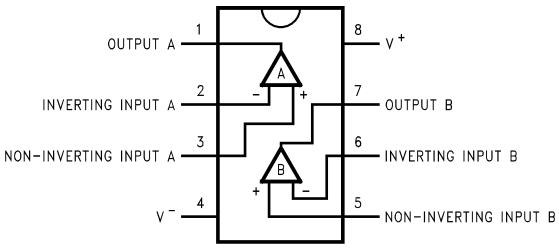

Figure 1. 8-Pin PDIP/SOIC/VSSOP Package
See Package Number P, D, or DGK

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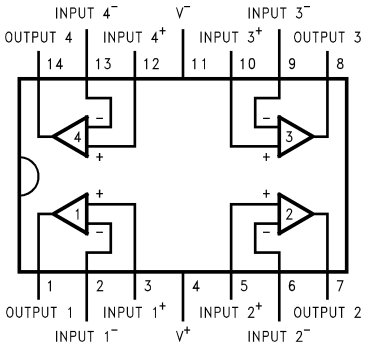

Figure 2. 14-Pin PDIP/SOIC Package
See Package Number NFF or D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	2000V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	12V
Current at Input Pin	±5 mA
Current at Output Pin(4)	±10 mA
Current at Power Supply Pin	35 mA
Lead Temperature (Soldering, 10 Seconds)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature(5)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Ratings(1)

Supply Voltage		$2.7V \le V^+ \le 11V$
Junction Temperature Range	LMC6572AI, LMC6572BI	$-40°C \le T_J \le +85°C$
	LMC6574AI, LMC6574BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	P Package, 8-Pin PDIP	115°C/W
	D Package, 8-Pin SOIC	193°C/W
	DGK Package, 8-Pin VSSOP	217°C/W
	NFF Package, 14-Pin PDIP	81°C/W
	D Package, 14-Pin SOIC	126°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

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2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ(1)	LMC6574AI LMC6572AI Limit(2)	LMC6574BI LMC6572BI Limit(2)	Units
V_{OS}	Input Offset Voltage	V^+ = 2.7V and 3V		0.5	3	7	mV
					3.5	**7.5**	Max
TCV_{OS}	Input Offset Voltage Average Drift			1.5			µV/°C
I_B	Input Current			0.02			pA
					10	**10**	Max
I_{OS}	Input Offset Current			0.01			pA
					6	**6**	Max
R_{IN}	Input Resistance			>1			Tera Ω
C_{IN}	Common-Mode Input Capacitance			3			pF
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.5V V^+ = 5V		75	63	60	dB
					60	**57**	Min
+PSRR	Positive Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V^- = 0V		75	67	60	dB
					65	**58**	Min
−PSRR	Negative Power Supply Rejection Ratio	−2.7V ≤ V^- ≤ −5V, V^+ = 0V		83	75	67	dB
					73	**65**	Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 2.7V and 3V for CMRR ≥ 50 dB		−0.1	−0.05	−0.05	V
					0	**0**	Max
				V^+ − 0.8	V^+ − 1.0	V^+ − 1.0	V
					V^+ − 1.3	**V^+ − 1.3**	Min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ(3)	Sourcing	1000			V/mV
			Sinking	500			V/mV
V_O	Output Swing	V^+ = 2.7V R_L = 100 kΩ to $V^+/2$		2.695	2.68	2.65	V
					2.66	**2.62**	Min
				0.005	0.03	0.06	V
					0.05	**0.09**	Max
		V^+ = 2.7V R_L = 5 kΩ to $V^+/2$		2.66	2.55	2.45	V
					2.45	**2.35**	Min
				0.04	0.15	0.25	V
					0.25	**0.35**	Max
		V^+ = 3V R_L = 100 kΩ to $V^+/2$		2.995	2.98	2.95	V
					2.96	**2.93**	Min
				0.005	0.03	0.06	V
					0.05	**0.09**	Max
		V^+ = 3V R_L = 5 kΩ to $V^+/2$		2.96	2.85	2.75	V
					2.75	**2.65**	Min
				0.04	0.15	0.25	V
					0.25	**0.35**	Max

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) V^+ = 3V, V_{CM} = 1.5V and R_L connected to 1.5V. For Sourcing tests, 1.5V ≤ V_O ≤ 2.5V. For Sinking tests, 0.5V ≤ V_O ≤ 1.5V.

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2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC6574AI LMC6572AI Limit(2)	LMC6574BI LMC6572BI Limit(2)	Units
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	6.0	4.0	3.0	mA
				3.0	**2.0**	Min
		Sinking, V_O = 2.7V	4.0	3.0	2.5	mA
				2.0	**1.5**	Min
I_S	Supply Current	Quad Package V^+ = +2.7V, $V_O = V^+/2$	160	240	240	µA
				280	**280**	Max
		Quad Package V^+ = +3V, $V_O = V^+/2$	160	240	240	µA
				280	**280**	Max
		Dual Package V^+ = +2.7V, $V_O = V^+/2$	80	120	120	µA
				140	**140**	Max
		Dual Package V^+ = +3V, $V_O = V^+/2$	80	120	120	µA
				140	**140**	Max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC6574AI LMC6572AI Limit(2)	LMC6574BI LMC6572BI Limit(2)	Units
SR	Slew Rate	V^+ = 2.7V and 3V(3)	90	30	30	V/ms
				10	**10**	Min
GBW	Gain-Bandwidth Product	V^+ = 3V	0.22			MHz
φ_m	Phase Margin		60			Deg
G_m	Gain Margin		12			dB
	Amp-to-Amp Isolation	See(4)	120			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	45			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.002			pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 1.0 V_{PP}	0.05			%

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, V^+ = 3V and R_L = 100 kΩ connected to 1.5V. Each amp excited in turn with 1 KHz to produce V_O = 2 V_{PP}.

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Typical Performance Characteristics

V_S = +3V, T_A = 25°C, Unless otherwise specified

Supply Current vs Supply Voltage (Dual Package)

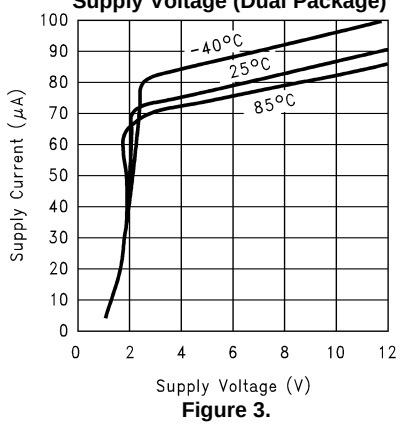

Figure 3.

Input Current vs Temperature

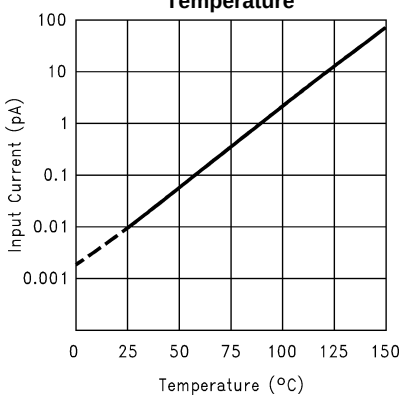

Figure 4.

Sourcing Current vs Output Voltage

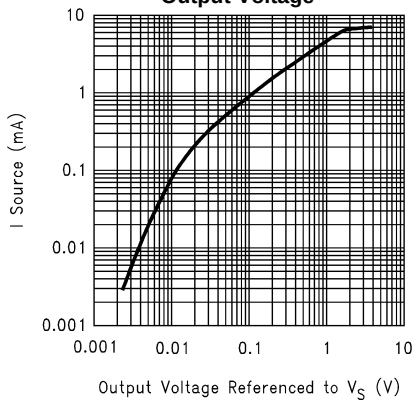

Figure 5.

Sinking Current vs Output Voltage

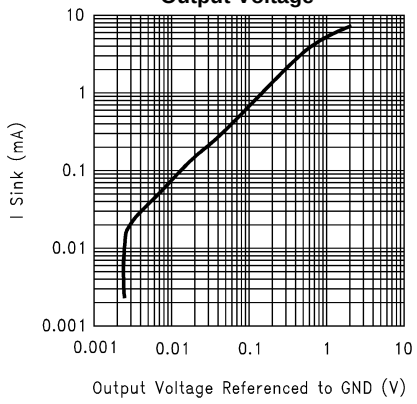

Figure 6.

Output Voltage Swing vs Supply Voltage

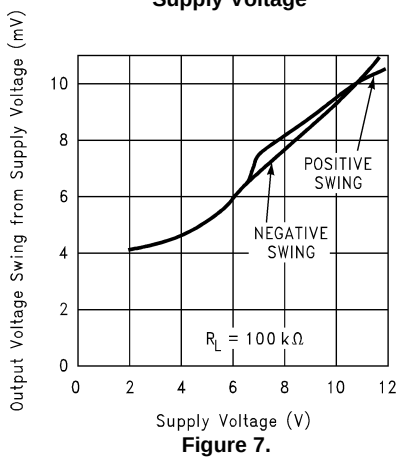

Figure 7.

Input Voltage Noise vs Frequency

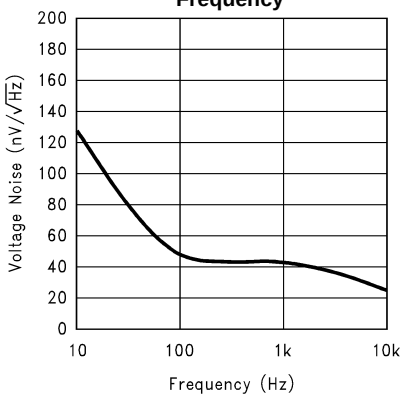

Figure 8.

Typical Performance Characteristics (continued)

V_S = +3V, T_A = 25°C, Unless otherwise specified

Crosstalk Rejection vs Frequency

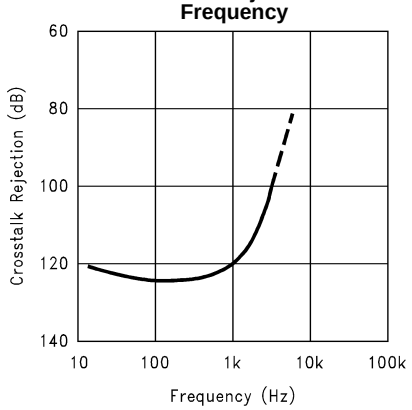

Figure 9.

Positive PSRR vs Frequency

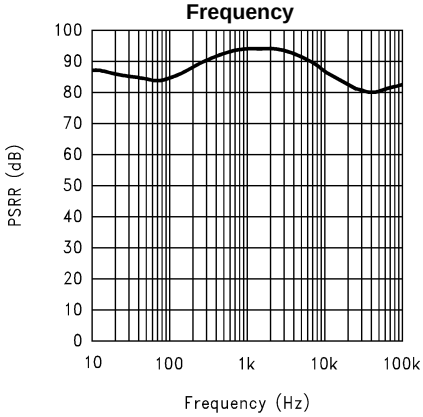

Figure 10.

Negative PSRR vs Frequency

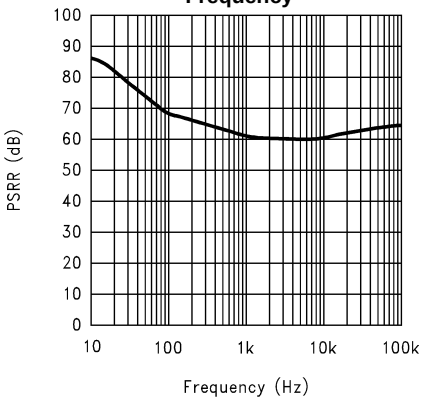

Figure 11.

CMRR vs Frequency

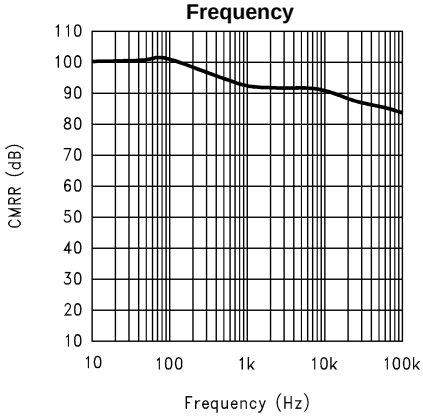

Figure 12.

Input Voltage vs Output Voltage (V_S = ±1.5)

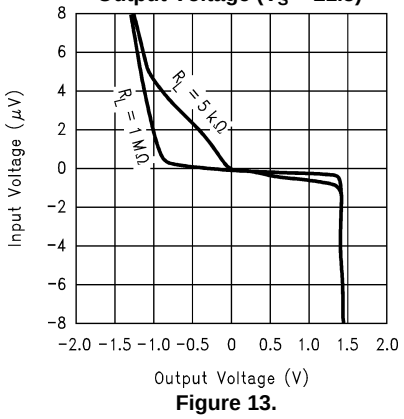

Figure 13.

Open Loop Frequency Response

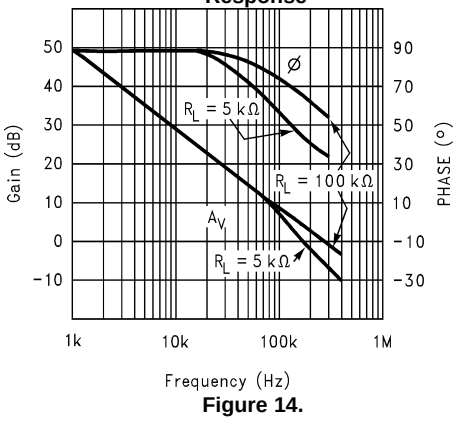

Figure 14.

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Typical Performance Characteristics (continued)

V_S = +3V, T_A = 25°C, Unless otherwise specified

Open Loop Frequency Response vs Temperature

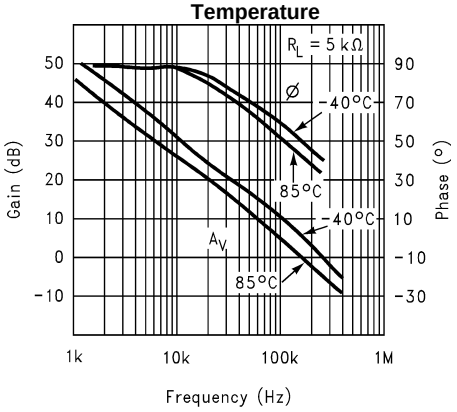

Figure 15.

Maximum Output Swing vs Frequency

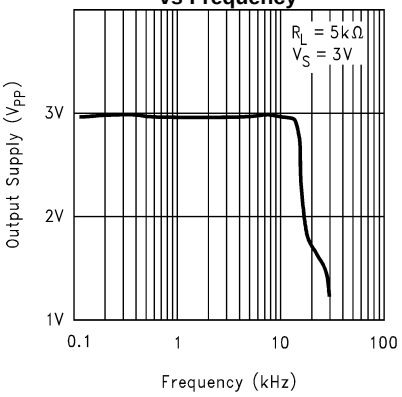

Figure 16.

Z_{OUT} vs Frequency

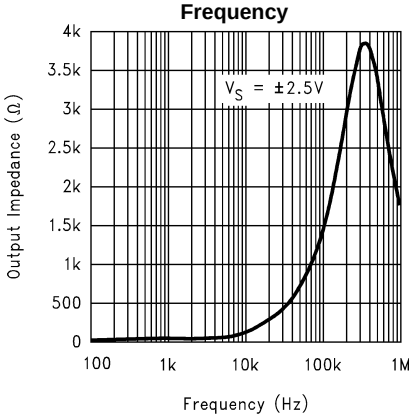

Figure 17.

Slew Rate vs Supply Voltage

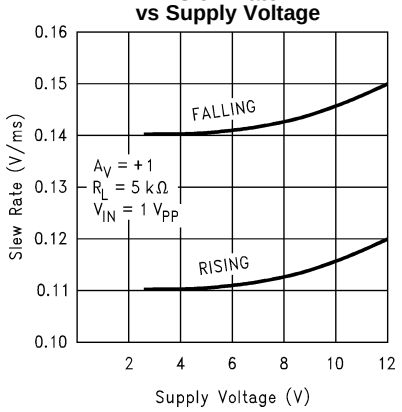

Figure 18.

Non-Inverting Large Signal Pulse Response

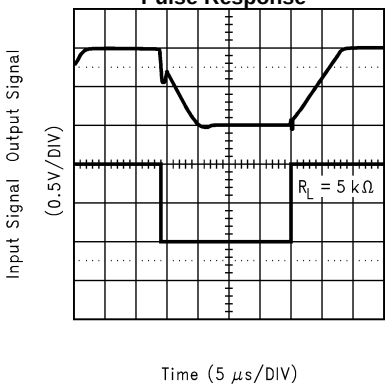

Figure 19.

Non-Inverting Small Signal Pulse Response

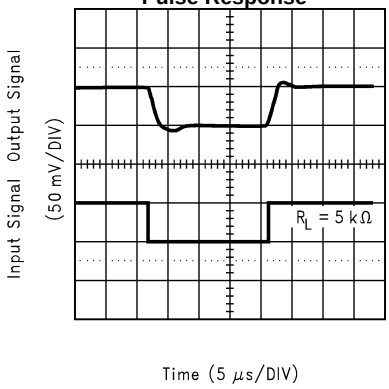

Figure 20.

Typical Performance Characteristics (continued)

V_S = +3V, T_A = 25°C, Unless otherwise specified

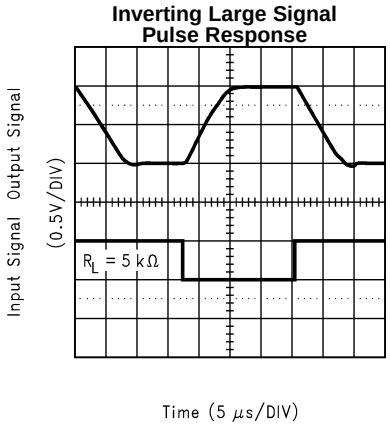

Figure 21.

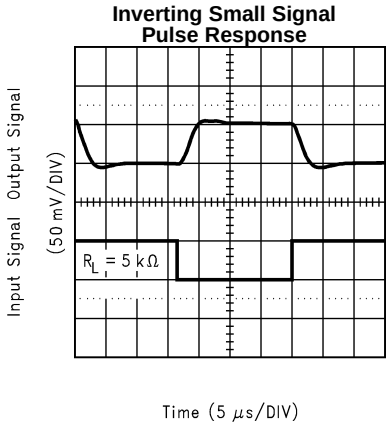

Figure 22.

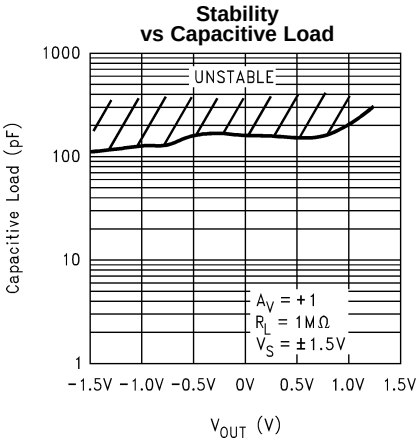

Figure 23.

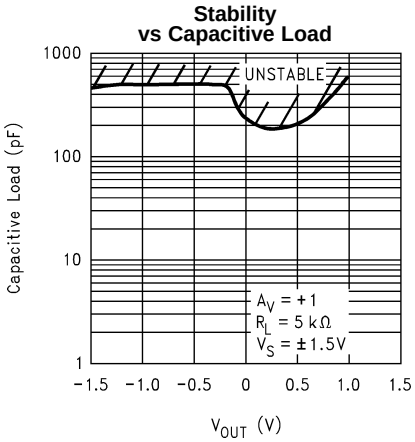

Figure 24.

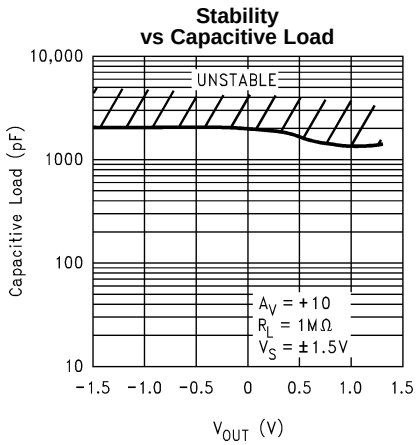

Figure 25.

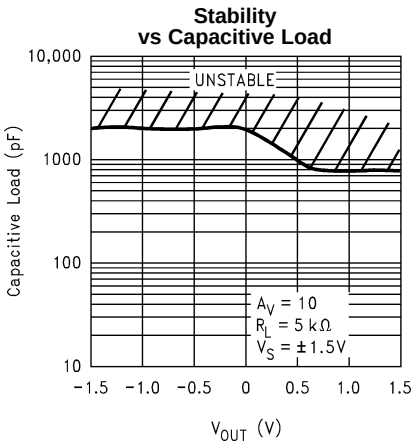

Figure 26.

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Typical Performance Characteristics (continued)

V_S = +3V, T_A = 25°C, Unless otherwise specified

Bandwidth vs Capacitive Load

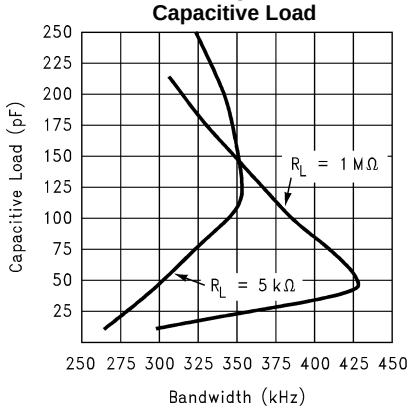

Figure 27.

Capacitive Load vs Phase Margin

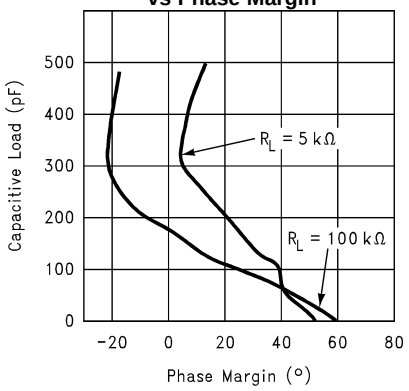

Figure 28.

Capacitive Load vs Gain Margin

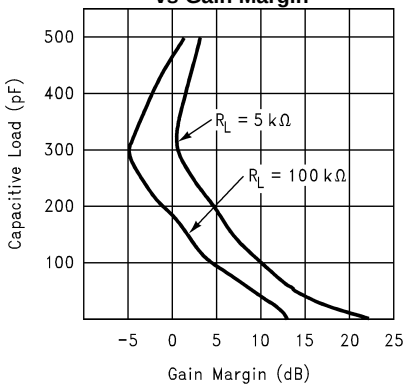

Figure 29.

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APPLICATIONS HINTS

LOW VOLTAGE AMPLIFIER TOPOLOGY

The LMC6574/2 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6574/2 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6574/2.

Although the LMC6574/2 is highly stable over a wide range of operating conditions, a large feedback resistor will react even with small values of capacitance at the input of the op-amp to reduce phase margin. The capacitance at the input of the op-amp comes from transducers, photodiodes and circuit board parasitics.

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 30) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

When high input impedances are demanded, guarding of the LMC6574/2 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

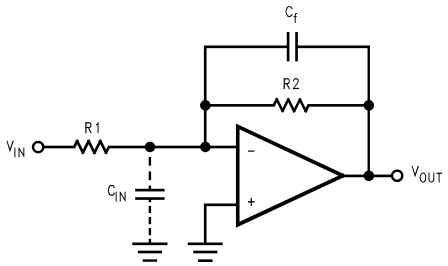

Figure 30. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 31.

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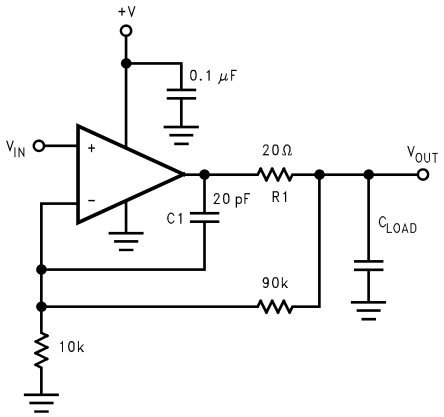


Figure 31. LMC6574/2 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 31, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6574/2, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6574/2's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 32. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6574/2's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 35 for typical connections of guard rings for standard op-amp configurations.

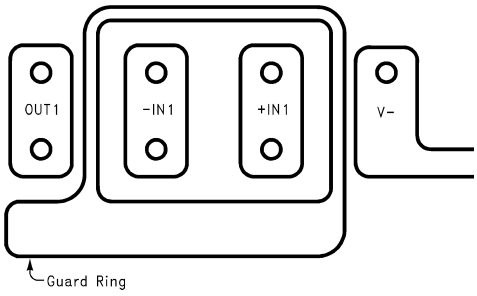


Figure 32. Example of Guard Ring in P.C. Board Layout

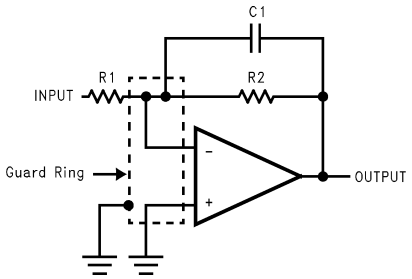


Figure 33. Inverting Amplifier

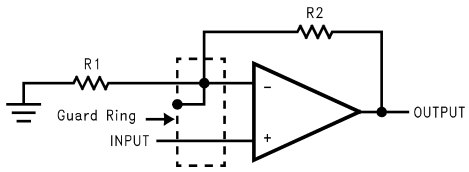
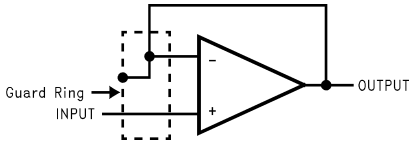


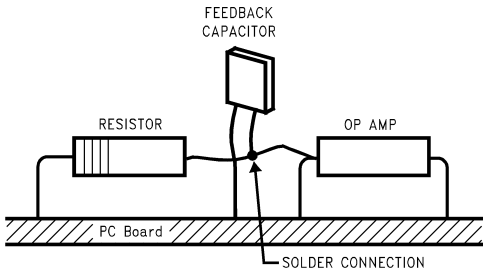
Figure 34. Non-Inverting Amplifier



Follower

Figure 35. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 36.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

Figure 36. Air Wiring

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SPICE MACROMODEL

A spice macromodel is available for the LMC6574/2. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

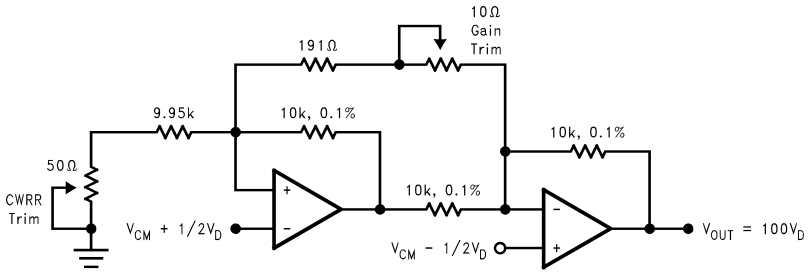

Figure 37. Low-Power Two-Op-Amp Instrumentation Amplifier

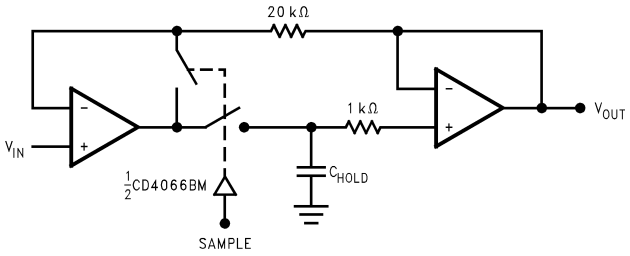

Figure 38. Sample and Hold

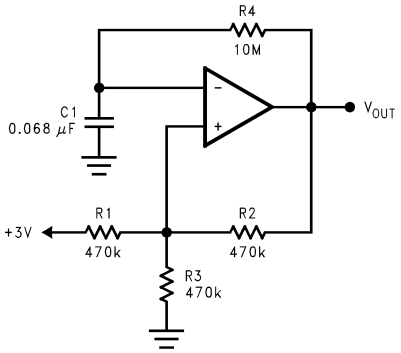

Figure 39. 1 Hz Square Wave Oscillator

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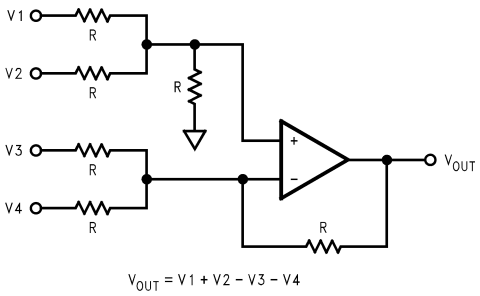

Figure 40. Adder/Subtractor Circuit

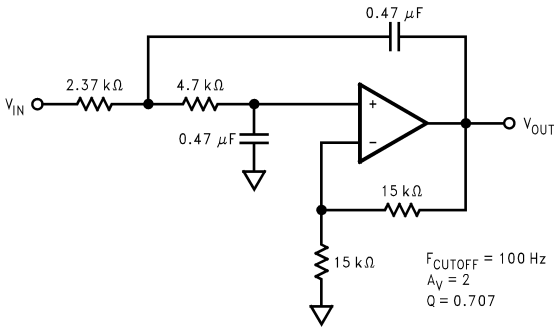

Figure 41. Low Pass Filter

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REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6572AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC65 72AIM	Samples
LMC6572AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC65 72AIM	Samples
LMC6572BIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC65 72BIM	Samples
LMC6572BIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC65 72BIM	Samples
LMC6574AIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6574 AIM	Samples
LMC6574AIMX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LMC6574 AIM	
LMC6574AIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6574 AIM	Samples
LMC6574BIM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6574 BIM	Samples
LMC6574BIMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC6574 BIM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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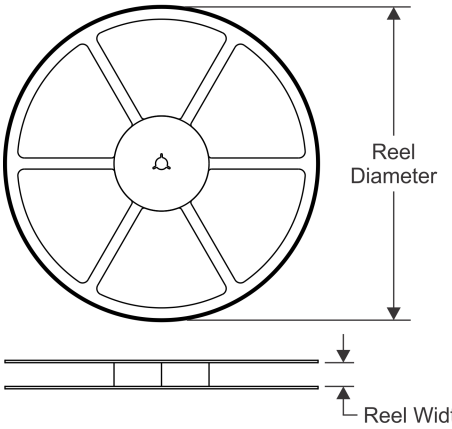
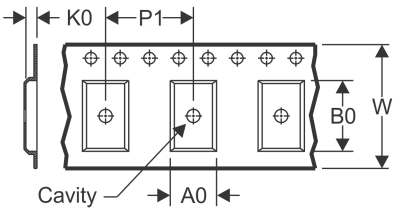
TAPE AND REEL INFORMATION

REEL DIMENSIONS

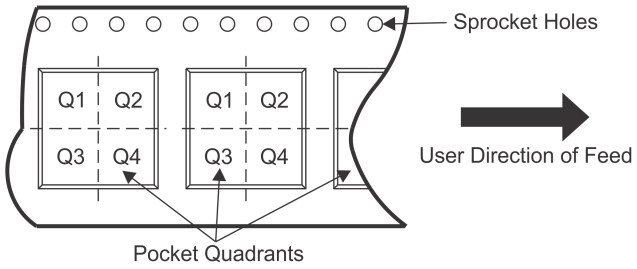


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

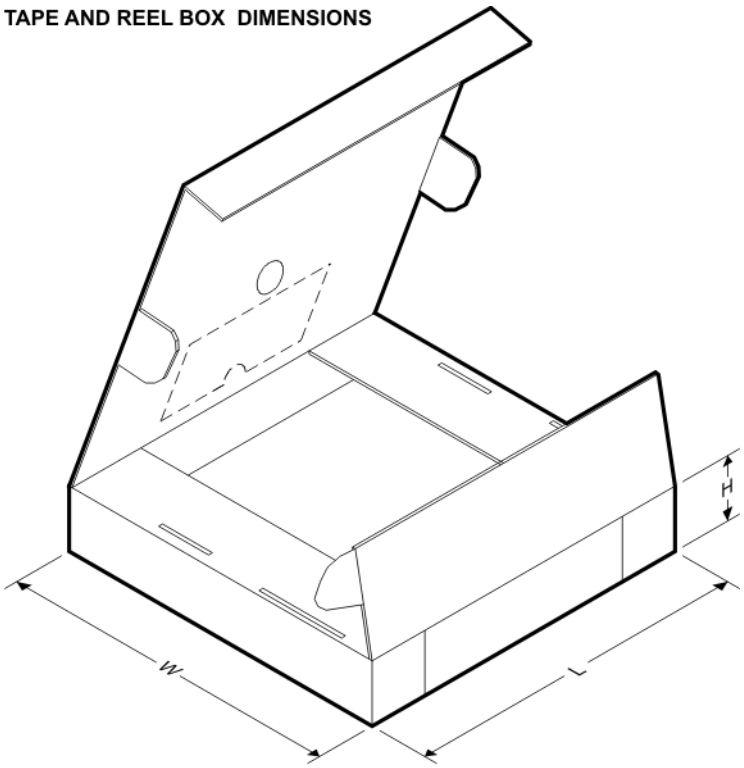
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6572AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6572BIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6574AIMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6574AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMC6574BIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

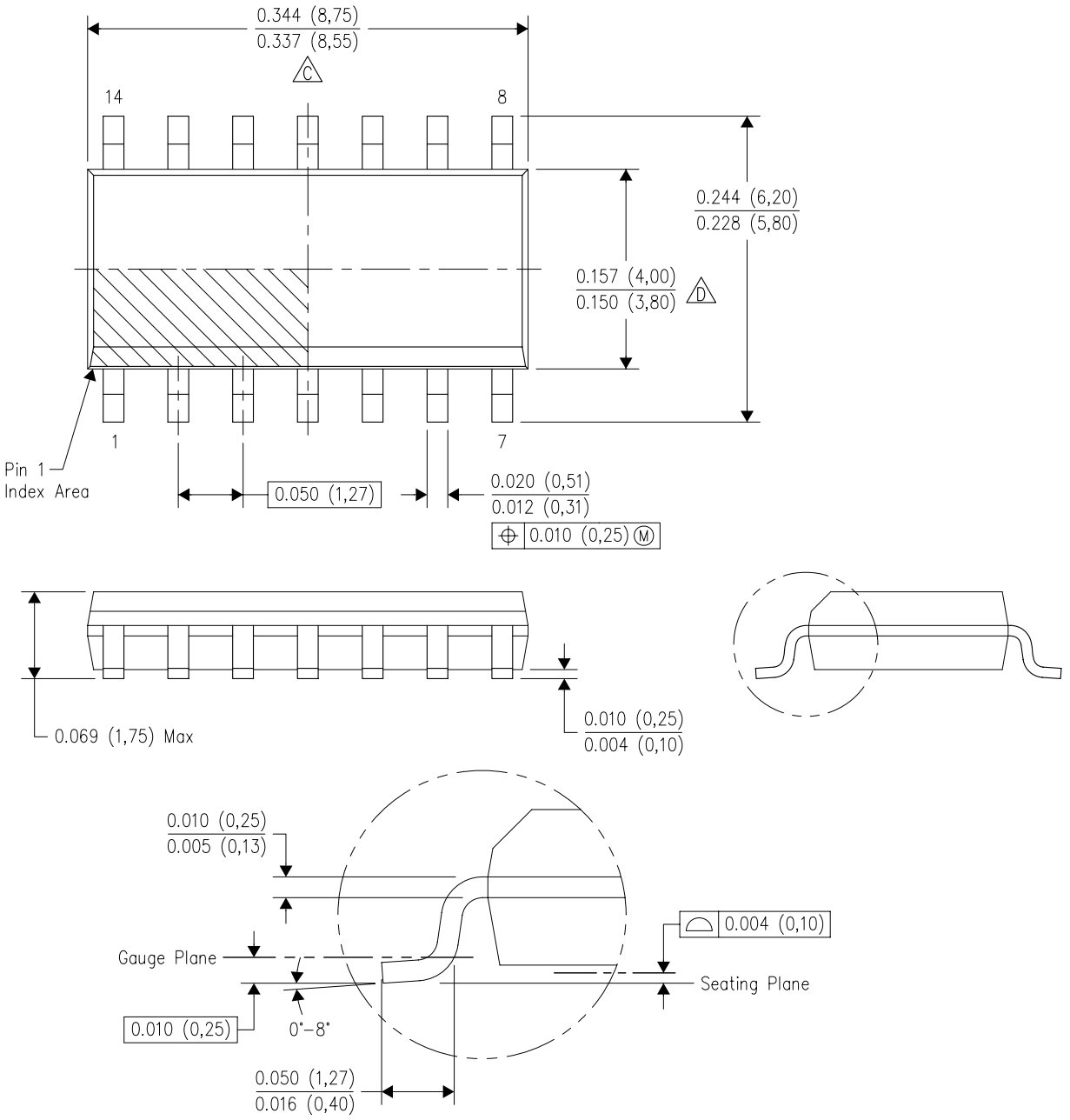
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6572AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6572BIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6574AIMX	SOIC	D	14	2500	367.0	367.0	35.0
LMC6574AIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMC6574BIMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



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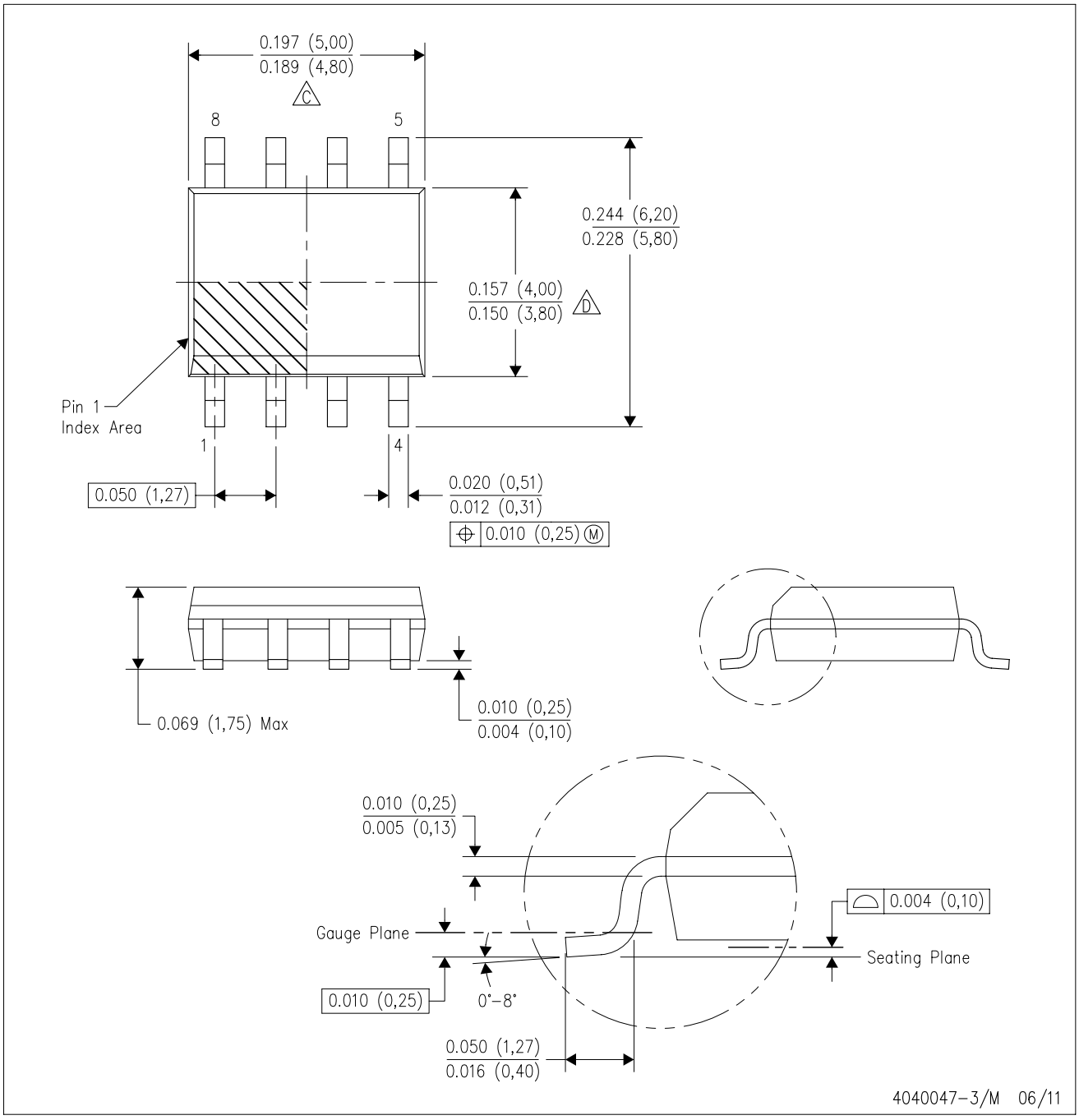
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



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