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General Description

PSoC® 6 MCU is a high-performance, ultra-low-power and secure MCU platform, purpose-built for IoT applications. The PSoC 63 with BLE product family, based on the PSoC 6 MCU platform, is a combination of a high-performance microcontroller with low-power flash technology, digital programmable logic, high-performance analog-to-digital conversion and standard communication and timing peripherals.

The PSoC 63 family provides wireless connectivity with BLE 5.0 compliance.

Features

32-bit Dual CPU Subsystem

- 150-MHz Arm® Cortex®-M4F (CM4) CPU with single-cycle multiply, floating point, and memory protection unit (MPU)
- 100-MHz Cortex-M0+ (CM0+) CPU with single-cycle multiply and MPU
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Active CPU current slope with 1.1-V core operation
 - Cortex-M4: 40 µA/MHz
 - Cortex-M0+: 20 µA/MHz
- Active CPU current slope with 0.9-V core operation
 - Cortex-M4: 22 µA/MHz
 - Cortex-M0+: 15 µA/MHz
- Two DMA controllers with 16 channels each

Memory Subsystem

- 1-MB application flash, 32-KB auxiliary flash (AUXflash), and 32-KB supervisory flash (Sflash); read-while-write (RWW) support. Two 8-KB flash caches, one for each CPU.
- 288-KB SRAM with power and data retention control
- One-time-programmable (OTP) 1-Kb eFuse array

Bluetooth Low Energy (Bluetooth Smart) BT 5.0 Subsystem

- 2.4-GHz RF transceiver with 50-W antenna drive
- Digital PHY
- Link Layer engine supporting master and slave modes
- Programmable output power: up to 4 dBm
- RX sensitivity: -95 dBm
- RSSI: 4-dB resolution
- 5.7 mA TX (0 dBm) and 6.7 mA RX (2 Mbps) current with 3.3-V battery and internal SIMO Buck converter
- Link Layer engine supports four connections simultaneously
- Supports 2 Mbps LE data rate

Low-Power 1.7-V to 3.6-V Operation

- Six power modes for fine-grained power management
- Deep Sleep mode current of 7 µA with 64-KB SRAM retention
- On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-Time Clock

Flexible Clocking Options

- On-chip crystal oscillators (4 to 35 MHz, and 32 kHz)
- Phase-locked Loop (PLL) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with ±2% accuracy
- Ultra-low-power 32-kHz Internal Low-speed Oscillator (ILO)
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Quad SPI (QSPI)/Serial Memory Interface (SMIF)

- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4-KB cache for greater XIP performance with lower power
- Supports single, dual, quad, dual-quad, and octal interfaces w/ throughput up to 640 Mbps

Serial Communication

- Nine run-time configurable serial communication blocks (SCBs)
 - Eight SCBs: configurable as SPI, I²C, or UARTs
 - One Deep Sleep SCB: configurable as SPI or I²C
- USB full-speed device interface

Audio Subsystem

- Two PDM channels and one I²S channel with TDM mode

Timing and Pulse-Width Modulation

- Thirty-two timer/counter pulse-width modulators (TCPWM)
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Programmable Analog

- 12-bit 1-Msps SAR ADC with differential and single-ended modes and 16-channel sequencer with result averaging
- Two low-power comparators available in Deep Sleep and Hibernate modes
- Built-in temp sensor connected to ADC
- One 12-bit voltage mode DAC with < 2-µs settling time
- Two opamps with low-power operation modes

Up to 84 Programmable GPIOs

- Two Smart I/O ports (16 I/Os) enable Boolean operations on GPIO pins; available during system Deep Sleep
- Programmable drive modes, strengths, and slew rates
- Six overvoltage-tolerant (OVT) pins

LCD

- LCD segment direct block support up to 61 segments and up to 8 commons
- Operates in Active, Sleep, and Deep Sleep modes

Capacitive Sensing

- Cypress CapSense provides best-in-class SNR, liquid tolerance, and proximity sensing
- Enables dynamic usage of both self and mutual sensing
- Automatic hardware tuning (SmartSense™)

Cryptography Accelerators

- Hardware acceleration for symmetric and asymmetric cryptographic methods and hash functions
- True Random Number Generator (TRNG) function

Programmable Digital

- 12 programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs to implement functions such as Communication peripherals (for example, LIN, UART, SPI, I²C, S/PDIF and other protocols), Waveform Generators, Pseudo-Random Sequence (PRS) generation, and many other functions.

Profiler

- Eight counters provide event or duration monitoring of on-chip resources

Packages

- 124-BGA and 104-MCSP; with USB
- 116-BGA, 104-MCSP, and 68-QFN; no USB

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Development Ecosystem

PSoC 6 MCU Resources

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC 6 MCU:

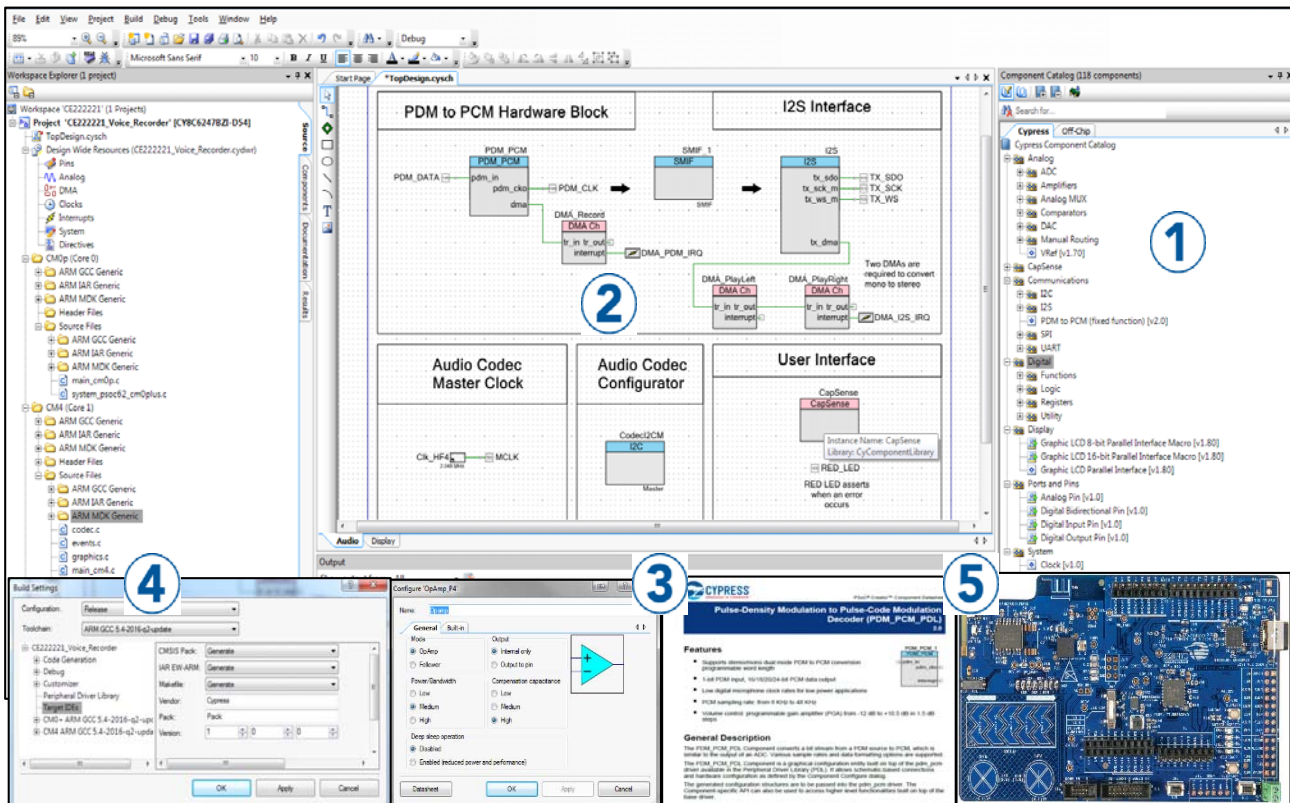
- **Overview:** [PSoC Portfolio](#), [PSoC Roadmap](#)
- **Product Selectors:** [PSoC 6 MCU](#)
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
 - [AN221774](#): Getting Started with PSoC 6 MCU
 - [AN210781](#): Getting Started with PSoC 6 MCU BLE
 - [AN218241](#): PSoC 6 MCU Hardware Design Guide
 - [AN213924](#): PSoC 6 MCU Device Firmware Update Guide
 - [AN215656](#): PSoC 6 MCU Dual-CPU System Design
 - [AN219528](#): PSoC 6 MCU Power Reduction Techniques
 - [AN221111](#): PSoC 6 MCU Creating a Secure System
 - [AN85951](#): PSoC 4, PSoC 6 MCU CapSense Design Guide
- **Code Examples** demonstrate product features and usage, and are also available on [Cypress GitHub repositories](#).
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of PSoC 6 MCU architecture and registers.
- **PSoC 6 MCU Programming Specification** provides the information necessary to program PSoC 6 MCU nonvolatile memory
- **Development Tools**
 - [ModusToolbox™](#) enables cross platform code development with a robust suite of tools and software libraries
 - [CY8CKIT-062-BLE](#) - PSoC 6 BLE Pioneer Kit: a hardware platform that enables design and debug of the PSoC 63 BLE product line.
 - [CY8CPROTO-063-BLE](#) PSoC 6 BLE Prototyping Kit: a low-cost PSoC 63 BLE kit with a snap-away form factor.
 - [PSoC 6 CAD libraries](#) provide footprint and schematic support for common tools. [BSDL files](#) are also available.
- **Training Videos** are available on a wide range of topics including the [PSoC 6 MCU 101 series](#)
- **Cypress Developer Community** enables connection with fellow PSoC developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated [PSoC 6 MCU Community](#)

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on PSoC 6 MCU. As shown below, with PSoC Creator, you can:

1. Explore the library of 200+ Components in PSoC Creator
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component Configuration Tools and the Component datasheets
4. Co-design your application firmware and hardware in the PSoC Creator IDE or build project for 3rd party IDE
5. Prototype your solution with the PSoC 6 Pioneer Kits. If a design change is needed, PSoC Creator and Components enable you to make changes on the fly without the need for hardware revisions.

Figure 1. PSoC Creator Schematic Entry and Components



ModusToolbox™ IDE and the PSoC 6 SDK

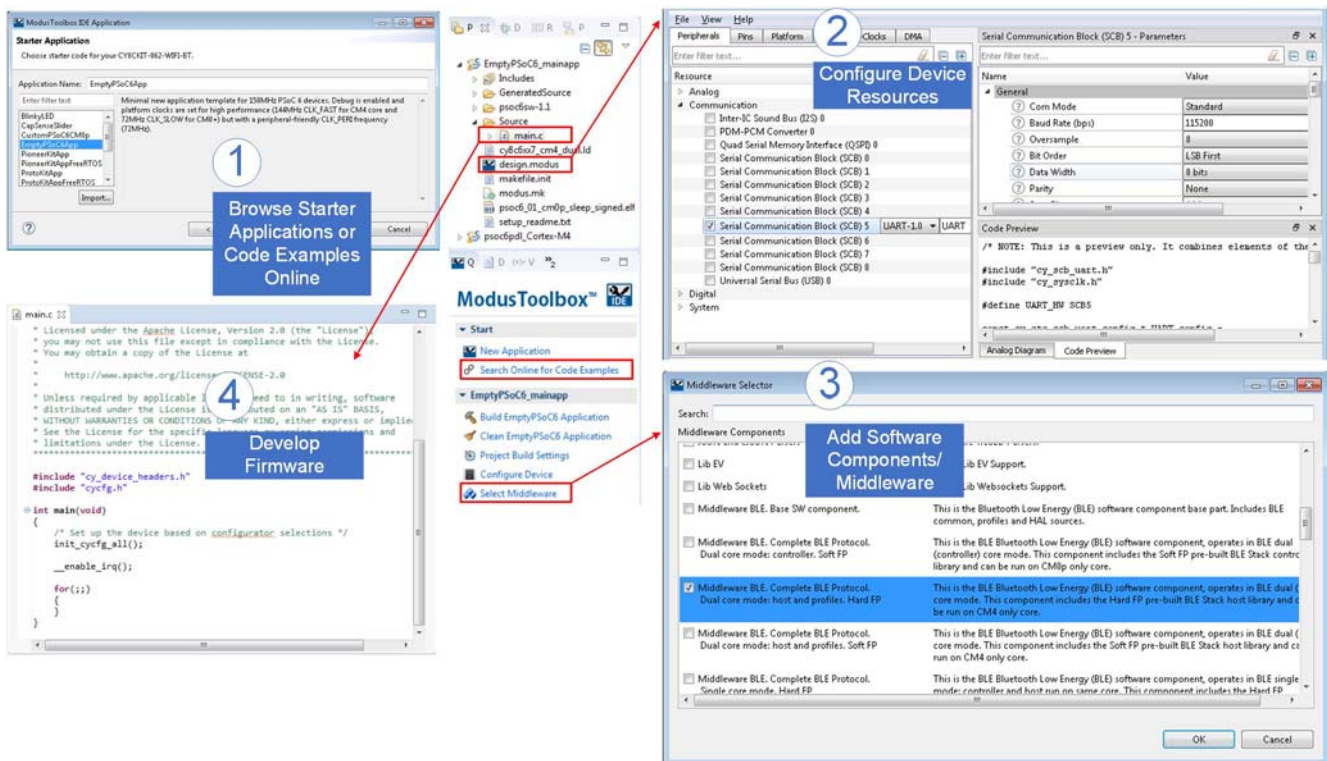
ModusToolbox is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox IDE and the PSoC 6 SDK. The ModusToolbox IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

The PSoC 6 SDK is the software development kit for the PSoC 6 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional detail on using the Cypress tools, refer to [AN221774: Getting Started with PSoC 6 MCU](#) and the documentation and help integrated into ModusToolbox. As [Figure 2](#) shows, with the ModusToolbox IDE, you can:

1. Create a new application based on a list of starter applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in *design.modus* to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

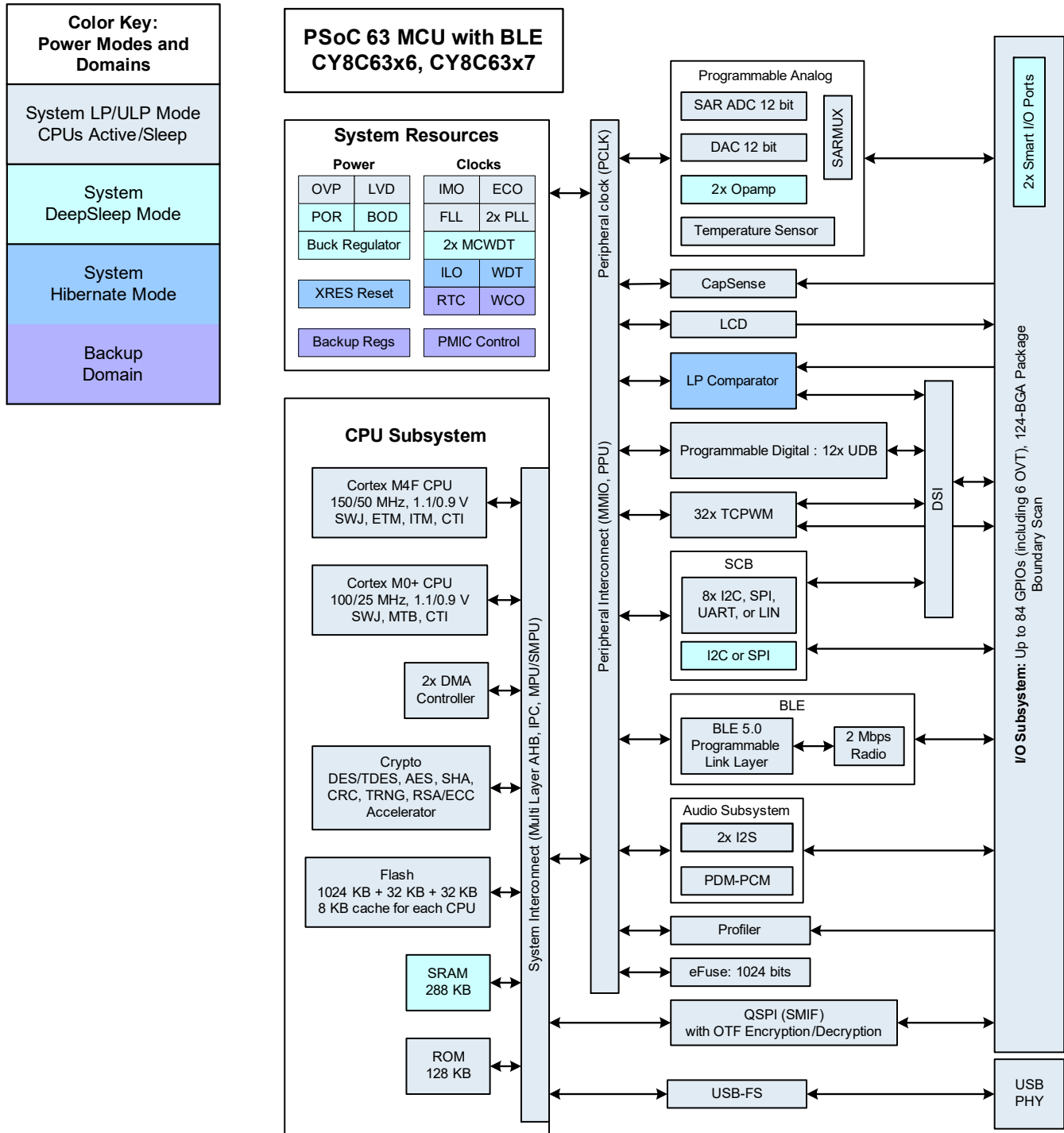
Figure 2. ModusToolbox IDE Resources and Middleware



Blocks and Functionality

Figure 3 shows the major subsystems and a simplified view of their interconnections. The color coding shows the lowest power mode where a block is still functional. For example, the SRAM is functional down to Deep Sleep mode.

Figure 3. Block Diagram



There are three debug access ports, one each for CM4 and CM0+, and a system port. The PSoC 6 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. All device interfaces can be permanently disabled (device security) for applications concerned about attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is settable by the user.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox and PSoC Creator Integrated Development Environments (IDE) provides fully integrated programming and debug support for these devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, PSoC 6 provides a very high level of security.

Functional Description

The following sections provide an overview of the features, capabilities and operation of each functional block identified in the block diagram in [Figure 3](#). For more detailed information, refer to the following three references.

- **Peripheral Driver Library (PDL) Application Programming Interface (API) Reference Manual.**

PDL provides low-level drivers for each resource in the device, and supports the entire PSoC 6 MCU portfolio. PDL is an element of the PSoC 6 SDK, which is installed as part of [ModusToolbox](#). With ModusToolbox installed, you can access the PDL API reference manual either from the Documentation tab of the Quick Panel, or you can navigate directly to it at `<install_directory>\ModusToolbox_<version>\libraries\psoc6sw-<version>\docs`. Using PDL should be the primary means of interacting with the PSoC 6 MCU hardware.

- **Architecture Technical Reference Manual (TRM)**

The architecture TRM provides the detailed description of each resource in the device. This is the next reference to use if it is necessary to understand the operation of the hardware below the software provided by PDL. It describes the architecture and functionality of each resource and explains the operation of each resource in all modes. It provides specific guidance regarding the use of associated registers.

- **Register Technical Reference Manual**

The register TRM provides the complete list of all registers in the device. It includes the breakdown of all register fields, their possible settings, read/write accessibility, and default states. All registers that have a reasonable use in typical applications have functions to access them from within PDL. Note that ModusToolbox and PDL may provide software default conditions for some registers that are different from and override the hardware defaults.

CPU and Memory Subsystem

PSoC 6 has multiple bus masters, as [Figure 3](#) shows. They are: CPUs, DMA controllers, and a Crypto block. Generally, all memory and peripherals can be accessed and shared by all bus masters through multi-layer Arm AMBA high-performance bus (AHB) arbitration. Accesses between CPUs can be synchronized using an inter-processor communication (IPC) block.

CPU

There are two Arm Cortex CPUs:

The Cortex-M4 (CM4) has single-cycle multiply, a floating-point unit (FPU), and a memory protection unit (MPU). It can run at up to 150 MHz. This is the main CPU, designed for a short interrupt response time, high code density, and high throughput.

CM4 implements a version of the Thumb instruction set based on Thumb-2 technology (defined in the *Armv7-M Architecture Reference Manual*). The Cortex M4 is used for user Application code.

The Cortex-M0+ (CM0+) has single-cycle multiply, and an MPU. It can run at up to 100 MHz; however, for CM4 speeds above 100 MHz, CM0+ and bus peripherals are limited to half the speed of CM4. Thus, for CM4 running at 150 MHz, CM0+ and peripherals are limited to 75 MHz.

CM0+ is the secondary CPU; it is used to implement system calls and device-level security, safety, and protection features. CM0+ provides a secure, uninterruptible boot function. This guarantees that post boot, system integrity is checked and memory and peripheral access privileges are enforced.

CM0+ implements the Armv6-M Thumb instruction set (defined in the *Armv6-M Architecture Reference Manual*).

The CPUs have the following power draw, at $V_{DD} = 3.3\text{ V}$ and using the internal buck regulator:

Table 1. Active Current Slope at $V_{DD} = 3.3\text{ V}$ Using the Internal Buck Regulator

| | | System Power Mode | |
|-----|------------|-----------------------------|-----------------------------|
| | | ULP | LP |
| CPU | Cortex-M0+ | 15 $\mu\text{A}/\text{MHz}$ | 20 $\mu\text{A}/\text{MHz}$ |
| | Cortex-M4 | 22 $\mu\text{A}/\text{MHz}$ | 40 $\mu\text{A}/\text{MHz}$ |

The CPUs can be selectively placed in their Sleep and Deep Sleep power modes as defined by Arm.

Both CPUs have nested vectored interrupt controllers (NVIC) for rapid and deterministic interrupt response, and wakeup interrupt controllers (WIC) for CPU wakeup from Deep Sleep power mode.

The CPUs have extensive debug support. PSoC 6 has a debug access port (DAP) that acts as the interface for device programming and debug. An external programmer or debugger (the “host”) communicates with the DAP through the device serial wire debug (SWD) or Joint Test Action Group (JTAG) interface pins. Through the DAP (and subject to device security restrictions), the host can access the device memory and peripherals as well as the registers in both CPUs.

Each CPU offers debug and trace features as follows:

- CM4 supports six hardware breakpoints and four watchpoints, 4-bit embedded trace macrocell (ETM), serial wire viewer (SWV), and printf()-style debugging through the single wire output (SWO) pin.
- CM0+ supports four hardware breakpoints and two watchpoints, and a micro trace buffer (MTB) with 4 KB dedicated RAM.

PSoC 6 also has an Embedded Cross Trigger for synchronized debugging and tracing of both CPUs.

Interrupts

PSoC 6 has 147 system and peripheral interrupt sources and supports interrupts and system exception on both CPUs. CM4 has 147 interrupt request lines (IRQ), with the interrupt source ‘n’ directly connected to IRQn. CM0+ has 32 interrupts IRQ[31:0] with configurable mapping of one system interrupt source to any of the IRQ[31:0].

Each interrupt supports configurable priority levels (eight levels for CM4 and four levels for CM0+). One system interrupt can be mapped to each of the CPUs' non-maskable interrupts (NMI). Up to 41 interrupt sources are capable of waking the device from Deep Sleep power mode using the WIC. Refer to the technical reference manual for details.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus. The descriptors for DMA channels can be in SRAM or flash. Therefore, the number of descriptors are limited only by the size of the memory. Each descriptor can transfer data in two nested loops with configurable address increments to the source and destination. The size of data transfer per descriptor varies based on the type of DMA channel. Refer to the technical reference manual for detail.

Cryptography Accelerator (Crypto)

This subsystem consists of hardware implementation and acceleration of cryptographic functions and random number generators.

The Crypto subsystem supports the following:

- Encryption/Decryption Functions
 - Data Encryption Standard (DES)
 - Triple DES (3DES)
 - Advanced Encryption Standard (AES) (128-, 192-, 256-bit)
 - Elliptic Curve Cryptography (ECC)
 - RSA cryptography functions
- Hashing functions
 - Secure Hash Algorithm (SHA)
 - SHA1
 - SHA224/256/384/512
- Message authentication functions (MAC)
 - Hashed message authentication code (HMAC)
 - Cipher-based message authentication code (CMAC)
- 32-bit cyclic redundancy code (CRC) generator
- Random number generators
 - Pseudo random number generator (PRNG)
 - True random number generator (TRNG)

Protection Units

PSoC 63 with BLE has multiple types of protection units to control erroneous or unauthorized access to memory and peripheral registers. CM4 and CM0+ have Arm MPUs for protection at the bus master level. Other bus masters use additional MPUs. Shared memory protection units (SMPUs) help implement memory protection for memory/ resources that are shared among multiple bus masters. Peripheral protection units (PPU) are similar to SMPUs but are designed for protecting the peripheral register space.

Protection units support memory and peripheral access attributes including address range, read/write, code/data, privilege level, secure/non-secure, and protection context.

Protection units are configured at secure boot to control access privileges and rights for bus masters and peripherals.

Up to eight protection contexts (secure boot is in protection context 0) allow access privileges for memory and system resources to be set by the secure boot process per protection context by bus master and code privilege level. Multiple protection contexts are supported on the CPUs and the other bus masters.

Memory

PSoC 6 contains flash, SRAM, ROM, and eFuse memory blocks.

■ Flash

There is up to 1 MB of application flash, organized in 256 KB sectors. There are also two 32-KB flash sectors:

- Auxiliary flash (AUXflash), typically used for EEPROM emulation
- Supervisory flash (Sflash). Data stored in Sflash includes device trim values, [Flash Boot](#) code, and encryption keys. After the device transitions into the Secure lifecycle stage, Sflash can no longer be changed.

The flash has 128-bit-wide accesses to reduce power. Write operations can be performed at the row level. A row is 512 bytes. Read operations are supported in both System Low Power and Ultra-Low Power modes, however write operations may not be performed in System Ultra-Low Power mode.

The flash has two caches, one for each CPU. Each cache is 8 KB, with 4-way set associativity.

■ SRAM

There is 288 KB of SRAM memory available for applications. It can be fully retained or retained in increments of user-designated 32-KB blocks.

■ ROM

The 128-KB ROM, also referred to as the supervisory ROM (SROM), provides code ([ROM Boot](#)) for several system functions. The PSoC 6 MCU ROM contains device initialization, flash write, security, eFuse programming, and other system-level routines. ROM code is executed only by the CM0+ CPU, in protection context 0. A system function can be initiated by either CPU, or through the DAP. This causes an NMI in CM0+, which causes CM0+ to execute the system function.

■ eFuse

A one-time-programmable (OTP) eFuse array consists of 1024 bits, of which 512 are reserved for system use, such as die ID, device ID, initial trim settings, device life cycle, and security settings. The remaining bits are available for storing security key information, hash values, unique IDs or similar custom content.

Each fuse is individually programmed; once programmed (or “blown”), its state cannot be changed. Blowing a fuse transitions it from the default state of 0 to 1. To program an eFuse, V_{DDIO} must be at $2.5\text{ V} \pm 5\%$, at 14 mA.

Because blowing an eFuse is an irreversible process, programming is recommended only in mass production programming under controlled factory conditions. For more information, see [PSoC 6 MCU Programming Specifications](#).

Boot Code

Two blocks of code, [ROM Boot](#) and [Flash Boot](#), are pre-programmed into the device and work together to provide device startup and configuration, basic security features, life-cycle stage management and other system functions.

■ ROM Boot

On a device reset, the boot code in ROM is the first code to execute. This code performs the following:

- Integrity checks of flash boot code
- Device trim setting (calibration)
- Setting the device protection units
- Setting device access restrictions for secure life-cycle states

ROM cannot be changed and acts as the Root of Trust in a secure system.

■ Flash Boot

Flash boot is a firmware module stored in Sflash and application flash. It ensures that only a validated application may run on the device. It also ensures that the firmware image has not been modified, such as by a malicious third party.

Flash boot:

- Is validated by ROM Boot
- Runs after ROM Boot and before the user application
- Verifies the integrity of the user application
- Enables system calls
- Configures the Debug Access Port
- Launches the user application in the CM0+ (CM4 for single-CPU devices).

If the user application cannot be validated, then flash boot ensures that the device is transitioned into a safe state.

Memory Map

Both CPUs have a fixed address map, with shared access to memory and peripherals. The 32-bit (4 GB) address space is divided into the regions shown in [Table 2](#). Note that code can be executed from the code and SRAM regions.

Table 2. Address Map for CM4 and CM0+

| Address Range | Name | Use |
|----------------------------|------------------------|---|
| 0x0000 0000 – 0x1FFF FFFF | Code | Program code region. Data can also be placed here. It includes the exception vector table, which starts at address 0. |
| 0x2000 0000 – 0x3FFF FFFF | SRAM | Data region. This region is not supported in PSoC 6. |
| 0x4000 0000 – 0x5FFF FFFF | Peripheral | All peripheral registers. Code cannot be executed from this region. CM4 bit-band in this region is not supported in PSoC 6. |
| 0x6000 0000 – 0x9FFF FFFF | External RAM | SMIF or Quad SPI, (see the QSPI Interface Serial Memory Interface (SMIF) section). Code can be executed from this region. |
| 0xA000 0000 – 0xDFFF FFFF | External Device | Not used. |
| 0xE000 0000 – 0xE00F FFFF | Private Peripheral Bus | Provides access to peripheral registers within the CPU core. |
| 0xE010 0A000 – 0xFFFF FFFF | Device | Device-specific system registers. |

The device memory map shown in [Table 3](#) applies to both CPUs. That is, the CPUs share access to all PSoC 6 MCU memory and peripheral registers. Note that code can be executed from the Code, SRAM, and External RAM regions.

Table 3. Internal Memory Address Map for CM4 and CM0+

| Address Range | Memory Type | Size |
|---------------------------|---|--------------|
| 0x0000 0000 – 0x0001 FFFF | ROM | 128 KB |
| 0x0800 0000 – 0x0804 7FFF | SRAM | Up to 288 KB |
| 0x1000 0000 – 0x100F FFFF | Application flash | Up to 1 MB |
| 0x1400 0000 – 0x1400 7FFF | Auxiliary flash, can be used for EEPROM emulation | 32 KB |
| 0x1600 0000 – 0x1600 7FFF | Supervisory flash | 32 KB |
| 0x1800 0000 – 0x1FFF FFFF | External memory execute in place region | Up to 128 MB |

Note that the SRAM is located in the Code region for both CPUs (see [Table 2](#)). There is no physical memory located in the CPUs' SRAM region.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) when the power supply drops below specified levels. The design guarantees safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the reset occurring. There are no voltage sequencing requirements.

The V_{DD} supply (1.7 to 3.6 V) powers an on-chip buck regulator or an LDO, selectable by the user. In addition, both the buck and the LDO offer a selectable (0.9 or 1.1 V) core operating voltage (V_{CCD}). The selection lets users choose between two system power modes:

- System Low Power (LP) operates V_{CCD} at 1.1 V and offers high performance, with no restrictions on any of the device configurations.
- System Ultra Low Power (ULP) operates V_{CCD} at 0.9 V for exceptional low power results, but imposes limitations on maximum clock speeds.

An additional backup domain adds an “always on” functionality using a separate power domain supplied by a backup supply (V_{BACKUP}) such as a battery or supercapacitor. It includes a real-time clock (RTC) with alarm feature, supported by a 32.768-kHz watch crystal oscillator (WCO), and power-management IC (PMIC) control. Pin 5 of Port 0 (P0.5) can be assigned as an enable signal for an external PMIC. RTC alarms can be used as a trigger for the PMIC enable signal.

Power Modes

PSoC 6 MCU can operate in four system and three CPU power modes. These modes are intended to minimize the average power consumption in an application. For more details on power modes and other power-saving configuration options, see the application note, [AN219528: PSoC 6 MCU Low-Power Modes and Power Reduction Techniques](#) and the [Architecture TRM, Power Modes](#) chapter.

Power modes supported by PSoC 6 MCUs, in the order of decreasing power consumption, are:

- System Low Power (LP) – All peripherals and CPU power modes are available at maximum speed
- System Ultra Low Power (ULP) – All peripherals and CPU power modes are available, but with limited speed
- CPU Active – CPU is executing code in system LP or ULP mode
- CPU Sleep – CPU code execution is halted in system LP or ULP mode
- CPU Deep Sleep – CPU code execution is halted and system Deep Sleep is requested in system LP or ULP mode
- System Deep Sleep – Only low-frequency peripherals are available after both CPUs enter CPU Deep Sleep mode
- System Hibernate – Device and I/O states are frozen and the device resets on wakeup

CPU Active, Sleep, and Deep Sleep are standard Arm-defined power modes supported by the Arm CPU instruction set architecture (ISA). LP, ULP, Deep Sleep and Hibernate modes are additional low-power modes supported by PSoC 6 MCU. Hibernate mode is the lowest power mode in the PSoC 6 MCU and on wakeup, the CPU and all peripherals go through a reset.

Clock System

The PSoC 63 clock system consists of the following (see [Figure 4](#)):

- IMO
- ILO/PILO
- Watch crystal oscillator (WCO)
- External MHz crystal oscillator (ECO)
- External clock input
- One PLL
- One FLL

Clocks may be buffered and brought out to a pin on a smart I/O port.

IMO Clock Source

The IMO is the primary source of internal clocking. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is $\pm 2\%$ and its current consumption is less than 10 μA .

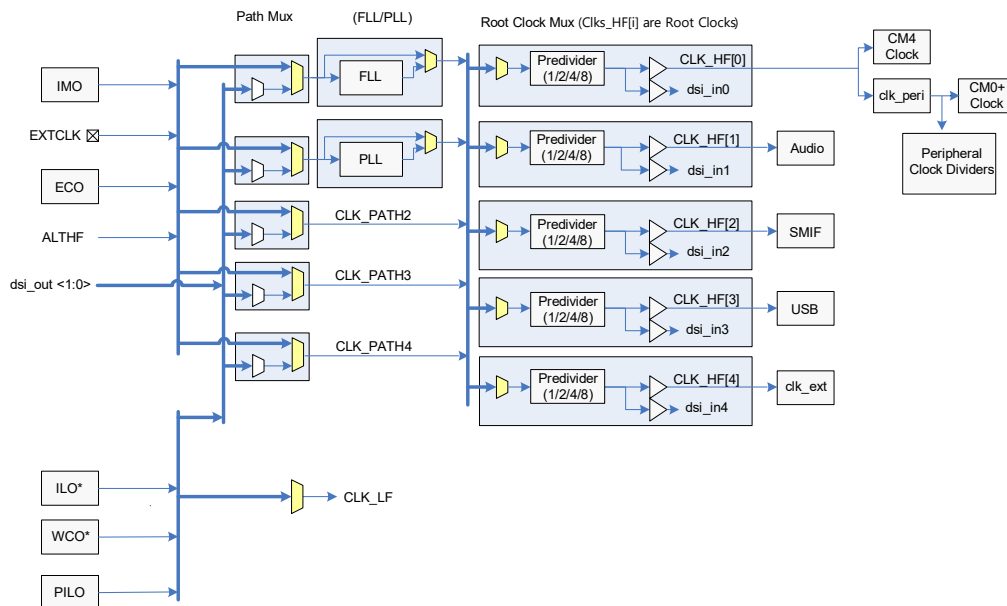
ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which operates in all power modes. The ILO can be calibrated against a higher accuracy clock for better accuracy.

Precision ILO (PILO)

PILO is an additional source that can provide a more accurate 32.768-kHz clock than ILO when periodically calibrated using a high-accuracy clock such as the ECO. The PILO works in Deep Sleep and higher modes. It does not work in Hibernate mode.

Figure 4. Clocking Diagram



Watchdog Timers (WDT, MCWDT)

PSoC 6 has one WDT and two multi-counter WDTs (MCWDT). The WDT has a 16-bit free-running counter. Each MCWDT has two 16-bit counters and one 32-bit counter, with multiple operating modes. All of the 16-bit counters can generate a watchdog device reset. All of the counters can generate an interrupt on a match event.

The WDT is clocked by the ILO. It can do interrupt/wakeup generation in LP/ULP, Deep Sleep, and Hibernate power modes. The MCWDTs are clocked by LFCLK (ILO or WCO). It can do periodic interrupt / wakeup generation in LP/ULP and Deep Sleep power modes.

Clock Dividers

Integer and fractional clock dividers are provided for peripheral use and timing purposes. There are:

- Eight 8-bit clock dividers
- Sixteen 16-bit integer clock dividers
- Four 16.5-bit fractional clock dividers
- One 24.5-bit fractional clock divider

Trigger Routing

PSoC 6 MCU contains a trigger multiplexer block. This is a collection of digital multiplexers and switches that are used for routing trigger signals between peripheral blocks and between GPIOs and peripheral blocks.

Use cases include:

- Routing the ADC end of conversion signal to DMA to move the ADC result into memory
- Routing the comparator output to trigger a timer, etc.

Some of the trigger multiplexers include logic for inversion and edge detection of trigger signals.

Reset

PSoC 6 MCU can be reset from a variety of sources:

- Power-on reset (POR) to hold the device in reset while the power supply ramps up to the level required for the device to function properly. POR activates automatically at power-up.
- Brown-out detect (BOD) reset to monitor the digital voltage supply V_{DD} and generate a reset if V_{DD} falls below the minimum required logic operating voltage.
- External reset (XRES) to reset the device using an external input. The XRES pin is active LOW – a logic '1' on the pin has no effect and a logic '0' causes reset. The pin is pulled to logic '1' inside the device. XRES is available as a dedicated pin.
- Watchdog timer (WDT or MCWDT) to reset the device if firmware fails to service it within a specified timeout period.
- Software-initiated reset to reset the device on demand using firmware.
- Logic-protection fault can trigger an interrupt to a fault handler or reset the device if unauthorized operating conditions occur; for example, reaching a debug breakpoint while executing privileged code.
- Hibernate wakeup reset to bring the device out of the Hibernate low-power mode.

Reset events are asynchronous and guarantee reversion to a known state. Some of the reset sources are recorded in a register, which is retained through reset and allows software to determine the cause of the reset.

BLE Radio and Subsystem

PSoC 63 with BLE incorporates a Bluetooth Smart subsystem that contains the Physical Layer (PHY) and Link Layer (LL) engines with an embedded security engine. The physical layer consists of the digital PHY and the RF transceiver that transmits and receives GFSK packets at 2 Mbps over a 2.4-GHz ISM band, which is compliant with Bluetooth Smart Bluetooth Specification 5.0. The baseband controller is a composite hardware and firmware implementation that supports both master and slave modes. Key protocol elements, such as HCI and link control, are implemented in firmware. Time-critical functional blocks, such as encryption, CRC, data whitening, and access code correlation, are implemented in hardware (in the LL engine).

The RF transceiver contains an integrated balun, which provides a single-ended RF port pin to drive a 50-Ω antenna via a matching/filtering network. In the receive direction, this block converts the RF signal from the antenna to a digital bit stream after performing GFSK demodulation. In the transmit direction, this block performs GFSK modulation and then converts a digital baseband signal to a radio frequency before transmitting it to air through the antenna.

Key features of BLESS are as follows:

- Master and slave single-mode protocol stack with logical link control and adaptation protocol (L2CAP), attribute (ATT), and security manager (SM) protocols
- API access to generic attribute profile (GATT), generic access profile (GAP), and L2CAP
- L2CAP connection-oriented channel (Bluetooth 4.1 feature)
- GAP features
 - Broadcaster, Observer, Peripheral, and Central roles
 - Security mode 1: Level 1, 2, and 3
 - User-defined advertising data
 - Multiple bond support
- GATT features
 - GATT client and server
 - Supports GATT sub-procedures
 - 32-bit universally unique identifier (UUID) (Bluetooth 4.1 feature)
- Security Manager (SM)
 - Pairing methods: Just works, Passkey Entry, and Out of Band
 - LE Secure Connection Pairing model
 - Authenticated man-in-the-middle (MITM) protection and data signing
- Link Layer (LL)
 - Master and Slave roles
 - 128-bit AES engine
 - Low-duty cycle advertising
 - LE Ping
- Supports all SIG-adopted BLE profiles
- Power levels for Adv (1.28s, 31 bytes, 0 dBm) and Con (300 ms, 0 byte, 0 dBm) are 42 μW and 70 μW respectively

Programmable Analog Subsystem

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. One of three internal reference voltages may be used for the ADC reference voltage. The references are, V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.2 V and trimmed to $\pm 1\%$). An external reference may also be used, by either driving the VREF pin or routing an external reference to GPIO pin P9.7. These reference options allow ratio-metric readings or absolute readings at the accuracy of the reference used. The input range of the ADC is the full supply voltage between V_{SS} and V_{DDA}/V_{DDIOA} . The SAR ADC may be configured with a mix of single ended and differential signals in the same configuration.

The SAR ADC's sample-and-hold (S/H) aperture is programmable to allow sufficient time for signals with a high impedance to settle sufficiently, if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve performance in noisy conditions, an external bypass capacitor for the internal reference amplifier (through the fixed "VREF" pin), may be added.

The SAR is connected to a fixed set of pins through an input multiplexer. The multiplexer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The result of each channel is buffered, so that an interrupt may be triggered only when a full scan of all channels is complete. Also, a pair of range registers can be set to detect and cause an interrupt if an input exceeds a minimum and/or maximum value. This allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software. The SAR can also be connected, under firmware control, to most other GPIO pins via the Analog Multiplexer Bus (AMUXBUS). The SAR is not available in Deep Sleep and Hibernate modes as it requires a high -speed clock (up to 18 MHz). The SAR operating range is 1.71 to 3.6 V.

Temperature Sensor

An on-chip temperature sensor is part of the SAR and may be scanned by the SAR ADC. It consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor may be connected directly to the SAR ADC as one of the measurement channels. The ADC digitizes the temperature sensor's output and a Cypress-supplied software function may be used to convert the reading to temperature which includes calibration and linearization.

12-bit Digital-Analog Converter

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 2 μs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output using an opamp in the CTBm block.

Continuous Time Block (CTBm) with Two Opamps

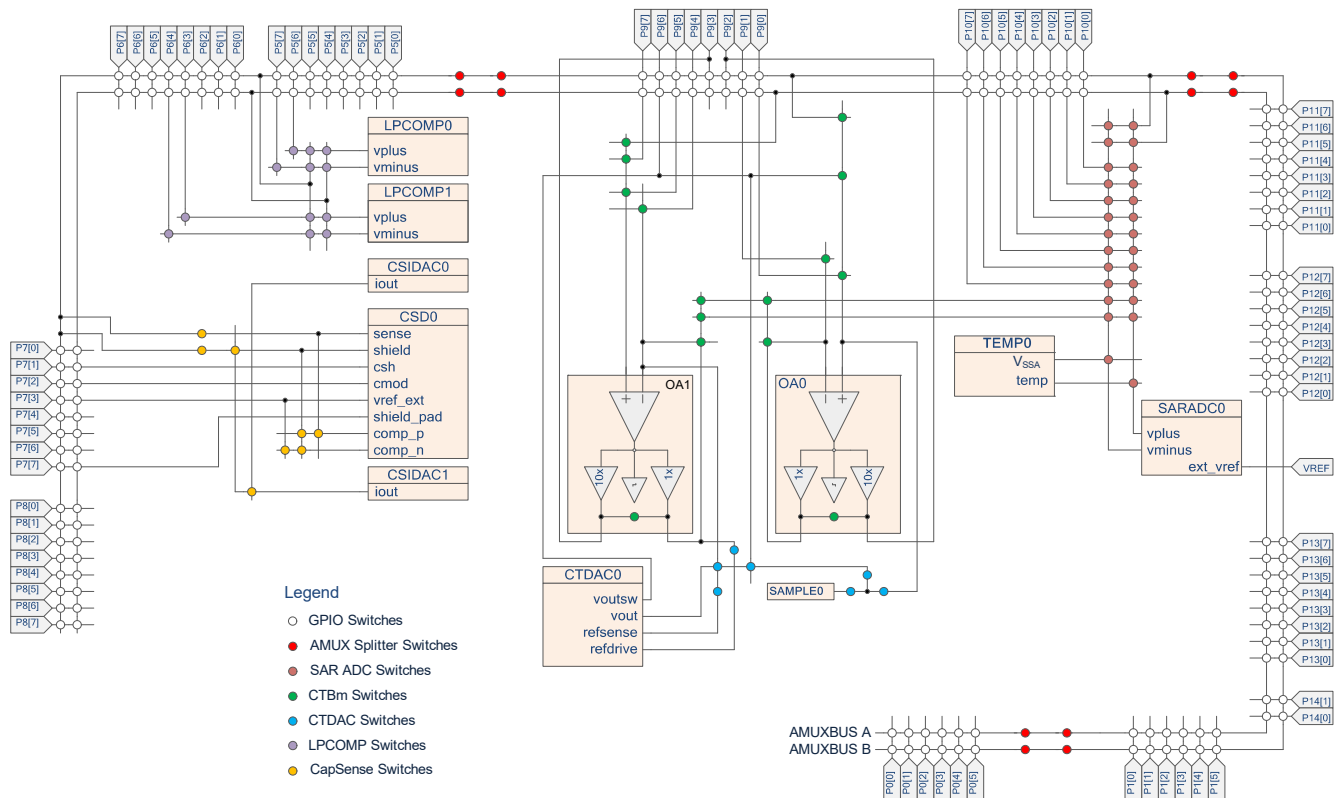
This block consists of two opamps, which have their inputs and outputs connected to pins and other analog blocks, as Figure 5 shows. They have three power modes (high, medium, and low) and a comparator mode. The Opamps can be used to buffer SAR inputs and DAC outputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware.

The opamps also support operation in system Deep Sleep mode, with lower performance and reduced power consumption.

Low-Power Comparators

Two low-power comparators are provided, which can operate in all power modes. This allows other analog system resources to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Figure 5. Analog Subsystem



Programmable Digital

Smart I/O

Smart I/O™ is a programmable logic fabric that enables Boolean operations on signals traveling from device internal resources to the GPIO pins or on signals traveling into the device from external sources. The Smart I/O block sits between the GPIO pins and the high-speed I/O matrix (HSIOM) and is dedicated to a single port.

There are two Smart I/O blocks: one on Port 8 and one on Port 9. When the Smart I/O is not enabled, all signals on Port 8 and Port 9 bypass the Smart I/O hardware.

Smart I/O supports:

- System Deep Sleep operation
- Boolean operations without CPU intervention
- Asynchronous or synchronous (clocked) operation

Each Smart I/O block contains a data unit (DU) and eight look up tables (LUTs).

The DU:

- Performs unique functions based on a selectable opcode.
- Can source input signals from internal resources, the GPIO port, or a value in the DU register.

Each LUT:

- Has three selectable input sources. The input signals may be sourced from another LUT, an internal resource, an external signal from a GPIO pin, or from the DU.
- Acts as a programmable Boolean logic table.
- Can be synchronous or asynchronous.

Universal Digital Blocks (UDBs) and Port Interfaces

PSoC 63 has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

- The TCPWM supports the following operational modes:
 - Timer-counter with compare
 - Timer-counter with capture
 - Quadrature decoding
 - Pulse width modulation (PWM)
 - Pseudo-random PWM
 - PWM with dead time
- Up, down, and up/down counting modes.
- Clock prescaling (division by 1, 2, 4, ... 64, 128)
- Double buffering of compare/capture and period values
- Underflow, overflow, and capture/compare output signals
- Supports interrupt on:
 - Terminal count – Depends on the mode; typically occurs on overflow or underflow
 - Capture/compare – The count is captured to the capture register or the counter value equals the value in the compare register

- Complementary output for PWMs

- Selectable start, reload, stop, count, and capture event signals for each TCPWM with rising edge, falling edge, both edges, and level trigger options. The TCPWM has a Kill input to force outputs to a predetermined state.

In this device there are:

- Eight 32-bit TCPWMs
- Twenty-four 16-bit TCPWMs

Serial Communication Blocks (SCB)

PSoC 62 has 9 SCBs:

- Eight can implement either I²C, UART, or SPI.
- One SCB (SCB #8) can operate in Deep Sleep with an external clock, this SCB can be either SPI slave or I²C slave.

I²C Mode: The SCB can implement a full multi-master and slave interface (it is capable of multimaster arbitration). This block can operate at speeds of up to 1 Mbps (Fast Mode Plus). It also supports EzI²C that creates a mailbox address range in the memory of PSoC 63 and effectively reduces the I²C communication to reading from and writing to an array in the memory. The SCB supports a 256-byte FIFO for receive and transmit.

The I²C peripheral is compatible with I²C standard-mode, Fast Mode, and Fast Mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 8 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface will operate with a 25-MHz SPI Clock.

USB Full-Speed Dual Role Host and Device Interface

PSoC 63 with BLE incorporates a dual-role USB Host and Device interface. The device can have up to eight endpoints. A 512 byte SRAM buffer is provided and DMA is supported.

QSPI Interface Serial Memory Interface (SMIF)

A serial memory interface is provided, running at up to 80 MHz. It supports single, dual, quad, dual-quad and octal SPI configurations, and supports up to four external memory devices. It supports two modes of operation:

- Memory-mapped I/O (MMIO), a command mode interface that provides data access via the SMIF registers and FIFOs
- Execute in Place (XIP), in which AHB reads and writes are directly translated to SPI read and write transfers.

In XIP mode, the external memory is mapped into the PSoC 6 MCU internal address space, enabling code execution directly from the external memory. To improve performance, a 4-KB cache is included. XIP mode also supports AES-128 on-the-fly encryption and decryption, enabling secure storage and access of code and data in the external memory.

LCD Block

This block drives LCD commons and segments; routing is available to most of the GPIOs. The LCD block has two modes of operation: high speed (8 MHz) and low speed (32 kHz). Both modes operate in system LP and ULP modes. Low-speed mode operates with reduced contrast in system Deep Sleep mode - review the number of common and segment lines, viewing angle requirements, and prototype performance before using this mode.

GPIO

PSoC 63 with BLE has up to 84 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Hold mode for latching previous state (used for retaining the I/O state in system Hibernate mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are up to 8 pins in width. Data output and pin state registers store, respectively, the values to be driven on the pins and the input states of the pins.

Every pin can generate an interrupt if enabled; each port has an interrupt request (IRQ) associated with it.

The port 1 pins are capable of overvoltage-tolerant (OVT) operation, where the input voltage may be higher than V_{DD} . OVT pins are commonly used with I²C, to allow powering the chip OFF while maintaining a physical connection to an operating I²C bus without affecting its functionality.

GPIO pins can be ganged to source or sink higher values of current. GPIO pins, including OVT pins, may not be pulled up higher than the absolute maximum; see [Electrical Specifications](#).

During power-on and reset, the pins are forced to the analog input drive mode, with input and output buffers disabled, so as not to crowbar any inputs and/or cause excess turn-on current.

A multiplexing network known as the high-speed I/O matrix (HSIOM) is used to multiplex between various peripheral and analog signals that may connect to an I/O pin.

Special-Function Peripherals

Audio Subsystem

This subsystem consists of the following hardware blocks:

- One Inter-IC Sound (I²S) interface
- Two pulse-density modulation to pulse-code modulation decoder channels

The I²S interface implements two independent hardware FIFO buffers – TX and RX, which can operate in master or slave mode. The following features are supported:

- Multiple data formats – I²S, left-justified, Time Division Multiplexed (TDM) mode A, and TDM mode B
- Programmable channel/word lengths – 8/16/18/20/24/32 bits
- Internal/external clock operation. Up to 192 ksps
- Interrupt mask events – trigger, not empty, full, overflow, underflow, watchdog
- Configurable FIFO trigger level with DMA support

The I²S interface is commonly used to connect with audio codecs, simple DACs, and digital microphones.

The PDM-to-PCM decoder implements a single hardware RX FIFO that decodes a stereo or mono 1-bit PDM input stream to PCM data output. The following features are supported:

- Programmable data output word length – 16/18/20/24 bits
- Programmable gain amplifier (PGA) for volume control – from -12 dB to +10.5 dB in 1.5 dB steps
- Configurable PDM clock generation. Range from 384 kHz to 3.072 MHz
- Droop correction and configurable decimation rate for sampling; up to 48 ksps
- Programmable high-pass filter gain
- Interrupt mask events – not empty, overflow, trigger, underflow
- Configurable FIFO trigger level with DMA support

The PDM-to-PCM decoder is commonly used to connect to digital PDM microphones. Up to two microphones can be connected to the same PDM Data line.

CapSense Subsystem

CapSense is supported in PSoC 6 MCU through a CapSense sigma-delta (CSD) hardware block. It is designed for high-sensitivity self-capacitance and mutual-capacitance measurements, and is specifically built for user interface solutions.

In addition to CapSense, the CSD hardware block supports three general-purpose functions. These are available when CapSense is not being used. Alternatively, two or more functions can be time-multiplexed in an application under firmware control. The four functions supported by the CSD hardware block are:

- CapSense
- 10-bit ADC
- Programmable current sources (IDAC)
- Comparator

CapSense

Capacitive touch sensors are designed for user interfaces that rely on human body capacitance to detect the presence of a finger on or near a sensor. Cypress CapSense solutions bring elegant, reliable, and simple capacitive touch sensing functions to applications including IoT, industrial, automotive, and home appliances.

The Cypress-proprietary CapSense technology offers the following features:

- Best-in-class signal-to-noise ratio (SNR) and robust sensing under harsh and noisy conditions
- Self-capacitance (CSD) and mutual-capacitance (CSX) sensing methods
- Support for various widgets, including buttons, matrix buttons, sliders, touchpads, and proximity sensors
- High-performance sensing across a variety of materials
- Best-in-class liquid tolerance
- SmartSense™ auto-tuning technology that helps avoid complex manual tuning processes
- Superior immunity against external noise
- Spread-spectrum clocks for low radiated emissions
- Gesture and built-in self-test libraries
- Ultra-low power consumption
- An integrated graphical CapSense tuner for real-time tuning, testing, and debugging

ADC

The CapSense subsystem slope ADC offers the following features:

- Selectable 8- or 10-bit resolution
- Selectable input range: GND to V_{REF} and GND to V_{DDA} on any GPIO input
- Measurement of V_{DDA} against an internal reference without the use of GPIO or external components

IDAC

The CSD block has two programmable current sources, which offer the following features:

- 7-bit resolution
- Sink and source current modes
- A current source programmable from 37.5 nA to 609 μ A
- Two IDACs that can be used in parallel to form one 8-bit IDAC

Comparator

The CapSense subsystem comparator operates in the System Low Power and Ultra-Low Power modes. The inverting input is connected to an internal programmable reference voltage and the non-inverting input can be connected to any GPIO via the AMUXBUS.

CapSense Hardware Subsystem

Figure 6 shows the high-level hardware overview of the CapSense subsystem, which includes a delta sigma converter, internal clock dividers, a shield driver, and two programmable current sources.

The inputs are managed through analog multiplexed buses (AMUXBUS A/B). The input and output of all functions offered by the CSD block can be provided on any GPIO or on a group of GPIOs under software control, with the exception of the comparator output and external capacitors that use dedicated GPIOs.

Self-capacitance is supported by the CSD block using AMUXBUS A, an external modulator capacitor, and a GPIO for each sensor. There is a shield electrode (optional) for self-capacitance sensing. This is supported using AMUXBUS B and an optional external shield tank capacitor (to increase the drive capability of the shield driver) should this be required. Mutual-capacitance is supported by the CSD block using AMUXBUS A, two external integrated capacitors, and a GPIO for transmit and receive electrodes.

The ADC does not require an external component. Any GPIO that can be connected to AMUXBUS A can be an input to the ADC under software control. The ADC can accept V_{DDA} as an input without needing GPIOs (for applications such as battery voltage measurement).

The two programmable current sources (IDACs) in general-purpose mode can be connected to AMUXBUS A or B. They can therefore connect to any GPIO pin. The comparator resides in the delta-sigma converter. The comparator inverting input can be connected to the reference. Both comparator inputs can be connected to any GPIO using AMUXBUS B; see Figure 5. The reference has a direct connection to a dedicated GPIO; see Table 6.

The CSD block can operate in active and sleep CPU power modes, and seamlessly transition between LP and ULP system modes. It can be powered down in Deep Sleep and Hibernate modes. Upon wakeup from Hibernate mode, the CSD block requires re-initialization. However, operation can be resumed without re-initialization upon exit from Deep Sleep mode, under firmware control.

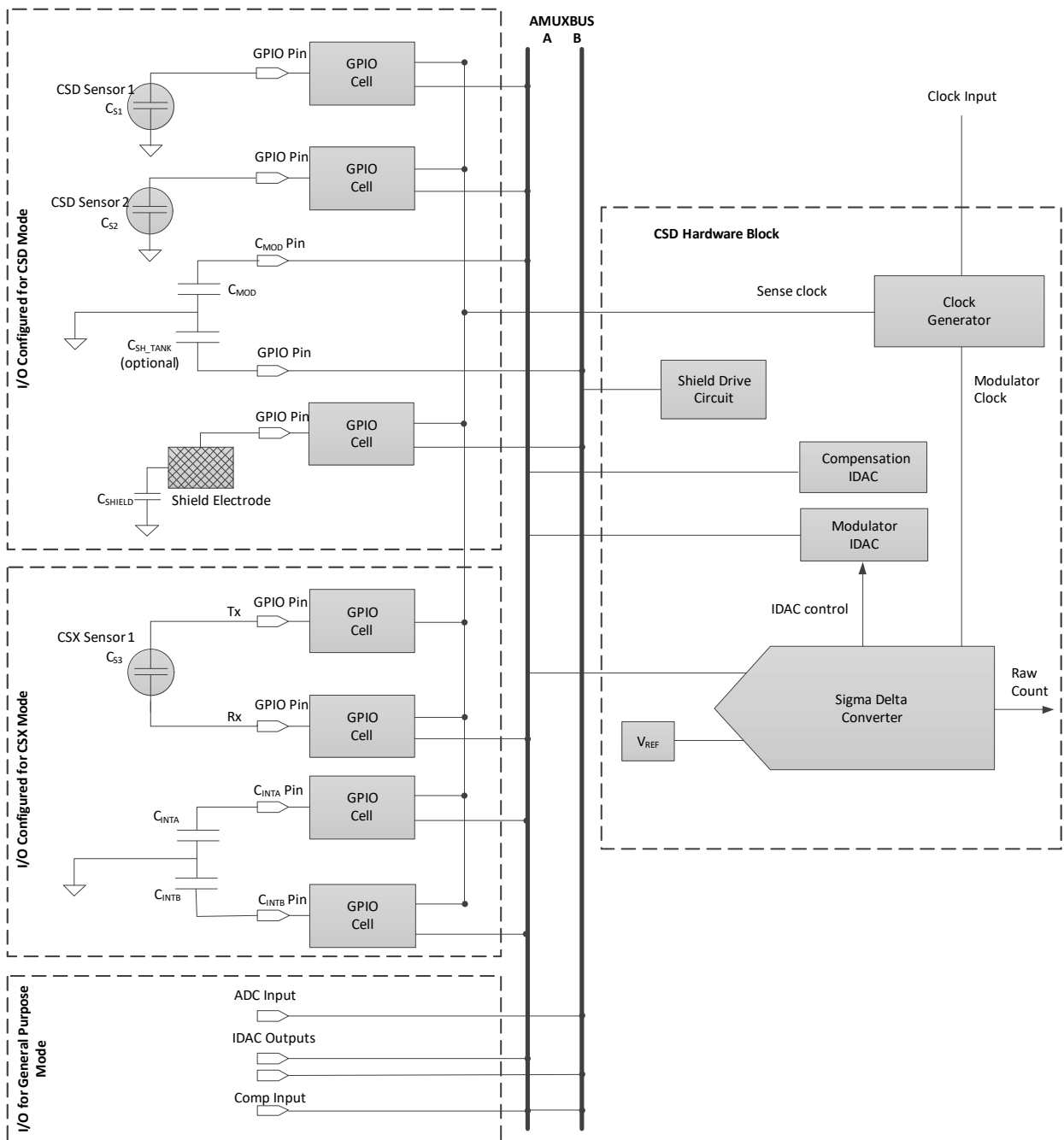
Figure 6. CapSense Hardware Subsystem


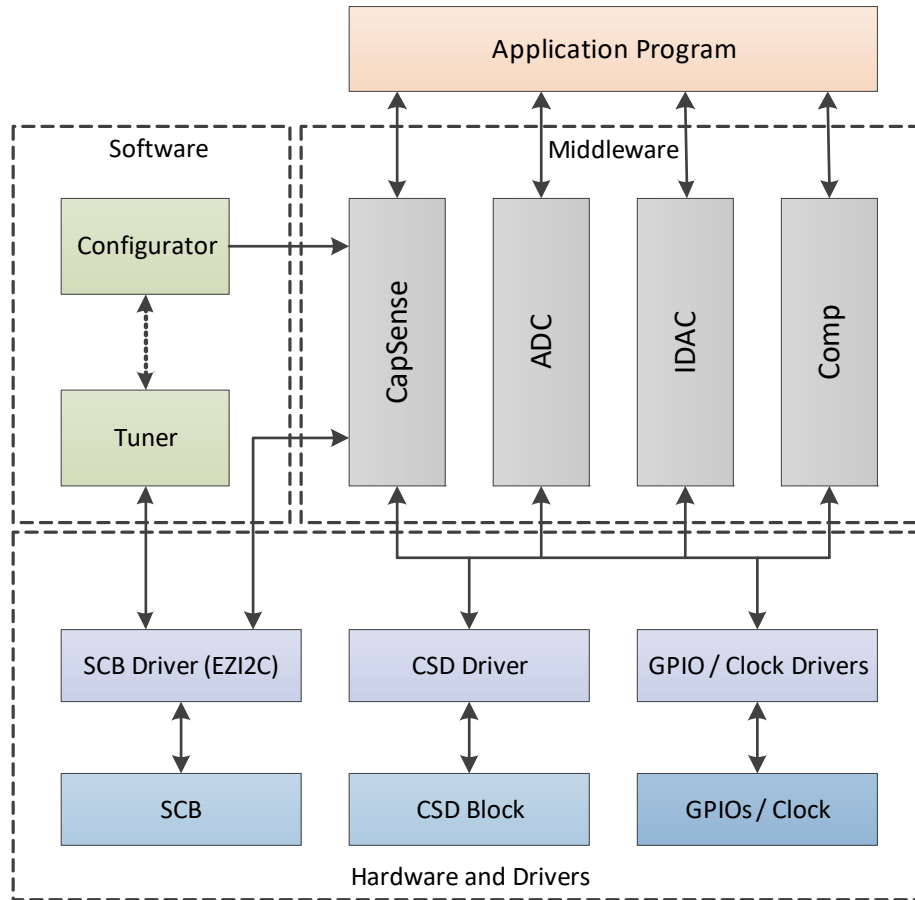
Figure 7 shows the high-level software overview. Cypress provides a middleware library for each function to enable quick integration. User applications interact only with middleware to implement functions of the CSD block. The middleware interacts with underlying drivers to access hardware as necessary. The CSD driver facilitates time-multiplexing of the CSD hardware if more than one piece of CSD-related middleware is present in a project. It prevents access conflicts in this case.

CapSense middleware has configurator software to enable fast configuration and incorporating it into middleware. It also has a tuner for performance evaluation and real-time tuning of the system. Both can be launched from the ModusToolbox IDE or in standalone mode. The tuner requires the EZ12C communication interface in the application to enable real-time tuning capability. The tuner can update configuration parameters directly in the device as well as in the configurator.

CapSense and ADC middleware use the CSD interrupt to implement non-blocking sensing and A-to-D conversion. Therefore, interrupt service routines are a defined part of the middleware, which must be initialized by the application. Middleware and drivers can operate on either CPU. Cypress recommends using the middleware only in one CPU. If both CPUs must access the CSD driver, memory access should be managed in the application.

Refer to [AN85951: PSoC 4 and PSoC 6 MCU CapSense Design Guide](#) for more details on CSX sensing, CSD sensing, shield electrode usage and its benefits, and capacitive system design guidelines. Refer to the middleware API reference guide available in the PSoC 6 SDK for more detail on middleware.

Figure 7. CapSense Software/Firmware Subsystem



Pinouts

Note: The CY8C63x6/CY8C63x7 [datasheet web page](#) contains a spreadsheet with a consolidated list of pinouts and pin alternate functions with HSIOM mapping.

GPIO ports are powered by V_{DDx} pins as follows:

- P0: V_{BACKUP}
- P1: V_{DDD} . Port 1 pins are overvoltage tolerant (OVT).
- P5, P6, P7, P8: V_{DDIO1}
- P9, P10: V_{DDIOA} , V_{DDA} (V_{DDIOA} , when present, and V_{DDA} must be connected together on the PCB)
- P11, P12, P13: V_{DDIO0}
- P14: V_{DDUSB}

Figure 8. Device Pinout for 68-QFN Package^[1]

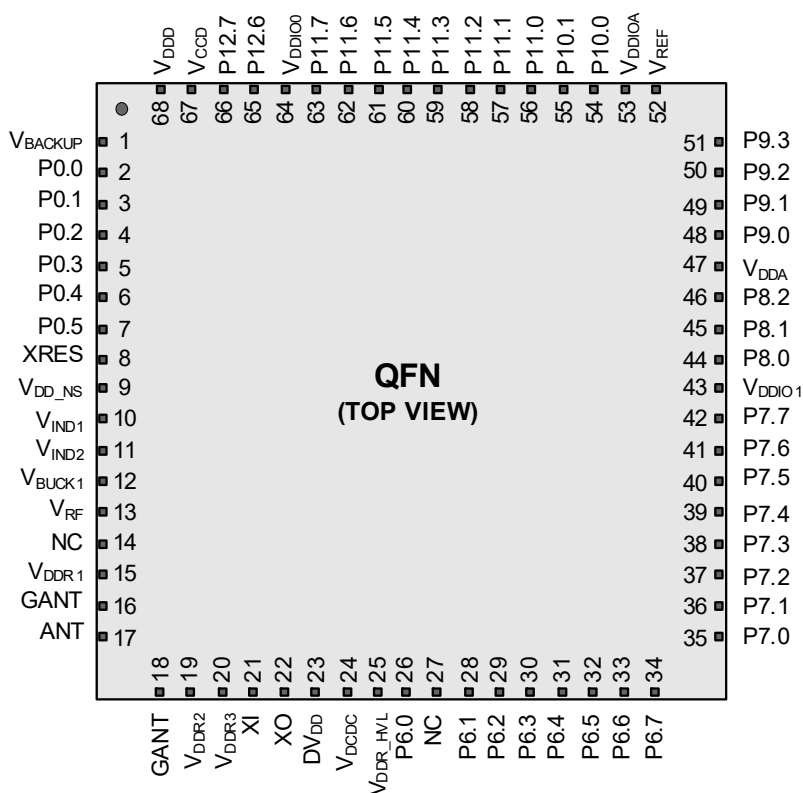


Table 4. Packages and Pin Information

| Pin | Packages | | | | |
|-------------|----------|---------|-------------------|---------------------|--------|
| | 124-BGA | 116-BGA | 104-MCSP (no USB) | 104-MCSP (with USB) | 68-QFN |
| V_{DDD} | A13 | B1 | C6 | | 68 |
| V_{CCD} | B13 | A2 | C7 | | 67 |
| V_{DDA} | M13 | A9 | A1 | | 47 |
| V_{DDIOA} | N13 | - | - | | 53 |
| V_{DDIO0} | D11 | B3 | B6 | | 64 |

Note
1. The center pad on the QFN package should be connected to PCB ground relative to device V_{DDx} for best mechanical, thermal, and electrical performance. For more information, see AN72845, Design Guidelines for QFN Devices.

Table 4. Packages and Pin Information (continued)

| Pin | Packages | | | | |
|----------------------|-------------------------------|--|----------------------|------------------------|---------|
| | 124-BGA | 116-BGA | 104-MCSP (no USB) | 104-MCSP (with USB) | 68-QFN |
| V _{DDIO1} | M4 | G10 | D1 | | 43 |
| V _{BACKUP} | A10 | C1 | C9 | | 1 |
| V _{DDUSB} | A2 | - | - | H7 | - |
| V _{SS} | C11, D4, D10, K4, K10, M12 | B2, B9, D1, H2, H9 | D4, D7, F4, G7, P1 | | GND PAD |
| V _{SSR} | A1, B1, B2, C3, D1, E3, G2 | J1, K2, K3, K4, K5, L1, L3, L4, L5, M3, M8 | M3, N9, P3, P6, P7 | | GND PAD |
| V _{DD_NS} | A5 | H3 | G9 | | 9 |
| V _{IND1} | B5 | F1 | G8 | | 10 |
| V _{IND2} | B4 | G1 | H8 | | 11 |
| V _{BUCK1} | C4 | G2 | J8 | F9 | 12 |
| V _{RF} | A4 | H1 | H9 | | 13 |
| V _{DCDC} | F3 | M7 | P4 | | 24 |
| V _{DDR1} | C2 | L2 | L9 | | 15 |
| V _{DDR2} | E2 | M1 | P9 | | 19 |
| V _{DDR3} | D2 | M2 | P8 | | 20 |
| DV _{DD} | F2 | M6 | M4 | | 23 |
| V _{DDR_HVL} | G3 | L7 | L2 | | 25 |
| XRES | A8 | E2 | E5 | | 8 |
| V _{REF} | N12 | B10 | - | | 52 |
| ANT | C1 | K1 | M9 | | 17 |
| GANT | - | - | - | | 16, 18 |
| XI | F1 | M4 | M5 | | 21 |
| XO | E1 | M5 | P5 | | 22 |
| P0.0 | C9 | C2 | D8 | | 2 |
| P0.1 | B9 | D3 | E6 | | 3 |
| P0.2 | A9 | E4 | D9 | | 4 |
| P0.3 | C8 | E3 | E7 | | 5 |
| P0.4 | B8 | F3 | E8 | | 6 |
| P0.5 | C7 | D2 | E9 | | 7 |
| P1.0 | B7 | G3 | F5 | | - |
| P1.1 | A7 | F2 | F6 | | - |
| P1.2 | C6 | J5 | - | | - |
| P1.3 | B6 | J4 | F9 | - | - |
| P1.4 | A6 | J3 | F8 | | - |
| P1.5 | C5 | J2 | F7 | | - |
| P5.0 | G1 | L6 | J7 | | - |
| P5.1 | H3 | K6 | J5 | | - |
| P5.2 | H2 | J6 | J6 | | - |
| P5.3 | H1 | K7 | H7 | H6 | - |
| P5.4 | J3 | J7 | H6 | H5 | - |

Table 4. Packages and Pin Information (continued)

| Pin | Packages | | | | |
|-------|----------|---------|----------------------|------------------------|--------|
| | 124-BGA | 116-BGA | 104-MCSP (no USB) | 104-MCSP (with USB) | 68-QFN |
| P5.5 | J2 | L8 | J4 | | - |
| P5.6 | J1 | M9 | K3 | | - |
| P5.7 | K1 | - | K4 | | - |
| P6.0 | K2 | K8 | J3 | | 26 |
| P6.1 | K3 | J8 | K2 | | 28 |
| P6.2 | L3 | L9 | M2 | | 29 |
| P6.3 | L2 | K9 | L1 | | 30 |
| P6.4 | L1 | J9 | J2 | | 31 |
| P6.5 | M2 | M10 | K1 | | 32 |
| P6.6 | M1 | L10 | N2 | | 33 |
| P6.7 | N2 | K10 | M1 | | 34 |
| P7.0 | N3 | J10 | N1 | | 35 |
| P7.1 | M3 | H10 | G6 | | 36 |
| P7.2 | N4 | H8 | H4 | | 37 |
| P7.3 | N1 | H7 | G5 | | 38 |
| P7.4 | L4 | H6 | H3 | | 39 |
| P7.5 | N5 | G9 | H2 | | 40 |
| P7.6 | M5 | G8 | G3 | | 41 |
| P7.7 | L5 | G7 | G2 | | 42 |
| P8.0 | N6 | F10 | G4 | | 44 |
| P8.1 | M6 | F9 | G1 | | 45 |
| P8.2 | L6 | F8 | F3 | | 46 |
| P8.3 | N7 | F7 | F2 | | - |
| P8.4 | M7 | G6 | F1 | | - |
| P8.5 | L7 | E9 | E3 | | - |
| P8.6 | N8 | E8 | E1 | | - |
| P8.7 | M8 | E7 | E2 | | - |
| P9.0 | L9 | D10 | D2 | | 48 |
| P9.1 | M9 | D9 | C1 | | 49 |
| P9.2 | N9 | D8 | D3 | | 50 |
| P9.3 | L8 | D7 | B1 | | 51 |
| P9.4 | N10 | C10 | - | | - |
| P9.5 | M10 | C9 | - | | - |
| P9.6 | L10 | C8 | - | | - |
| P9.7 | N11 | C7 | - | | - |
| P10.0 | M11 | B8 | C2 | | 54 |
| P10.1 | L13 | A8 | B2 | | 55 |
| P10.2 | L12 | F6 | C3 | | - |
| P10.3 | L11 | E6 | E4 | | - |
| P10.4 | K13 | D6 | A2 | | - |
| P10.5 | K12 | B7 | A3 | | - |

Table 4. Packages and Pin Information *(continued)*

| Pin | Packages | | | | |
|------------------|----------|---------|----------------------|------------------------|--------|
| | 124-BGA | 116-BGA | 104-MCSP (no USB) | 104-MCSP (with USB) | 68-QFN |
| P10.6 | K11 | A7 | D5 | | - |
| P10.7 | J13 | - | B3 | | - |
| P11.0 | J12 | F5 | C4 | | 56 |
| P11.1 | J11 | E5 | C5 | | 57 |
| P11.2 | H13 | D5 | D6 | | 58 |
| P11.3 | H12 | C6 | B4 | | 59 |
| P11.4 | H11 | B6 | A4 | | 60 |
| P11.5 | G13 | A6 | B5 | | 61 |
| P11.6 | G12 | B5 | A5 | | 62 |
| P11.7 | G11 | A5 | A6 | | 63 |
| P12.0 | F13 | A4 | B7 | | - |
| P12.1 | F12 | B4 | A7 | | - |
| P12.2 | F11 | C4 | B8 | | - |
| P12.3 | E13 | A3 | A8 | | - |
| P12.4 | E12 | C5 | C8 | | - |
| P12.5 | E11 | D4 | - | | - |
| P12.6 | D13 | G5 | - | | 65 |
| P12.7 | D12 | H5 | - | | 66 |
| P13.0 | A12 | H4 | A9 | | - |
| P13.1 | C13 | G4 | B9 | | - |
| P13.2 | C12 | - | - | | - |
| P13.3 | B12 | - | - | | - |
| P13.4 | B11 | - | - | | - |
| P13.5 | A11 | - | - | | - |
| P13.6 | C10 | F4 | - | | - |
| P13.7 | B10 | C3 | - | | - |
| P14.0 / USBDP | B3 | - | - | J8 | - |
| P14.1 / USBDM | A3 | - | - | J9 | - |
| NC | D3 | - | H5, J9, P2 | P2 | 14, 27 |

Each Port Pin has multiple alternate functions. These are defined in Table 5.

Table 5. Multiple Alternate Functions^[2]

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|--------------------------|-------|----------------|--------|-------------------|------------------|----------------------|--------------------|------------------------|-----------------------|------------------------|---------|---------|-------|-----------------|-------|
| P0.0 | tcpwm[0].line[0]:0 | tcpwm[1].line[0]:0 | | srss.ext_clk:0 | | | | scb[0].spi_select1:0 | | | peri.tr_io_input[0]:0 | | | | | | |
| P0.1 | tcpwm[0].line_comp[0]:0 | tcpwm[1].line_comp[0]:0 | | | | | | scb[0].spi_select2:0 | | | peri.tr_io_input[1]:0 | | | | | cpuss.swj_trstn | |
| P0.2 | tcpwm[0].line[1]:0 | tcpwm[1].line[1]:0 | | | | scb[0].uart_rx:0 | scb[0].i2c_scl:0 | scb[0].spi_mosi:0 | | | | | | | | | |
| P0.3 | tcpwm[0].line_comp[1]:0 | tcpwm[1].line_comp[1]:0 | | | | scb[0].uart_tx:0 | scb[0].i2c_sda:0 | scb[0].spi_miso:0 | | | | | | | | | |
| P0.4 | tcpwm[0].line[2]:0 | tcpwm[1].line[2]:0 | | | | scb[0].uart_rts:0 | | scb[0].spi_clk:0 | | | | peri.tr_io_output[0]:2 | | | | | |
| P0.5 | tcpwm[0].line_comp[2]:0 | tcpwm[1].line_comp[2]:0 | | srss.ext_clk:1 | | scb[0].uart_cts:0 | | scb[0].spi_select0:0 | | | | peri.tr_io_output[1]:2 | | | | | |
| P1.0 | tcpwm[0].line[3]:0 | tcpwm[1].line[3]:0 | | | | scb[7].uart_rx:0 | scb[7].i2c_scl:0 | scb[7].spi_mosi:0 | | | peri.tr_io_input[2]:0 | | | | | | |
| P1.1 | tcpwm[0].line_comp[3]:0 | tcpwm[1].line_comp[3]:0 | | | | scb[7].uart_tx:0 | scb[7].i2c_sda:0 | scb[7].spi_miso:0 | | | peri.tr_io_input[3]:0 | | | | | | |
| P1.2 | tcpwm[0].line[4]:4 | tcpwm[1].line[12]:1 | | | | scb[7].uart_rts:0 | | scb[7].spi_clk:0 | | | | | | | | | |
| P1.3 | tcpwm[0].line_comp[4]:4 | tcpwm[1].line_comp[12]:1 | | | | scb[7].uart_cts:0 | | scb[7].spi_select0:0 | | | | | | | | | |
| P1.4 | tcpwm[0].line[5]:4 | tcpwm[1].line[13]:1 | | | | | | scb[7].spi_select1:0 | | | | | | | | | |
| P1.5 | tcpwm[0].line_comp[5]:4 | tcpwm[1].line_comp[14]:1 | | | | | | scb[7].spi_select2:0 | | | | | | | | | |
| P5.0 | tcpwm[0].line[4]:0 | tcpwm[1].line[4]:0 | | | | scb[5].uart_rx:0 | scb[5].i2c_scl:0 | scb[5].spi_mosi:0 | audioss.clk_i2s_if | peri.tr_io_input[10]:0 | | | | | | | |
| P5.1 | tcpwm[0].line_comp[4]:0 | tcpwm[1].line_comp[4]:0 | | | | scb[5].uart_tx:0 | scb[5].i2c_sda:0 | scb[5].spi_miso:0 | audioss.tx_sck | peri.tr_io_input[11]:0 | | | | | | | |
| P5.2 | tcpwm[0].line[5]:0 | tcpwm[1].line[5]:0 | | | | scb[5].uart_rts:0 | | scb[5].spi_clk:0 | audioss.tx_ws | | | | | | | | |

Note

- The notation for a signal is of the form IPName[x].signal_name[u]:y.
IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
For example, the name tcpwm[0].line_comp[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_comp # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 5. Multiple Alternate Functions^[2] (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|---------------------------|----------------------------|------------------|--------|--------|-------------------|------------------|----------------------|--------|------------------------|------------------------|---------|-------------------|--------------------|-------|-----------------------|----------------------|
| P5.3 | tcpwm[0].line_comp_l[5]:0 | tcpwm[1].line_comp_l[5]:0 | | | | scb[5].uart_cts:0 | | scb[5].spi_select0:0 | | audioss.tx_sdo | | | | | | | |
| P5.4 | tcpwm[0].line[6]:0 | tcpwm[1].line[6]:0 | | | | | | scb[5].spi_select1:0 | | audioss.rx_sck | | | | | | | |
| P5.5 | tcpwm[0].line_comp_l[6]:0 | tcpwm[1].line_comp_l[6]:0 | | | | | | scb[5].spi_select2:0 | | audioss.rx_ws | | | | | | | |
| P5.6 | tcpwm[0].line[7]:0 | tcpwm[1].line[7]:0 | | | | | | scb[5].spi_select3:0 | | audioss.rx_sdi | | | | | | | |
| P5.7 | tcpwm[0].line_comp_l[7]:0 | tcpwm[1].line_comp_l[7]:0 | | | | | | scb[3].spi_select3:0 | | | | | | | | | |
| P6.0 | tcpwm[0].line[0]:1 | tcpwm[1].line[8]:0 | scb[8].i2c_scl:0 | | | scb[3].uart_rx:0 | scb[3].i2c_scl:0 | scb[3].spi_mosi:0 | | | | | | cpuss.fault_out[0] | | | scb[8].spi_mosi:0 |
| P6.1 | tcpwm[0].line_comp_l[0]:1 | tcpwm[1].line_comp_l[8]:0 | scb[8].i2c_sda:0 | | | scb[3].uart_tx:0 | scb[3].i2c_sda:0 | scb[3].spi_miso:0 | | | | | | cpuss.fault_out[1] | | | scb[8].spi_miso:0 |
| P6.2 | tcpwm[0].line[1]:1 | tcpwm[1].line[9]:0 | | | | scb[3].uart_rts:0 | | scb[3].spi_clk:0 | | | | | | | | | scb[8].spi_clk:0 |
| P6.3 | tcpwm[0].line_comp_l[1]:1 | tcpwm[1].line_comp_l[9]:0 | | | | scb[3].uart_cts:0 | | scb[3].spi_select0:0 | | | | | | | | | scb[8].spi_select0:0 |
| P6.4 | tcpwm[0].line[2]:1 | tcpwm[1].line[10]:0 | scb[8].i2c_scl:1 | | | scb[6].uart_rx:2 | scb[6].i2c_scl:2 | scb[6].spi_mosi:2 | | peri.tr_io_input[12]:0 | peri.tr_io_output[0]:1 | | | | | cpuss.swj_swo_tdo | scb[8].spi_mosi:1 |
| P6.5 | tcpwm[0].line_comp_l[2]:1 | tcpwm[1].line_comp_l[10]:0 | scb[8].i2c_sda:1 | | | scb[6].uart_tx:2 | scb[6].i2c_sda:2 | scb[6].spi_miso:2 | | peri.tr_io_input[13]:0 | peri.tr_io_output[1]:1 | | | | | cpuss.swj_sw_doe_tdi | scb[8].spi_miso:1 |
| P6.6 | tcpwm[0].line[3]:1 | tcpwm[1].line[11]:0 | | | | scb[6].uart_rts:2 | | scb[6].spi_clk:2 | | | | | | | | cpuss.swj_sw_dio_tms | scb[8].spi_clk:1 |
| P6.7 | tcpwm[0].line_comp_l[3]:1 | tcpwm[1].line_comp_l[11]:0 | | | | scb[6].uart_cts:2 | | scb[6].spi_select0:2 | | | | | | | | cpuss.swj_sw_clk_tclk | scb[8].spi_select0:1 |
| P7.0 | tcpwm[0].line[4]:1 | tcpwm[1].line[12]:0 | | | | scb[4].uart_rx:1 | scb[4].i2c_scl:1 | scb[4].spi_mosi:1 | | peri.tr_io_input[14]:0 | | | cpuss.trace_clock | | | | |
| P7.1 | tcpwm[0].line_comp_l[4]:1 | tcpwm[1].line_comp_l[12]:0 | | | | scb[4].uart_tx:1 | scb[4].i2c_sda:1 | scb[4].spi_miso:1 | | peri.tr_io_input[15]:0 | | | | | | | |

Note

- The notation for a signal is of the form IPName[x].signal_name[u]:y.
IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
For example, the name tcpwm[0].line_comp_l[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_comp_l # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 5. Multiple Alternate Functions^[2] (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 | |
|--------------|-------------------------|---------------------------|-------|--------|--------|-------------------|------------------|----------------------|-------------------|---------|---------|---------|------------------------------|-----------------------|-------|-------|------------------------|-----------------------|
| P7.2 | tcpwm[0].line[5]:1 | tcpwm[1].line[13]:0 | | | | scb[4].uart_rts:1 | | scb[4].spi_clk:1 | | | | | | | | | | |
| P7.3 | tcpwm[0].line_comp[5]:1 | tcpwm[1].line_compl[13]:0 | | | | scb[4].uart_cts:1 | | scb[4].spi_select0:1 | | | | | | | | | | |
| P7.4 | tcpwm[0].line[6]:1 | tcpwm[1].line[14]:0 | | | | | | scb[4].spi_select1:1 | | | | | bless.ext_lina_rx_ctl_out | cpuss.trace_data[3]:2 | | | | |
| P7.5 | tcpwm[0].line_comp[6]:1 | tcpwm[1].line_compl[14]:0 | | | | | | scb[4].spi_select2:1 | | | | | bless.ext_pax_ctl_out | cpuss.trace_data[2]:2 | | | | |
| P7.6 | tcpwm[0].line[7]:1 | tcpwm[1].line[15]:0 | | | | | | scb[4].spi_select3:1 | | | | | bless.ext_palina_chip_en_out | cpuss.trace_data[1]:2 | | | | |
| P7.7 | tcpwm[0].line_comp[7]:1 | tcpwm[1].line_compl[15]:0 | | | | | | scb[3].spi_select1:0 | cpuss.clk_fm_pump | | | | | cpuss.trace_data[0]:2 | | | | |
| P8.0 | tcpwm[0].line[0]:2 | tcpwm[1].line[16]:0 | | | | scb[4].uart_rx:0 | scb[4].i2c_scl:0 | scb[4].spi_mosi:0 | | | | | | | | | peri.tr_io_input[16]:0 | |
| P8.1 | tcpwm[0].line_comp[0]:2 | tcpwm[1].line_compl[16]:0 | | | | scb[4].uart_tx:0 | scb[4].i2c_sda:0 | scb[4].spi_miso:0 | | | | | | | | | peri.tr_io_input[17]:0 | |
| P8.2 | tcpwm[0].line[1]:2 | tcpwm[1].line[17]:0 | | | | scb[4].uart_rts:0 | | scb[4].spi_clk:0 | | | | | | | | | | |
| P8.3 | tcpwm[0].line_comp[1]:2 | tcpwm[1].line_compl[17]:0 | | | | scb[4].uart_cts:0 | | scb[4].spi_select0:0 | | | | | | | | | | |
| P8.4 | tcpwm[0].line[2]:2 | tcpwm[1].line[18]:0 | | | | | | scb[4].spi_select1:0 | | | | | | | | | | |
| P8.5 | tcpwm[0].line_comp[2]:2 | tcpwm[1].line_compl[18]:0 | | | | | | scb[4].spi_select2:0 | | | | | | | | | | |
| P8.6 | tcpwm[0].line[3]:2 | tcpwm[1].line[19]:0 | | | | | | scb[4].spi_select3:0 | | | | | | | | | | |
| P8.7 | tcpwm[0].line_comp[3]:2 | tcpwm[1].line_compl[19]:0 | | | | | | scb[3].spi_select2:0 | | | | | | | | | | |
| P9.0 | tcpwm[0].line[4]:2 | tcpwm[1].line[20]:0 | | | | scb[2].uart_rx:0 | scb[2].i2c_scl:0 | scb[2].spi_mosi:0 | | | | | | | | | peri.tr_io_input[18]:0 | cpuss.trace_data[3]:0 |

Note

2. The notation for a signal is of the form IPName[x].signal_name[u]:y.
 IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
 For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 5. Multiple Alternate Functions^[2] (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|---------------------------|-------|--------|--------|-------------------|------------------|----------------------|------------------|---------|------------------------|---------|------------------------|-----------------------|-------|-------|-------|
| P9.1 | tcpwm[0].line_comp[4]:2 | tcpwm[1].line_compl[20]:0 | | | | scb[2].uart_tx:0 | scb[2].i2c_sda:0 | scb[2].spi_miso:0 | | | peri.tr_io_input[19]:0 | | | cpuss.trace_data[2]:0 | | | |
| P9.2 | tcpwm[0].line[5]:2 | tcpwm[1].line[21]:0 | | | | scb[2].uart_rts:0 | | scb[2].spi_clk:0 | | | pass.dsi_ctb_cmp0:1 | | | cpuss.trace_data[1]:0 | | | |
| P9.3 | tcpwm[0].line_comp[5]:2 | tcpwm[1].line_compl[21]:0 | | | | scb[2].uart_cts:0 | | scb[2].spi_select0:0 | | | pass.dsi_ctb_cmp1:1 | | | cpuss.trace_data[0]:0 | | | |
| P9.4 | tcpwm[0].line[7]:5 | tcpwm[1].line[0]:2 | | | | | | scb[2].spi_select1:0 | | | | | | | | | |
| P9.5 | tcpwm[0].line_comp[7]:5 | tcpwm[1].line_compl[0]:2 | | | | | | scb[2].spi_select2:0 | | | | | | | | | |
| P9.6 | tcpwm[0].line[0]:6 | tcpwm[1].line[1]:2 | | | | | | scb[2].spi_select3:0 | | | | | | | | | |
| P9.7 | tcpwm[0].line_comp[0]:6 | tcpwm[1].line_compl[1]:2 | | | | | | | | | | | | | | | |
| P10.0 | tcpwm[0].line[6]:2 | tcpwm[1].line[22]:0 | | | | scb[1].uartrx:1 | scb[1].i2c_scl:1 | scb[1].spi_mosi:1 | | | | | peri.tr_io_input[20]:0 | cpuss.trace_data[3]:1 | | | |
| P10.1 | tcpwm[0].line_comp[6]:2 | tcpwm[1].line_compl[22]:0 | | | | scb[1].uartrx:1 | scb[1].i2c_sda:1 | scb[1].spi_miso:1 | | | | | peri.tr_io_input[21]:0 | cpuss.trace_data[2]:1 | | | |
| P10.2 | tcpwm[0].line[7]:2 | tcpwm[1].line[23]:0 | | | | scb[1].uart_rts:1 | | scb[1].spi_clk:1 | | | | | | cpuss.trace_data[1]:1 | | | |
| P10.3 | tcpwm[0].line_comp[7]:2 | tcpwm[1].line_compl[23]:0 | | | | scb[1].uart_cts:1 | | scb[1].spi_select0:1 | | | | | | cpuss.trace_data[0]:1 | | | |
| P10.4 | tcpwm[0].line[0]:3 | tcpwm[1].line[0]:1 | | | | | | scb[1].spi_select1:1 | audioss.pdm_clk | | | | | | | | |
| P10.5 | tcpwm[0].line_comp[0]:3 | tcpwm[1].line_compl[0]:1 | | | | | | scb[1].spi_select2:1 | audioss.pdm_data | | | | | | | | |
| P10.6 | tcpwm[0].line[1]:6 | tcpwm[1].line[2]:2 | | | | | | scb[1].spi_select3:1 | | | | | | | | | |
| P10.7 | tcpwm[0].line_comp[1]:6 | tcpwm[1].line_compl[2]:2 | | | | | | | | | | | | | | | |

Note

2. The notation for a signal is of the form IPName[x].signal_name[u]:y.
 IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
 For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 5. Multiple Alternate Functions^[2] (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 | |
|--------------|-------------------------|--------------------------|-------|--------|------------------|-------------------|------------------|----------------------|------------------|---------|---------|---------|------------------------|---------|-------|-------|-------|------------------------|
| P11.0 | tcpwm[0].line[1]:3 | tcpwm[1].line[1]:1 | | | smif.spi_select2 | scb[5].uart_rx:1 | scb[5].i2c_scl:1 | scb[5].spi_mosi:1 | | | | | | | | | | peri.tr_io_input[22]:0 |
| P11.1 | tcpwm[0].line_comp[1]:3 | tcpwm[1].line_compl[1]:1 | | | smif.spi_select1 | scb[5].uart_tx:1 | scb[5].i2c_sda:1 | scb[5].spi_miso:1 | | | | | | | | | | peri.tr_io_input[23]:0 |
| P11.2 | tcpwm[0].line[2]:3 | tcpwm[1].line[2]:1 | | | smif.spi_select0 | scb[5].uart_rts:1 | | scb[5].spi_clk:1 | | | | | | | | | | |
| P11.3 | tcpwm[0].line_comp[2]:3 | tcpwm[1].line_compl[2]:1 | | | smif.spi_data3 | scb[5].uart_cts:1 | | scb[5].spi_select0:1 | | | | | peri.tr_io_output[0]:0 | | | | | |
| P11.4 | tcpwm[0].line[3]:3 | tcpwm[1].line[3]:1 | | | smif.spi_data2 | | | scb[5].spi_select1:1 | | | | | peri.tr_io_output[1]:0 | | | | | |
| P11.5 | tcpwm[0].line_comp[3]:3 | tcpwm[1].line_compl[3]:1 | | | smif.spi_data1 | | | scb[5].spi_select2:1 | | | | | | | | | | |
| P11.6 | | | | | smif.spi_data0 | | | scb[5].spi_select3:1 | | | | | | | | | | |
| P11.7 | | | | | smif.spi_clk | | | | | | | | | | | | | |
| P12.0 | tcpwm[0].line[4]:3 | tcpwm[1].line[4]:1 | | | smif.spi_data4 | scb[6].uart_rx:0 | scb[6].i2c_scl:0 | scb[6].spi_mosi:0 | | | | | | | | | | peri.tr_io_input[24]:0 |
| P12.1 | tcpwm[0].line_comp[4]:3 | tcpwm[1].line_compl[4]:1 | | | smif.spi_data5 | scb[6].uart_tx:0 | scb[6].i2c_sda:0 | scb[6].spi_miso:0 | | | | | | | | | | peri.tr_io_input[25]:0 |
| P12.2 | tcpwm[0].line[5]:3 | tcpwm[1].line[5]:1 | | | smif.spi_data6 | scb[6].uart_rts:0 | | scb[6].spi_clk:0 | | | | | | | | | | |
| P12.3 | tcpwm[0].line_comp[5]:3 | tcpwm[1].line_compl[5]:1 | | | smif.spi_data7 | scb[6].uart_cts:0 | | scb[6].spi_select0:0 | | | | | | | | | | |
| P12.4 | tcpwm[0].line[6]:3 | tcpwm[1].line[6]:1 | | | smif.spi_select3 | | | scb[6].spi_select1:0 | audioss.pdm_clk | | | | | | | | | |
| P12.5 | tcpwm[0].line_comp[6]:3 | tcpwm[1].line_compl[6]:1 | | | | | | scb[6].spi_select2:0 | audioss.pdm_data | | | | | | | | | |
| P12.6 | tcpwm[0].line[7]:3 | tcpwm[1].line[7]:1 | | | | | | scb[6].spi_select3:0 | | | | | | | | | | |
| P12.7 | tcpwm[0].line_comp[7]:3 | tcpwm[1].line_compl[7]:1 | | | | | | | | | | | | | | | | |

Note

2. The notation for a signal is of the form IPName[x].signal_name[u]:y.
 IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
 For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 5. Multiple Alternate Functions^[2] (continued)

| Port/ Pin | ACT #0 | ACT #1 | DS #2 | ACT #4 | ACT #5 | ACT #6 | ACT #7 | ACT #8 | ACT #9 | ACT #10 | ACT #12 | ACT #13 | ACT #14 | ACT #15 | DS #4 | DS #5 | DS #6 |
|--------------|-------------------------|---------------------------|-------|--------|--------|-------------------|------------------|----------------------|--------|---------|------------------------|---------|---------|---------|-------|-------|-------|
| P13.0 | tcpwm[0].line[0]:4 | tcpwm[1].line[8]:1 | | | | scb[6].uart_rx:1 | scb[6].i2c_scl:1 | scb[6].spi_mosi:1 | | | peri.tr_io_input[26]:0 | | | | | | |
| P13.1 | tcpwm[0].line_comp[0]:4 | tcpwm[1].line_compl[8]:1 | | | | scb[6].uart_tx:1 | scb[6].i2c_sda:1 | scb[6].spi_miso:1 | | | peri.tr_io_input[27]:0 | | | | | | |
| P13.2 | tcpwm[0].line[1]:4 | tcpwm[1].line[9]:1 | | | | scb[6].uart_rts:1 | | scb[6].spi_clk:1 | | | | | | | | | |
| P13.3 | tcpwm[0].line_comp[1]:4 | tcpwm[1].line_compl[9]:1 | | | | scb[6].uart_cts:1 | | scb[6].spi_select0:1 | | | | | | | | | |
| P13.4 | tcpwm[0].line[2]:4 | tcpwm[1].line[10]:1 | | | | | | scb[6].spi_select1:1 | | | | | | | | | |
| P13.5 | tcpwm[0].line_comp[2]:4 | tcpwm[1].line_compl[10]:1 | | | | | | scb[6].spi_select2:1 | | | | | | | | | |
| P13.6 | tcpwm[0].line[3]:4 | tcpwm[1].line[11]:1 | | | | | | scb[6].spi_select3:1 | | | | | | | | | |
| P13.7 | tcpwm[0].line_comp[3]:4 | tcpwm[1].line_compl[11]:1 | | | | | | | | | | | | | | | |

Note

- The notation for a signal is of the form IPName[x].signal_name[u]:y.
IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Analog, Smart I/O, and DSI alternate Port Pin functionality is provided in [Table 6](#).

Table 6. Port Pin Analog, Smart I/O, and DSI Functions

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|------|------------------|---------------------------------------|-------------------|---------|
| P0.0 | P0.0 | wco_in | | dsi[0].port_if[0] | |
| P0.1 | P0.1 | wco_out | | dsi[0].port_if[1] | |
| P0.2 | P0.2 | | | dsi[0].port_if[2] | |
| P0.3 | P0.3 | | | dsi[0].port_if[3] | |
| P0.4 | P0.4 | | pmic_wakeup_in hibernate_wakeup[1] | dsi[0].port_if[4] | |
| P0.5 | P0.5 | | pmic_wakeup_out | dsi[0].port_if[5] | |
| P1.0 | P1.0 | | | dsi[1].port_if[0] | |
| P1.1 | P1.1 | | | dsi[1].port_if[1] | |
| P1.2 | P1.2 | | | dsi[1].port_if[2] | |
| P1.3 | P1.3 | | | dsi[1].port_if[3] | |
| P1.4 | P1.4 | | hibernate_wakeup[0] | dsi[1].port_if[4] | |
| P1.5 | P1.5 | | | dsi[1].port_if[5] | |
| P2.0 | P2.0 | | | dsi[2].port_if[0] | |
| P2.1 | P2.1 | | | dsi[2].port_if[1] | |
| P2.2 | P2.2 | | | dsi[2].port_if[2] | |
| P2.3 | P2.3 | | | dsi[2].port_if[3] | |
| P2.4 | P2.4 | | | dsi[2].port_if[4] | |
| P2.5 | P2.5 | | | dsi[2].port_if[5] | |
| P2.6 | P2.6 | | | dsi[2].port_if[6] | |
| P2.7 | P2.7 | | | dsi[2].port_if[7] | |
| P3.0 | P3.0 | | | | |
| P3.1 | P3.1 | | | | |
| P3.2 | P3.2 | | | | |
| P3.3 | P3.3 | | | | |
| P3.4 | P3.4 | | | | |
| P3.5 | P3.5 | | | | |
| P4.0 | P4.0 | | | dsi[0].port_if[6] | |
| P4.1 | P4.1 | | | dsi[0].port_if[7] | |
| P4.2 | P4.2 | | | dsi[1].port_if[6] | |
| P4.3 | P4.3 | | | dsi[1].port_if[7] | |
| P5.0 | P5.0 | | | dsi[3].port_if[0] | |
| P5.1 | P5.1 | | | dsi[3].port_if[1] | |
| P5.2 | P5.2 | | | dsi[3].port_if[2] | |
| P5.3 | P5.3 | | | dsi[3].port_if[3] | |
| P5.4 | P5.4 | | | dsi[3].port_if[4] | |
| P5.5 | P5.5 | | | dsi[3].port_if[5] | |
| P5.6 | P5.6 | lpcomp.inp_comp0 | | dsi[3].port_if[6] | |
| P5.7 | P5.7 | lpcomp.inn_comp0 | | dsi[3].port_if[7] | |

Table 6. Port Pin Analog, Smart I/O, and DSI Functions (continued)

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|-------|--------------------------------------|------------|--------------------|------------------|
| P6.0 | P6.0 | | | dsi[4].port_if[0] | |
| P6.1 | P6.1 | | | dsi[4].port_if[1] | |
| P6.2 | P6.2 | lpcomp.inp_comp1 | | dsi[4].port_if[2] | |
| P6.3 | P6.3 | lpcomp.inn_comp1 | | dsi[4].port_if[3] | |
| P6.4 | P6.4 | | | dsi[4].port_if[4] | |
| P6.5 | P6.5 | | | dsi[4].port_if[5] | |
| P6.6 | P6.6 | | swd_data | dsi[4].port_if[6] | |
| P6.7 | P6.7 | | swd_clk | dsi[4].port_if[7] | |
| P7.0 | P7.0 | | | dsi[5].port_if[0] | |
| P7.1 | P7.1 | csd.cmodpadd csd.cmodpads | | dsi[5].port_if[1] | |
| P7.2 | P7.2 | csd.csh_tankpadd csd.csh_tankpads | | dsi[5].port_if[2] | |
| P7.3 | P7.3 | csd.vref_ext | | dsi[5].port_if[3] | |
| P7.4 | P7.4 | | | dsi[5].port_if[4] | |
| P7.5 | P7.5 | | | dsi[5].port_if[5] | |
| P7.6 | P7.6 | | | dsi[5].port_if[6] | |
| P7.7 | P7.7 | csd.cshieldpads | | dsi[5].port_if[7] | |
| P8.0 | P8.0 | | | dsi[11].port_if[0] | smartio[8].io[0] |
| P8.1 | P8.1 | | | dsi[11].port_if[1] | smartio[8].io[1] |
| P8.2 | P8.2 | | | dsi[11].port_if[2] | smartio[8].io[2] |
| P8.3 | P8.3 | | | dsi[11].port_if[3] | smartio[8].io[3] |
| P8.4 | P8.4 | | | dsi[11].port_if[4] | smartio[8].io[4] |
| P8.5 | P8.5 | | | dsi[11].port_if[5] | smartio[8].io[5] |
| P8.6 | P8.6 | | | dsi[11].port_if[6] | smartio[8].io[6] |
| P8.7 | P8.7 | | | dsi[11].port_if[7] | smartio[8].io[7] |
| P9.0 | P9.0 | ctb_oa0+ | | dsi[10].port_if[0] | smartio[9].io[0] |
| P9.1 | P9.1 | ctb_oa0- | | dsi[10].port_if[1] | smartio[9].io[1] |
| P9.2 | P9.2 | ctb_oa0_out | | dsi[10].port_if[2] | smartio[9].io[2] |
| P9.3 | P9.3 | ctb_oa1_out | | dsi[10].port_if[3] | smartio[9].io[3] |
| P9.4 | P9.4 | ctb_oa1- | | dsi[10].port_if[4] | smartio[9].io[4] |
| P9.5 | P9.5 | ctb_oa1+ | | dsi[10].port_if[5] | smartio[9].io[5] |
| P9.6 | P9.6 | ctb_oa0+ or ctdac_out | | dsi[10].port_if[6] | smartio[9].io[6] |
| P9.7 | P9.7 | ctb_oa1+ or ext_vref | | dsi[10].port_if[7] | smartio[9].io[7] |
| P10.0 | P10.0 | sarmux[0] | | dsi[9].port_if[0] | |
| P10.1 | P10.1 | sarmux[1] | | dsi[9].port_if[1] | |
| P10.2 | P10.2 | sarmux[2] | | dsi[9].port_if[2] | |
| P10.3 | P10.3 | sarmux[3] | | dsi[9].port_if[3] | |

Table 6. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

| Port/Pin | Name | Analog | Digital HV | DSI | SMARTIO |
|----------|-------|--------------|------------|-------------------|---------|
| P10.4 | P10.4 | sarmux[4] | | dsi[9].port_if[4] | |
| P10.5 | P10.5 | sarmux[5] | | dsi[9].port_if[5] | |
| P10.6 | P10.6 | sarmux[6] | | dsi[9].port_if[6] | |
| P10.7 | P10.7 | sarmux[7] | | dsi[9].port_if[7] | |
| P11.0 | P11.0 | | | dsi[8].port_if[0] | |
| P11.1 | P11.1 | | | dsi[8].port_if[1] | |
| P11.2 | P11.2 | | | dsi[8].port_if[2] | |
| P11.3 | P11.3 | | | dsi[8].port_if[3] | |
| P11.4 | P11.4 | | | dsi[8].port_if[4] | |
| P11.5 | P11.5 | | | dsi[8].port_if[5] | |
| P11.6 | P11.6 | | | dsi[8].port_if[6] | |
| P11.7 | P11.7 | | | dsi[8].port_if[7] | |
| P12.0 | P12.0 | | | dsi[7].port_if[0] | |
| P12.1 | P12.1 | | | dsi[7].port_if[1] | |
| P12.2 | P12.2 | | | dsi[7].port_if[2] | |
| P12.3 | P12.3 | | | dsi[7].port_if[3] | |
| P12.4 | P12.4 | | | dsi[7].port_if[4] | |
| P12.5 | P12.5 | | | dsi[7].port_if[5] | |
| P12.6 | P12.6 | srss.eco_in | | dsi[7].port_if[6] | |
| P12.7 | P12.7 | srss.eco_out | | dsi[7].port_if[7] | |
| P13.0 | P13.0 | | | dsi[6].port_if[0] | |
| P13.1 | P13.1 | | | dsi[6].port_if[1] | |
| P13.2 | P13.2 | | | dsi[6].port_if[2] | |
| P13.3 | P13.3 | | | dsi[6].port_if[3] | |
| P13.4 | P13.4 | | | dsi[6].port_if[4] | |
| P13.5 | P13.5 | | | dsi[6].port_if[5] | |
| P13.6 | P13.6 | | | dsi[6].port_if[6] | |
| P13.7 | P13.7 | | | dsi[6].port_if[7] | |

Power Supply Considerations

The following power system diagrams show typical connections for power pins for all supported packages.

In these diagrams, the package pin is shown with the pin name, for example "V_{DDA}, M13". For V_{DDx} pins, the I/O port that is powered by that pin is also shown, for example "V_{DD}, A13; I/O port P1".

Figure 9. 124-BGA Power Connection Diagram

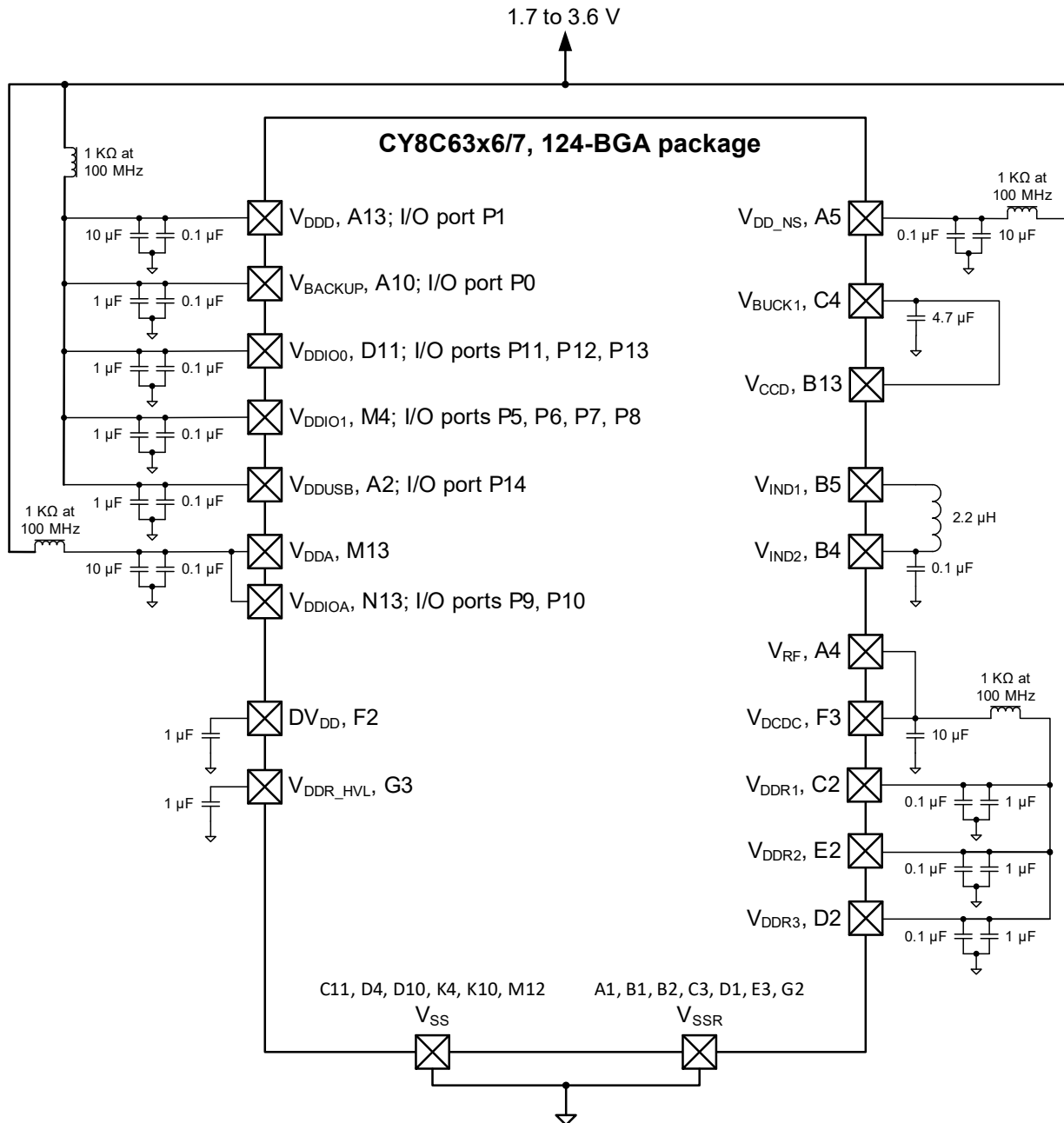


Figure 10. 116-BGA Power Connection Diagram

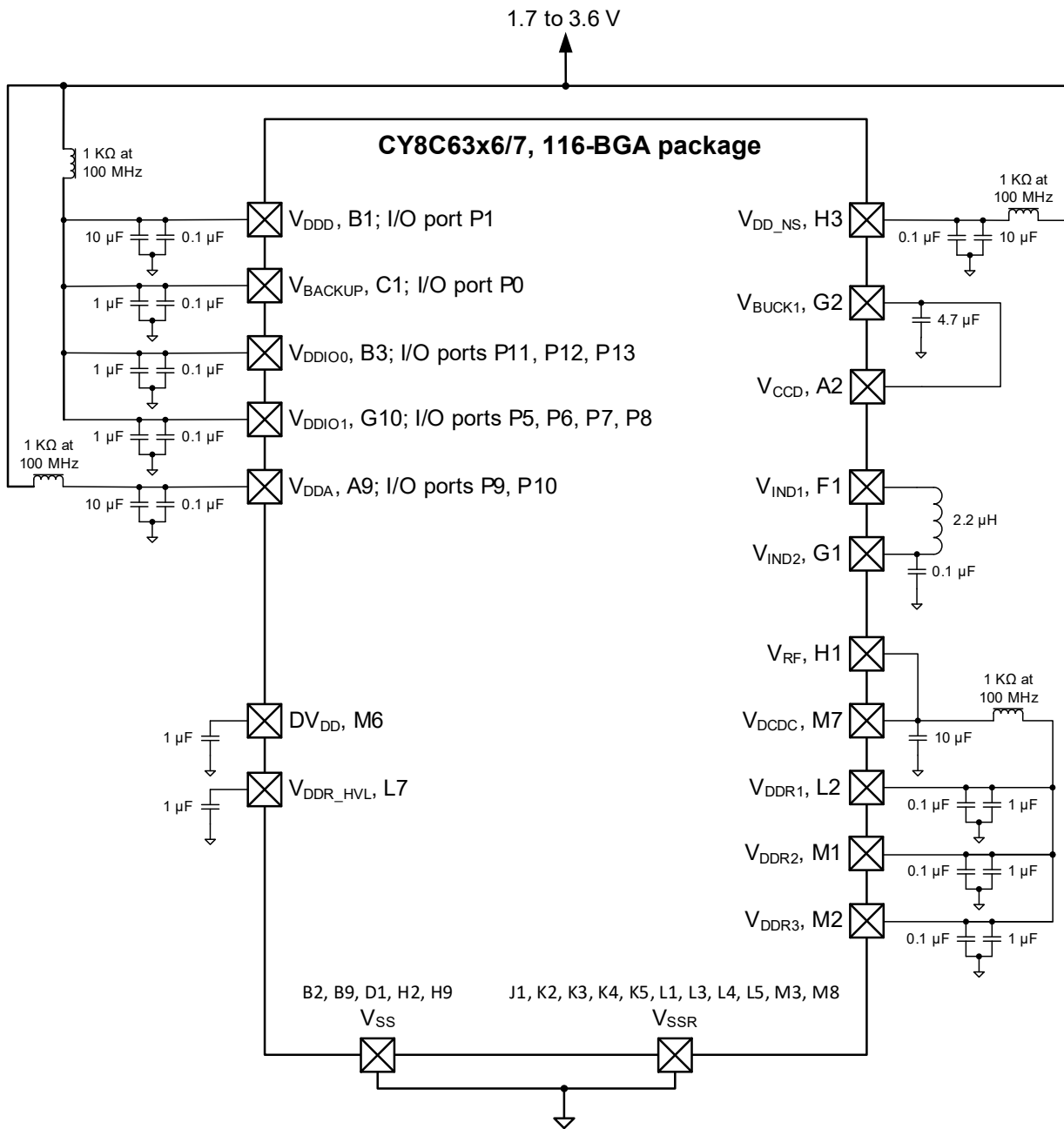


Figure 11. 104-MCSP Power Connection Diagram

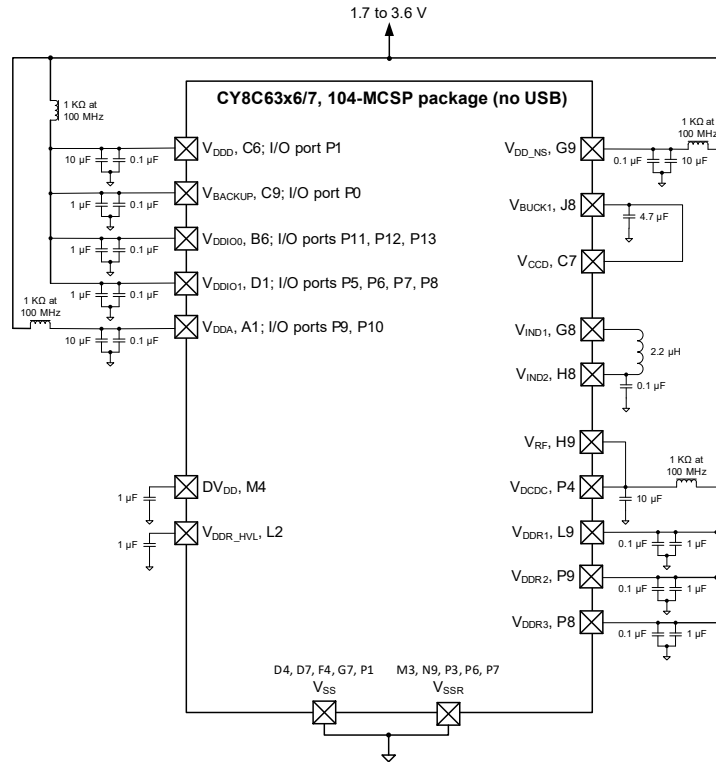
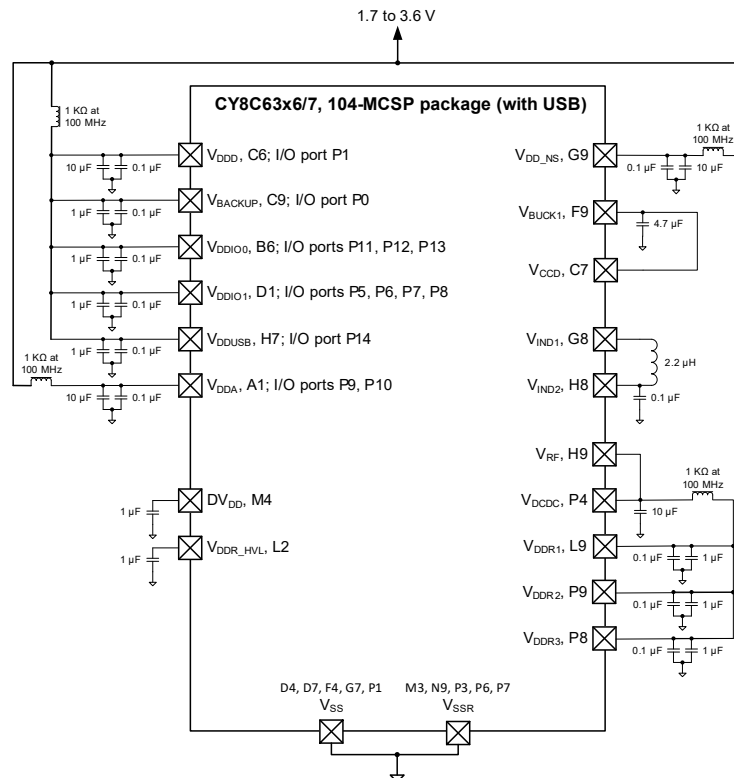
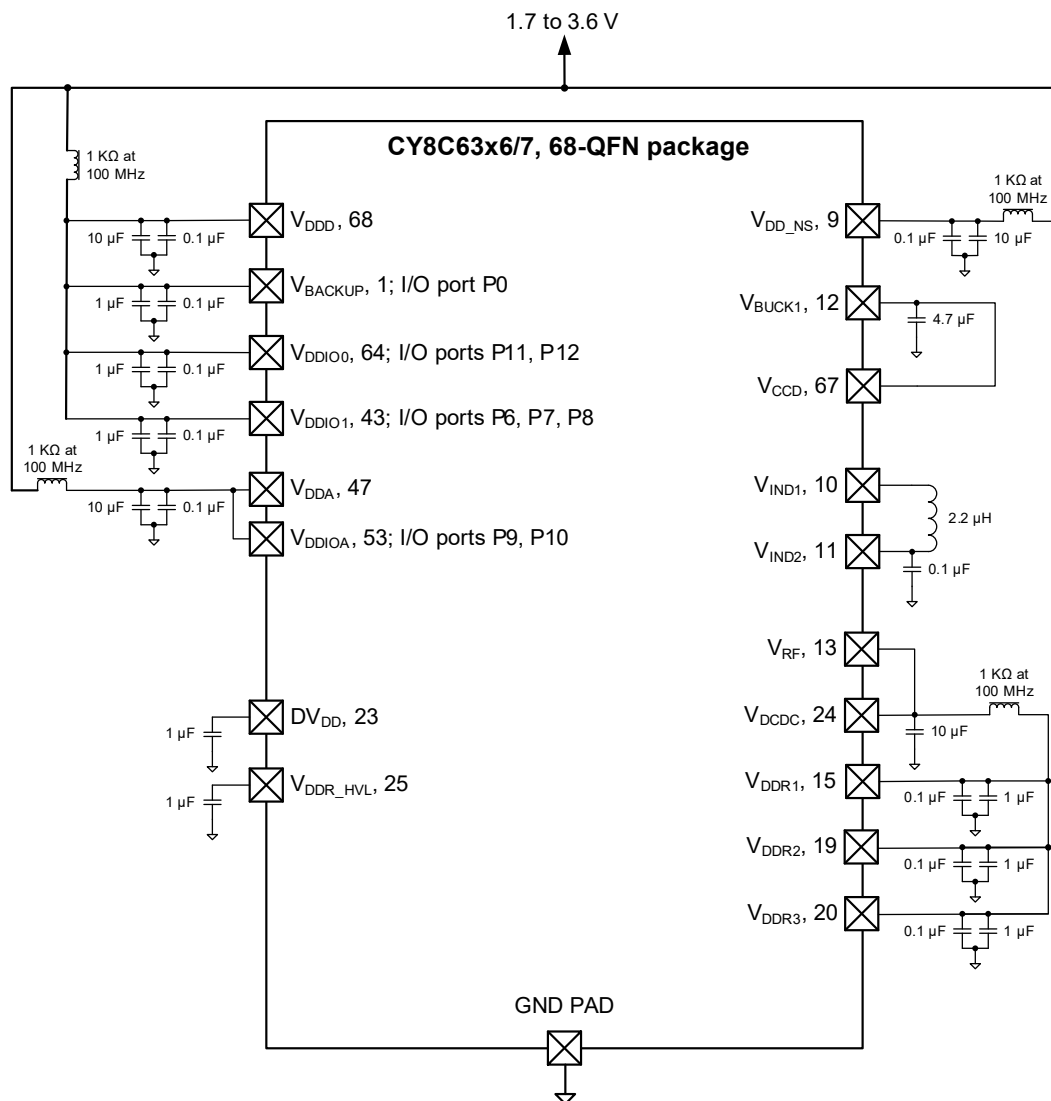


Figure 12. 104-MCSP-USB Power Connection Diagram



In the QFN package, all internal grounds are routed to the metal pad (epad) in the package. This pad must be grounded on the PCB. In addition, the two antenna ground pins (GANT1 and GANT2) on the 68-QFN package should also be connected to the epad ground on the PCB with as short a connection as possible.

Figure 13. 68-QFN Power Connection Diagram



There are as many as eight V_{DDx} supply pins, depending on the package, and multiple V_{SS} ground pins. The power pins are:

- V_{DD_D} : the main digital supply. It powers the low dropout (LDO) regulators and I/O port 1³.
- V_{CCD} : the main LDO output. It requires a 4.7- μ F capacitor for regulation. The LDO can be turned off when V_{CCD} is driven from the switching regulator (see V_{BUCK1} below). For more information, see the power system block diagram in the device technical reference manual (TRM).

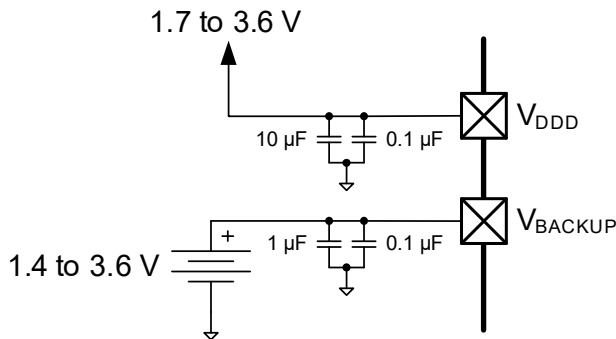
- V_{DDA} : the supply for the analog peripherals. It is also the supply for I/O ports 9 and 10 when V_{DDIOA} is not present.
- V_{DDIOA} : the supply for I/O ports 9 and 10. If it is present in the device package, it must be connected to V_{DDA} .
- V_{DDIO_0} : the supply for I/O ports 11, 12, and 13.
- V_{DDIO_1} : the supply for I/O ports 5, 6, 7, and 8.

Note

3. Port 1 is not available in the 68-QFN package.

- V_{BACKUP} : the supply for the backup domain, which includes the 32-kHz WCO and the RTC. It can be a separate supply as low as 1.4 V, for battery or supercapacitor backup, as Figure 14 shows. Otherwise it is connected to V_{DDD} . It powers I/O port 0.

Figure 14. Separate Battery Connection to V_{BACKUP}



- V_{DDUSB} : the supply for the USB peripheral and the USBDP and USBDM pins. It must be 2.85 V to 3.6 V for USB operation. If USB is not used, it can be 1.7 V to 3.6 V, and the USB pins can be used as limited-capability GPIOs on I/O port 14.

Table 7 shows a summary of the I/O port supplies:

Table 7. I/O Port Supplies

| Port | Supply | Alternate Supply |
|------------|---------------------|------------------|
| 0 | V_{BACKUP} | V_{DDD} |
| 1 | V_{DDD} | - |
| 5, 6, 7, 8 | V_{DDIO1} | - |
| 9, 10 | V_{DDIOA} | V_{DDA} |
| 11, 12, 13 | V_{DDIO0} | - |
| 14 | V_{DDUSB} | - |

- V_{SS} and V_{SSR} : ground pins for the above supplies. All ground pins should be connected together to a common ground.

In addition to the LDO regulator, a single input multiple output (SIMO) switching regulator is included. It provides two regulated outputs using a single inductor. The regulator pins are:

- $V_{\text{DD_NS}}$: the regulator supply.
- V_{IND1} and V_{IND2} : the inductor and capacitor connections.
- V_{BUCK1} : the first regulator output. It is typically used to drive V_{CCD} , see above
- V_{RF} : the second regulator output. It is typically used to drive the BLE radio power pins: V_{DCDC} and V_{DDR_X} .

A set of power pins for the BLE radio are included. They are:

- V_{DCDC} : the radio digital supply.
- V_{DDR1} , V_{DDR2} , and V_{DDR3} : the radio analog supplies.
- DV_{DD} : the radio digital LDO output. It requires a 1 μF capacitor for regulation.
- $V_{\text{DDR_HVL}}$: the radio analog LDO output. It requires a 1 μF capacitor for regulation.

The various V_{DD} power pins are not connected together on chip. They can be connected off chip, in one or more separate nets. If separate power nets are used, they can be isolated from noise from the other nets using optional ferrite beads, as indicated in the diagrams.

No external load should be placed on V_{CCD} , V_{RF} , or any of the switching regulator power pins; whether or not the switching regulator is used.

There are no power pin sequencing requirements; power supplies may be brought up in any order. The power management system holds the device in reset until all power pins are at the voltage levels required for proper operation.

Note: If a battery is installed on the PCB first, V_{DDD} must be cycled for at least 50 μs . This prevents premature drain of the battery during product manufacture and storage.

Bypass capacitors must be connected to a common ground from the V_{DD_X} and other pins, as indicated in the diagrams. Typical practice for systems in this frequency range is to use a 10- μF or 1- μF capacitor in parallel with a smaller capacitor (0.1 μF , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated for optimal bypassing.

All capacitors and inductors should be $\pm 20\%$ or better. The capacitor connected to V_{IND2} should be 100 nF. The recommended inductor value is 2.2 μH $\pm 20\%$ (for example, TDK MLP2012H2R2MT0S1).

It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the applied voltage is a significant percentage of the rated working voltage.

For more information on pad layout, refer to [PSoC 6 CAD libraries](#).

Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings^[4]

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------------------------|--|------|-----|-----------------------|------|----------------------|
| SID1 | V _{DD_ABS} | Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA}) | -0.5 | - | 4 | V | |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SSD} | -0.5 | - | 1.2 | V | |
| SID3 | V _{GPIO_ABS} | GPIO voltage; V _{DDD} or V _{DDA} | -0.5 | - | V _{DD} + 0.5 | V | |
| SID4 | I _{GPIO_ABS} | Current per GPIO | -25 | - | 25 | mA | |
| SID5 | I _{GPIO_injection} | GPIO injection current per pin | -0.5 | - | 0.5 | mA | |
| SID3A | ESD_HBM | Electrostatic discharge Human Body Model | 2200 | - | - | V | |
| SID3B | ESD_HBM_ANT | Electrostatic discharge Human Body Model; Antenna Pin | 500 | - | - | V | RF pin |
| SID4A | ESD_CDM | Electrostatic discharge Charged Device Model | 500 | - | - | V | |
| SID4B | ESD_CDM_ANT | Electrostatic discharge Charged Device Model; Antenna Pin | 200 | - | - | V | RF pin |
| SID4C | ESD_CDM_X | Electrostatic discharge Charged Device Model; XI, XO pins | 200 | - | - | V | XI, XO Pins |
| SID5A | LU | Pin current for latchup-free operation | -100 | - | 100 | mA | |

Note: All specifications are valid for -40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Note

- Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device-Level Specifications
Table 9. Power Supply Range, CPU Current, and Transition Time Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|---------------------|---|------|------|------|------|--|
| DC Specifications | | | | | | | |
| SID6 | V _{DDD} | Internal Regulator and Port 1 GPIO Supply | 1.7 | – | 3.6 | V | – |
| SID7 | V _{DDA} | Analog Power Supply Voltage. Shorted to V _{DDIOA} on PCB. | 1.7 | – | 3.6 | V | Internally unregulated supply |
| SID7A | V _{DDIO1} | GPIO Supply for Ports 5 to 8 when present | 1.7 | – | 3.6 | V | V _{DDIO_1} must be ≥ V _{DDA} . |
| SID7B | V _{DDIO0} | GPIO Supply for Ports 11 to 13 when present | 1.7 | – | 3.6 | V | – |
| SID7E | V _{DDIO0} | Supply for eFuse Programming | 2.38 | 2.5 | 2.62 | V | – |
| SID7C | V _{DDIO2} | GPIO Supply for Ports 2 to 4 on BGA 124 only | 1.7 | – | 3.6 | V | – |
| SID7D | V _{DDIOA} | GPIO Supply for Ports 9 to 10. Must be connected to V _{DDA} on PCB. | 1.7 | – | 3.6 | V | – |
| SID7F | V _{DDUSB} | Supply for Port 14 (USB or GPIO) when present | 1.7 | – | 3.6 | V | Min. supply is 2.85 V for USB |
| SID6B | V _{BACKUP} | Backup Power and GPIO Port 0 supply when present | 1.7 | – | 3.6 | V | Min. is 1.4 V when V _{DDD} is removed. |
| SID8 | V _{CCD1} | Output voltage (for core logic bypass) | – | 1.1 | – | V | High-speed mode |
| SID9 | V _{CCD2} | Output voltage (for core logic bypass) | – | 0.9 | – | V | ULP mode. Valid for –20 to 85 °C. |
| SID10 | C _{EFC} | External regulator voltage (V _{CCD}) bypass | 3.8 | 4.7 | 5.6 | μF | X5R ceramic or better; Value for 0.8 to 1.2 V. |
| SID11 | C _{EXC} | Power supply decoupling capacitor | – | 10 | – | μF | X5R ceramic or better |
| LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO) | | | | | | | |
| Cortex M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF1 | I _{DD1} | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 2.3 | 3.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 3.1 | 3.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 5.7 | 6.5 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDF2 | I _{DD2} | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | – | 0.9 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.2 | 1.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.8 | 3.5 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC1 | I _{DD3} | Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone. | – | 6.3 | 7 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 9.7 | 11.2 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 14.4 | 15.1 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDC2 | I _{DD4} | Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO & FLL. Dhrystone. | – | 4.8 | 5.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 7.4 | 8.4 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 11.3 | 12 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |

Table 9. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|-------------------|--|-----|------|-----|------|--|
| SIDC3 | I _{DD5} | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO & FLL. Dhrystone | - | 2.4 | 3.4 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 3.7 | 4.1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 6.3 | 7.2 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDC4 | I _{DD6} | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone. | - | 0.9 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.3 | 1.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 3 | 3.8 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF3 | I _{DD7} | Execute from Flash; CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1). | - | 2.4 | 3.3 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 3.2 | 3.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 5.6 | 6.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDF4 | I _{DD8} | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | - | 0.8 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.1 | 1.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 2.60 | 3.4 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC5 | I _{DD9} | Execute from Cache; CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone. | - | 3.8 | 4.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 5.9 | 6.5 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 9 | 9.7 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDC6 | I _{DD10} | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.8 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.20 | 1.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 2.60 | 3.4 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS1 | I _{DD11} | CM4 Sleep 100 MHz; CM0+ Sleep 25 MHz. With IMO & FLL. | - | 1.5 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 2.2 | 2.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 4 | 4.6 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDS2 | I _{DD12} | CM4 Sleep 50 MHz; CM0+ Sleep 25 MHz. With IMO & FLL. | - | 1.2 | 1.9 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.7 | 2.2 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 3.4 | 4.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDS3 | I _{DD13} | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | - | 0.7 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1 | 1.5 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 2.4 | 3.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS4 | I _{DD14} | CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL. | - | 1.3 | 2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.9 | 2.4 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | - | 3.80 | 4.6 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |

Table 9. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-------------------|--|-----|------|-----|------|--|
| SIDS5 | I _{DD15} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.3 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1 | 1.5 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.4 | 3.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA1 | I _{DD16} | Execute from Flash; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1). | – | 0.9 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.2 | 1.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.8 | 3.5 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDLPA2 | I _{DD17} | Execute from Cache; CM4 LPA 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.9 | 1.5 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.3 | 1.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.9 | 3.7 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA3 | I _{DD18} | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | – | 0.8 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.1 | 1.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.7 | 3.6 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| SIDLPA4 | I _{DD19} | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | – | 0.8 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1.2 | 1.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.7 | 3.6 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS1 | I _{DD20} | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | – | 0.7 | 1.1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 1 | 1.5 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.4 | 3.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS3 | I _{DD22} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | – | 0.6 | 1.1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 0.9 | 1.5 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| | | | – | 2.4 | 3.3 | mA | V _{DDD} = 1.8 to 3.3 V, LDO, Max at 85 °C |
| ULP RANGE POWER SPECIFICATIONS (for V_{CCD} = 0.9 V using the Buck). ULP mode is valid from –20 to +85 °C. | | | | | | | |
| Cortex M4. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF5 | I _{DD3} | Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1). | – | 1.7 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 2.1 | 2.4 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDF6 | I _{DD4} | Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1) | – | 0.56 | 0.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 0.75 | 1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC8 | I _{DD10} | Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone. | – | 1.6 | 2.2 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 2.4 | 2.7 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDC9 | I _{DD11} | Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | – | 0.65 | 0.8 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | – | 0.8 | 1.1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |

Table 9. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-------------------|--|-----|------|------|------|---|
| Cortex M0+. Active Mode | | | | | | | |
| Execute with Cache Disabled (Flash) | | | | | | | |
| SIDF7 | I _{DD16} | Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1). | - | 1 | 1.4 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.34 | 1.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDF8 | I _{DD17} | Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1). | - | 0.54 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.73 | 1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Execute with Cache Enabled | | | | | | | |
| SIDC10 | I _{DD18} | Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone. | - | 0.91 | 1.25 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.34 | 1.6 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDC11 | I _{DD19} | Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.51 | 0.72 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.73 | 0.95 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M4. Sleep Mode | | | | | | | |
| SIDS7 | I _{DD21} | CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 0.76 | 1.1 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 1.1 | 1.4 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDS8 | I _{DD22} | CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO. | - | 0.42 | 0.65 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.59 | 0.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M0+. Sleep Mode | | | | | | | |
| SIDS9 | I _{DD23} | CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL. | - | 0.62 | 0.9 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.88 | 1.1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDS10 | I _{DD24} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.41 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.58 | 0.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA5 | I _{DD25} | Execute from Flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1). | - | 0.52 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.76 | 1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDLPA6 | I _{DD26} | Execute from Cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone. | - | 0.54 | 0.76 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.78 | 1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPA7 | I _{DD27} | Execute from Flash. CM4 Off, CM0+ Active 8 MHz. With IMO. While (1). | - | 0.51 | 0.75 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.75 | 1 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| SIDLPA8 | I _{DD28} | Execute from Cache. CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone. | - | 0.48 | 0.7 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.7 | 0.95 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M4. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS5 | I _{DD29} | CM4 Sleep 8 MHz, CM0 Sleep 8 MHz. With IMO. | - | 0.4 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.57 | 0.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |
| Cortex M0+. Minimum Regulator Current Mode | | | | | | | |
| SIDLPS7 | I _{DD31} | CM4 Off, CM0+ Sleep 8 MHz. With IMO. | - | 0.39 | 0.6 | mA | V _{DDD} = 3.3 V, Buck ON, Max at 60 °C |
| | | | - | 0.56 | 0.8 | mA | V _{DDD} = 1.8 V, Buck ON, Max at 60 °C |

Table 9. Power Supply Range, CPU Current, and Transition Time Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|------------------------------------|------------------------|--|-----|-----|-----|------|-------------------------|
| Deep Sleep Mode | | | | | | | |
| SIDDS1 | I _{DD33A} | With internal Buck enabled and 64K SRAM retention | – | 7 | – | μA | Max value is at 85 °C |
| SIDDS1_B | I _{DD33A_B} | With internal Buck enabled and 64K SRAM retention | – | 7 | – | μA | Max value is at 60 °C |
| SIDDS2 | I _{DD33B} | With internal Buck enabled and 256K SRAM retention | – | 9 | – | μA | Max value is at 85 °C |
| SIDDS2_B | I _{DD33B_B} | With internal Buck enabled and 256K SRAM retention | – | 9 | – | μA | Max value is at 60 °C |
| Hibernate Mode | | | | | | | |
| SIDHIB1 | I _{DD34} | V _{DDD} = 1.8 V | – | 300 | – | nA | No clocks running |
| SIDHIB2 | I _{DD34A} | V _{DDD} = 3.3 V | – | 800 | – | nA | No clocks running |
| Power Mode Transition Times | | | | | | | |
| SID12 | T _{LPACT_ACT} | Minimum Regulator Current to LP transition time | – | – | 35 | μs | Including PLL lock time |
| SID13 | T _{DS_LPACT} | Deep Sleep to LP transition time | – | – | 25 | μs | Guaranteed by design |
| SID14 | T _{HIB_ACT} | Hibernate to LP transition time | – | 500 | – | μs | Including PLL lock time |

XRES

Table 10. XRES DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------------------|--|--------------------------|-----|--------------------------|------|--------------------------|
| SID17 | T _{XRES_IDD} | IDD when XRES asserted | – | 300 | – | nA | V _{DDD} = 1.8 V |
| SID17A | T _{XRES_IDD_1} | IDD when XRES asserted | – | 800 | – | nA | V _{DDD} = 3.3 V |
| SID77 | V _{IH} | Input Voltage high threshold | 0.7 * V _{DD} | – | – | V | CMOS Input |
| SID78 | V _{IL} | Input Voltage low threshold | – | – | 0.3 * V _{DD} | V | CMOS Input |
| SID80 | C _{IN} | Input Capacitance | – | 3 | – | pF | – |
| SID81 | V _{HYSXRES} | Input voltage hysteresis | – | 100 | – | mV | – |
| SID82 | I _{DIODE} | Current through protection diode to V _{DD} /V _{SS} | – | – | 100 | μA | – |

Table 11. XRES AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------------------|---|-----|-----|-----|------|--------------------------|
| SID15 | T _{XRES_ACT} | POR or XRES release to Active transition time | – | 750 | – | μs | Normal mode, 50 MHz M0+. |
| SID16 | T _{XRES_PW} | XRES Pulse width | 5 | – | – | μs | – |

GPIO

Table 12. GPIO DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------------|---|-----------------|-----|----------------|------------|---------------------------|
| SID57 | V_{IH} | Input voltage high threshold | $0.7 * V_{DD}$ | – | – | V | CMOS Input |
| SID57A | I_{IHS} | Input current when Pad > V_{DDIO} for OVT inputs | – | – | 10 | μA | Per I ² C Spec |
| SID58 | V_{IL} | Input voltage low threshold | – | – | $0.3 * V_{DD}$ | V | CMOS Input |
| SID241 | V_{IH} | LVTTL input, $V_{DD} < 2.7 V$ | $0.7 * V_{DD}$ | – | – | V | – |
| SID242 | V_{IL} | LVTTL input, $V_{DD} < 2.7 V$ | – | – | $0.3 * V_{DD}$ | V | – |
| SID243 | V_{IH} | LVTTL input, $V_{DD} \geq 2.7 V$ | 2.0 | – | – | V | – |
| SID244 | V_{IL} | LVTTL input, $V_{DD} \geq 2.7 V$ | – | – | 0.8 | V | – |
| SID59 | V_{OH} | Output voltage high level | $V_{DD} - 0.5$ | – | – | V | $I_{OH} = 8 mA$ |
| SID62A | V_{OL} | Output voltage low level | – | – | 0.4 | V | $I_{OL} = 8 mA$ |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| SID65 | I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DD} = 3.0 V$ |
| SID65A | I_{IL_CTBM} | Input leakage on CTBm input pins | – | – | 4 | nA | – |
| SID66 | C_{IN} | Input Capacitance | – | – | 5 | pF | – |
| SID67 | V_{HYSTTL} | Input hysteresis LVTTL $V_{DD} > 2.7 V$ | 100 | 0 | – | mV | – |
| SID68 | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 * V_{DD}$ | – | – | mV | – |
| SID69 | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μA | – |
| SID69A | I_{TOT_GPIO} | Maximum Total Source or Sink Chip Current | – | – | 200 | mA | – |

Table 13. GPIO AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------|---|-----|-----|-----|------|--|
| SID70 | T_{RISEF} | Rise time in Fast Strong Mode. 10% to 90% of V_{DD} | – | – | 2.5 | ns | Load = 15 pF, 8 mA drive strength |
| SID71 | T_{FALLF} | Fall time in Fast Strong Mode. 10% to 90% of V_{DD} | – | – | 2.5 | ns | Load = 15 pF, 8 mA drive strength |
| SID72 | T_{RISES_1} | Rise time in Slow Strong Mode. 10% to 90% of V_{DD} | 52 | – | 142 | ns | Load = 15 pF, 8 mA drive strength, $V_{DD} \leq 2.7 V$ |
| SID72A | T_{RISES_2} | Rise time in Slow Strong Mode. 10% to 90% of V_{DD} | 48 | – | 102 | ns | Load = 15 pF, 8 mA drive strength, $2.7 V < V_{DD} \leq 3.6 V$ |
| SID73 | T_{FALLS_1} | Fall time in Slow Strong Mode. 10% to 90% of V_{DD} | 44 | – | 211 | ns | Load = 15 pF, 8 mA drive strength, $V_{DD} \leq 2.7 V$ |
| SID73A | T_{FALLS_2} | Fall time in Slow Strong Mode. 10% to 90% of V_{DD} | 42 | – | 93 | ns | Load = 15 pF, 8 mA drive strength, $2.7 V < V_{DD} \leq 3.6 V$ |

Table 13. GPIO AC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------------------|--|------------------------------|-----|------|------|---|
| SID73G | T _{FALL_I2C} | Fall time (30% to 70% of V _{DD}) in Slow Strong mode | 20 * V _{DDIO} / 5.5 | – | 250 | ns | Clload = 10 pF to 400 pF, 8-mA drive strength |
| SID74 | F _{GPIOOUT1} | GPIO Fout. Fast Strong mode. | – | – | 100 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID75 | F _{GPIOOUT2} | GPIO Fout; Slow Strong mode. | – | – | 16.7 | MHz | 90/10%, 15-pF load, 60/40 duty cycle |
| SID76 | F _{GPIOOUT3} | GPIO Fout; Fast Strong mode. | – | – | 7 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID245 | F _{GPIOOUT4} | GPIO Fout; Slow Strong mode. | – | – | 3.5 | MHz | 90/10%, 25-pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DD} ≤ 3.6 V | – | – | 100 | MHz | 90/10% V _{IO} |

Analog Peripherals

Opamp

Table 14. Opamp Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------------------|---|-----|------|------------------------------------|------|--|
| | I _{DD} | Opamp Block current. No load. | – | – | – | | – |
| SID269 | I _{DD_HI} | Power = Hi | – | 1300 | 1500 | μA | – |
| SID270 | I _{DD_MED} | Power = Med | – | 450 | 600 | μA | – |
| SID271 | I _{DD_LOW} | Power = Lo | – | 250 | 350 | μA | – |
| | GBW | Load = 50 pF, 0.1 mA. V _{D_{DDA}} ≥ 2.7 V | – | – | – | | – |
| SID272 | G _{BW_HI} | Power = Hi | 6 | – | – | MHz | – |
| SID273 | G _{BW_MED} | Power = Med | 3 | – | – | MHz | – |
| SID274 | G _{BW_LO} | Power = Lo | 1 | – | – | MHz | – |
| | I _{OUT_MAX} | V _{D_{DDA}} ≥ 2.7 V, 500 mV from rail | – | – | – | | – |
| SID275 | I _{OUT_MAX_HI} | Power = Hi | 10 | – | – | mA | – |
| SID276 | I _{OUT_MAX_MID} | Power = Mid | 10 | – | – | mA | – |
| SID277 | I _{OUT_MAX_LO} | Power = Lo | – | 5 | – | mA | – |
| | I _{OUT} | V _{D_{DDA}} = 1.71 V, 500 mV from rail | – | – | – | | – |
| SID278 | I _{OUT_MAX_HI} | Power = Hi | 4 | – | – | mA | – |
| SID279 | I _{OUT_MAX_MID} | Power = Mid | 4 | – | – | mA | – |
| SID280 | I _{OUT_MAX_LO} | Power = Lo | – | 2 | – | mA | – |
| SID281 | V _{IN} | Input voltage range | 0 | – | V _{D_{DDA}} – 0.2 | V | Charge pump ON |
| SID282 | V _{CM} | Input common mode voltage | 0 | – | V _{D_{DDA}} – 1.5 | V | Charge pump OFF, V _{D_{DDA}} ≥ 2.7 V |
| | V _{OUT} | V _{D_{DDA}} ≥ 2.7 V | – | – | – | | – |
| SID283 | V _{OUT_1} | Power = Hi, Iload = 10 mA | 0.5 | – | V _{D_{DDA}} – 0.5 | V | – |
| SID284 | V _{OUT_2} | Power = Hi, Iload = 1 mA | 0.2 | – | V _{D_{DDA}} – 0.2 | V | – |
| SID285 | V _{OUT_3} | Power = Med, Iload = 1 mA | 0.2 | – | V _{D_{DDA}} – 0.2 | V | – |

Table 14. Opamp Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|------------------------|------------------------|--|-----|------|------------------------------------|---------|---|
| SID286 | V _{OUT_4} | Power = Lo, Iload = 0.1 mA | 0.2 | – | V _{D_{DDA}} – 0.2 | V | – |
| SID288 | V _{OS_TR} | Offset voltage | –1 | ±0.5 | 1 | mV | Power = Hi, 0.2 V < V _{OUT} < (V _{D_{DDA}} – 0.2 V) |
| SID288A | V _{OS_TR} | Offset voltage | – | ±1 | – | mV | Power = Med |
| SID288B | V _{OS_TR} | Offset voltage | – | ±2 | – | mV | Power = Lo |
| SID290 | V _{OS_DR_TR} | Offset voltage drift | –10 | ±3 | 10 | µV/°C | Power = Hi, 0.2 V < V _{OUT} < (V _{D_{DDA}} – 0.2 V) |
| SID290A | V _{OS_DR_TR} | Offset voltage drift | – | ±10 | – | µV/°C | Power = Med |
| SID290B | V _{OS_DR_TR} | Offset voltage drift | – | ±10 | – | µV/°C | Power = Lo |
| SID291 | CMRR | DC Common mode rejection ratio | 67 | 80 | – | dB | V _{D_{DDA}} ≥ 2.7 V |
| SID292 | PSRR | Power supply rejection ratio at 1 kHz, 10-mV ripple | 70 | 85 | – | dB | V _{D_{DDA}} ≥ 2.7 V |
| SID65A | I _{IL_CTBM} | Input leakage on CTBm input pins | – | – | 4 | nA | – |
| Noise | | | | | | | |
| SID293 | VN1 | Input-referred, 1 Hz–1 GHz, power = Hi | – | 100 | – | µVrms | – |
| SID294 | VN2 | Input-referred, 1 kHz, power = Hi | – | 180 | – | nV/rtHz | – |
| SID295 | VN3 | Input-referred, 10 kHz, power = Hi | – | 70 | – | nV/rtHz | – |
| SID296 | VN4 | Input-referred, 100 kHz, power = Hi | – | 38 | – | nV/rtHz | – |
| SID297 | CLOAD | Stable up to max. load. Performance specs at 50 pF. | – | – | 125 | pF | – |
| SID298 | SLEW_RATE | Output slew rate | 4 | – | – | V/µs | Clload = 50 pF, Power = Hi, V _{D_{DDA}} ≥ 2.7 V |
| SID299 | T _{OP_WAKE} | From disable to enable, no external RC dominating | – | 25 | – | µs | – |
| | COMP_MODE | Comparator mode; 50-mV overdrive, Trise = Tfall (approx.) | – | – | – | – | – |
| SID300 | T _{PD1} | Response time; power = Hi | – | 150 | – | ns | – |
| SID301 | T _{PD2} | Response time; power = Med | – | 400 | – | ns | – |
| SID302 | T _{PD3} | Response time; power = Lo | – | 2000 | – | ns | – |
| SID303 | V _{HYST_OP} | Hysteresis | – | 10 | – | mV | – |
| Deep Sleep Mode | | Mode 1 - Full reference current (Higher GBW) Mode 2 – Approximately 1/10th reference current (Lower Power Consumption) ^[5] | | | | | Deep Sleep mode operation: V _{D_{DDA}} ≥ 2.7 V. V _{IN} is 0.2 to V _{D_{DDA}} – 1.5 V |
| SID_DS_1 | I _{DD_HI_M1} | Mode 1, High current | – | 1300 | 1500 | µA | Typ at 25 °C |
| SID_DS_2 | I _{DD_MED_M1} | Mode 1, Medium current | – | 460 | 600 | µA | Typ at 25 °C |
| SID_DS_3 | I _{DD_LOW_M1} | Mode 1, Low current | – | 230 | 350 | µA | Typ at 25 °C |
| SID_DS_4 | I _{DD_HI_M2} | Mode 2, High current | – | 120 | – | µA | 25 °C |

Note

5. Reference current is supplied by AREF (analog reference) block.

Table 14. Opamp Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|-----------|-------------------------|------------------------|-----|-----|-----|------|---|
| SID_DS_5 | I _{DD_MED_M2} | Mode 2, Medium current | – | 60 | – | μA | 25 °C |
| SID_DS_6 | I _{DD_LOW_M2} | Mode 2, Low current | – | 15 | – | μA | 25 °C |
| SID_DS_7 | GBW_HI_M1 | Mode 1, High current | – | 4 | – | MHz | 25 °C |
| SID_DS_8 | GBW_MED_M1 | Mode 1, Medium current | – | 2 | – | MHz | 25 °C |
| SID_DS_9 | GBW_LOW_M1 | Mode 1, Low current | – | 0.5 | – | MHz | 25 °C |
| SID_DS_10 | GBW_HI_M2 | Mode 2, High current | – | 0.5 | – | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_11 | GBW_MED_M2 | Mode 2, Medium current | – | 0.2 | – | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_12 | GBW_LOW_M2 | Mode 2, Low current | – | 0.1 | – | MHz | 20-pF load, no DC load 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_13 | V _{OS_HI_M1} | Mode 1, High current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_14 | V _{OS_MED_M1} | Mode 1, Medium current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_15 | V _{OS_LOW_M1} | Mode 1, Low current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_16 | V _{OS_HI_M2} | Mode 2, High current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_17 | V _{OS_MED_M2} | Mode 2, Medium current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_18 | V _{OS_LOW_M2} | Mode 2, Low current | – | 5 | – | mV | 25 °C, 0.2 V to V _{DDA} – 1.5 V |
| SID_DS_19 | I _{OUT_HI_M1} | Mode 1, High current | – | 10 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |
| SID_DS_20 | I _{OUT_MED_M1} | Mode 1, Medium current | – | 10 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |
| SID_DS_21 | I _{OUT_LOW_M1} | Mode 1, Low current | – | 4 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |
| SID_DS_22 | I _{OUT_HI_M2} | Mode 2, High current | – | 1 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |
| SID_DS_23 | I _{OUT_MED_M2} | Mode 2, Medium current | – | 1 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |
| SID_DS_24 | I _{OUT_LOW_M2} | Mode 2, Low current | – | 0.5 | – | mA | Output is 0.5 V to V _{DDA} – 0.5 V |

Low-Power (LP) Comparator
Table 15. LP Comparator DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------------|---|-----|-----|-----|------|------------------------|
| SID84 | V _{OFFSET1} | Input offset voltage for COMP1. Normal power mode. | –10 | – | 10 | mV | COMP0 offset is ±25 mV |
| SID85A | V _{OFFSET2} | Input offset voltage. Low-power mode. | –25 | ±12 | 25 | mV | – |
| SID85B | V _{OFFSET3} | Input offset voltage. Ultra low-power mode. | –25 | ±12 | 25 | mV | – |
| SID86 | V _{HYST1} | Hysteresis when enabled in Normal mode | – | – | 60 | mV | – |

Table 15. LP Comparator DC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------------|---|-----|-----|--------------------------|------|----------------------|
| SID86A | V _{HYST2} | Hysteresis when enabled in Low-power mode | – | – | 80 | mV | – |
| SID87 | V _{ICM1} | Input common mode voltage in Normal mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID247 | V _{ICM2} | Input common mode voltage in Low power mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID247A | V _{ICM3} | Input common mode voltage in Ultra low power mode | 0 | – | V _{DDIO1} – 0.1 | V | – |
| SID88 | CMRR | Common mode rejection ratio in Normal power mode | 50 | – | – | dB | – |
| SID89 | I _{CMP1} | Block Current, Normal mode | – | – | 150 | μA | – |
| SID248 | I _{CMP2} | Block Current, Low power mode | – | – | 10 | μA | – |
| SID259 | I _{CMP3} | Block Current in Ultra low-power mode | – | 0.3 | 0.85 | μA | – |
| SID90 | Z _{CMP} | DC Input impedance of comparator | 35 | – | – | MΩ | – |

Table 16. LP Comparator AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------------|---|-----|-----|------|------|----------------------------|
| SID91 | T _{RESP1} | Response time, Normal mode, 100 mV overdrive | – | – | 100 | ns | – |
| SID258 | T _{RESP2} | Response time, Low power mode, 100 mV overdrive | – | – | 1000 | ns | – |
| SID92 | T _{RESP3} | Response time, Ultra-low power mode, 100 mV overdrive | – | – | 20 | μs | – |
| SID92E | T _{CMP_EN1} | Time from Enabling to operation | – | – | 10 | μs | Normal and Low-power modes |
| SID92F | T _{CMP_EN2} | Time from Enabling to operation | – | – | 50 | μs | Ultra low-power mode |

Table 17. Temperature Sensor Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------------|-----------------------------|-----|-----|-----|------|----------------------|
| SID93 | T _{SENSACC} | Temperature sensor accuracy | –5 | ±1 | 5 | °C | –40 to +85 °C |

Table 18. Internal Reference Specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------------|-------------|-------|-----|-------|------|----------------------|
| SID93R | V _{REFBG} | – | 1.188 | 1.2 | 1.212 | V | – |

SAR ADC

Table 19. 12-bit SAR ADC DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------|--|-----------------|-----|------------------|------|---------------------------------|
| SID94 | A_RES | SAR ADC Resolution | – | – | 12 | bits | – |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | – | 8 full speed. |
| SID96 | A-CHNKS_D | Number of channels - differential | – | – | 8 | – | Diff inputs use neighboring I/O |
| SID97 | A-MONO | Monotonicity | – | – | – | – | Yes |
| SID98 | A_GAINERR | Gain error | – | – | ±0.2 | % | With external reference. |
| SID99 | A_OFFSET | Input offset voltage | – | – | 2 | mV | Measured with 1-V reference |
| SID100 | A_ISAR_1 | Current consumption at 1 Msps | – | – | 1 | mA | At 1 Msps. External Bypass Cap. |
| SID100A | A_ISAR_2 | Current consumption at 1 Msps. Reference = V _{DD} | – | – | 1.25 | mA | At 1 Msps. External Bypass Cap. |
| SID101 | A_VINS | Input voltage range - single-ended | V _{SS} | – | V _{DDA} | V | – |
| SID102 | A_VIND | Input voltage range - differential | V _{SS} | – | V _{DDA} | V | – |
| SID103 | A_INRES | Input resistance | – | – | 2.2 | kΩ | – |
| SID104 | A_INCAP | Input capacitance | – | – | 10 | pF | – |

Table 20. 12-bit SAR ADC AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-----------|--|-----|-----|-----|------|--|
| 12-bit SAR ADC AC Specifications | | | | | | | |
| SID106 | A_PSR | Power supply rejection ratio | 70 | – | – | dB | – |
| SID107 | A_CMRR | Common mode rejection ratio | 66 | – | – | dB | Measured at 1 V. |
| One Megasample per second mode: | | | | | | | |
| SID108 | A_SAMP_1 | Sample rate with external reference bypass cap. | – | – | 1 | MSPS | – |
| SID108A | A_SAMP_2 | Sample rate with no bypass cap; Reference = V _{DD} | – | – | 250 | kSPS | – |
| SID108B | A_SAMP_3 | Sample rate with no bypass cap. Internal reference. | – | – | 100 | kSPS | – |
| SID109 | A_SINAD | Signal-to-noise and Distortion ratio (SINAD). V _{DDA} = 2.7 to 3.6 V, 1 Msps. | 64 | – | – | dB | F _{in} = 10 kHz |
| SID111A | A_INL | Integral Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msps | –2 | – | 2 | LSB | Measured with internal V _{REF} = 1.2 V and bypass cap. |
| SID111B | A_INL | Integral Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msps | –4 | – | 4 | LSB | Measured with external V _{REF} ≥ 1 V and V _{IN} common mode < 2 * V _{ref} . |
| SID112A | A_DNL | Differential Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msps | –1 | – | 1.4 | LSB | Measured with internal V _{REF} = 1.2 V and bypass cap. |
| SID112B | A_DNL | Differential Non Linearity. V _{DDA} = 2.7 to 3.6 V, 1 Msps | –1 | – | 1.7 | LSB | Measured with external V _{REF} ≥ 1 V and V _{IN} common mode < 2 * V _{ref} . |
| SID113 | A_THD | Total harmonic distortion. V _{DDA} = 2.7 to 3.6 V, 1 Msps. | – | – | –65 | dB | F _{in} = 10 kHz |

DAC

Table 21. 12-bit DAC DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------|----------------------------------|-----|-----|-----|------------|-----------------------|
| SID108D | DAC_RES | DAC resolution | – | – | 12 | bits | – |
| SID111D | DAC_INL | Integral Non-Linearity | –4 | – | 4 | LSB | – |
| SID112D | DAC_DNL | Differential Non Linearity | –2 | – | 2 | LSB | Monotonic to 11 bits. |
| SID99D | DAC_OFFSET | Output Voltage zero offset error | –2 | – | 1 | mV | For 000 (hex) |
| SID103D | DAC_OUT_RES | DAC Output Resistance | – | 15 | – | k Ω | – |
| SID100D | DAC_IDD | DAC Current | – | – | 125 | μ A | – |
| SID101D | DAC_QIDD | DAC Current when DAC stopped | – | – | 1 | μ A | – |

Table 22. 12-bit DAC AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------|--|-----|-----|-----|---------|---|
| SID109D | DAC_CONV | DAC Settling time | – | – | 2 | μ s | Driving through CTBm buffer; 25-pF load |
| SID110D | DAC_Wakeup | Time from Enabling to ready for conversion | – | – | 10 | μ s | – |

CSD

Table 23. CapSense Sigma-Delta (CSD) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|------------------------------|----------------------------|---|-----|-----|------------------------|---------|--|
| CSD V2 Specifications | | | | | | | |
| SYS.PER#3 | V _{DD_RIPPLE} | Max allowed ripple on power supply, DC to 10 MHz | – | – | \pm 50 | mV | V _{DDA} > 2 V (with ripple), 25 °C T _A , Sensitivity = 0.1 pF |
| SYS.PER#16 | V _{DD_RIPPLE_1.8} | Max allowed ripple on power supply, DC to 10 MHz | – | – | \pm 25 | mV | V _{DDA} > 1.75 V (with ripple), 25 °C T _A , Parasitic Capacitance (C _P) < 20 pF, Sensitivity \geq 0.4 pF |
| SID.CSD.BLK | I _{CSD} | Maximum block current | | | 4500 | μ A | – |
| SID.CSD#15 | V _{REF} | Voltage reference for CSD and Comparator | 0.6 | 1.2 | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} \geq 0.6 V |
| SID.CSD#15A | V _{REF_EXT} | External Voltage reference for CSD and Comparator | 0.6 | | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} \geq 0.6 V |
| SID.CSD#16 | I _{DAC1IDD} | IDAC1 (7-bits) block current | – | – | 1900 | μ A | – |
| SID.CSD#17 | I _{DAC2IDD} | IDAC2 (7-bits) block current | – | – | 1900 | μ A | – |
| SID308 | V _{CSD} | Voltage range of operation | 1.7 | – | 3.6 | V | 1.71 to 3.6 V |
| SID308A | V _{COMPIDAC} | Voltage compliance range of IDAC | 0.6 | – | V _{DDA} – 0.6 | V | V _{DDA} – V _{REF} \geq 0.6 V |
| SID309 | I _{DAC1DNL} | DNL | –1 | – | 1 | LSB | – |
| SID310 | I _{DAC1INL} | INL | –3 | – | 3 | LSB | If V _{DDA} < 2 V then for LSB of 2.4 μ A or less |
| SID311 | I _{DAC2DNL} | DNL | –1 | – | 1 | LSB | – |
| SID312 | I _{DAC2INL} | INL | –3 | – | 3 | LSB | If V _{DDA} < 2 V then for LSB of 2.4 μ A or less |

Table 23. CapSense Sigma-Delta (CSD) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|------------------------|--|------|-----|------|-------|------------------------------------|
| SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization | | | | | | | |
| SID313_1A | SNRC_1 | SRSS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 9.5-pF max. capacitance |
| SID313_1B | SNRC_2 | SRSS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 31-pF max. capacitance |
| SID313_1C | SNRC_3 | SRSS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 61-pF max. capacitance |
| SID313_2A | SNRC_4 | PASS Reference. IMO + FLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 12-pF max. capacitance |
| SID313_2B | SNRC_5 | PASS Reference. IMO + FLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 47-pF max. capacitance |
| SID313_2C | SNRC_6 | PASS Reference. IMO + FLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3A | SNRC_7 | PASS Reference. IMO + PLL Clock Source. 0.1-pF sensitivity | 5 | – | – | Ratio | 27-pF max. capacitance |
| SID313_3B | SNRC_8 | PASS Reference. IMO + PLL Clock Source. 0.3-pF sensitivity | 5 | – | – | Ratio | 86-pF max. capacitance |
| SID313_3C | SNRC_9 | PASS Reference. IMO + PLL Clock Source. 0.6-pF sensitivity | 5 | – | – | Ratio | 168-pF max. capacitance |
| SID314 | I _{DAC1CRT1} | Output current of IDAC1 (7 bits) in low range | 4.2 | | 5.7 | μA | LSB = 37.5-nA typ |
| SID314A | I _{DAC1CRT2} | Output current of IDAC1(7 bits) in medium range | 33.7 | | 45.6 | μA | LSB = 300-nA typ. |
| SID314B | I _{DAC1CRT3} | Output current of IDAC1(7 bits) in high range | 270 | | 365 | μA | LSB = 2.4-μA typ. |
| SID314C | I _{DAC1CRT12} | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | | 11.4 | μA | LSB = 37.5-nA typ. 2X output stage |
| SID314D | I _{DAC1CRT22} | Output current of IDAC1(7 bits) in medium range, 2X mode | 67 | | 91 | μA | LSB = 300-nA typ. 2X output stage |
| SID314E | I _{DAC1CRT32} | Output current of IDAC1(7 bits) in high range, 2X mode. V _{DDA} > 2 V | 540 | | 730 | μA | LSB = 2.4-μA typ. 2X output stage |
| SID315 | I _{DAC2CRT1} | Output current of IDAC2 (7 bits) in low range | 4.2 | | 5.7 | μA | LSB = 37.5-nA typ. |
| SID315A | I _{DAC2CRT2} | Output current of IDAC2 (7 bits) in medium range | 33.7 | | 45.6 | μA | LSB = 300-nA typ. |
| SID315B | I _{DAC2CRT3} | Output current of IDAC2 (7 bits) in high range | 270 | | 365 | μA | LSB = 2.4-μA typ. |
| SID315C | I _{DAC2CRT12} | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | | 11.4 | μA | LSB = 37.5-nA typ. 2X output stage |
| SID315D | I _{DAC2CRT22} | Output current of IDAC2(7 bits) in medium range, 2X mode | 67 | | 91 | μA | LSB = 300-nA typ. 2X output stage |
| SID315E | I _{DAC2CRT32} | Output current of IDAC2(7 bits) in high range, 2X mode. V _{DDA} > 2V | 540 | | 730 | μA | LSB = 2.4-μA typ. 2X output stage |
| SID315F | I _{DAC3CRT13} | Output current of IDAC in 8-bit mode in low range | 8 | | 11.4 | μA | LSB = 37.5-nA typ. |

Table 23. CapSense Sigma-Delta (CSD) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|---------------------------|---|-----|-----|-----|------|--|
| SID315G | I _{DAC3CRT23} | Output current of IDAC in 8-bit mode in medium range | 67 | | 91 | μA | LSB = 300-nA typ. |
| SID315H | I _{DAC3CRT33} | Output current of IDAC in 8-bit mode in high range. V _{DDA} > 2V | 540 | | 730 | μA | LSB = 2.4-μA typ. |
| SID320 | I _{DACOFFSET} | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink |
| SID321 | I _{DACGAIN} | Full-scale error less offset | – | – | ±15 | % | LSB = 2.4-μA typ. |
| SID322 | I _{DACMISMATCH1} | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5-nA typ. |
| SID322A | I _{DACMISMATCH2} | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 6 | LSB | LSB = 300-nA typ. |
| SID322B | I _{DACMISMATCH3} | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 5.8 | LSB | LSB = 2.4-μA typ. |
| SID323 | I _{DACSET8} | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load. |
| SID324 | I _{DACSET7} | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load. |
| SID325 | CMOD | External modulator capacitor. | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap. |

Table 24. CSD ADC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---------------------------------|----------------|-----------------------------------|-----|-----|-----|------|--|
| CSDv2 ADC Specifications | | | | | | | |
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SID95 | A_CHNLS_S | Number of channels - single ended | – | – | – | 16 | – |
| SIDA97 | A-MONO | Monotonicity | – | – | Yes | – | V _{REF} mode |
| SIDA98 | A_GAINERR_VREF | Gain error | – | 0.6 | – | % | Reference Source: SRSS (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA98A | A_GAINERR_VDDA | Gain error | – | 0.2 | – | % | Reference Source: SRSS (V _{REF} = 1.20 V, V _{DDA} < 2.2V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA99 | A_OFFSET_VREF | Input offset voltage | – | 0.5 | – | LSb | After ADC calibration, Ref. Src = SRSS, (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |
| SIDA99A | A_OFFSET_VDDA | Input offset voltage | – | 0.5 | – | LSb | After ADC calibration, Ref. Src = SRSS, (V _{REF} = 1.20 V, V _{DDA} < 2.2 V), (V _{REF} = 1.6 V, 2.2 V < V _{DDA} < 2.7 V), (V _{REF} = 2.13 V, V _{DDA} > 2.7 V) |

Table 24. CSD ADC Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------|---|-----------|-----|-----------|---------------|--|
| SIDA100 | A_ISAR_VREF | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA100A | A_ISAR_VDDA | Current consumption | – | 0.3 | – | mA | CSD ADC Block current |
| SIDA101 | A_VINS_VREF | Input voltage range - single ended | V_{SSA} | – | V_{REF} | V | ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA101A | A_VINS_VDDA | Input voltage range - single ended | V_{SSA} | – | V_{DDA} | V | ($V_{REF} = 1.20\text{ V}$, $V_{DDA} < 2.2\text{ V}$), ($V_{REF} = 1.6\text{ V}$, $2.2\text{ V} < V_{DDA} < 2.7\text{ V}$), ($V_{REF} = 2.13\text{ V}$, $V_{DDA} > 2.7\text{ V}$) |
| SIDA103 | A_INRES | Input charging resistance | – | 15 | – | k Ω | – |
| SIDA104 | A_INCAP | Input capacitance | – | 41 | – | pF | – |
| SIDA106 | A_PSRR | Power supply rejection ratio (DC) | – | 60 | – | dB | – |
| SIDA107 | A_TACQ | Sample acquisition time | – | 10 | – | μs | Measured with 50- Ω source impedance. 10 μs is default software driver acquisition time setting. Settling to within 0.05%. |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = $F_{hclk}/(2^{(N+2)})$. Clock frequency = 50 MHz. | – | 25 | – | μs | Does not include acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = $F_{hclk}/(2^{(N+2)})$. Clock frequency = 50 MHz. | – | 60 | – | μs | Does not include acquisition time. |
| SIDA109 | A_SND_VRE | Signal-to-noise and Distortion ratio (SINAD) | – | 57 | – | dB | Measured with 50- Ω source impedance |
| SIDA109A | A_SND_VDDA | Signal-to-noise and Distortion ratio (SINAD) | – | 52 | – | dB | Measured with 50- Ω source impedance |
| SIDA111 | A_INL_VREF | Integral Non Linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50- Ω source impedance |
| SIDA111A | A_INL_VDDA | Integral Non Linearity. 11.6 ksps | – | – | 2 | LSB | Measured with 50- Ω source impedance |
| SIDA112 | A_DNL_VREF | Differential Non Linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50- Ω source impedance |
| SIDA112A | A_DNL_VDDA | Differential Non Linearity. 11.6 ksps | – | – | 1 | LSB | Measured with 50- Ω source impedance |

Digital Peripherals
Table 25. Timer/Counter/PWM (TCPWM) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--------------|----------------|--|-------------|-----|-----|---------------|--|
| SID.TCPWM.1 | I_{TCPWM1} | Block current consumption at 8 MHz | – | – | 70 | μA | All modes (TCPWM) |
| SID.TCPWM.2 | I_{TCPWM2} | Block current consumption at 24 MHz | – | – | 180 | μA | All modes (TCPWM) |
| SID.TCPWM.2A | I_{TCPWM3} | Block current consumption at 50 MHz | – | – | 270 | μA | All modes (TCPWM) |
| SID.TCPWM.2B | I_{TCPWM4} | Block current consumption at 100 MHz | – | – | 540 | μA | All modes (TCPWM) |
| SID.TCPWM.3 | $TCPWM_{FREQ}$ | Operating frequency | – | – | 100 | MHz | $F_c \text{ max} = F_{cpu}$ Maximum = 100 MHz |
| SID.TCPWM.4 | $TPWM_{ENEXT}$ | Input Trigger Pulse Width for all Trigger Events | $2 / F_c$ | – | – | ns | Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. F_c is counter operating frequency. |
| SID.TCPWM.5 | $TPWM_{EXT}$ | Output Trigger Pulse widths | $1.5 / F_c$ | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs |
| SID.TCPWM.5A | TC_{RES} | Resolution of Counter | $1 / F_c$ | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWM_{RES} | PWM Resolution | $1 / F_c$ | – | – | ns | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | Q_{RES} | Quadrature inputs resolution | $2 / F_c$ | – | – | ns | Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar. |

Table 26. Serial Communication Block (SCB) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-------------|--|-----|-----|-----|---------------|----------------------|
| Fixed I²C DC Specifications | | | | | | | |
| SID149 | I_{I2C1} | Block current consumption at 100 kHz | – | – | 30 | μA | – |
| SID150 | I_{I2C2} | Block current consumption at 400 kHz | – | – | 80 | μA | – |
| SID151 | I_{I2C3} | Block current consumption at 1 Mbps | – | – | 180 | μA | – |
| SID152 | I_{I2C4} | I2C enabled in Deep Sleep mode | – | – | 1.7 | μA | At 60 °C |
| Fixed I²C AC Specifications | | | | | | | |
| SID153 | F_{I2C1} | Bit Rate | – | – | 1 | Mbps | – |
| Fixed UART DC Specifications | | | | | | | |
| SID160 | I_{UART1} | Block current consumption at 100 kbps | – | – | 30 | μA | – |
| SID161 | I_{UART2} | Block current consumption at 1000 kbps | – | – | 180 | μA | – |
| Fixed UART AC Specifications | | | | | | | |
| SID162A | F_{UART1} | Bit Rate | – | – | 3 | Mbps | ULP Mode |
| SID162B | F_{UART2} | | – | – | 8 | | LP Mode |
| Fixed SPI DC Specifications | | | | | | | |
| SID163 | I_{SPI1} | Block current consumption at 1Mbps | – | – | 220 | μA | – |

Table 26. Serial Communication Block (SCB) Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|---------------------------------|--|-----|-----|--|------|--|
| SID164 | I _{SPI2} | Block current consumption at 4 Mbps | – | – | 340 | μA | – |
| SID165 | I _{SPI3} | Block current consumption at 8 Mbps | – | – | 360 | μA | – |
| SID165A | I _{SP14} | Block current consumption at 25 Mbps | – | – | 800 | μA | – |
| Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID166 | F _{SPI} | SPI Operating Frequency Master and Externally Clocked Slave | – | – | 25 | MHz | 14-MHz max for ULP (0.9 V) mode |
| SID166A | F _{SPI_IC} | SPI Slave Internally Clocked | – | – | 15 | MHz | 5-MHz max for ULP (0.9 V) mode |
| SID166B | F _{SPI_EXT} | SPI Operating Frequency Master (F _{SCB} is SPI Clock) | – | – | F _{SCB} /4 | MHz | F _{SCB} max is 100 MHz in LP mode, 25 MHz max in ULP mode |
| Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID167 | T _{DMO} | MOSI Valid after SClk driving edge | – | – | 12 | ns | 20-ns max for ULP (0.9 V) mode |
| SID168 | T _{DSI} | MISO Valid before SClk capturing edge | 5 | – | – | ns | Full clock, late MISO sampling |
| SID169 | T _{HMO} | MOSI data hold time | 0 | – | – | ns | Referred to Slave capturing edge |
| SID169A | T _{SSELMCK1} | SSEL Valid to first SCK Valid edge | 18 | – | – | ns | Referred to Master clock edge |
| SID169B | T _{SSELMCK2} | SSEL Hold after last SCK Valid edge | 18 | – | – | ns | Referred to Master clock edge |
| Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise. | | | | | | | |
| SID170 | T _{DMI} | MOSI Valid before SClk Capturing edge | 5 | – | – | ns | – |
| SID171A | T _{D_{SO}_EXT} | MISO Valid after SClk driving edge in Ext. Clk. mode | – | – | 20 | ns | 35-ns max. for ULP (0.9 V) mode |
| SID171 | T _{D_{SO}} | MISO Valid after SClk driving edge in Internally Clk. Mode | – | – | T _{D_{SO}_EXT} + 3 * T _{Scb} | ns | T _{scb} is Serial Comm. Block clock period. |
| SID171B | T _{D_{SO}} | MISO Valid after SClk driving edge in Internally Clk. Mode with Median filter enabled. | – | – | T _{D_{SO}_EXT} + 4 * T _{Scb} | ns | T _{scb} is Serial Comm. Block clock period. |
| SID172 | T _{H_{SO}} | Previous MISO data hold time | 5 | – | – | ns | – |
| SID172A | T _{SSEL_SCK1} | SSEL Valid to first SCK Valid edge | 65 | – | – | ns | – |
| SID172B | T _{SSEL_SCK2} | SSEL Hold after Last SCK Valid edge | 65 | – | – | ns | – |

LCD Specifications
Table 27. LCD Direct Drive DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------------------------|--|-----|-----|------|------|---------------------------------------|
| SID154 | I _{LCDLOW} | Operating current in low-power mode | – | 5 | – | μA | 16 × 4 small segment display at 50 Hz |
| SID155 | C _{LCD_{CAP}} | LCD capacitance per segment/common driver | – | 500 | 5000 | pF | – |
| SID156 | LCD _{OFFSET} | Long-term segment offset | – | 20 | – | mV | – |
| SID157 | I _{LCDOP1} | PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C. | – | 0.6 | – | mA | 32 × 4 segments 50 Hz |
| SID158 | I _{LCDOP2} | PWM Mode current. 3.3-V bias. 8-MHz IMO. 25 °C. | – | 0.5 | – | mA | 32 × 4 segments 50 Hz |

Table 28. LCD Direct Drive AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------------|----------------|-----|-----|-----|------|----------------------|
| SID159 | F _{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | – |

Memory

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and 1.71 V to 3.6 V, except where noted.

Flash

Table 29. Flash DC Specifications^[6]

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------------|---------------------------|-----|-----|-----|------|----------------------|
| SID173A | I _{PE} | Erase and program current | – | – | 6 | mA | – |

Table 30. Flash AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------------------|---|-------|-----|-----|---------|----------------------|
| SID174 | T _{ROWWRITE} | Row write time (erase & program) | – | – | 16 | ms | Row = 512 bytes |
| SID175 | T _{ROWERASE} | Row erase time | – | – | 11 | ms | – |
| SID176 | T _{ROWPROGRAM} | Row program time after erase | – | – | 5 | ms | – |
| SID178 | T _{BULKERASE} | Bulk erase time (1024 KB) | – | – | 11 | ms | – |
| SID179 | T _{SECTORERASE} | Sector erase time (256 KB) | – | – | 11 | ms | 512 rows per sector |
| SID178S | T _{SSERIAE} | Subsector erase time | – | – | 11 | ms | 8 rows per subsector |
| SID179S | T _{SSWRITE} | Subsector write time; 1 erase plus 8 program times | – | – | 51 | ms | – |
| SID180S | T _{SWRITE} | Sector write time; 1 erase plus 512 program times | – | – | 2.6 | seconds | – |
| SID180 | T _{DEVPROG} | Total device write time | – | – | 15 | seconds | – |
| SID181 | F _{END} | Flash Endurance | 100 k | – | – | cycles | – |
| SID182 | F _{RET1} | Flash Retention. T _A ≤ 25 °C, 100 k P/E cycles | 10 | – | – | years | – |
| SID182A | F _{RET2} | Flash Retention. T _A ≤ 85 °C, 10 k P/E cycles | 10 | – | – | years | – |
| SID182B | F _{RET3} | Flash Retention. T _A ≤ 55 °C, 20 k P/E cycles | 20 | – | – | years | – |
| SID256 | T _{WS100} | Number of Wait states at 100 MHz | 3 | – | – | – | – |
| SID257 | T _{WS50} | Number of Wait states at 50 MHz | 2 | – | – | – | – |

Note

6. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Power-on-Reset

Table 31. Power-On-Reset with Brown-out DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|------------------------|--|------|-----|-----|-------|--|
| Precise POR (PPOR) Specifications | | | | | | | |
| SID190 | V _{FALLPPOR} | BOD trip voltage in Active and Sleep modes. V _{DDD} . | 1.54 | – | – | V | BOD Reset guaranteed for levels below 1.54 V |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep. V _{DDD} | 1.54 | – | – | V | – |
| SID192A | V _{DDRAMP} | Maximum power supply ramp rate (any supply) | – | – | 100 | mV/μs | Active mode |

Table 32. POR with Brown-out AC Specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------------------|---|-----|-----|-----|-------|--------------------------|
| SID194A | V _{DDRAMP_DS} | Maximum power supply ramp rate (any supply) in Deep Sleep | – | – | 10 | mV/μs | BOD operation guaranteed |

Voltage Monitors

Table 33. Voltage Monitors DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|---------------------|---------------|------|------|------|------|----------------------|
| SID195R | V _{HVD0} | | 1.18 | 1.23 | 1.27 | V | – |
| SID195 | V _{HVDI1} | | 1.38 | 1.43 | 1.47 | V | – |
| SID196 | V _{HVDI2} | | 1.57 | 1.63 | 1.68 | V | – |
| SID197 | V _{HVDI3} | | 1.76 | 1.83 | 1.89 | V | – |
| SID198 | V _{HVDI4} | | 1.95 | 2.03 | 2.1 | V | – |
| SID199 | V _{HVDI5} | | 2.05 | 2.13 | 2.2 | V | – |
| SID200 | V _{HVDI6} | | 2.15 | 2.23 | 2.3 | V | – |
| SID201 | V _{HVDI7} | | 2.24 | 2.33 | 2.41 | V | – |
| SID202 | V _{HVDI8} | | 2.34 | 2.43 | 2.51 | V | – |
| SID203 | V _{HVDI9} | | 2.44 | 2.53 | 2.61 | V | – |
| SID204 | V _{HVDI10} | | 2.53 | 2.63 | 2.72 | V | – |
| SID205 | V _{HVDI11} | | 2.63 | 2.73 | 2.82 | V | – |
| SID206 | V _{HVDI12} | | 2.73 | 2.83 | 2.92 | V | – |
| SID207 | V _{HVDI13} | | 2.82 | 2.93 | 3.03 | V | – |
| SID208 | V _{HVDI14} | | 2.92 | 3.03 | 3.13 | V | – |
| SID209 | V _{HVDI15} | | 3.02 | 3.13 | 3.23 | V | – |
| SID211 | LVI_IDD | Block current | – | 5 | 15 | μA | – |

Table 34. Voltage Monitors AC Specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------------|---------------------------|-----|-----|-----|------|----------------------|
| SID212 | T _{MONTRIP} | Voltage monitor trip time | – | – | 170 | ns | – |

SWD and Trace Interface
Table 35. SWD and Trace Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|--------------|---|------------|-----|-----------|------|---|
| SID214 | F_SWCLK2 | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 25 | MHz | LP mode. $V_{CCD} = 1.1\text{ V}$ |
| SID214L | F_SWCLK2L | $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ | – | – | 12 | MHz | ULP mode. $V_{CCD} = 0.9\text{ V}$. |
| SID215 | T_SWDI_SETUP | $T = 1/f\text{ SWCLK}$ | $0.25 * T$ | – | – | ns | – |
| SID216 | T_SWDI_HOLD | $T = 1/f\text{ SWCLK}$ | $0.25 * T$ | – | – | ns | – |
| SID217 | T_SWDO_VALID | $T = 1/f\text{ SWCLK}$ | – | – | $0.5 * T$ | ns | – |
| SID217A | T_SWDO_HOLD | $T = 1/f\text{ SWCLK}$ | 1 | – | – | ns | – |
| SID214T | F_TRCLK_LP1 | With Trace Data setup/hold times of 2/1 ns respectively | – | – | 75 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$ |
| SID215T | F_TRCLK_LP2 | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 70 | MHz | LP Mode. $V_{DD} = 1.1\text{ V}$ |
| SID216T | F_TRCLK_ULP | With Trace Data setup/hold times of 3/2 ns respectively | – | – | 25 | MHz | ULP Mode. $V_{DD} = 0.9\text{ V}$ |

Internal Main Oscillator
Table 36. IMO DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------------|--------------------------------|-----|-----|-----|------|----------------------|
| SID218 | I _{IMO1} | IMO operating current at 8 MHz | – | 9 | 15 | μA | – |

Table 37. IMO AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|----------------------|---------------------------------------|-----|------|-----|------|----------------------|
| SID223 | F _{IMOTOL1} | Frequency variation centered on 8 MHz | – | – | ±2 | % | – |
| SID227 | T _{JITR} | Cycle-to-Cycle and Period jitter | – | ±250 | – | ps | – |

Internal Low-Speed Oscillator
Table 38. ILO DC Specification

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------------|---------------------------------|-----|-----|-----|------|----------------------|
| SID231 | I _{ILO2} | ILO operating current at 32 kHz | – | 0.3 | 0.7 | μA | – |

Table 39. ILO AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------------------|--------------------------|------|-----|------|------|--|
| SID234 | T _{STARTILO1} | ILO startup time | – | – | 7 | μs | Startup time to 95% of final frequency |
| SID236 | T _{LIODUTY} | ILO Duty cycle | 45 | 50 | 55 | % | – |
| SID237 | F _{ILOTRIM1} | 32-kHz trimmed frequency | 28.8 | 32 | 36.1 | kHz | – |

Crystal Oscillator

Table 40. ECO Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------------------------------|---------------------|--|-----|--------|------|------|--------------------------------|
| MHz ECO DC Specifications | | | | | | | |
| SID316 | I _{DD_MHz} | Block operating current with Cload up to 18 pF | – | 800 | 1600 | μA | Max = 33 MHz, Type = 16 MHz |
| MHz ECO AC Specifications | | | | | | | |
| SID317 | F_MHz | Crystal frequency range | 4 | – | 35 | MHz | – |
| kHz ECO DC Specification | | | | | | | |
| SID318 | I _{DD_kHz} | Block operating current with 32-kHz crystal | – | 0.38 | 1 | μA | – |
| SID321E | ESR32K | Equivalent Series Resistance | – | 80 | – | kΩ | – |
| SID322E | PD32K | Drive level | – | – | 1 | μW | – |
| kHz ECO AC Specification | | | | | | | |
| SID319 | F_kHz | 32-kHz trimmed frequency | – | 32.768 | – | kHz | – |
| SID320 | Ton_kHz | Startup time | – | – | 500 | ms | – |
| SID320E | F _{TOL32K} | Frequency tolerance | – | 50 | 250 | ppm | – |

External Clock

Table 41. External Clock Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------------------|---|-----|-----|-----|------|----------------------|
| SID305 | EXTCLK _{FREQ} | External Clock input Frequency | 0 | – | 100 | MHz | – |
| SID306 | EXTCLK _{DUTY} | Duty cycle; Measured at V _{DD/2} | 45 | – | 55 | % | – |

PLL

Table 42. PLL Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------|---------------------------------|-----|------|-----|------|--------------------------|
| SID305P | PLL_LOCK | Time to achieve PLL Lock | – | 16 | 35 | μs | – |
| SID306P | PLL_OUT | Output frequency from PLL Block | – | – | 150 | MHz | – |
| SID307P | PLL_IDD | PLL Current | – | 0.55 | 1.1 | mA | Typ at 100 MHz out. |
| SID308P | PLL_JTR | Period Jitter | – | – | 150 | ps | 100-MHz output frequency |

Clock Source Switching Time

Table 43. Clock Source Switching Time Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|------------------------|--|-----|-----|-----------------|---------|----------------------|
| SID262 | TCLK _{SWITCH} | Clock switching from clk1 to clk2 in clock periods | – | – | 4 clk1 + 3 clk2 | periods | – |

FLL
Table 44. Frequency Locked Loop (FLL) Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|---------------|--|-------|-----|--------|-------------------|---|
| SID450 | FLL_RANGE | Input frequency range. | 0.001 | – | 100 | MHz | Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input. |
| SID451 | FLL_OUT_DIV2 | Output frequency range. $V_{CCD} = 1.1\text{ V}$ | 24.00 | – | 100.00 | MHz | Output range of FLL divided-by-2 output |
| SID451A | FLL_OUT_DIV2 | Output frequency range. $V_{CCD} = 0.9\text{ V}$ | 24.00 | – | 50.00 | MHz | Output range of FLL divided-by-2 output |
| SID452 | FLL_DUTY_DIV2 | Divided-by-2 output; High or Low | 47.00 | – | 53.00 | % | – |
| SID454 | FLL_WAKEUP | Time from stable input clock to 1% of final value on deep sleep wakeup | – | – | 7.50 | μs | With IMO input, less than 10 °C change in temperature while in Deep Sleep, and $F_{out} \geq 50\text{ MHz}$. |
| SID455 | FLL_JITTER | Period jitter (1 sigma at 100 MHz) | – | – | 35.00 | ps | 50 ps at 48 MHz, 35 ps at 100 MHz |
| SID456 | FLL_CURRENT | CCO + Logic current | – | – | 5.50 | $\mu\text{A/MHz}$ | – |

UDB
Table 45. UDB AC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-----------------------------|--|-----|-----|-----|------|----------------------|
| Data Path Performance | | | | | | | |
| SID249 | $F_{\text{MAX-TIMER}}$ | Max frequency of 16-bit timer in a UDB pair | – | – | 100 | MHz | – |
| SID250 | $F_{\text{MAX-ADDER}}$ | Max frequency of 16-bit adder in a UDB pair | – | – | 100 | MHz | – |
| SID251 | $F_{\text{MAX_CRC}}$ | Max frequency of 16-bit CRC/PRS in a UDB pair | – | – | 100 | MHz | – |
| PLD Performance in UDB | | | | | | | |
| SID252 | $F_{\text{MAX_PLD}}$ | Max frequency of 2-pass PLD function in a UDB pair | – | – | 100 | MHz | – |
| Clock to Output Performance | | | | | | | |
| SID253 | $T_{\text{CLK_OUT_UDB1}}$ | Prop. delay for clock in to data out | – | 5 | – | ns | – |
| UDB Port Adaptor Specifications | | | | | | | |
| <i>Conditions: 10-pF load, 3-V V_{DDIO} and V_{DDD}</i> | | | | | | | |
| SID263 | T_{LCLKDO} | LCLK to Output delay | – | – | 11 | ns | – |
| SID264 | T_{DINLCLK} | Input setup time to LCLK rising edge | – | – | 7 | ns | – |
| SID265 | $T_{\text{DINLCLKHLD}}$ | Input hold time from LCLK rising edge | 5 | – | – | ns | – |
| SID266 | T_{LCLKHIZ} | LCLK to Output tristated | – | – | 28 | ns | – |
| SID267 | T_{FLCLK} | LCLK frequency | – | – | 33 | MHz | – |
| SID268 | T_{LCLKDUTY} | LCLK duty cycle (percentage high) | 40% | – | 60% | % | – |

Note

7. The undivided output of the FLL must be a minimum of 2.5X the input frequency.

USB

Table 46. USB Specifications (USB requires LP Mode 1.1-V Internal Supply)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---------------------------------|-----------------|---|-------|-----|------|------|---|
| USB Block Specifications | | | | | | | |
| SID322U | Vusb_3.3 | Device supply for USB operation | 3.15 | – | 3.6 | V | USB Configured |
| SID323U | Vusb_3 | Device supply for USB operation (functional operation only) | 2.85 | – | 3.6 | V | USB Configured |
| SID325U | Iusb_config | Device supply current in Active mode | – | 8 | – | mA | V _{DDD} = 3.3 V |
| SID328 | Isub_suspend | Device supply current in Sleep mode | – | 0.5 | – | mA | V _{DDD} = 3.3 V, Device connected |
| SID329 | Isub_suspend | Device supply current in Sleep mode | – | 0.3 | – | mA | V _{DDD} = 3.3 V, Device disconnected |
| SID330U | USB_Drive_Res | USB driver impedance | 28 | – | 44 | Ω | Series resistors are on chip |
| SID331U | USB_Pulldown | USB pull-down resistors in Host mode | 14.25 | – | 24.8 | kΩ | – |
| SID332U | USB_Pullup_Idle | Idle mode range | 900 | – | 1575 | Ω | Bus idle |
| SID333U | USB_Pullup | Active mode | 1425 | – | 3090 | Ω | Upstream device transmitting |

QSPI

Table 47. QSPI Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|---------------|---|---------------------------|-----|------|------|--|
| SMIF QSPI Specifications. All specs with 15-pF load. | | | | | | | |
| SID390Q | Fsmifclock | SMIF QSPI output clock frequency | – | – | 80 | MHz | LP mode (1.1 V) |
| SID390QU | Fsmifclocku | SMIF QSPI output clock frequency | – | – | 50 | MHz | ULP mode (0.9 V). Guaranteed by Char. |
| SID397Q | Idd_qspi | Block current in LP mode (1.1 V) | – | – | 1900 | μA | LP mode (1.1 V) |
| SID398Q | Idd_qspi_u | Block current in ULP mode (0.9 V) | – | – | 590 | μA | ULP mode (0.9 V) |
| SID391Q | Tsetup | Input data set-up time with respect to clock capturing edge | 4.5 | – | – | ns | – |
| SID392Q | Tdatahold | Input data hold time with respect to clock capturing edge | 0 | – | – | ns | – |
| SID393Q | Tdataoutvalid | Output data valid time with respect to clock falling edge | – | – | 3.7 | ns | 7.5-ns max for ULP mode (0.9 V) |
| SID394Q | Tholdtime | Output data hold time with respect to clock rising edge | 3 | – | – | ns | – |
| SID395Q | Tseloutvalid | Output Select valid time with respect to clock rising edge | – | – | 7.5 | ns | 15-ns max for ULP mode (0.9 V) |
| SID396Q | Tselouthold | Output Select hold time with respect to clock rising edge | 0.5*T _{sc} lk | – | – | ns | T _{sc} lk = Fsmifclk cycle time |

Audio Subsystem

Table 48. Audio Subsystem Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|--------------|--|-------|-----------|--------|------|---------------------------------------|
| PDM Specifications | | | | | | | |
| SID400P | PDM_IDD1 | PDM Active current, Stereo operation, 1-MHz clock | – | 175 | – | µA | 16-bit audio at 16 ksps |
| SID401 | PDM_IDD2 | PDM Active current, Stereo operation, 3-MHz clock | – | 600 | – | µA | 24-bit audio at 48 ksps |
| SID402 | PDM_JITTER | RMS Jitter in PDM clock | –200 | – | 200 | ps | – |
| SID403 | PDM_CLK | PDM Clock speed | 0.384 | – | 3.072 | MHz | – |
| SID403A | PDM_BLK_CLK | PDM Block input clock | 1.024 | – | 49.152 | MHz | – |
| SID403B | PDM_SETUP | Data input set-up time to PDM_CLK edge | 10 | – | – | ns | – |
| SID403C | PDM_HOLD | Data input hold time to PDM_CLK edge | 10 | – | – | ns | – |
| SID404 | PDM_OUT | Audio sample rate | 8 | – | 48 | ksps | – |
| SID405 | PDM_WL | Word Length | 16 | – | 24 | bits | – |
| SID406 | PDM_SNR | Signal-to-Noise Ratio (A-weighted) | – | 100 | – | dB | PDM input, 20 Hz to 20 kHz BW |
| SID407 | PDM_DR | Dynamic Range (A-weighted) | – | 100 | – | dB | 20 Hz to 20 kHz BW, –60 dB FS |
| SID408 | PDM_FR | Frequency Response | –0.2 | – | 0.2 | dB | DC to 0.45. DC Blocking filter off. |
| SID409 | PDM_SB | Stop Band | – | 0.56 6 | – | f | – |
| SID410 | PDM_SBA | Stop Band Attenuation | – | 60 | – | dB | – |
| SID411 | PDM_GAIN | Adjustable Gain | –12 | – | 10.5 | dB | PDM to PCM, 1.5 dB/step |
| SID412 | PDM_ST | Startup time | – | 48 | – | | WS (Word Select) cycles |
| I2S Specifications. The same for LP and ULP modes unless stated otherwise. | | | | | | | |
| SID413 | I2S_WORD | Length of I2S Word | 8 | – | 32 | bits | – |
| SID414 | I2S_WS | Word Clock frequency in LP mode | – | – | 192 | kHz | 12.288-MHz bit clock with 32-bit word |
| SID414M | I2S_WS_U | Word Clock frequency in ULP mode | – | – | 48 | kHz | 3.072-MHz bit clock with 32-bit word |
| SID414A | I2S_WS_TDM | Word Clock frequency in TDM mode for LP | – | – | 48 | kHz | Eight 32-bit channels |
| SID414X | I2S_WS_TDM_U | Word Clock frequency in TDM mode for ULP | – | – | 12 | kHz | Eight 32-bit channels |
| I2S Slave Mode | | | | | | | |
| SID430 | TS_WS | WS Setup Time to the Following Rising Edge of SCK for LP Mode | 5 | – | – | ns | – |
| SID430U | TS_WS | WS Setup Time to the Following Rising Edge of SCK for ULP Mode | 11 | – | – | ns | – |

Table 48. Audio Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|------------------------|-------------|--|-----------------------|-----|----------------|------|--|
| SID430A | TH_WS | WS Hold Time to the Following Edge of SCK | TMCLK_SOC + 5 | – | – | ns | – |
| SID432 | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for LP mode | – (TMCLK_SOC + 25) | – | TMCLK_SOC + 25 | ns | Associated clock edge depends on selected polarity |
| SID432U | TD_SDO | Delay Time of TX_SDO Transition from Edge of TX_SCK for ULP mode | – (TMCLK_SOC + 70) | – | TMCLK_SOC + 70 | ns | Associated clock edge depends on selected polarity |
| SID433 | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in Lp Mode | 5 | – | – | ns | – |
| SID433U | TS_SDI | RX_SDI Setup Time to the Following Edge of RX_SCK in ULP mode | 11 | – | – | ns | – |
| SID434 | TH_SDI | RX_SDI Hold Time to the Rising Edge of RX_SCK | TMCLK_SOC + 5 | – | – | ns | – |
| SID435 | TSCKCY | TX/RX_SCK Bit Clock Duty Cycle | 45 | – | 55 | % | – |
| I2S Master Mode | | | | | | | |
| SID437 | TD_WS | WS Transition Delay from Falling Edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID437U | TD_WS_U | WS Transition Delay from Falling Edge of SCK in ULP mode | –10 | – | 40 | ns | – |
| SID438 | TD_SDO | SDO Transition Delay from Falling Edge of SCK in LP mode | –10 | – | 20 | ns | – |
| SID438U | TD_SDO | SDO Transition Delay from Falling Edge of SCK in ULP mode | –10 | – | 40 | ns | – |
| SID439 | TS_SDI | SDI Setup Time to the Associated Edge of SCK | 5 | – | – | ns | Associated clock edge depends on selected polarity |
| SID440 | TH_SDI | SDI Hold Time to the Associated Edge of SCK | TMCLK_SOC + 5 | – | – | ns | T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity. |
| SID443 | TSCKCY | SCK Bit Clock Duty Cycle | 45 | – | 55 | % | – |
| SID445 | FMCLK_SOC | MCLK_SOC Frequency in LP mode | 1.024 | – | 98.304 | MHz | FMCLK_SOC = 8 * Bit-clock |
| SID445U | FMCLK_SOC_U | MCLK_SOC Frequency in ULP mode | 1.024 | – | 24.576 | MHz | FMCLK_SOC_U = 8 * Bit-clock |
| SID446 | TMCLKCY | MCLK_SOC Duty Cycle | 45 | – | 55 | % | – |
| SID447 | TJITTER | MCLK_SOC Input Jitter | –100 | – | 100 | ps | – |

Smart I/O

Table 49. Smart I/O Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-----------|--------------------------|-----|-----|-----|------|----------------------|
| SID420 | SMIO_BYP | Smart I/O Bypass delay | – | – | 2 | ns | – |
| SID421 | SMIO_LUT | Smart I/O LUT prop delay | – | 8 | – | ns | – |

Precision ILO (PILO)

Table 50. PILO Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|----------|-------------------|---|------|-------|-----|------|-------------------------------|
| SID 430R | I _{PILO} | Operating current | – | 1.2 | 4 | μA | – |
| SID431 | F _{PILO} | PILO nominal frequency | – | 32768 | – | Hz | T = 25 °C with 20-ppm crystal |
| SID432R | ACC_PILO | PILO accuracy with periodic calibration | –500 | – | 500 | ppm | – |

BLE

Table 51. BLE Subsystem Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|-----------|---|-----|-----|-----|------|--|
| RF Receiver Specifications (1 Mbps) | | | | | | | |
| SID317R | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –95 | – | dBm | Across RF Operating Frequency Range |
| SID317RR | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –93 | – | dBm | 255-byte packet length, across Frequency Range |
| SID318R | RXS,DIRTY | RX Sensitivity with Dirty Transmitter | – | –92 | – | dBm | RF-PHY Specification (RCV-LE/CA/01/C) |
| SID319R | PRXMAX | Maximum received signal strength at < 0.1% PER | – | 0 | – | dBm | RF-PHY Specification (RCV-LE/CA/06/C) |
| SID320R | CI1 | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX | – | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID321R | CI2 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 1 MHz | – | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID322R | CI3 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz | – | –26 | –17 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID323R | CI4 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 3 MHz | – | –33 | –27 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID324R | CI5 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE) | – | –20 | –9 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID325R | CI6 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 1 MHz) | – | –28 | –15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| RF Receiver Specifications (2 Mbps) | | | | | | | |
| SID326 | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –92 | – | dBm | Across RF Operating Frequency Range |

Table 51. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-----------|--|-----|-----|-----|------|--|
| SID326R | RXS,IDLE | RX Sensitivity with Ideal Transmitter | – | –90 | – | dBm | 255-byte packet length, across Frequency Range |
| SID327 | RXS,DIRTY | RX Sensitivity with Dirty Transmitter | – | –89 | – | dBm | RF-PHY Specification (RCV-LE/CA/01/C) |
| SID328R | PRXMAX | Maximum received signal strength at < 0.1% PER | – | 0 | – | dBm | RF-PHY Specification (RCV-LE/CA/06/C) |
| SID329R | CI1 | Co-channel interference, Wanted Signal at –67 dBm and Interferer at FRX | – | 9 | 21 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID330 | CI2 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 2 MHz | – | 3 | 15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID331 | CI3 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at FRX ± 4 MHz | – | –26 | –17 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID332 | CI4 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at ≥ FRX ± 6 MHz | – | –33 | –27 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID333 | CI5 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE) | – | –20 | –9 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| SID334 | CI6 | Adjacent channel interference Wanted Signal at –67 dBm and Interferer at Image frequency (FIMAGE ± 2MHz) | – | –28 | –15 | dB | RF-PHY Specification (RCV-LE/CA/03/C) |
| RF Receiver Specification (1 & 2 Mbps) | | | | | | | |
| SID338 | OBB1 | Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F = 30–2000 MHz | –30 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID339 | OBB2 | Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F = 2003–2399 MHz | –35 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID340 | OBB3 | Out of Band Blocking, Wanted Signal at –67 dBm and Interferer at F= 2484–2997MHz | –35 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID341 | OBB4 | Out of Band Blocking Wanted Signal at –67 dBm and Interferer at F= 3000–12750 MHz | –30 | –27 | – | dBm | RF-PHY Specification (RCV-LE/CA/04/C) |
| SID342 | IMD | Intermodulation Performance Wanted Signal at –64 dBm and 1 Mbps BLE, 3rd, 4th and 5th offset channel | –50 | – | – | dBm | RF-PHY Specification (RCV-LE/CA/05/C) |
| SID343 | RXSE1 | Receiver Spurious emission 30 MHz to 1.0 GHz | – | – | –57 | dBm | 100-kHz measurement bandwidth ETSI EN300 328 V2.1.1 |
| SID344 | RXSE2 | Receiver Spurious emission 1.0 GHz to 12.75 GHz | – | – | –53 | dBm | 1-MHz measurement bandwidth ETSI EN300 328 V2.1.1 |

Table 51. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--------------------------------------|--------------|--|------|-----|-------|--------------------|--|
| RF Transmitter Specifications | | | – | – | – | – | |
| SID345 | TXP,ACC | RF Power Accuracy | –1 | – | 1 | dB | – |
| SID346 | TXP,RANGE | Frequency Accuracy | – | 24 | – | dB | –20 dBm to +4 dBm |
| SID347 | TXP,0dBm | Output Power, 0 dB Gain setting | – | 0 | – | dBm | – |
| SID348 | TXP,MAX | Output Power, Maximum Power Setting | – | 4 | – | dBm | – |
| SID349 | TXP,MIN | Output Power, Minimum Power Setting | – | –20 | – | dBm | – |
| SID350 | F2AVG | Average Frequency deviation for 10101010 pattern | 185 | – | – | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID350R | F2AVG_2M | Average Frequency deviation for 10101010 pattern for 2 Mbps | 370 | – | – | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID351 | F1AVG | Average Frequency deviation for 11110000 pattern | 225 | 250 | 275 | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID351R | F1AVG_2M | Average Frequency deviation for 11110000 pattern for 2 Mbps | 450 | 500 | 550 | kHz | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID352 | EO | Eye opening = $\Delta F2AVG/\Delta F1AVG$ | 0.8 | – | – | – | RF-PHY Specification (TRM-LE/CA/05/C) |
| SID353 | FTX,ACC | Frequency Accuracy | –150 | – | 150 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID354 | FTX,MAXDR | Maximum Frequency Drift | –50 | – | 50 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID355 | FTX,INITDR | Initial Frequency drift | –20 | – | 20 | kHz | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID356 | FTX,DR | Maximum Drift Rate | –20 | – | 20 | kHz/ 50 μ s | RF-PHY Specification (TRM-LE/CA/06/C) |
| SID357 | IBSE1 | In Band Spurious Emission at 2 MHz offset (1 Mbps) In Band Spurious Emission at 4 MHz offset (2 Mbps) | – | – | –20 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| SID358 | IBSE2 | In Band Spurious Emission at \geq 3 MHz offset (1 Mbps) In Band Spurious Emission at \geq 6 MHz offset (2 Mbps) | – | – | –30 | dBm | RF-PHY Specification (TRM-LE/CA/03/C) |
| SID359 | TXSE1 | Transmitter Spurious Emissions (Averaging), < 1.0 GHz | – | – | –55.5 | dBm | FCC-15.247 |
| SID360 | TXSE2 | Transmitter Spurious Emissions (Averaging), > 1.0 GHz | – | – | –41.5 | dBm | FCC-15.247 |
| RF Current Specification | | | | | | | |
| SID361 | IRX1_wb | Receive Current (1 Mbps) | – | 6.7 | – | mA | V _{DD_NS} = V _{DD} = 3.3 V current with buck |
| SID362 | ITX1_wb_0dBm | TX Current at 0 dBm setting (1 Mbps) | – | 5.7 | – | mA | V _{DD_NS} = V _{DD} = 3.3 V current with buck |
| SID363 | IRX1_nb | Receive Current (1 Mbps) | – | 11 | – | mA | V _{DD} current without buck |
| SID364 | ITX1_nb_0dBm | TX Current at 0-dBm setting (1 Mbps) | – | 10 | – | mA | V _{DD} current without buck |

Table 51. BLE Subsystem Specifications (continued)

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|--|---------------|--|------|------|------|------|---|
| SID365 | ITX1_nb_4dBm | TX Current at 4-dBm setting (1 Mbps) | – | 13 | – | mA | V _{DDD} current without buck |
| SID365R | ITX1_wb_4dBm | TX Current at 4-dBm setting (1 Mbps) | – | 8.5 | – | mA | V _{DD_NS} = V _{DDD} = 3.3 V current with buck |
| SID366 | ITX1_nb_20dBm | TX Current at –20-dBm setting (1 Mbps) | – | 7 | – | mA | V _{DDD} current without buck |
| SID367 | IRX2_wb | Receive Current (2 Mbps) | – | 7 | – | mA | V _{DD_NS} = V _{DDD} = 3.3 V current with buck |
| SID368 | ITX2_wb_0dBm | TX Current at 0-dBm setting (2 Mbps) | – | 5.7 | – | mA | V _{DD_NS} = V _{DDD} = 3.3 V current with buck |
| SID369 | IRX2_nb | Receive Current (2 Mbps) | – | 11.3 | – | mA | V _{DDD} current without buck |
| SID370 | ITX2_nb_0dBm | TX Current at 0-dBm setting (2 Mbps) | – | 10 | – | mA | V _{DDD} current without buck |
| SID371 | ITX2_nb_4dBm | TX Current at 4-dBm setting (2 Mbps) | – | 13 | – | mA | V _{DDD} current without buck |
| SID371R | ITX2_wb_4dBm | TX Current at 4-dBm setting (2 Mbps) | – | 8.5 | – | mA | V _{DD_NS} = V _{DDD} = 3.3 V current with buck |
| SID372 | ITX2_nb_20dBm | TX Current at –20-dBm setting (2 Mbps) | – | 7 | – | mA | V _{DDD} current without buck |
| General RF Specification | | | | | | | |
| SID373 | FREQ | RF operating frequency | 2400 | – | 2482 | MHz | – |
| SID374 | CHBW | Channel spacing | – | 2 | – | MHz | – |
| SID375 | DR1 | On-air Data Rate (1 Mbps) | – | 1000 | – | kbps | – |
| SID376 | DR2 | On-air Data Rate (2 Mbps) | – | 2000 | – | kbps | – |
| SID377 | TXSUP | Transmitter Startup time | – | 80 | 82 | μs | – |
| SID378 | RXSUP | Receiver Startup time | – | 80 | 82 | μs | – |
| RSSI Specification | | | | | | | |
| SID379 | RSSI,ACC | RSSI Accuracy | –4 | – | 4 | dB | –95 dBm to –20 dBm measurement range |
| SID380 | RSSI,RES | RSSI Resolution | – | 1 | – | dB | – |
| SID381 | RSSI,PER | RSSI Sample Period | – | 6 | – | μs | – |
| System-Level BLE Specifications | | | | | | | |
| SID433R | Adv_Pwr | 1.28s, 32 bytes, 0 dBm | – | 42 | – | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID434R | Conn_Pwr_300 | 300 ms, 0 byte, 0 dBm | – | 70 | – | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID435R | Conn_Pwr_1S | 1000 ms, 0 byte, 0 dBm | – | 30 | – | μW | 3.3 V, Buck, w/o Deep Sleep current |
| SID436R | Conn_Pwr_4S | 4000 ms, 0 byte, 0 dBm | – | 4 | – | μW | 3.3 V, Buck, w/o Deep Sleep current |

Table 52. ECO Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details / Conditions |
|---|-----------|------------------------------|-----|-----|-----|------|--|
| 16-MHz Crystal Oscillator | | | | | | | |
| SID382 | FXO1 | Crystal frequency | – | 16 | – | MHz | – |
| SID383 | ESR1 | Equivalent series resistance | – | 100 | 250 | Ω | – |
| SID384 | Txostart1 | Startup time | – | 400 | – | μs | Frequency Stable (16 MHz ±50 ppm) |
| SID385 | IXO1 | Operating current | – | 300 | – | μA | Includes crystal current, LDO and BG |
| 32-MHz Crystal Oscillator | | | | | | | |
| SID386 | FXO2 | Crystal frequency | – | 32 | – | MHz | – |
| SID387 | ESR2 | Equivalent series resistance | – | 50 | 100 | Ω | – |
| SID388 | Txostart2 | Startup time | – | 400 | – | μs | Frequency Stable (32 MHz ±50 ppm) |
| SID389 | IXO2 | Operating current | – | 350 | – | μA | Includes crystal current, LDO and BG |
| 16-MHz and 32-MHz Crystal Oscillator | | | | | | | |
| SID390 | FTOL | Frequency tolerance | –20 | – | 20 | ppm | After trimming, including aging and temp drift |
| SID391 | PD | Drive level | – | – | 100 | μW | – |

Ordering Information

Table 53 lists the CY8C63x6 and CY8C63x7 part numbers and features. All devices include a BLE radio, DC-DC converter, QSPI SMIF, ADC, DAC, 9 SCBs, 32 TCPWMs, 2 PDM, and I2S. See also the [product selector guide](#).

Table 53. BLE Series Part Numbers

| Family | MPN | CPU Speed (CM4) | CPU Speed (CM0+) | Single CPU/Dual CPU | ULP/LP | Flash (KB) | SRAM (KB) | No. of CTBMs | No. of UDBs | CapSense | CRYPTO | Secure Boot | USB | GPIOs | Package |
|--------|-------------------|-----------------|------------------|---------------------|--------|------------|-----------|--------------|-------------|----------|--------|-------------|-----|-------|--------------|
| 63 | CY8C6336LQI-BLF02 | 150 | – | Single | LP | 512 | 128 | 0 | 0 | No | No | No | No | 36 | 68-QFN |
| | CY8C6336LQI-BLF42 | 150 | – | Single | LP | 512 | 128 | 0 | 0 | Yes | Yes | No | No | 36 | 68-QFN |
| | CY8C6347LQI-BLD52 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | Yes | Yes | No | 36 | 68-QFN |
| | CY8C6336BZI-BLF03 | 150 | – | Single | LP | 512 | 128 | 0 | 0 | No | No | No | No | 78 | 116-BGA |
| | CY8C6316BZI-BLF03 | 50 | – | Single | ULP | 512 | 128 | 0 | 0 | No | No | No | No | 78 | 116-BGA |
| | CY8C6316BZI-BLF53 | 50 | – | Single | ULP | 512 | 128 | 1 | 12 | Yes | Yes | No | No | 78 | 116-BGA |
| | CY8C6337BZI-BLF13 | 150 | – | Single | LP | 1024 | 288 | 0 | 0 | Yes | No | No | No | 78 | 116-BGA |
| | CY8C6336BZI-BLD13 | 150 | 100 | Dual | LP | 512 | 128 | 0 | 0 | Yes | No | No | No | 78 | 116-BGA |
| | CY8C6347BZI-BLD43 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | Yes | Yes | No | 78 | 116-BGA |
| | CY8C6347BZI-BLD33 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | No | No | No | 78 | 116-BGA |
| | CY8C6347BZI-BLD53 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | Yes | Yes | No | 78 | 116-BGA |
| | CY8C6336BZI-BLF04 | 150 | – | Single | LP | 512 | 128 | 0 | 0 | No | No | No | Yes | 84 | 124-BGA |
| | CY8C6316BZI-BLF04 | 50 | – | Single | ULP | 512 | 128 | 0 | 0 | No | No | No | Yes | 84 | 124-BGA |
| | CY8C6316BZI-BLF54 | 50 | – | Single | ULP | 512 | 128 | 1 | 12 | Yes | Yes | No | Yes | 84 | 124-BGA |
| | CY8C6337BZI-BLF14 | 150 | – | Single | LP | 1024 | 288 | 0 | 0 | Yes | No | No | Yes | 84 | 124-BGA |
| | CY8C6336BZI-BLD14 | 150 | 100 | Dual | LP | 512 | 128 | 0 | 0 | Yes | No | No | Yes | 84 | 124-BGA |
| | CY8C6347BZI-BLD44 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | Yes | Yes | Yes | 84 | 124-BGA |
| | CY8C6347BZI-BLD34 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | No | No | Yes | 84 | 124-BGA |
| | CY8C6347BZI-BLD54 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | Yes | Yes | Yes | 84 | 124-BGA |
| | CY8C6347FMI-BLD13 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | No | No | No | 70 | 104-MCSP |
| | CY8C6347FMI-BLD43 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | Yes | Yes | No | 70 | 104-MCSP |
| | CY8C6347FMI-BLD33 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | No | No | No | 70 | 104-MCSP |
| | CY8C6347FMI-BLD53 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | Yes | Yes | No | 70 | 104-MCSP |
| | CY8C6347FMI-BUD13 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | No | No | Yes | 69 | 104-MCSP-USB |
| | CY8C6347FMI-BUD43 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 0 | 0 | Yes | Yes | Yes | Yes | 69 | 104-MCSP-USB |
| | CY8C6347FMI-BUD33 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | No | No | Yes | 69 | 104-MCSP-USB |
| | CY8C6347FMI-BUD53 | 150/50 | 100/25 | Dual | FLEX | 1024 | 288 | 1 | 12 | Yes | Yes | Yes | Yes | 69 | 104-MCSP-USB |

PSoC 6 MPN Decoder
CY XX 6 A B C DD E - FF G H I JJ K L

| Field | Description | Values | Meaning |
|-------|--------------------------|------------|-------------------|
| CY | Cypress | CY | Cypress |
| XX | Firmware | 8C | Standard |
| | | B0 | Secure Boot v1 |
| | | S0 | Std. Secure - AWS |
| 6 | Architecture | 6 | PSoC 6 |
| A | Line | 0 | Value |
| | | 1 | Programmable |
| | | 2 | Performance |
| | | 3 | Connectivity |
| | | 4 | Security |
| B | Speed | 2 | 100 MHz |
| | | 3 | 150 MHz |
| | | 4 | 150/50 MHz |
| C | Memory Size (Flash/SRAM) | 0-3 | RFU |
| | | 4 | 256K/128K |
| | | 5 | 512K/256K |
| | | 6 | 512K/128K |
| | | 7 | 1024K/288K |
| | | 8 | 1024K/512K |
| | | 9 | RFU |
| | | A | 2048K/1024K |
| DD | Package | AZ, AX | TQFP |
| | | LQ | QFN |
| | | BZ | BGA |
| | | FM | M-CSP |
| | | FN, FD, FT | WLCSP |

| Field | Description | Values | Meaning |
|-------|-------------------------------|--------|----------------------------|
| E | Temperature Range | C | Consumer |
| | | I | Industrial |
| | | Q | Extended Industrial |
| FF | Feature Code | S2-S6 | Cypress internal |
| | | BL | Integrated BLE |
| G | CPU Core | F | Single Core |
| | | D | Dual Core |
| H | Attributes Code | 0-9 | Feature set |
| I | GPIO count | 1 | 31-50 |
| | | 2 | 51-70 |
| | | 3 | 71-90 |
| | | 4 | 91-110 |
| JJ | Engineering sample (optional) | ES | Engineering samples or not |
| K | Die Revision (optional) | | Base |
| | | A1-A9 | Die revision |
| L | Tape/Reel Shipment (optional) | T | Tape and Reel shipment |

Packaging

This product line is offered in four packages: 68-QFN, 116-BGA, 124-BGA, 104-MCSP.

Table 54. Package Dimensions

| Spec ID# | Package | Description | Package Drawing Number |
|----------|----------|---|------------------------|
| PKG_1 | 124-BGA | 124-BGA, 9 × 9 × 1 mm height with 0.65-mm pitch | 001-97718 |
| PKG_2 | 104-MCSP | 104-MCSP, 3.8 × 5 × 0.65 mm height with 0.35-mm pitch | 002-16508 |
| PKG_4 | 116-BGA | 116-BGA, 5.2 × 6.4 × 0.70 mm height with 0.5-mm pitch | 002-16574 |
| PKG_5 | 68-QFN | 68-QFN, 8 × 8 × 1 mm height with 0.4-mm pitch | 001-96836 |

Table 55. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------------------------|------------|-----|-------|-----|---------|
| T _A | Operating ambient temperature | – | –40 | 25.00 | 85 | °C |
| T _J | Operating junction temperature | – | –40 | – | 100 | °C |
| T _{JA} | Package θ _{JA} (124-BGA) | – | – | 64.3 | – | °C/watt |
| T _{JC} | Package θ _{JC} (124-BGA) | – | – | 37 | – | °C/watt |
| T _{JA} | Package θ _{JA} (116-BGA) | – | – | 36.5 | – | °C/watt |
| T _{JC} | Package θ _{JC} (116-BGA) | – | – | 12 | – | °C/watt |
| T _{JA} | Package θ _{JA} (104-CSP) | – | – | 33.7 | – | °C/watt |
| T _{JC} | Package θ _{JC} (104-CSP) | – | – | 0.2 | – | °C/watt |
| T _{JA} | Package θ _{JA} (68-QFN) | – | – | 21.6 | – | °C/watt |
| T _{JC} | Package θ _{JC} (68-QFN) | – | – | 7.2 | – | °C/watt |

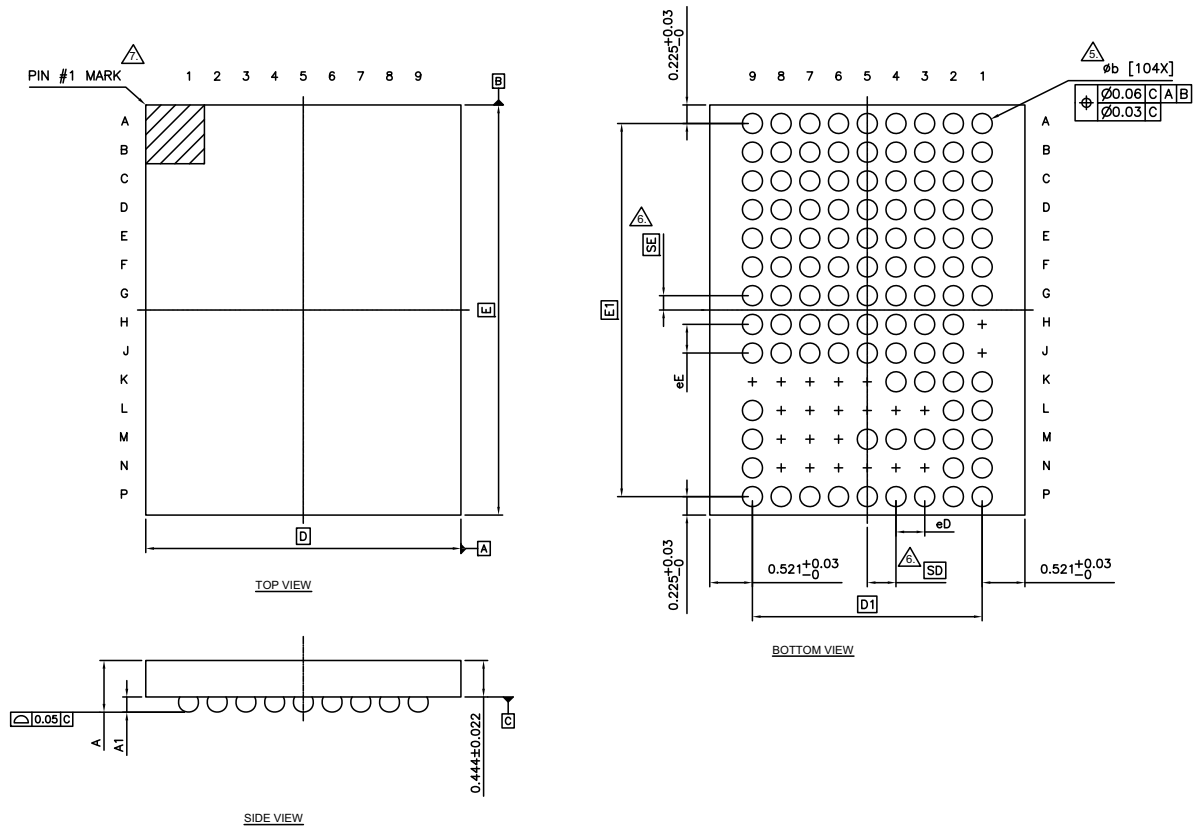
Table 56. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|------------------------------|--------------------------|----------------------------------|
| 124-BGA, 116-BGA, and 68-QFN | 260 °C | 30 seconds |
| 104-MCSP | 260 °C | 30 seconds |

Table 57. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|------------------------------|-------|
| 124-BGA, 116-BGA, and 68-QFN | MSL 3 |
| 104-MCSP | MSL 1 |

Figure 15. 104-WLCSP 3.8 × 5.0 × 0.65 mm



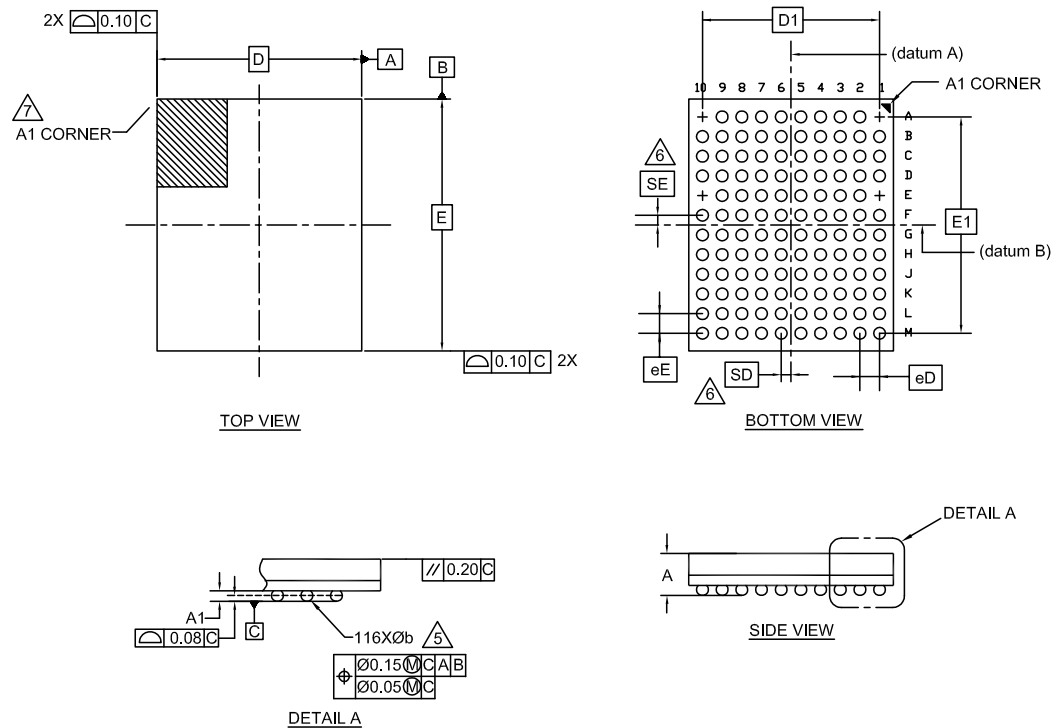
| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.650 |
| A1 | 0.167 | 0.185 | 0.203 |
| D | 3.791 | 3.841 | 3.891 |
| E | 4.95 | 5.00 | 5.05 |
| D1 | 2.80 BSC | | |
| E1 | 4.55 BSC | | |
| MD | 9 | | |
| ME | 14 | | |
| N | 104 | | |
| Ø b | 0.215 | 0.245 | 0.275 |
| eD | 0.335 | 0.350 | 0.365 |
| eE | 0.335 | 0.350 | 0.365 |
| SD | 0.35 BSC | | |
| SE | 0.175 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
 - SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
 - "e" REPRESENTS THE SOLDER BALL GRID PITCH.
 - SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- ▲ DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- ▲ "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- ▲ A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
 - JEDEC SPECIFICATION NO. REF. : N/A.

002-16508 *E

Figure 16. 116-BGA 5.2 × 6.4 × 0.70 mm



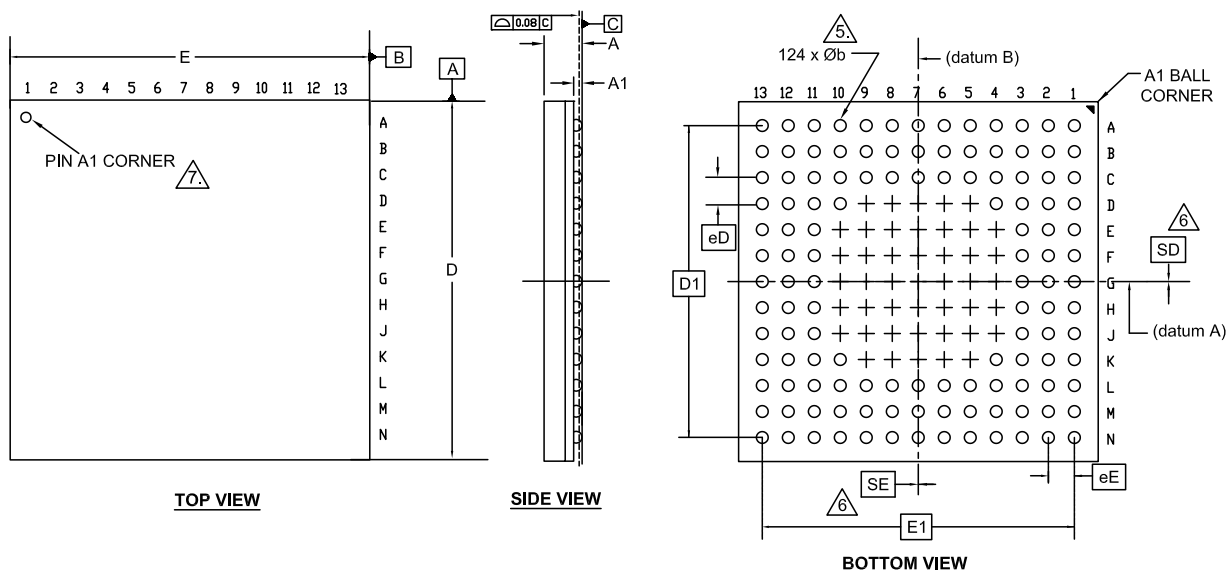
| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 0.70 |
| A1 | 0.16 | 0.21 | 0.26 |
| D | 5.20 BSC | | |
| E | 6.40 BSC | | |
| D1 | 4.50 BSC | | |
| E1 | 5.50 BSC | | |
| MD | 10 | | |
| ME | 12 | | |
| N | 116 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eD | 0.50 BSC | | |
| eE | 0.50 BSC | | |
| SD | 0.25 BSC | | |
| SE | 0.25 BSC | | |

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
 - SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
 - "e" REPRESENTS THE SOLDER BALL GRID PITCH.
 - SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- ⚠️ DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- ⚠️ "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- ⚠️ A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
 - JEDEC SPECIFICATION NO. REF: N/A

002-16574 *B

Figure 17. 124-BGA 9.0 × 9.0 × 1.0 mm



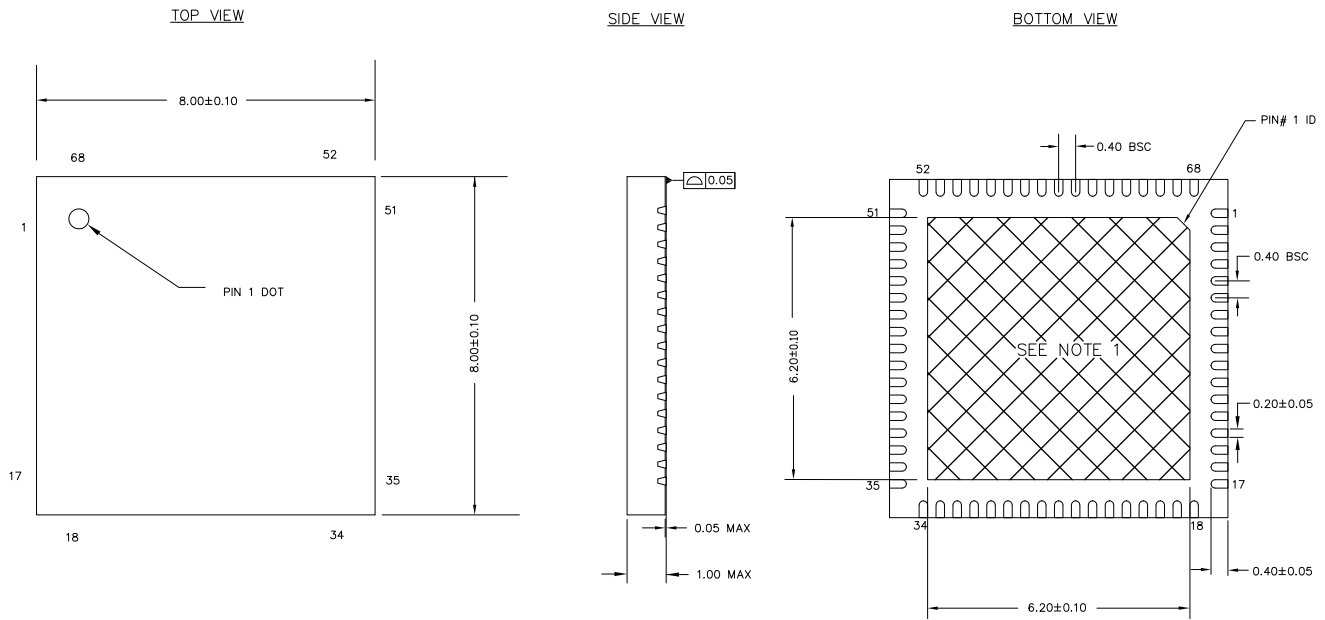
| SYMBOL | DIMENSIONS | | |
|--------|------------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | 0.21 | 0.26 |
| D | 8.90 | 9.00 | 9.10 |
| E | 8.90 | 9.00 | 9.10 |
| D1 | 7.80 BSC | | |
| E1 | 7.80 BSC | | |
| MD | 13 | | |
| ME | 13 | | |
| N | 124 | | |
| ∅ b | 0.25 | 0.30 | 0.35 |
| eD | 0.65 BSC | | |
| eE | 0.65 BSC | | |
| SD | 0 | | |
| SE | 0 | | |

NOTES:


- ALL DIMENSIONS ARE IN MILLIMETERS.
- SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
- JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

Figure 18. 68 QFN 8 × 8 × 1 mm



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-96836 *A

Acronyms

| Acronym | Description |
|---------|---|
| 3DES | triple DES (data encryption standard) |
| ADC | analog-to-digital converter |
| AES | advanced encryption standard |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| AMUX | analog multiplexer |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| BGA | ball grid array |
| BOD | brown-out detect |
| CAD | computer aided design |
| CCO | current controlled oscillator |
| CM0+ | Cortex-M0+, an Arm CPU |
| CM4 | Cortex-M4, an Arm CPU |
| CMAC | cipher-based message authentication code |
| CMOS | complementary metal-oxide-semiconductor, a process technology for IC fabrication |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CSD | CapSense Sigma-Delta |
| CSX | Cypress mutual capacitance sensing method. See also CSD |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DAP | debug access port |
| DES | data encryption standard |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DSI | digital system interconnect |
| DU | data unit |
| ECC | elliptic curve cryptography |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |
| FIFO | first-in, first-out |
| FLL | frequency locked loop |

| Acronym | Description |
|--------------------------|---|
| FPU | floating-point unit |
| FS | full-speed |
| GND | Ground |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HMAC | Hash-based message authentication code |
| HSIOM | high-speed I/O matrix |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| I ² S | inter-IC sound |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| IoT | internet of things |
| IPC | inter-processor communication |
| IRQ | interrupt request |
| ISR | interrupt service routine |
| JTAG | Joint Test Action Group |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol |
| LP | low power |
| LS | low-speed |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVTTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MCWDT | multi-counter watchdog timer |
| MISO | master-in slave-out |
| MMIO | memory-mapped input output |
| MOSI | master-out slave-in |
| MPU | memory protection unit |
| MSL | moisture sensitivity level |
| Msp/s | million samples per second |
| MTB | micro trace buffer |
| MUL | multiplier |
| NC | no connect |
| NMI | nonmaskable interrupt |

| Acronym | Description |
|---------|--|
| NVIC | nested vectored interrupt controller |
| OTP | one-time programmable |
| OVT | overvoltage tolerant |
| PASS | programmable analog subsystem |
| PCB | printed circuit board |
| PCM | pulse code modulation |
| PDM | pulse density modulation |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLL | phase-locked loop |
| PMIC | power management integrated circuit |
| POR | power-on reset |
| PPU | peripheral protection unit |
| PRNG | pseudo random number generator |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| QD | quadrature decoder |
| QSPI | quad serial peripheral interface |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| ROM | read-only memory |
| RSA | Rivest–Shamir–Adleman, a public-key cryptography algorithm |
| RTC | real-time clock |
| RX | receive |
| S/H | sample and hold |
| SAR | successive approximation register |
| SARMUX | SAR ADC multiplexer bus |
| SCB | serial communication block |
| Sflash | supervisory flash |
| SHA | secure hash algorithm |
| SINAD | signal to noise and distortion ratio |
| SNR | signal-to-noise ration |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SROM | supervisory read-only memory |
| SRSS | system resources subsystem |
| SWD | serial wire debug, a test protocol |
| SWJ | serial wire JTAG |

| Acronym | Description |
|---------|--|
| SWO | single wire output |
| SWV | serial-wire viewer |
| TCPWM | timer, counter, pulse-width modulator |
| TDM | time division multiplexed |
| TQFP | thin quad flat package |
| TRM | technical reference manual |
| TRNG | true random number generator |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| ULP | ultra-low power |
| USB | Universal Serial Bus |
| WCO | watch crystal oscillator |
| WDT | watchdog timer |
| WIC | wakeup interrupt controller |
| WLCSP | wafer level chip scale package |
| XIP | execute-in-place |
| XRES | external reset input pin |

Document Conventions

Unit of Measure

Table 58. Unit of Measure

| Symbol | Unit of Measure |
|--------|---------------------------|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| chr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msp | measuresamples per second |
| μA | microampere |
| μF | microfarad |

Table 58. Unit of Measure (continued)

| Symbol | Unit of Measure |
|--------|----------------------|
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

Errata

This section describes the errata for the PSoC 63 Product Family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number | Device Characteristics |
|-------------|------------------------|
| CY8C6XX | PSoC 63 Product Family |

PSoC 63 Qualification Status

Production

PSoC 63 Errata Summary

Noise is caused in supply and ground traces when multiple outputs switch. The amount of noise is dependent on the number of outputs, the drive strength of the output drivers, the frequency of the switching, and the impact on specific ports. The noise is worse at higher voltages ($V_{DD} = 2.7\text{ V}$ and higher) and should not be an issue with 1.8 V externally regulated (that is, $V_{DD} = 1.8\text{ V} \pm 5\%$) designs.

For cases where there are large numbers of GPIOs switching simultaneously, the following errata conditions are applicable. Note that the exact number cannot be specified as there are too many system-dependent conditions.

This table defines the errata applicability to available PSoC 63 family devices.

| Items | CY8C6XX 63 | Silicon Revision | Fix Status |
|---|------------|------------------|--|
| [1] Drive mode strength must be limited. | All | *C silicon | Investigation underway. Fix planned by Q3'20 |
| [2] CapSense use is restricted to Ports 6 and 7 with switching restrictions on other ports. | All | *C silicon | Investigation underway. Fix planned by Q3'20 |
| [3] Switching noise can cause ADC errors due to voltage reference noise. | All | *C silicon | Investigation underway. Fix planned by Q3'20 |
| [4] Port Usage restrictions must be applied. | All | *C silicon | Investigation underway. Fix planned by Q3'20 |

| 1. Drive mode strength must be limited. | |
|---|--|
| Problem Definition | <p>There are four Drive mode strengths: DM0, DM1, DM2, and DM3, DM0 being the strongest and DM3 the weakest in order. Usage of DM0 can cause noise in supply and ground lines for simultaneous outputs switching. Drive mode strength must be limited to DM2 for all GPIOs except for the 80 MHz QSPI clock which may use DM1.</p> <p>The V_{OL} and V_{OH} specs are affected as follows (also applies to V_{DDIO}, V_{DDIOA}, and V_{DDA} pins):</p> <p>$V_{DD} < 2.7\text{ V}$: $V_{OL} = 0.5\text{ V}$ @ $I_{OL} = 6\text{ mA}$. $V_{OH} = V_{DD} - 0.5\text{ V}$, $I_{OH} = 6\text{ mA}$.</p> <p>$V_{DD} \geq 2.7\text{ V}$: $V_{OL} = 0.4$ @ $I_{OL} = 6\text{ mA}$. $V_{OH} = V_{DD} - 0.5\text{ V}$, $I_{OH} = 6\text{ mA}$.</p> |
| Parameters Affected | Drive mode settings. |
| Trigger Condition(s) | Simultaneous outputs switching with high drive strength |
| Scope of Impact | Causes supply and ground noise, which can affect ADC and CapSense operation |
| Workaround | Follow drive mode strength restrictions. Drive Mode 2 (DM2) should be used for all ports except for the 80-MHz QSPI clock, which should be DM1 |
| Fix Status | Investigation underway. Fix planned by Q3'20. |

| 2. CapSense use is restricted to Ports 6 and 7 with switching restrictions on other ports. | |
|---|--|
| Problem Definition | GPIO simultaneous switching creates noise which can affect CapSense accuracy in unrestricted use |
| Parameters Affected | CapSense sensitivity and accuracy |
| Trigger Condition(s) | Noise caused by GPIO simultaneous output switching during CapSense operation |
| Scope of Impact | CapSense may produce erroneous results due to noise coupling from switching GPIOs. |
| Workaround | For CapSense usage, the following restrictions apply: <ol style="list-style-type: none"> Limit switching on Port 1 to 1 MHz (no more than 2 outputs) with slow slew rate. CapSense pins are restricted to Ports 6 and 7. No other GPIO output activity is allowed on Ports 6 and 7. Switching in Ports 5 and 8 is restricted to 1 MHz (no more than 2 outputs) with slow slew rate setting. CapSense must use the SRSS reference. |
| Fix Status | Investigation underway. Fix planned by Q3'20. |

| 3. Switching noise can cause ADC errors due to voltage reference noise. | |
|--|---|
| Problem Definition | 12-bit SAR ADC Counts are affected by switching noise |
| Parameters Affected | ADC accuracy |
| Trigger Condition(s) | Switching noise caused by GPIO simultaneous switching |
| Scope of Impact | ADC accuracy will be impacted |
| Workaround | Restrict switching on Ports 9 and 10 (analog input ports). The Programmable Analog Sub-System (PASS), including the SAR ADC, is connected to Ports 9 and 10. With no switching on Ports 9 and 10, the ADC error may be up to 4 LSB counts. Switching in Ports 9 and 10 is restricted to 1 MHz (no more than 2 outputs) with slow slew rate setting and, in this case, the ADC error may be up to 12 counts. |
| Fix Status | Investigation underway; Fix planned by Q3'20. |

| 4. Port Usage restrictions must be applied. | |
|--|---|
| Problem Definition | GPIO simultaneous switching causes supply and ground noise that adversely affects other on-chip subsystems). |
| Parameters Affected | CapSense and ADC results |
| Trigger Condition(s) | GPIO simultaneous switching with unrestricted strengths and frequency. |
| Scope of Impact | Incorrect results may cause false sensing or failure to sense for CapSense and inaccurate results for the SAR ADC (may not deliver 12-bit accuracy). |
| Workaround | Follow Port Usage restrictions: <ol style="list-style-type: none"> Switching on Port 0 must be restricted to less than 8 MHz. Switching on Port 1 must be restricted to less than 1 MHz with slow rate and no more than 2 outputs. Ports 9 and 10 must be restricted to 8 MHz when not using the ADC and the restrictions stated earlier used when the ADC is used. Use VREF from System Resource Subsystem (SRSS) for CapSense |
| Fix Status | Investigation underway. Fix planned by Q3'20. |

Revision History

| Description Title: PSoC 6 MCU: CY8C63x6, CY8C63x7 Datasheet Document Number: 002-18787 | | | |
|---|---------|-----------------|---|
| Revision | ECN | Submission Date | Description of Change |
| *F | 6164322 | 05/03/2018 | Release of production datasheet. |
| *G | 6250376 | 07/17/2018 | Corrected document number in the revision history table. |
| *H | 6522270 | 04/01/2019 | Updated Functional Description . Added "Pinouts for 104-MCSP with USB" table in Pinouts . Added package diagram (spec 001-97718 *B). Added a note in Table 4 . Updated Table 9 , Table 26 , and Table 40 in Electrical Specifications . Updated Features, Blocks and Functionality , I/O Clock Source , One-Time-Programmable (OTP) eFuse , Packaging , and Ordering Information . Updated Figure 4 (spec 002-16508 *D to *E) in Packaging . Corrected Unit usage throughout the document. Added Errata . Updated Copyright information in Sales page. |
| *I | 6663531 | 09/20/2019 | Updated the title. Added UDB in Acronyms . |
| *J | 6757930 | 12/20/2019 | Updated Features . Updated Blocks and Functionality and Functional Description Updated Pinouts and Power Supply Considerations . |
| *K | 6842918 | 03/31/2020 | Updated Features . Updated Functional Description . Updated Pinouts . Updated PSoC 6 MPN Decoder . |

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