Value Line Receiver

Applications

- Ultra low-power wireless applications operating in the 315/433/868/915 MHz ISM/SRD bands
- Wireless alarm and security systems
- Industrial monitoring and control
- Remote Controls
- Toys
- Home and building automation

Key Features

RF Performance

- Receive sensitivity down to −116 dBm at 0.6 kbps
- Programmable data rate from 0.6 to 600 kbps
- Frequency bands: 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz
- 2-FSK, 4-FSK, GFSK, and OOK supported

Digital Features

- Flexible support for packet oriented systems;
- On-chip support for sync word detection, flexible packet length, and automatic CRC calculation

Low-Power Features

- 200 nA sleep mode current consumption
- Fast start-up time; 240 µs from sleep to RX mode
- 64-byte RX FIFO

General

- Few external components; Completely on-chip frequency synthesizer, no external filters or RF switch needed
- Green package: RoHS compliant and no antimony or bromine
- Small size (QLP 4x4 mm package, 20 pins)
- Suited for systems targeting compliance with EN 300 220 V2.3.1 (Europe) and FCC CFR Part 15 (US)
- Support for asynchronous and synchronous serial transmit mode for backwards compatibility with existing radio communication protocols

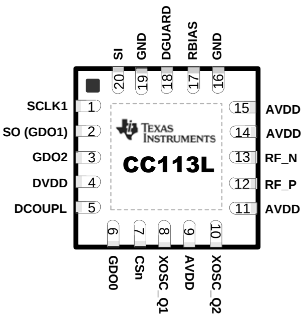
Product Description

The **CC113L** is a cost optimized sub-1 GHz RF receiver for the 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz frequency bands. The circuit is based on the popular **CC1101** RF transceiver, and RF performance characteristics are identical. The **CC115L** transmitter together with the **CC113L** receiver enable a low cost RF link.

The RF receiver is integrated with a highly configurable baseband demodulator. The modem supports various modulation formats and has a configurable data rate up to 600 kbps.

CC113L provides extensive hardware support for packet handling, data buffering and burst transmissions.

The main operating parameters and the 64-byte receive FIFO of **CC113L** can be controlled via an SPI interface. In a typical system, the **CC113L** will be used together with a microcontroller and a few additional passive components.



This product shall not be used in any of the following products or systems without prior express written permission from Texas Instruments:

implantable cardiac rhythm management systems, including without limitation pacemakers, defibrillators and cardiac resynchronization devices,
external cardiac rhythm management systems that communicate directly with one or more implantable medical devices; or
other devices used to monitor or treat cardiac function, including without limitation pressure sensors, biochemical sensors and neurostimulators.
Please contact lpw-medical-approval@list.ti.com if your application might fall within the category described above.

Abbreviations

Abbreviations used in this data sheet are described below.

2-FSK	Binary Frequency Shift Keying	LSB	Least Significant Bit
4-FSK	Quaternary Frequency Shift Keying	MCU	Microcontroller Unit
ADC	Analog to Digital Converter	MSB	Most Significant Bit
AFC	Automatic Frequency Compensation	N/A	Not Applicable
AGC	Automatic Gain Control	NRZ	Non Return to Zero (Coding)
AMR	Automatic Meter Reading	OOK	On-Off Keying
BER	Bit Error Rate	PCB	Printed Circuit Board
BT	Bandwidth-Time product	PD	Power Down
CFR	Code of Federal Regulations	PER	Packet Error Rate
CRC	Cyclic Redundancy Check	PLL	Phase Locked Loop
CS	Carrier Sense	POR	Power-On Reset
DC	Direct Current	PTAT	Proportional To Absolute Temperature
DVGA	Digital Variable Gain Amplifier	QLP	Quad Leadless Package
ESR	Equivalent Series Resistance	QPSK	Quadrature Phase Shift Keying
FCC	Federal Communications Commission	RC	Resistor-Capacitor
FIFO	First-In-First-Out	RF	Radio Frequency
FS	Frequency Synthesizer	RSSI	Received Signal Strength Indicator
GFSK	Gaussian shaped Frequency Shift Keying	RX	Receive, Receive Mode
IF	Intermediate Frequency	SMD	Surface Mount Device
I/Q	In-Phase/Quadrature	SPI	Serial Peripheral Interface
ISM	Industrial, Scientific, Medical	SRD	Short Range Devices
LC	Inductor-Capacitor	VCO	Voltage Controlled Oscillator
LNA	Low Noise Amplifier	XOSC	Crystal Oscillator
LO	Local Oscillator	XTAL	Crystal

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1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD + 0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N, DCOUPL, RBIAS	–0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020
ESD		750	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD		400	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)

Table 1: Absolute Maximum Ratings

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

2 Operating Conditions

The operating conditions for CC113L are listed in Table 2 below.

Parameter	Min	Max	Unit	Condition
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Max	Unit	Condition/Note
Frequency range	300	348	MHz	
	387	464	MHz	If using a 27 MHz crystal, the lower frequency limit for this band is 392 MHz
	779	928	MHz	
Data rate	0.6	500	kBaud	2-FSK
	0.6	250	kBaud	GFSK and OOK
	0.6	300	kBaud	4-FSK (the data rate in kbps will be twice the baud rate)
				Optional Manchester encoding (the data rate in kbps will be half the baud rate)

Table 3: General Characteristics

4 Electrical Specifications

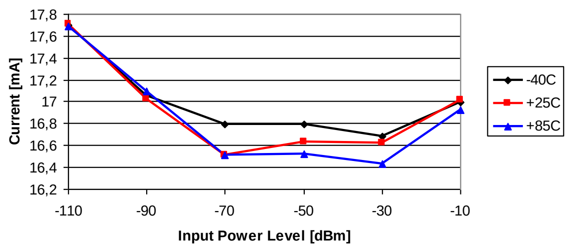
4.1 Current Consumption

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using [1] and [2]. Reduced current settings (MDMCFG2.DEM_DCFILT_OFF=1) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See Table 5 for additional details on current consumption and sensitivity.

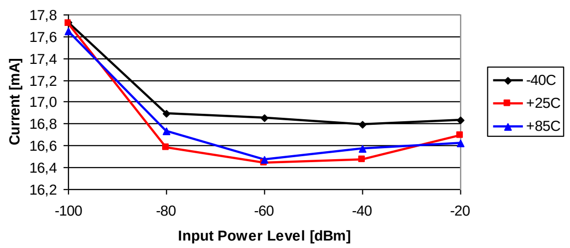
Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		0.2	1	μA	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
		100		μA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with MCSM0.OSC_FORCE_ON set)
		165		μA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		1.7		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		8.4		mA	The current consumption for the intermediate states when going from IDLE to RX, including the calibration state
Current consumption, 315 MHz		15.4		mA	Receive mode, 1.2 kBaud, reduced current, input at sensitivity limit
		14.4		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.2		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		14.3		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		16.5		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
Current consumption, 433 MHz		16.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.7		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		17.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.7		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 868/915 MHz		15.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		16.9		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.

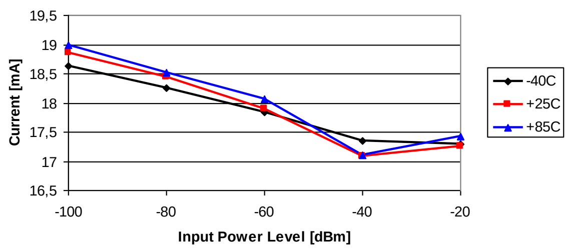
Table 4: Current Consumption



1.2 kBaud GFSK



38.4 kBaud GFSK



250 kBaud GFSK

Figure 1: Typical RX Current Consumption over Temperature and Input Power Level, 868/915 MHz, Sensitivity Optimized Setting

4.2 RF Receive Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using [1] and [2].

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
Spurious emissions		–68 –66	–57 –47	dBm dBm	25 MHz - 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit) Above 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit) Typical radiated spurious emission is –49 dBm measured at the VCO frequency
RX latency		9		bit	Serial operation. Time from start of reception until data is available on the receiver data output pin is equal to 9 bit
315 MHz					
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (2-FSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–111		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.2 mA to 15.4 mA at the sensitivity limit. The sensitivity is typically reduced to -109 dBm
433 MHz					
0.6 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 14.3 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–116		dBm	
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.0 mA to 16.0 mA at the sensitivity limit. The sensitivity is typically reduced to –110 dBm
38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	
250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–95		dBm	

Parameter	Min	Typ	Max	Unit	Condition/Note
868/915 MHz					
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.7 mA to 15.7 mA at sensitivity limit. The sensitivity is typically reduced to –109 dBm
Saturation		–14		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [5]
Adjacent channel rejection ±100 kHz offset		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing See Figure 2 for selectivity performance at other offset frequencies
Image channel rejection		31		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 –50 –40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 2 for blocking performance at other offset frequencies
38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.7 mA to 15.6 mA at the sensitivity limit. The sensitivity is typically reduced to -102 dBm
Saturation		–16		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [5]
Adjacent channel rejection –200 kHz offset +200 kHz offset		 12 25		 dB dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing See Figure 3 for blocking performance at other offset frequencies
Image channel rejection		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 –50 –40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 3 for blocking performance at other offset frequencies
250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–95		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.9 mA to 16.9 mA at the sensitivity limit. The sensitivity is typically reduced to –91 dBm
Saturation		–17		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [5]
Adjacent channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing See Figure 4 for blocking performance at other offset frequencies
Image channel rejection		14		dB	IF frequency 304 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 –50 –40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 4 for blocking performance at other offset frequencies

Parameter	Min	Typ	Max	Unit	Condition/Note
4-FSK, 125 kBaud data rate (250 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 127 kHz deviation, 406 kHz digital channel filter bandwidth)					
Receiver sensitivity		–96		dBm	
4-FSK, 250 kBaud data rate (500 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 254 kHz deviation, 812 kHz digital channel filter bandwidth					
Receiver sensitivity		–91		dBm	
4-FSK, 300 kBaud data rate (600 kbps), sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (1% packet error rate, 20 bytes packet length, 228 kHz deviation, 812 kHz digital channel filter bandwidth)					
Receiver sensitivity		–89		dBm	

Table 5: RF Receive Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–105	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–96	–92	–97	–95	–92	–97	–94	–92
Sensitivity [dBm] 500 kBaud	–91	–90	–86	–91	–90	–86	–91	–90	–86

Table 6: Typical Sensitivity over Temperature and Supply Voltage, 868 MHz, Sensitivity Optimized Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–104	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–94	–92	–97	–95	–92	–97	–95	–92
Sensitivity [dBm] 500 kBaud	–91	–89	–86	–91	–90	–86	–91	–89	–86

Table 7: Typical Sensitivity over Temperature and Supply Voltage, 915 MHz, Sensitivity Optimized Setting

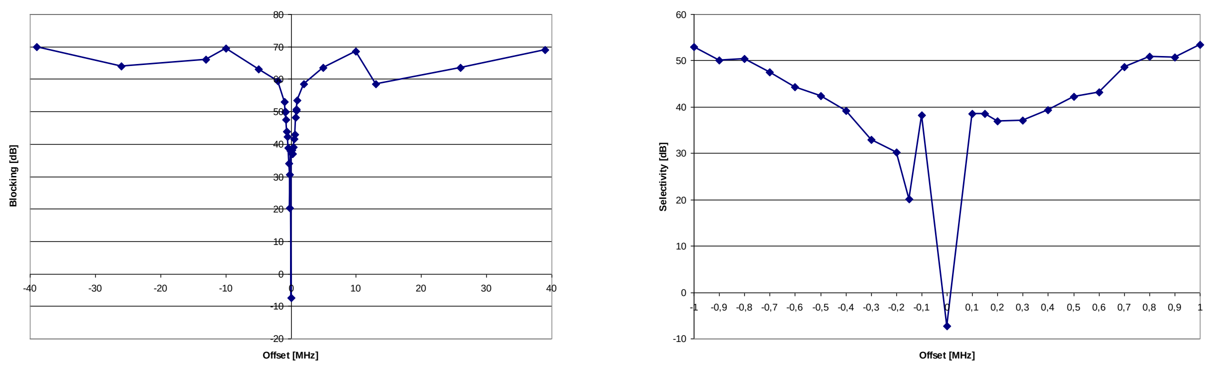


Figure 2: Typical Selectivity at 1.2 kBaud Data Rate, 868.3 MHz, GFSK, 5.2 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 kHz

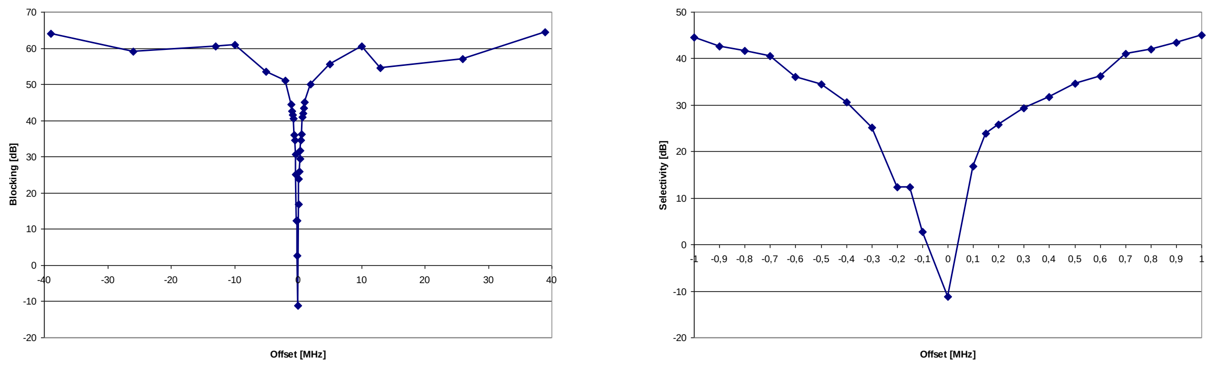


Figure 3: Typical Selectivity at 38.4 kBaud Data Rate, 868 MHz, GFSK, 20 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

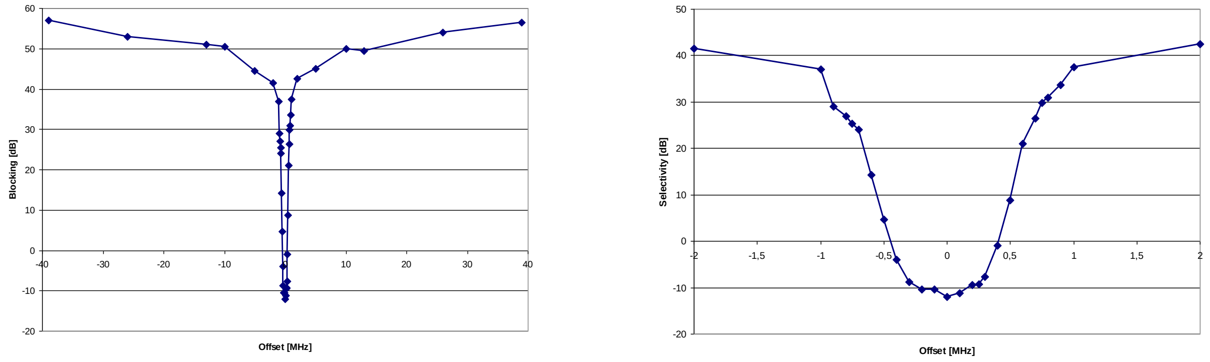


Figure 4: Typical Selectivity at 250 kBaud Data Rate, 868 MHz, GFSK, IF Frequency is 304 kHz and the Digital Channel Filter Bandwidth is 540 kHz

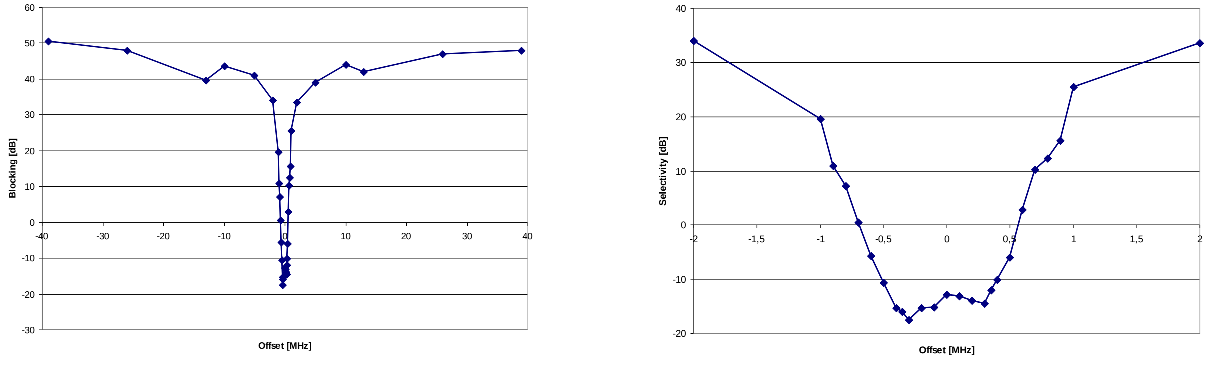


Figure 5: Typical Selectivity at 500 kBaud Data Rate, 868 MHz, GFSK, IF Frequency is 355 kHz and the Digital Channel Filter Bandwidth is 812 kHz

4.3 Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using [1] and [2].

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		µs	This parameter is to a large degree crystal dependent. Measured on [1] and [2] using crystal AT-41CD2 from NDK

Table 8: Crystal Oscillator Parameters

4.4 Frequency Synthesizer Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results are obtained using [1] and [2]. Min figures are given using a 27 MHz crystal. Typ. and max figures are given using a 26 MHz crystal

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26 - 27 MHz crystal. The resolution (in Hz) is equal for all frequency bands
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing
RF carrier phase noise		–92		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		–98		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		–107		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		–119		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		–129		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on time (See Table 26)	72	75	75	µs	Time from leaving the IDLE state until arriving in the RX state, when not performing calibration. Crystal oscillator running.
PLL calibration time (See Table 27)	685	712	724	µs	Calibration can be initiated manually or automatically before entering or after leaving RX

Table 9: Frequency Synthesizer Parameters

4.5 DC Characteristics

T_A = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD – 0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD – 0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	–50	nA	Input equals 0 V
Logic "1" input current	N/A	50	nA	Input equals VDD

Table 10: DC Characteristics

4.6 Power-On Reset

For proper Power-On-Reset functionality the power supply should comply with the requirements in Table 11 below. Otherwise, the chip should be assumed to have unknown state until transmitting an `SRES` strobe over the SPI interface. See Section 18.1 on page 36 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power-on and power-off

Table 11: Power-On Reset Requirements

5 Pin Configuration

The **CC113L** pin-out is shown in Figure 6 and Table 12. See Section 23 for details on the I/O configuration.

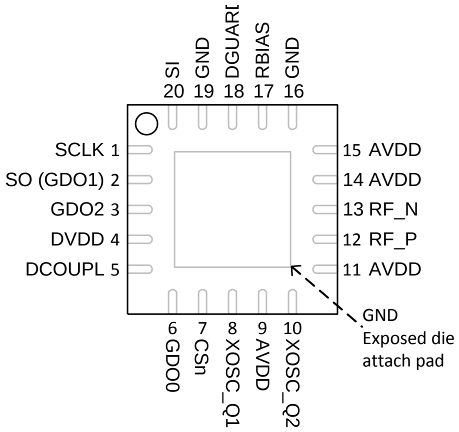


Figure 6: Pinout Top View

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip

Pin #	Pin Name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling **NOTE:** This pin is intended for use with the CC113L only. It cannot be used to provide supply voltage to other devices
6	GDO0	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial output RX data
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode
14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 12: Pinout Overview

6 Circuit Description

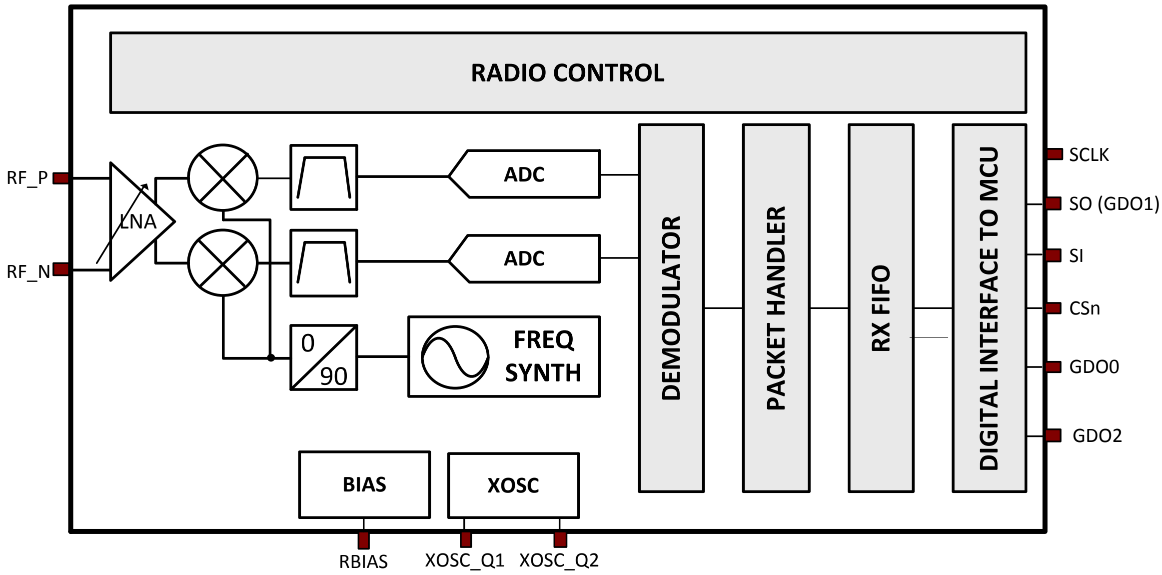


Figure 7: CC113L Simplified Block Diagram

A simplified block diagram of CC113L is shown in Figure 7.

CC113L features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation, and bit/packet synchronization are performed digitally.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degree phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

7 Application Circuit

Figure 8 shows the low cost CC113LEM application circuit ([10] and [11]) (see Table 13 for component values).

The designs in [1] and [2] were used for CC113L characterization. The application circuits are shown in Figure 9 and Figure 10 (see Table 14 for component values).

7.1 Bias Resistor

The 56 kΩ bias resistor R171 is used to set an accurate bias current

7.2 Balun and RF Matching

The balun component values and their placement are important to keep the performance optimized. Gerber files and schematics for the reference designs are available for download from the TI website

7.2.1 Balun and RF Matching (low cost application circuit)

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C131, L132, C122, L122, see Figure 8) form a balun that converts single-ended RF signal at the antenna to a differential RF signal on CC113L. C124 is needed for DC blocking.

The balun components also matches the CC113L input impedance to a 50 Ω source. C126 provides DC blocking and is only needed if there is a DC path in the antenna.

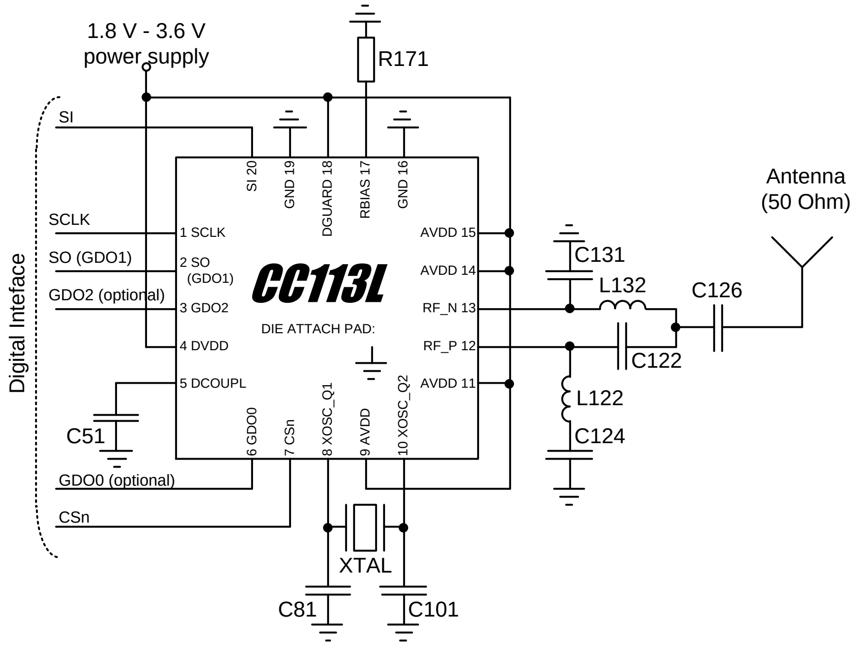


Figure 8: Low Cost Application Circuit and Evaluation Circuit 315/433/868/915 MHz (excluding supply decoupling capacitors) ([10] and [11])

Component	Value at 315 MHz	Value at 433 MHz	Value at 868/915 MHz
C124	220 pF	220 pF	100 pF
C122	6.8 pF	3.9 pF	2.2 pF
C126	220 pF	220 pF	100 pF
C131	6.8 pF	3.9 pF	2.2 pF
L122	33 nH	27 nH	12 nH
L132	33 nH	27 nH	12 nH

Table 13: External Components (low cost application circuit)

7.2.2 Balun and RF Matching (characterization circuit)

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C131, C122, L122, and L132 in Figure 9 and L121, L131, C121, L122, C131, C122, and L132 in Figure 10) form a balun that converts single-ended RF signal at the antenna to a differential RF signal on CC113L. C124 is needed for DC blocking.

The balun components also matches the CC113L input impedance to a 50 Ω source. C126 provides DC blocking and is only needed if there is a DC path in the antenna.

Note that the 315/433 MHz design [1] use Murata LQG15 multi-layer inductors while the 868/915 MHz design [2] use Murata LQW15 wire-wound inductors.

L123, L124, and C123 (plus C125 in Figure 9) form an LC low-pass filter. This filter is not required for an RX-only design and can be omitted.

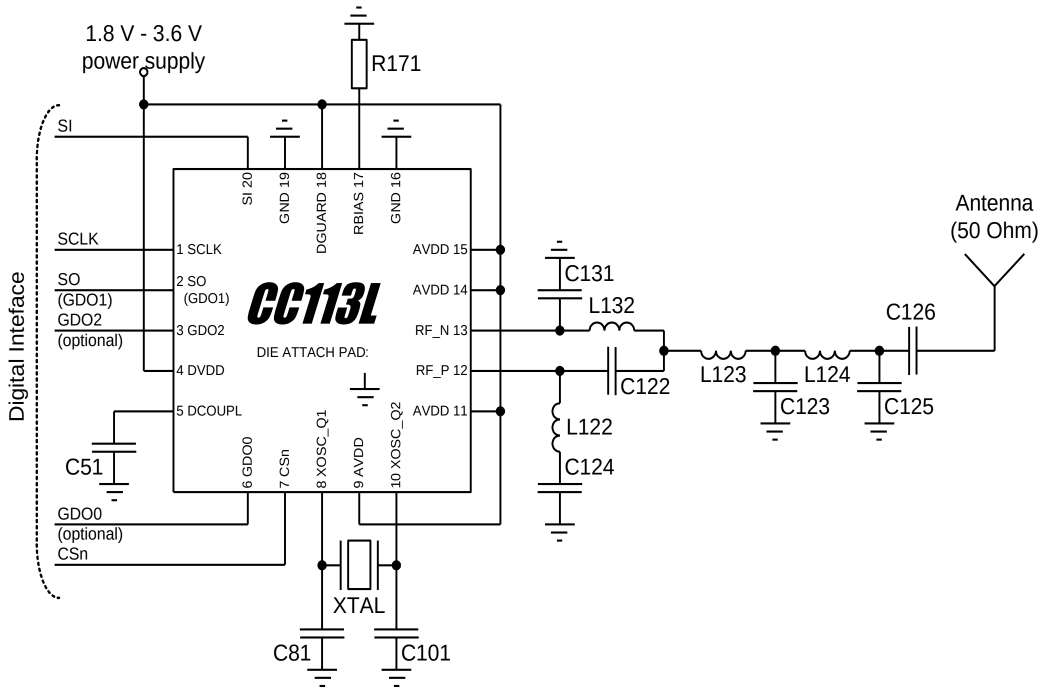


Figure 9: Characterization Circuit 315/433 MHz (excluding supply decoupling capacitors) ([1])

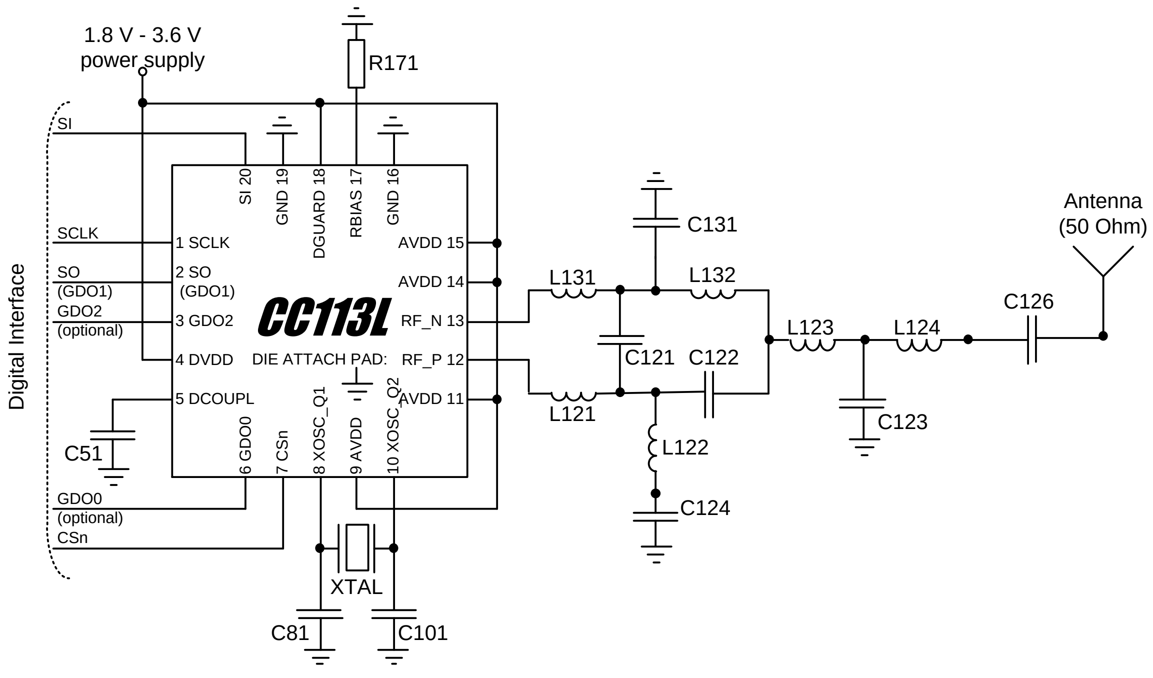


Figure 10: Characterization Circuit 868/915 MHz (excluding supply decoupling capacitors) ([2])

Component	Value at 315 MHz	Value at 433 MHz	Value at 868/915 MHz
C121			1 pF
C122	6.8 pF	3.9 pF	1.5 pF
C123	12 pF	8.2 pF	3.3 pF
C124	220 pF	220 pF	100 pF
C125	6.8 pF	5.6 pF	
C126	220 pF	220 pF	100 pF
C131	6.8 pF	3.9 pF	1.5 pF
L121			12 nH
L122	33 nH	27 nH	18 nH
L123	18 nH	22 nH	12 nH
L124	33 nH	27 nH	12 nH
L131			12 nH
L132	33 nH	27 nH	18 nH

Table 14: External Components (characterization circuits)

7.3 Crystal

A crystal in the frequency range 26 - 27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see Section 4.3 on page 12).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

Avoid routing digital signals with sharp edges close to XOSC_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

7.4 Reference Signal

The chip can alternatively be operated with a reference signal from 26 - 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. When using a full-swing digital signal, this capacitor can be omitted. The XOSC_Q2 line must be left un-connected. C81 and C101 can be omitted when using a reference signal.

7.5 Power Supply Decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. The CC113LEM reference designs ([10] and [11]) should be followed closely.

7.6 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground.

In the CC113LEM reference designs ([10] and [11]), 5 vias are placed inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using "tented" vias reduces the solder paste coverage below 100%. See Figure 11 for top solder resist and top paste masks.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the CC113L supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane by separate vias. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary. Routing in the ground plane underneath the chip or the balun/RF matching circuit, or between the chip's ground vias and the decoupling capacitor's ground vias should be avoided. This improves the grounding and ensures the shortest possible current return path.

Avoid routing digital signals with sharp edges close to XOSC_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components with different sizes than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC11xL Development Kit with a fully assembled CC113L Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The schematic, BOM and layout Gerber files are all available from the TI website ([10] and [11]).

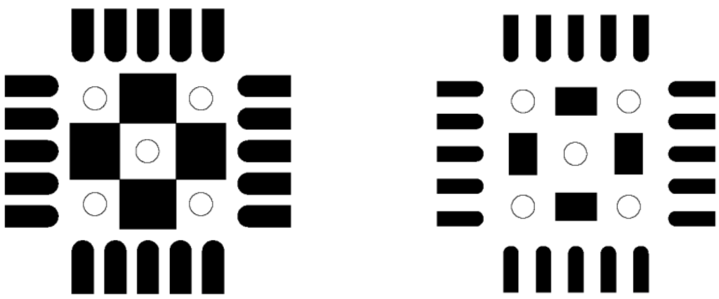


Figure 11: Left: Top Solder Resist Mask (Negative). Right: Top Paste Mask. Circles are Vias

8 Configuration Overview

CC113L can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. See Section 10 for more description of the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power-down
- Receive mode
- Carrier Frequency / RF channel
- Data rate
- Modulation format
- RX channel filter bandwidth
- Data buffering with the 64-byte RX FIFO
- Packet radio hardware support

Details of each configuration register can be found in Section 26 starting on page 45.

Figure 12 shows a simplified state diagram that explains the main CC113L states together with typical usage and current consumption. For detailed information on controlling the CC113L state machine, and a complete state diagram, see Section 18, starting on page 35.

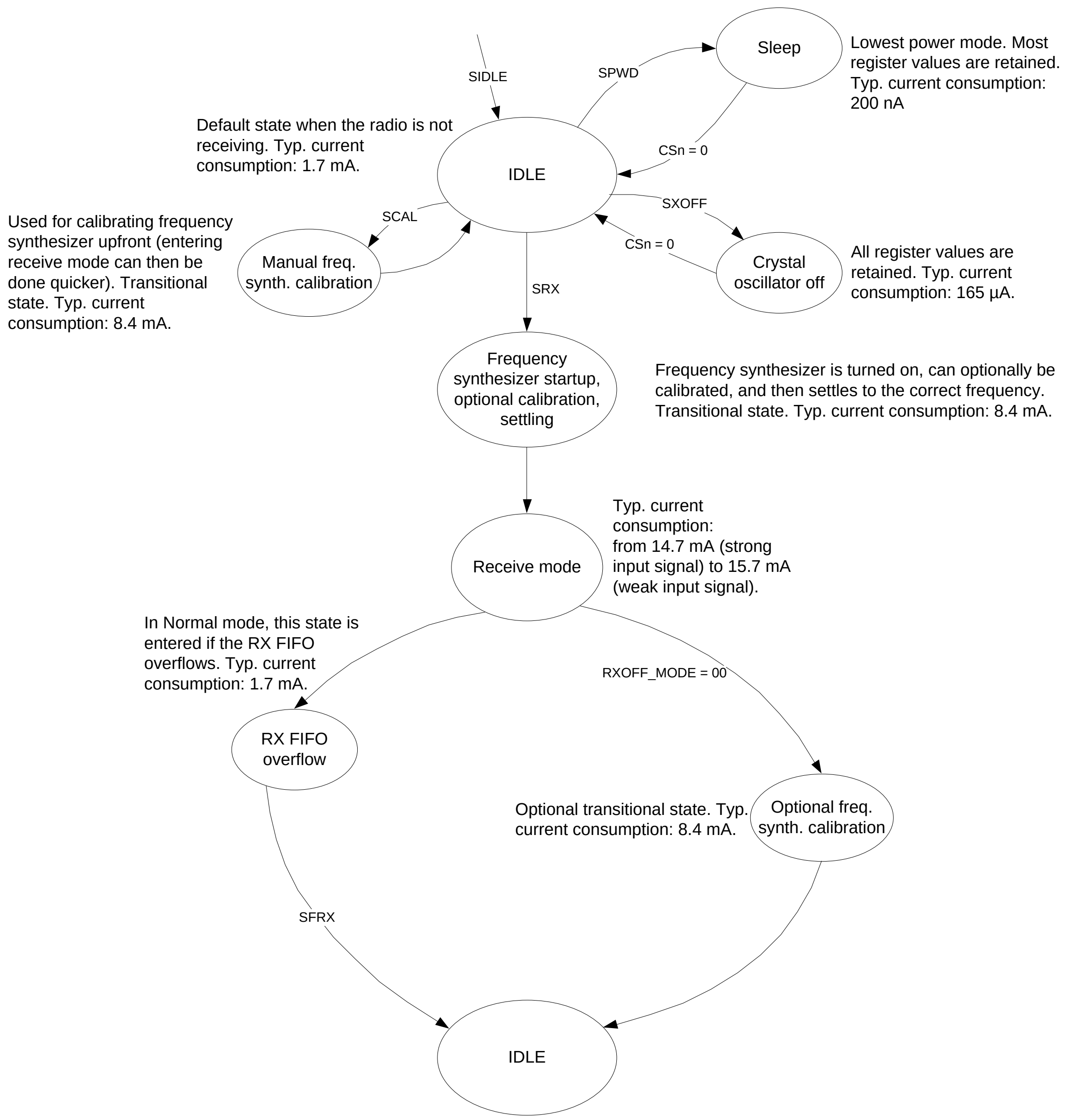


Figure 12: Simplified Radio Control State Diagram, with Typical Current Consumption at 1.2 kBaud Data Rate and MDMCFG2.DEM_DCFILT_OFF=1 (current optimized). Frequency Band = 868 MHz

9 Configuration Software

CC113L can be configured using the SmartRF™ Studio software [4]. The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

After chip reset, all the registers have default values as shown in the tables in Section 26. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

10 4-wire Serial Configuration and Data Interface

CC113L is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where CC113L is the slave. This interface is also used to read buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R/$\overline{W}$ bit, a burst access bit (B), and a 6-bit address (A_5 - A_0).

The CSn pin must be kept low during transfers on the SPI bus. If CSn goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 13 with reference to Table 15.

When CSn is pulled low, the MCU must wait until CC113L SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

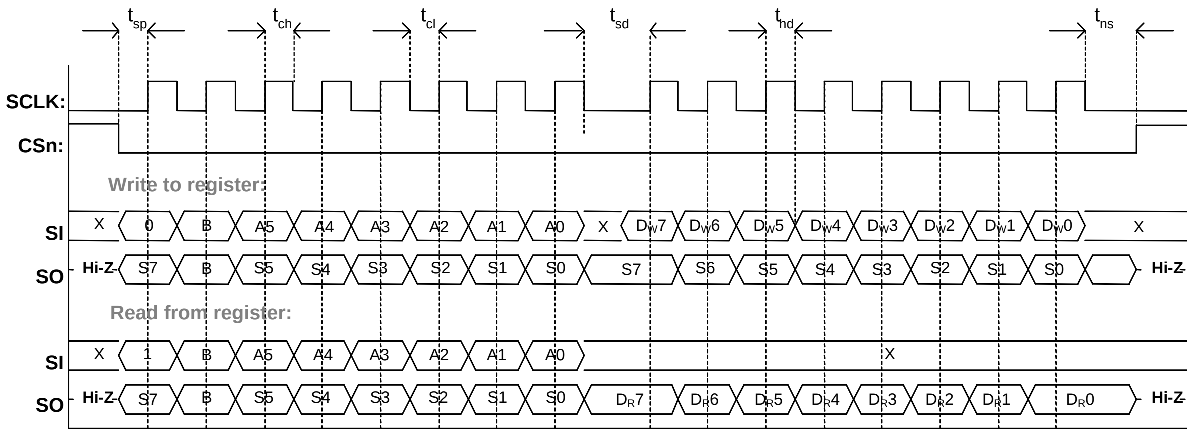


Figure 13: Configuration Registers Write and Read Operations

<table>
<tr><th>Parameter</th><th colspan="2">Description</th><th>Min</th><th>Max</th><th>Units</th></tr>
<tr><td rowspan="3">f_{SCLK}</td><td colspan="2">SCLK frequency
100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).</td><td>-</td><td>10</td><td rowspan="3">MHz</td></tr>
<tr><td colspan="2">SCLK frequency, single access. No delay between address and data byte</td><td>-</td><td>9</td></tr>
<tr><td colspan="2">SCLK frequency, burst access. No delay between address and data byte, or between data bytes</td><td>-</td><td>6.5</td></tr>
<tr><td>$t_{sp,pd}$</td><td colspan="2">CSn low to positive edge on SCLK, in power-down mode</td><td>150</td><td>-</td><td>µs</td></tr>
<tr><td>t_{sp}</td><td colspan="2">CSn low to positive edge on SCLK, in active mode</td><td>20</td><td>-</td><td>ns</td></tr>
<tr><td>t_{ch}</td><td colspan="2">Clock high</td><td>50</td><td>-</td><td>ns</td></tr>
<tr><td>t_{cl}</td><td colspan="2">Clock low</td><td>50</td><td>-</td><td>ns</td></tr>
<tr><td>t_{rise}</td><td colspan="2">Clock rise time</td><td>-</td><td>40</td><td>ns</td></tr>
<tr><td>t_{fall}</td><td colspan="2">Clock fall time</td><td>-</td><td>40</td><td>ns</td></tr>
<tr><td rowspan="2">t_{sd}</td><td rowspan="2">Setup data (negative SCLK edge) to positive edge on SCLK
(t_{sd} applies between address and data bytes, and between data bytes)</td><td>Single access</td><td>55</td><td>-</td><td rowspan="2">ns</td></tr>
<tr><td>Burst access</td><td>76</td><td>-</td></tr>
<tr><td>t_{hd}</td><td colspan="2">Hold data after positive edge on SCLK</td><td>20</td><td>-</td><td>ns</td></tr>
<tr><td>t_{ns}</td><td colspan="2">Negative edge on SCLK to CSn high.</td><td>20</td><td>-</td><td>ns</td></tr>
</table>

Table 15: SPI Interface Timing Requirements

Note: The minimum $t_{sp,pd}$ figure in Table 15 can be used in cases where the user does not read the CHIP_RDYn signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150 µs in Table 15 is the crystal oscillator start-up time measured on [1] and [2] using crystal AT-41CD2 from NDK.

10.1 Chip Status Byte

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the CC113L on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP_RDYn signal and this signal must go low before the first positive edge of SCLK. The CHIP_RDYn signal indicates that the crystal is running.

Bits 6, 5, and 4 comprise the STATE value. This value reflects the state of the chip. The XOSC and power to the digital core are on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state.

The last four bits (3:0) in the status byte contains FIFO_BYTES_AVAILABLE. For these bits to give any valid information, the R/$\overline{W}$ bit in the header byte must be set to 1. The FIFO_BYTES_AVAILABLE field will then contain the number of bytes that can be read from the RX FIFO. When FIFO_BYTES_AVAILABLE=15, 15 or more bytes can be read. The RX FIFO should not be emptied before the complete packet has been received (see the CC113L Errata Notes [3] for more details).

Table 16 gives a status byte summary.

Bits	Name	Description		
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.		
6:4	STATE[2:0]	Indicates the current main state machine mode		
		Value	State	Description
		000	IDLE	IDLE state (Also reported for some transitional states instead of SETTLING or CALIBRATE)
		001	RX	Receive mode
		010	Reserved	
		011	Reserved	
		100	CALIBRATE	Frequency synthesizer calibration is running
		101	SETTLING	PLL is settling
		110	RXFIFO_OVERFLOW	RX FIFO has overflowed. Read out any useful data, then flush the FIFO with `SFRX`
		111	Reserved	
3:0	FIFO_BYTES_AVAILABLE[3:0]	The number of bytes available in the RX FIFO		

Table 16: Status Byte Summary

10.2 Register Access

The configuration registers on the ***CC113L*** are located on SPI addresses from 0x00 to 0x2E. Table 31 on page 46 lists all configuration registers. It is highly recommended to use SmartRF Studio [4] to generate optimum register settings. The detailed description of each register is found in Section 26.1 and Section 26.2, starting on page 49. All configuration registers can be both written to and read. The R/$\overline{W}$ bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit (B) in the header byte. The address bits (A_5 - A_0) set the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30 - 0x3D, the burst bit is used to select between status registers when burst bit is one, and command strobes when burst bit is zero. See more in Section 10.3 below. Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

10.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (e.g. `MARCSTATE` or `RXBYTES`), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from `RXBYTES` being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the ***CC113L*** Errata Notes [3] for more details.

10.4 Command Strobes

Command Strobes may be viewed as single byte instructions to ***CC113L***. By addressing a command strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable receive mode, enable calibration etc. The 8 command strobes are listed in Table 30 on page 45.

> **Note:** An SIDLE strobe will clear all pending command strobes until IDLE state is reached. This means that if for example an SIDLE strobe is issued while the radio is in RX state, any other command strobes issued before the radio reaches IDLE state will be ignored.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the R/W̄ bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written. The R/W̄ bit should be set to one if the `FIFO_BYTES_AVAILABLE` field in the status byte should be interpreted.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an `SRES` strobe is being issued, one will have to wait for SO to go low again before the next header byte can be issued as shown in Figure 14. The command strobes are executed immediately, with the exception of the `SPWD` and the `SXOFF` strobes, which are executed when CSn goes high.

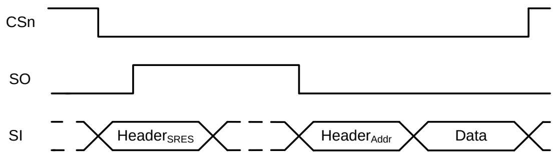


Figure 14: SRES Command Strobe

10.5 RX FIFO Access

The 64-byte RX FIFO is accessed through the 0x3F address. The RX FIFO is write-only and the R/W̄ bit should therefore be one.

The burst bit is used to determine if the RX FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte, a new header byte is expected; hence, CSn can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the RX FIFO:

- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

The RX FIFO may be flushed by issuing a `SFRX` command strobe. A `SFRX` command strobe can only be issued in the IDLE, or RXFIFO_OVERFLOW states. The RX FIFO is flushed when going to the SLEEP state.

Figure 15 gives a brief overview of different register access types possible.

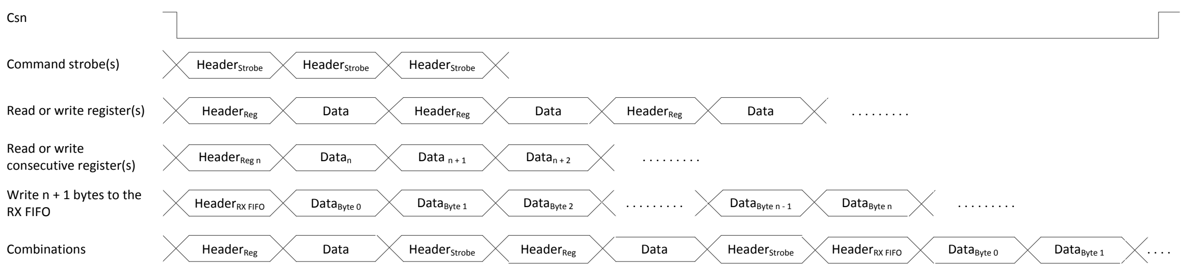


Figure 15: Register Access Types

11 Microcontroller Interface and Pin Configuration

In a typical system, CC113L will interface to a microcontroller. This microcontroller must be able to:

- Program CC113L into different modes
- Read buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn)

11.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 10 on page 21.

11.2 General Control and Status Pins

The CC113L has two dedicated configurable pins (GDO0 and GDO2) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See Section 23 on page 41 for more details on the signals that can be programmed.

GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options, the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

12 Data Rate Programming

The data rate expected in receive mode is programmed by the `MDMCFG3.DRATE_M` and the `MDMCFG4.DRATE_E` configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE\_E = \log_2\left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}}\right)$$

$$DRATE\_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE\_E}} - 256$$

If `DRATE_M` is rounded to the nearest integer and becomes 256, increment `DRATE_E` and use `DRATE_M` = 0.

The data rate can be set from 0.6 kBaud to 500 kBaud with the minimum step size according to Table 17 below. See Table 3 for the minimum and maximum data rates for the different modulation formats.

Min Data Rate [kBaud]	Typical Data Rate [kBaud]	Max Data Rate [kBaud]	Data rate Step Size [kBaud]
0.6	1.0	0.79	0.0015
0.79	1.2	1.58	0.0031
1.59	2.4	3.17	0.0062
3.17	4.8	6.33	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.3	0.0496
25.4	38.4	50.7	0.0992
50.8	76.8	101.4	0.1984
101.6	153.6	202.8	0.3967
203.1	250	405.5	0.7935
406.3	500	500	1.5869

Table 17: Data Rate Step Size (assuming a 26 MHz crystal)

13 Receiver Channel Filter Bandwidth

In order to meet different channel width requirements, the receiver channel filter is programmable. The `MDMCFG4.CHANBW_E` and `MDMCFG4.CHANBW_M` configuration registers control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency.

The following formula gives the relation between the register settings and the channel filter bandwidth:

$$BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$$

Table 18 lists the channel filter bandwidths supported by the CC113L.

MDMCFG4. CHANBW_M	MDMCFG4.CHANBW_E			
	00	01	10	11
00	812	406	203	102
01	650	325	162	81
10	541	270	135	68
11	464	232	116	58

Table 18: Channel Filter Bandwidths [kHz] (assuming a 26 MHz crystal)

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel centre tolerance due to crystal inaccuracy should also be subtracted from the channel filter bandwidth. The following example illustrates this:

With the channel filter bandwidth set to 500 kHz, the signal should stay within 80% of 500 kHz, which is 400 kHz. Assuming 915 MHz frequency and ±20 ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is ±40 ppm of 915 MHz, which is ±37 kHz. If the whole transmitted signal bandwidth is to be received within 400 kHz, the transmitted signal bandwidth should be maximum 400 kHz - 2·37 kHz, which is 326 kHz.

By compensating for a frequency offset between the transmitter and the receiver, the filter bandwidth can be reduced and the sensitivity can be improved, see more in DN005 [9] and in Section 14.1.

14 Demodulator, Symbol Synchronizer, and Data Decision

CC113L contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation is performed digitally. To generate the RSSI level (see Section 17.2 for more information), the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

14.1 Frequency Offset Compensation

The CC113L has a very fine frequency resolution (see Table 9). This feature can be used to compensate for frequency offset and drift.

When using 2-FSK, GFSK, or 4-FSK modulation, the demodulator will compensate for the offset between the transmitter and receiver frequency within certain limits, by estimating the centre of the received data. The frequency offset compensation configuration is controlled from the `FOCCFG` register. By compensating for a large frequency offset between the transmitter and the receiver, the sensitivity can be improved, see DN005 [9].

The tracking range of the algorithm is selectable as fractions of the channel bandwidth with the `FOCCFG.FOC_LIMIT` configuration register.

If the `FOCCFG.FOC_BS_CS_GATE` bit is set, the offset compensator will freeze until carrier sense asserts. This may be useful when the radio is in RX for long periods with no traffic, since the algorithm may drift to the boundaries when trying to track noise.

The tracking loop has two gain factors, which affects the settling time and noise sensitivity of the algorithm. `FOCCFG.FOC_PRE_K` sets the gain before the sync word is detected, and `FOCCFG.FOC_POST_K` selects the gain after the sync word has been found.

Note: Frequency offset compensation is not supported for OOK modulation

The estimated frequency offset value is available in the `FREQEST` status register. This can be used for permanent frequency offset compensation. By writing the value from `FREQEST` into `FSCTRL0.FREQOFF`, the frequency synthesizer will automatically be adjusted according to the estimated frequency offset. More details regarding this permanent frequency compensation algorithm can be found in DN015 [6].

14.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in Section 12 on page 25. Re-synchronization is performed continuously to adjust for error in the incoming symbol rate.

14.3 Byte Synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16 bit configurable field (can be repeated to get a 32 bit) that must be inserted at the start of the packet by the transmitter (for example the CC115L, CC110L, or CC1101). The MSB in the sync word must be transmitted first. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word will also function as a system identifier, since only packets with the correct predefined sync word will be received if the sync word detection is enabled in register MDMCFG2 (see Section 17.1). The sync word detector correlates against the user-configured 16 or 32 bit sync word. The correlation threshold can be set to 15/16, 16/16, or 30/32 bits match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is configured through the SYNC1 and SYNC0 registers.

15 Packet Handling Hardware Support

The CC113L has built-in hardware support for packet oriented radio protocols and the packet handler can be configured to implement the following (if enabled):

- Preamble detection
- Sync word detection
- CRC computation and CRC check
- One byte address check
- Packet length check (length byte checked against a programmable maximum length)

Optionally, two status bytes (see Table 19 and Table 20) with RSSI value and CRC status can be appended in the RX FIFO.

Bit	Field Name	Description
7:0	RSSI	RSSI value

Table 19: Received Packet Status Byte 1 (first byte appended after the data)

Bit	Field Name	Description
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	Reserved	

Table 20: Received Packet Status Byte 2 (second byte appended after the data)

Note: Register fields that control the packet handling features should only be altered when CC113L is in the IDLE state.

15.1 Packet Format

The CC113L can be configured to receive packets of different format and the packet should consists of the following items (see Figure 16):

- Preamble
- Synchronization word
- Optional length byte
- Optional address byte
- Payload
- Optional 2 byte CRC

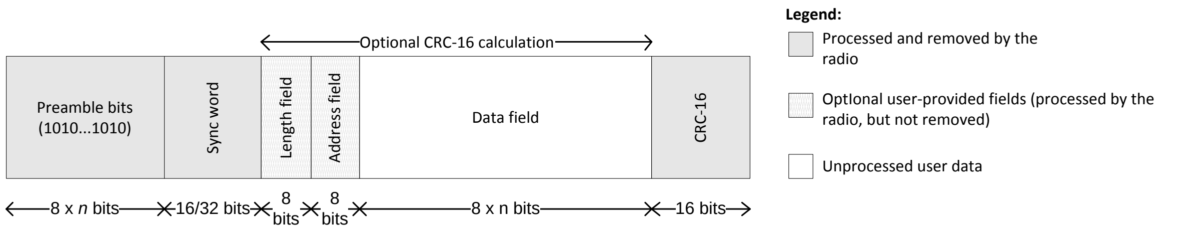


Figure 16: Packet Format

The preamble pattern is an alternating sequence of ones and zeros that the receiver uses for bit synchronisation.

The synchronization word is a two-byte value set in the `SYNC1` and `SYNC0` registers. The sync word provides byte synchronization of the incoming packet. A one-byte sync word can be emulated by setting the `SYNC1` value to the preamble pattern. It is also possible to emulate a 32 bit sync word by setting `MDMCFG2.SYNC_MODE` to 3 or 7. The sync word searched for is the two-byte sync word repeated twice.

CC113L supports both constant packet length protocols and variable length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting `PKTCTRL0.LENGTH_CONFIG=0`. The desired packet length is set by the `PKTLEN` register. This value must be different from 0.

In variable packet length mode, `PKTCTRL0.LENGTH_CONFIG=1`, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional CRC. The `PKTLEN` register is used to set the maximum packet length allowed. Any packet received with a length byte with a value greater than `PKTLEN` will be discarded. The `PKTLEN` value must be different from 0.

With `PKTCTRL0.LENGTH_CONFIG=2`, the packet length is set to infinite and reception will continue until turned off manually. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by **CC113L**.

> **Note:** The minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

15.1.1 Arbitrary Length Field Configuration

The packet length register, `PKTLEN`, can be reprogrammed during RX. In combination with fixed packet length mode (`PKTCTRL0.LENGTH_CONFIG=0`), this opens the possibility to have a different length field configuration than supported for variable length packets (in variable packet length mode the length byte is the first byte after the sync word). At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the `PKTLEN` value is set according to this value. The end of packet will occur when the byte counter in the packet handler is equal to the `PKTLEN` register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

15.1.2 Packet Length > 255

The packet automation control register, `PKTCTRL0`, can be reprogrammed during RX. This opens the possibility to receive packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode (`PKTCTRL0.LENGTH_CONFIG=2`) must be active. When receiving, the MCU reads out enough bytes to interpret the length field in the packet and sets the `PKTLEN` register to mod(length, 256). When less than 256 bytes remains of the packet, the MCU disables infinite packet length mode and activates fixed packet length mode (`PKTCTRL0.LENGTH_CONFIG=0`). When the internal byte counter reaches the `PKTLEN` value, the reception ends (the radio enters the state determined by `RXOFF_MODE)`. Automatic

CRC appending/checking can also be used (by setting PKTCTRL0.CRC_EN=1).

When for example a 600-byte packet is to be received, the MCU should do the following (see also Figure 17)

- Set PKTCTRL0.LENGTH_CONFIG=2.
- Receive enough bytes to interpret the length field
- Program the PKTLEN register to mod(600, 256) = 88.
- Receive at least 345 bytes (600 - 255)
- Set PKTCTRL0.LENGTH_CONFIG=0.
- The reception ends when the packet counter reaches 88. A total of 600 bytes have been received.

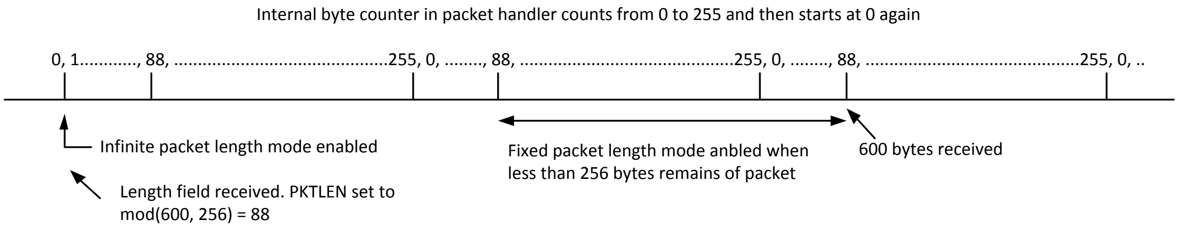


Figure 17: Packet Length > 255

15.2 Packet Filtering

CC113L supports three different types of packet filtering; address filtering, maximum length filtering, and CRC filtering.

15.2.1 Address Filtering

Setting PKTCTRL1.ADR_CHK to any other value than zero enables the packet address filter. The packet handler engine will compare the destination address byte in the packet with the programmed node address in the ADDR register and the 0x00 broadcast address when PKTCTRL1.ADR_CHK=10 or both the 0x00 and 0xFF broadcast addresses when PKTCTRL1.ADR_CHK=11. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

If the received address matches a valid address when using infinite packet length mode and address filtering is enabled, 0xFF will be written into the RX FIFO followed by the address byte and then the payload data.

15.2.2 Maximum Length Filtering

In variable packet length mode, PKTCTRL0.LENGTH_CONFIG=1, the PKTLEN.PACKET_LENGTH register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

15.2.3 CRC Filtering

The filtering of a packet when CRC check fails is enabled by setting PKTCTRL1.CRC_AUTOFLUSH=1. The CRC auto flush function will flush the entire RX FIFO if the CRC check fails. After auto flushing the RX FIFO, the next state depends on the MCSM1.RXOFF_MODE setting.

When using the auto flush function, the maximum packet length is 63 bytes in variable packet length mode and 64 bytes in fixed packet length mode. Note that when PKTCTRL1.APPEND_STATUS is enabled, the maximum allowed packet length is reduced by two bytes in order to make room in the RX FIFO for the two status bytes appended at the end of the packet. Since the entire RX FIFO is flushed when the CRC check fails, the previously received packet must be read out of the RX FIFO before receiving the current packet. The MCU must not read from the current packet until the CRC has been checked as OK.

15.3 Packet Handling

In RX mode, the demodulator and packet handler will search for a valid sync word. When found, the demodulator has obtained both bit and byte synchronization and will receive the first payload byte.

When variable packet length mode is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length mode is used, the packet handler will accept the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

At the end of the payload, the packet handler will optionally write two extra packet status bytes (see Table 19 and Table 20) that contain CRC status, link quality indication, and RSSI value.

15.4 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been received. Additionally, for packets longer than 64 bytes, the RX FIFO needs to be read while in RX mode. This means that the MCU needs to know the number of bytes that can be read from the RX FIFO. There are two possible solutions to get the necessary status information:

a) Interrupt Driven Solution

The GDO pins can be used to give an interrupt when a sync word has been received or when a complete packet has been received by setting `IOCFGx.GDOx_CFG=0x06`. In addition, there are two configurations for the `IOCFGx.GDOx_CFG` register that can be used as an interrupt source to provide information on how many bytes that are in the RX FIFO (`IOCFGx.GDOx_CFG=0x00` and `IOCFGx.GDOx_CFG=0x01`). See Table 29 for more information.

b) SPI Polling

The `PKTSTATUS` register can be polled at a given rate to get information about the current GDO2 and GDO0 values respectively. The `RXBYTES` register can be polled at a given rate to get information about the number of bytes in the RX FIFO. Alternatively, the number of bytes in the RX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

It is recommended to employ an interrupt driven solution since high rate SPI polling reduces the RX sensitivity. Furthermore, as explained in Section 10.3 and the CC113L Errata Notes [3], when using SPI polling, there is a small, but finite, probability that a single read from registers `PKTSTATUS`, and `RXBYTES` is being corrupt. The same is the case when reading the chip status byte.

16 Modulation Formats

CC113L supports amplitude, frequency, and phase shift modulation formats. The desired modulation format is set in the `MDMCFG2.MOD_FORMAT` register.

Optionally, if the data has been Manchester coded on the transmitter side it can be decoded by the demodulator. This option is enabled by setting `MDMCFG2.MANCHESTER_EN=1`.

Note: Manchester encoding is not supported at the same time as using 4-FSK modulation

16.1 Frequency Shift Keying

CC113L supports 2-(G)FSK and 4-FSK modulation. When selecting 4-FSK, the preamble and sync word to be received needs to be 2-FSK (see Figure 13).

When 2-FSK/GFSK/4-FSK modulation is used, the `DEVIATN` register specifies the expected frequency deviation of incoming signals in RX and should be the same as the deviation of the transmitted signal for demodulation to be performed reliably and robustly.

The frequency deviation is programmed with the DEVIATION_M and DEVIATION_E values in the DEVIATN register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$$

The symbol encoding is shown in Table 21.

Format	Symbol	Coding
2-FSK/GFSK	'0'	– Deviation
	'1'	+ Deviation
4-FSK	'01'	– Deviation
	'00'	– 1/3·Deviation
	'10'	+1/3·Deviation
	'11'	+ Deviation

Table 21: Symbol Encoding for 2-FSK/GFSK and 4-FSK Modulation

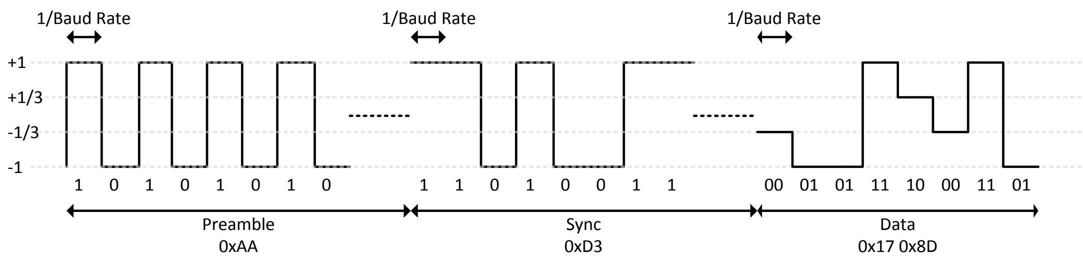


Figure 18: Data Sent Over the Air (MDMCFG2.MOD_FORMAT=100)

16.2 Amplitude Modulation

The amplitude modulation supported by ***CC113L*** is On-Off Keying (OOK).

When using OOK, the AGC settings from the SmartRF Studio [4] preferred FSK settings are not optimum. DN022 [8] gives guidelines on how to find optimum OOK settings from the preferred settings in SmartRF Studio [4]. The DEVIATN register setting has no effect when using OOK.

17 Received Signal Qualifiers and RSSI

CC113L has several qualifiers that can be used to increase the likelihood that a valid sync word is detected:

- Sync Word Qualifier
- RSSI
- Carrier Sense

17.1 Sync Word Qualifier

If sync word detection is enabled in the MDMCFG2 register, the ***CC113L*** will not start filling the RX FIFO and perform the packet filtering described in Section 15.2 before a valid sync word has been detected. The sync word qualifier mode is set by MDMCFG2.SYNC_MODE and is summarized in Table 22. Carrier sense in Table 22 is described in Section 17.3.

MDMCFG2. SYNC_MODE	Sync Word Qualifier Mode
000	No preamble/sync
001	15/16 sync word bits detected
010	16/16 sync word bits detected
011	30/32 sync word bits detected
100	No preamble/sync + carrier sense above threshold
101	15/16 + carrier sense above threshold
110	16/16 + carrier sense above threshold
111	30/32 + carrier sense above threshold

Table 22: Sync Word Qualifier Mode

17.2 RSSI

The RSSI value is an estimate of the signal power level in the chosen channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the RSSI status register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters the RX state.

> **Note**: It takes some time from the radio enters RX mode until a valid RSSI value is present in the RSSI register. Please see DN505 [7] for details on how the RSSI response time can be estimated.

The RSSI value is given in dBm with a ½ dB resolution. The RSSI update rate, f_{RSSI}, depends on the receiver filter bandwidth ($BW_{channel}$ is defined in Section 13) and AGCCTRL0.FILTER_LENGTH.

$$f_{RSSI} = \frac{2 \cdot BW_{channel}}{8 \cdot 2^{FILTER\_LENGTH}}$$

If PKTCTRL1.APPEND_STATUS is enabled, the last RSSI value of the packet is automatically added to the first byte appended after the payload.

The RSSI value read from the RSSI status register is a 2's complement number. The following procedure can be used to convert the RSSI reading to an absolute power level (RSSI_dBm)

1) Read the RSSI status register
2) Convert the reading from a hexadecimal number to a decimal number (RSSI_dec)
3) If RSSI_dec ≥ 128 then RSSI_dBm = (RSSI_dec - 256)/2 – RSSI_offset
4) Else if RSSI_dec < 128 then RSSI_dBm = (RSSI_dec)/2 – RSSI_offset

Table 23 gives typical values for the RSSI_offset. Figure 19 and Figure 20 show typical plots of RSSI readings as a function of input power level for different data rates.

Data rate [kBaud]	RSSI_offset [dB], 433 MHz	RSSI_offset [dB], 868 MHz
1.2	74	74
38.4	74	74
250	74	74
500	74	74

Table 23: Typical RSSI_offset Values

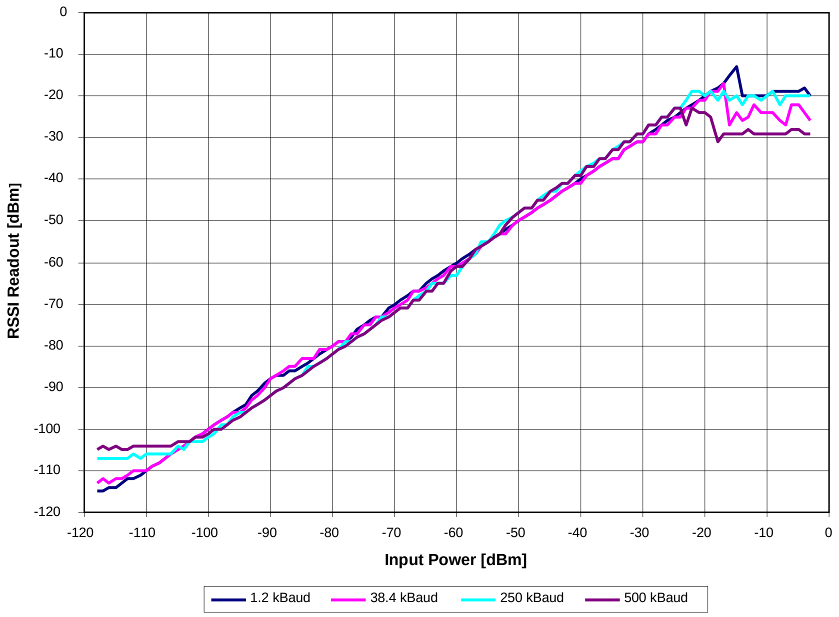


Figure 19: Typical RSSI Value vs. Input Power Level for Different Data Rates at 433 MHz

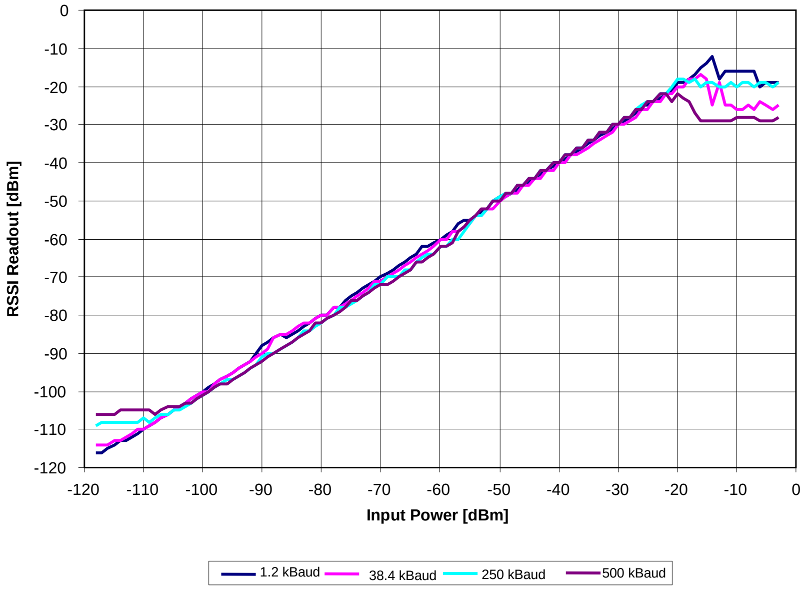


Figure 20: Typical RSSI Value vs. Input Power Level for Different Data Rates at 868 MHz

17.3 Carrier Sense (CS)

Carrier sense (CS) is used as a sync word qualifier and can be asserted based on two conditions which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold, and de-asserted when RSSI is below the same threshold (with hysteresis). See more in Section 17.3.1.
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next, and de-asserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with time varying noise floor. See more in Section 17.3.2.

Carrier sense can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed and is set by setting `MDMCFG2` . The carrier sense signal can be observed on one of the GDO pins by setting `IOCFGx.GDOx_CFG=14` and in the status register bit `PKTSTATUS.CS`.

17.3.1 CS Absolute Threshold

The absolute threshold related to the RSSI value depends on the following register fields:

- `AGCCTRL2.MAX_LNA_GAIN`
- `AGCCTRL2.MAX_DVGA_GAIN`
- `AGCCTRL1.CARRIER_SENSE_ABS_THR`
- `AGCCTRL2.MAGN_TARGET`

For given `AGCCTRL2.MAX_LNA_GAIN` and `AGCCTRL2.MAX_DVGA_GAIN` settings, the absolute threshold can be adjusted ±7 dB in steps of 1 dB using `CARRIER_SENSE_ABS_THR`.

The `MAGN_TARGET` setting is a compromise between blocker tolerance/selectivity and sensitivity. The value sets the desired signal level in the channel into the demodulator. Increasing this value reduces the headroom for blockers, and therefore close-in selectivity. It is strongly recommended to use SmartRF Studio [4] to generate the correct `MAGN_TARGET` setting. Table 24 and Table 25 show the typical RSSI readout values at the CS threshold at 2.4 kBaud and 250 kBaud data rate respectively. The default reset value for `CARRIER_SENSE_ABS_THR` = 0 (0 dB) has been used. `MAGN_TARGET` = 3 (33 dB) and 7 (42 dB) have been used for 2.4 kBaud and 250 kBaud data rate respectively. For other data rates, the user must generate similar tables to find the CS absolute threshold.

		MAX_DVGA_GAIN[1:0]			
		00	01	10	11
MAX_LNA_GAIN[2:0]	000	−97.5	−91.5	−85.5	−79.5
	001	−94	−88	−82.5	−76
	010	−90.5	−84.5	−78.5	−72.5
	011	−88	−82.5	−76.5	−70.5
	100	−85.5	−80	−73.5	−68
	101	−84	−78	−72	−66
	110	−82	−76	−70	−64
	111	−79	−73.5	−67	−61

Table 24: Typical RSSI Value in dBm at CS Threshold with `MAGN_TARGET` = 3 (33 dB) at 2.4 kBaud, 868 MHz

		MAX_DVGA_GAIN[1:0]			
		00	01	10	11
MAX_LNA_GAIN[2:0]	000	−90.5	−84.5	−78.5	−72.5
	001	−88	−82	−76	−70
	010	−84.5	−78.5	−72	−66
	011	−82.5	−76.5	−70	−64
	100	−80.5	−74.5	−68	−62
	101	−78	−72	−66	−60
	110	−76.5	−70	−64	−58
	111	−74.5	−68	−62	−56

Table 25: Typical RSSI Value in dBm at CS Threshold with `MAGN_TARGET` = 7 (42 dB) at 250 kBaud, 868 MHz

If the threshold is set high, i.e. only strong signals are wanted, the threshold should be adjusted upwards by first reducing the MAX_LNA_GAIN value and then the MAX_DVGA_GAIN value. This will reduce power consumption in the receiver front end, since the highest gain settings are avoided.

17.3.2 CS Relative Threshold

The relative threshold detects sudden changes in the measured signal level. This setting does not depend on the absolute signal level and is thus useful to detect signals in environments with a time varying noise floor. The register field `AGCCTRL1.CARRIER_SENSE_REL_THR` is used to enable/disable relative CS, and to select threshold of 6 dB, 10 dB, or 14 dB RSSI change.

18 Radio Control

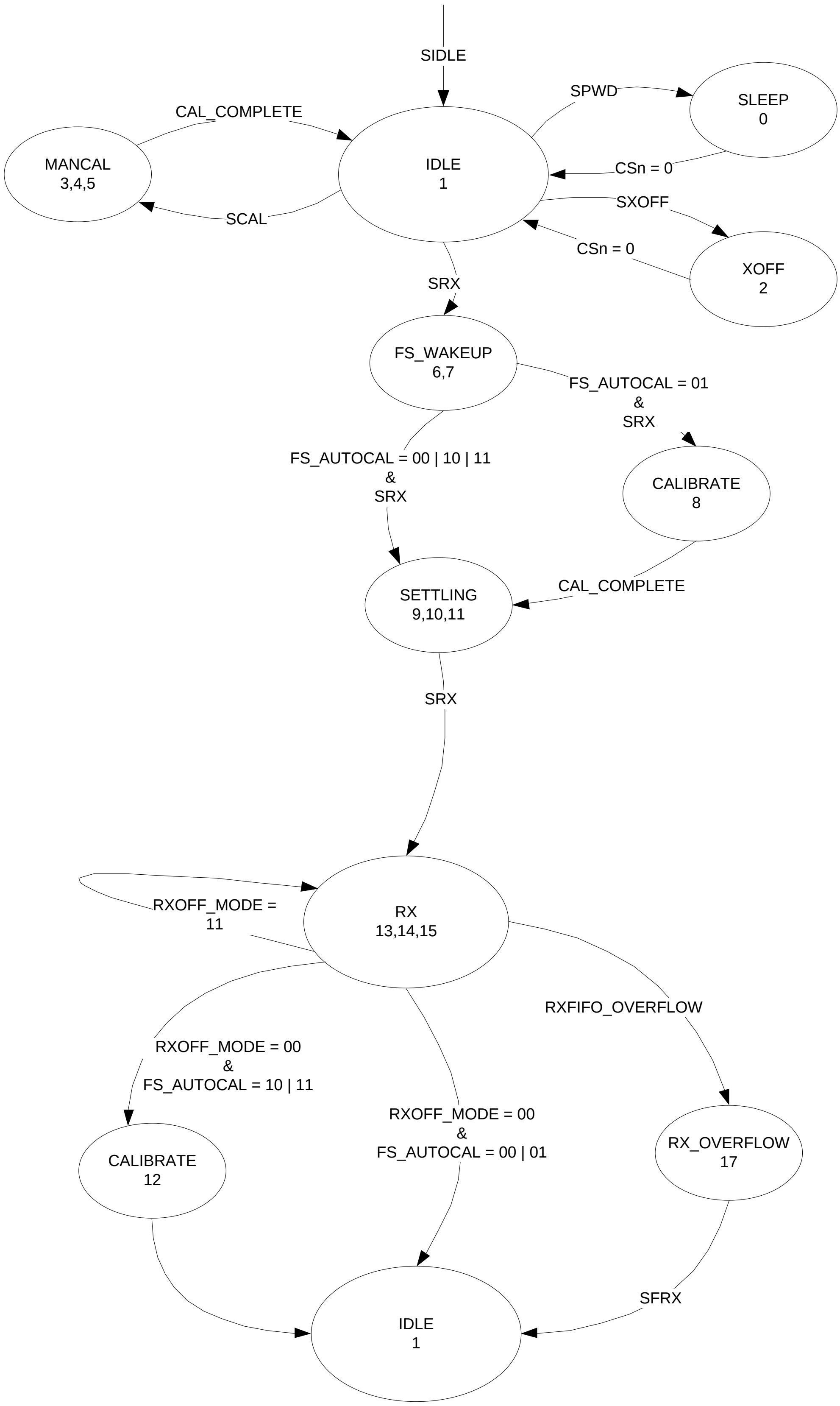


Figure 21: Complete Radio Control State Diagram

CC113L has a built-in state machine that is used to switch between different operational states (modes). The change of state is done either by using command strobes or by internal events such as RX FIFO overflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 12 on page 20. The complete radio control state diagram is shown in Figure 21. The numbers refer to the state number readable in the `MARCSTATE` status register. This register is primarily for test purposes.

18.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, i.e. automatic power-on reset (POR) or manual reset. After the automatic power-on reset or manual reset, it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK_XOSC/192. However, to optimize performance in RX, an alternative GDO setting from the settings found in Table 29 on page 42 should be selected.

18.1.1 Automatic POR

A power-on reset circuit is included in the **CC113L**. The minimum requirements stated in Table 11 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when `CHIP_RDYn` goes low. `CHIP_RDYn` is observed on the SO pin after CSn is pulled low. See Section 10.1 for more details on `CHIP_RDYn`.

When the **CC113L** reset is completed, the chip will be in the IDLE state and the crystal oscillator will be running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed, the SO pin will first go high, indicating that the crystal oscillator is not stabilized, before going low as shown in Figure 22.

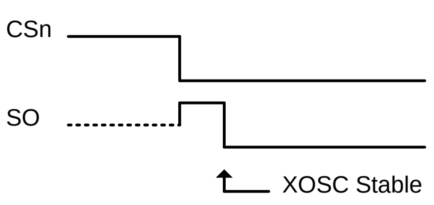


Figure 22: Power-On Reset

18.1.2 Manual Reset

The other global reset possibility on **CC113L** uses the `SRES` command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see Figure 23):

- Set SCLK = 1 and SI = 0.
- Strobe CSn low / high.
- Hold CSn low and then high for at least 40 µs relative to pulling CSn low
- Pull CSn low and wait for SO to go low (`CHIP_RDYn`).
- Issue the `SRES` strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

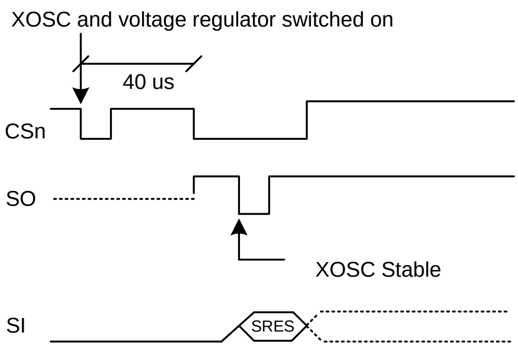


Figure 23: Power-On Reset with `SRES`

> Note that the above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the **CC113L** after this, it is only necessary to issue an `SRES` command strobe.

18.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if MCSM0.XOSC_FORCE_ON is set.

In the automatic mode, the XOSC will be turned off if the SXOFF or SPWD command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from the IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used as described in Section 10.1 on page 22.

If the XOSC is forced on, the crystal will always stay on even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in Section 4.3 on page 12.

18.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a SPWD command strobe has been sent on the SPI interface. The chip is then in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

18.4 Receive Mode (RX)

Receive mode is activated directly by the MCU by using the SRX command strobe.

The frequency synthesizer must be calibrated regularly. CC113L has one manual calibration option (using the SCAL strobe), and three automatic calibration options that are controlled by the MCSM0.FS_AUTOCAL setting:

- Calibrate when going from IDLE to RX
- Calibrate when going from RX to IDLE automatically[1]
- Calibrate every fourth time when going from RX to IDLE automatically[1]

If the radio goes from RX to IDLE by issuing an SIDLE strobe, calibration will not be performed. The calibration takes a constant number of XOSC cycles; see Table 26 for timing details regarding calibration.

When RX is activated, the chip will remain in receive mode until a packet is successfully received or until RX mode terminated due to lack of carrier sense (see Section 18.5). The probability that a false sync word is detected can be reduced by using CS together with maximum sync word length as described in Section 17. After a packet is successfully received, the radio controller goes to the state indicated by the MCSM1.RXOFF_MODE setting. The possible destinations are:

- IDLE
- RX: Start search for a new packet

Note: When MCSM1.RXOFF_MODE=11 and a packet has been received, it will take some time before a valid RSSI value is present in the RSSI register again even if the radio has never exited RX mode. This time is the same as the RSSI response time discussed in DN505 [7].

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state.

18.5 RX Termination

If the system expects the transmission to have started when entering RX mode, the MCSM2.RX_TIME_RSSI function can be used. The radio controller will then terminate RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold). See Section 17.3 on page 33 for details on Carrier Sense.

For OOK modulation, lack of carrier sense is only considered valid after eight symbol periods. Thus, the MCSM2.RX_TIME_RSSI function can be used in OOK mode when the distance between two “1” symbols is eight or less.

If RX terminates due to no carrier sense when the MCSM2.RX_TIME_RSSI function is used, the radio will always go back to IDLE,

[1] Not forced in IDLE by issuing an SIDLE strobe

regardless of the MCSM1.RXOFF_MODE setting.

18.6 Timing

18.6.1 Overall State Transition Times

The main radio controller needs to wait in certain states in order to make sure that the internal analog/digital parts have settled down and are ready to operate in the new states. A number of factors are important for the state transition times:

- The crystal oscillator frequency, f_{xosc}
- The value of the TEST0, TEST1, and FSCAL3 registers

Table 26 shows timing in crystal clock cycles for key state transitions.

Description	Transition Time	Transition Time [µs]
IDLE to RX, no calibration	$1953/f_{xosc}$	75.1
IDLE to RX, with calibration	$1953/f_{xosc}$ + FS calibration Time	799
RX to IDLE, no calibration	$2/f_{xosc}$	~0.1
RX to IDLE, with calibration	$2/f_{xosc}$ + FS calibration Time	724
Manual calibration	$283/f_{xosc}$ + FS calibration Time	735

Table 26: Overall State Transition Times (Example for 26 MHz crystal oscillator, 250 kBaud data rate, and TEST0 = 0x0B (maximum calibration time)).

18.6.2 Frequency Synthesizer Calibration Time

Table 27 summarizes the frequency synthesizer (FS) calibration times for possible settings of TEST0 and FSCAL3.CHP_CURR_CAL_EN. Setting FSCAL3.CHP_CURR_CAL_EN to 00_b disables the charge pump calibration stage. TEST0 is set to the values recommended by SmartRF Studio software [4]. The possible values for TEST0 when operating with different frequency bands are 0x09 and 0x0B. The SmartRF Studio software [4] always sets FSCAL3.CHP_CURR_CAL_EN to 10_b.

The calibration time can be reduced from 712/724 µs to 145/157 µs. See Section 25.2 on page 44 for more details.

TEST0	FSCAL3.CHP_CURR_CAL_EN	FS Calibration Time f_{xosc} = 26 MHz	FS Calibration Time f_{xosc} = 27 MHz
0x09	00_b	$3764/f_{xosc}$ = 145 us	$3764/f_{xosc}$ = 139 us
0x09	10_b	$18506/f_{xosc}$ = 712 us	$18506/f_{xosc}$ = 685 us
0x0B	00_b	$4073/f_{xosc}$ = 157 us	$4073/f_{xosc}$ = 151 us
0x0B	10_b	$18815/f_{xosc}$ = 724 us	$18815/f_{xosc}$ = 697 us

Table 27. Frequency Synthesizer Calibration Times (26/27 MHz crystal)

19 RX FIFO

The CC113L contains a 64-byte RX FIFO for received data and the SPI interface is used to read the RX FIFO (see Section 10.5 for more details). The FIFO controller will detect overflow in the RX FIFO.

When reading the RX FIFO the MCU must avoid reading it past its empty value since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

The chip status byte that is available on the SO pin while transferring the SPI header contains the fill grade of the RX FIFO (R/$\overline{W}$ = 1). Section 10.1 on page 22 contains more details on this.

The number of bytes in the RX FIFO can also be read from the status register RXBYTES.NUM_RXBYTES. If a received data byte is written to the RX FIFO at the exact same time as the last byte in the RX FIFO is read over the SPI interface, the RX FIFO pointer is not properly updated and the last read byte will be duplicated. To avoid this problem, the RX FIFO should never be emptied before the last byte of the packet is received.

For packet lengths less than 64 bytes it is recommended to wait until the complete packet has been received before reading it out of the RX FIFO.

If the packet length is larger than 64 bytes, the MCU must determine how many bytes can be read from the RX FIFO (RXBYTES.NUM_RXBYTES-1). The following software routine can be used:

1. Read RXBYTES.NUM_RXBYTES repeatedly at a rate specified to be at least twice that of which RF bytes are received until the same value is returned twice; store value in *n*.
2. If *n* < # of bytes remaining in packet, read *n*-1 bytes from the RX FIFO.
3. Repeat steps 1 and 2 until *n* = # of bytes remaining in packet.
4. Read the remaining bytes from the RX FIFO.

The 4-bit FIFOTHR.FIFO_THR setting is used to program threshold points in the FIFOs.

Table 28 lists the 16 FIFO_THR settings and the corresponding thresholds for the RX FIFO.

FIFO_THR	**Bytes in RX FIFO**
0 (0000)	4
1 (0001)	8
2 (0010)	12
3 (0011)	16
4 (0100)	20
5 (0101)	24
6 (0110)	28
7 (0111)	32
8 (1000)	36
9 (1001)	40
10 (1010)	44
11 (1011)	48
12 (1100)	52
13 (1101)	56
14 (1110)	60
15 (1111)	64

Table 28: FIFO_THR Settings and the Corresponding RX FIFO Thresholds

A signal will assert when the number of bytes in the RX FIFO is equal to or higher than the programmed threshold. This signal can be viewed on the GDO pins (see Table 29 on page 42).

Figure 24 shows the number of bytes in the RX FIFO when the threshold signal toggles in the case of FIFO_THR=13. Figure 25 shows the signal on the GDO pin as the RX FIFO is filled above the threshold, and then drained below in the case of FIFO_THR=13.

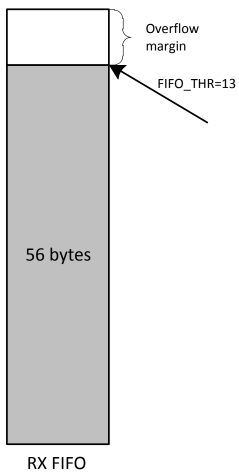


Figure 24: Example of RX FIFO at Threshold

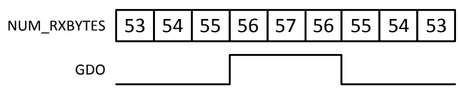


Figure 25: Number of Bytes in RX FIFO vs. the GDO Signal (GDOx_CFG=0x00 and FIFO_THR=13)

20 Frequency Programming

The frequency programming in CC113L is designed to minimize the programming needed when changing frequency.

To set up a system with channel numbers, the desired channel spacing is programmed with the MDMCFG0.CHANSPC_M and MDMCFG1.CHANSPC_E registers. The channel spacing registers are mantissa and exponent respectively. The base or start frequency is set by the 24 bit frequency word located in the FREQ2, FREQ1, and FREQ0 registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, CHANNR.CHAN, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot (FREQ + CHAN \cdot ((256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E-2}))$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get e.g. 1 MHz channel spacing, one solution is to use 333 kHz channel spacing and select each third channel in CHANNR.CHAN.

The preferred IF frequency is programmed with the FSCTRL1.FREQ_IF register. The IF frequency is given by:

$$f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$$

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency should only be updated when the radio is in the IDLE state

21 VCO

The VCO is completely integrated on-chip.

21.1 VCO and PLL Self-Calibration

The VCO characteristics vary with temperature and supply voltage changes as well as the desired operating frequency. In order to ensure reliable operation, CC113L includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 26 on page 38.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the MCSM0.FS_AUTOCAL register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

Note: The calibration values are maintained in SLEEP mode, so the calibration is still valid after waking up from SLEEP mode unless supply voltage or temperature has changed significantly.

To check that the PLL is in lock, the user can program register IOCFGx.GDOx_CFG to 0x0A, and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1, or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F. Refer also to the CC113L Errata Notes [3].

For more robust operation, the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

22 Voltage Regulators

CC113L contains several on-chip linear voltage regulators that generate the supply voltages needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 1 and Table 12 are not exceeded.

By setting the CSn pin low, the voltage regulator to the digital core turns on and the crystal oscillator starts. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in Table 15).

If the chip is programmed to enter power-down mode (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator for the digital core requires one external decoupling capacitor.

The voltage regulator output should only be used for driving the C113L.

23 General Purpose / Test Output Control Pins

The three digital output pins GDO0, GDO1, and GDO2 are general control pins configured with IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO2_CFG respectively. Table 29 shows the different signals that can be monitored on the GDO pins. These signals can be used as inputs to the MCU.

GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. The default value for GDO1 is 3-stated which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 135 - 141 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to IOCFG0.GDO0_CFG.

If the IOCFGx.GDOx_CFG setting is less than 0x20 and IOCFGx_GDOx_INV is 0 (1), the GDO0 and GDO2 pins will be hardwired to 0 (1), and the GDO1 pin will be hardwired to 1 (0) in the SLEEP state. These signals will be hardwired until the CHIP_RDYn signal goes low.

If the IOCFGx.GDOx_CFG setting is 0x20 or higher, the GDO pins will work as programmed also in SLEEP state. As an example, GDO1 is high impedance in all states if IOCFG1.GDO1_CFG=0x2E.

<table>
<tr><th>GDOx_CFG[5:0]</th><th colspan="2">Description</th></tr>
<tr><td>0 (0x00)</td><td colspan="2">Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold. De-asserts when RX FIFO is drained below the same threshold.</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold or the end of packet is reached. De-asserts when the RX FIFO is empty.</td></tr>
<tr><td>2 (0x02) - 3 (0x03)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">Asserts when the RX FIFO has overflowed. De-asserts when the FIFO has been flushed.</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">Asserts when sync word has been received, and de-asserts at the end of the packet. The pin will also de-assert when a packet is discarded due to address or maximum length filtering or when the radio enters RXFIFO_OVERFLOW state.</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">Asserts when a packet has been received with CRC OK. De-asserts when the first byte is read from the RX FIFO.</td></tr>
<tr><td>8 (0x08) - 9 (0x09)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>10 (0x0A)</td><td colspan="2">Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.</td></tr>
<tr><td>11 (0x0B)</td><td colspan="2">Serial Clock. Synchronous to the data in synchronous serial mode.
Data is set up on the falling edge by CC113L when GDOx_INV=0.</td></tr>
<tr><td>12 (0x0C)</td><td colspan="2">Serial Synchronous Data Output. Used for synchronous serial mode.</td></tr>
<tr><td>13 (0x0D)</td><td colspan="2">Serial Data Output. Used for asynchronous serial mode.</td></tr>
<tr><td>14 (0x0E)</td><td colspan="2">Carrier sense. High if RSSI level is above threshold. Cleared when entering IDLE mode.</td></tr>
<tr><td>15 (0x0F)</td><td colspan="2">CRC_OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.</td></tr>
<tr><td>16 (0x10) - 27 (0x1B)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>28 (0x1C)</td><td colspan="2">LNA_PD. Note: LNA_PD will have the same signal level in SLEEP and RX states. To control an external LNA in applications where the SLEEP state is used it is recommended to use GDOx_CFGx=0x2F instead.</td></tr>
<tr><td>29 (0x1D) – 38 (0x26)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>39 (0x27)</td><td colspan="2">CLK_32k.</td></tr>
<tr><td>40 (0x28)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>41 (0x29)</td><td colspan="2">CHIP_RDYn.</td></tr>
<tr><td>42 (0x2A)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>43 (0x2B)</td><td colspan="2">XOSC_STABLE.</td></tr>
<tr><td>44 (0x2C) – 45 (0x2D)</td><td colspan="2">Reserved - used for test.</td></tr>
<tr><td>46 (0x2E)</td><td colspan="2">High impedance (3-state).</td></tr>
<tr><td>47 (0x2F)</td><td colspan="2">HW to 0 (HW1 achieved by setting GDOx_INV=1). Can be used to control an external LNA</td></tr>
<tr><td>48 (0x30)</td><td>CLK_XOSC/1</td><td rowspan="16">Note: There are 3 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK_XOSC/192.

To optimize RF performance, these signals should not be used while the radio is in RX mode.</td></tr>
<tr><td>49 (0x31)</td><td>CLK_XOSC/1.5</td></tr>
<tr><td>50 (0x32)</td><td>CLK_XOSC/2</td></tr>
<tr><td>51 (0x33)</td><td>CLK_XOSC/3</td></tr>
<tr><td>52 (0x34)</td><td>CLK_XOSC/4</td></tr>
<tr><td>53 (0x35)</td><td>CLK_XOSC/6</td></tr>
<tr><td>54 (0x36)</td><td>CLK_XOSC/8</td></tr>
<tr><td>55 (0x37)</td><td>CLK_XOSC/12</td></tr>
<tr><td>56 (0x38)</td><td>CLK_XOSC/16</td></tr>
<tr><td>57 (0x39)</td><td>CLK_XOSC/24</td></tr>
<tr><td>58 (0x3A)</td><td>CLK_XOSC/32</td></tr>
<tr><td>59 (0x3B)</td><td>CLK_XOSC/48</td></tr>
<tr><td>60 (0x3C)</td><td>CLK_XOSC/64</td></tr>
<tr><td>61 (0x3D)</td><td>CLK_XOSC/96</td></tr>
<tr><td>62 (0x3E)</td><td>CLK_XOSC/128</td></tr>
<tr><td>63 (0x3F)</td><td>CLK_XOSC/192</td></tr>
</table>

Table 29: GDOx Signal Selection (x = 0, 1, or 2)

24 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the CC113L to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller, and simplify software development.

24.1 Asynchronous Serial Operation

Asynchronous transfer is included in the CC113L for backward compatibility with systems that are already using the asynchronous data transfer.

When asynchronous transfer is enabled, all packet handling support is disabled and it is not possible to use Manchester encoding.

Asynchronous serial mode is enabled by setting PKTCTRL0.PKT_FORMAT to 3. Data output can be on GDO0, GDO1, or GDO2. This is set by the IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG and IOCFG2.GDO2_CFG fields.

In asynchronous serial mode no data decision is done on-chip and the raw data is put on the data output line. When using asynchronous serial mode make sure the interfacing MCU does proper oversampling and that it can handle the jitter on the data output line. The MCU should tolerate a jitter of ±1/8 of a bit period as the data stream is time-discrete using 8 samples per bit.

In asynchronous serial mode there will be glitches of 37 - 38.5 ns duration (1/XOSC) occurring infrequently and with random periods. A simple RC filter can be added to the data output line between CC113L and the MCU to get rid of the 37 - 38.5 ns glitches if considered a problem. The filter 3 dB cut-off frequency needs to be high enough so that the data is not filtered and at the same time low enough to remove the glitch. As an example, for 2.4 kBaud data rate a 1 kΩ resistor and 2.7 nF capacitor can be used. This gives a 3 dB cut-off frequency of 59 kHz.

24.2 Synchronous Serial Operation

Setting PKTCTRL0.PKT_FORMAT to 1 enables synchronous serial mode. When using this mode, sync detection should be disabled together with CRC calculation (MDMCFG2.SYNC_MODE=000 and PKTCTRL0.CRC_EN=0). Infinite packet length mode should be used (PKTCTRL0.LENGTH_CONFIG=10_b).

In synchronous serial mode, data is transferred on a two-wire serial interface. The CC113L provides a clock that is used to sample data on the data output line. The data output pin can be any of the GDO pins. This is set by the IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO2_CFG fields. The RX latency is 9 bits.

The MCU must handle preamble and sync word detection in software, together with CRC calculation.

25 System Considerations and Guidelines

25.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. Short Range Devices (SRDs) for license free operation below 1 GHz are usually operated in the 315 MHz, 433 MHz, 868 MHz or 915 MHz frequency bands. The CC113L is specifically designed for such use with its 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz operating ranges. The most important regulations when using the CC113L in the 315 MHz, 433 MHz, 868 MHz, or 915 MHz frequency bands are EN 300 220 V2.3.1 (Europe) and FCC CFR47 part 15 (USA).

For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.

Please note that compliance with regulations is dependent on the complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

25.2 Calibration in Multi-Channel Systems

CC115L is highly suited for multi-channel systems due to its agile frequency synthesizer and effective communication interface.

Charge pump current, VCO current, and VCO capacitance array calibration data is required for each frequency when implementing a multi-channel system. There are 3 ways of obtaining the calibration data from the chip:

1) Calibration for every frequency change. The PLL calibration time is 712/724 µs (26 MHz crystal and `TEST0 =` 0x09/0B, see Table 27). The blanking interval between each frequency is then 787/799 µs.

2) Perform all necessary calibration at startup and store the resulting `FSCAL3`, `FSCAL2`, and `FSCAL1` register values in MCU memory. The VCO capacitance calibration `FSCAL1` register value must be found for each RF frequency to be used. The VCO current calibration value and the charge pump current calibration value available in `FSCAL2` and `FSCAL3` respectively are not dependent on the RF frequency, so the same value can therefore be used for all RF frequencies for these two registers. Between each frequency change, the calibration process can then be replaced by writing the `FSCAL3`, `FSCAL2` and `FSCAL1` register values that corresponds to the next RF frequency. The PLL turn on time is approximately 75 µs (Table 26). The blanking interval between each frequency hop is then approximately 75 µs.

3) Run calibration on a single frequency at startup. Next write 0 to `FSCAL3[5:4]` to disable the charge pump calibration. After writing to `FSCAL3[5:4]`, strobe `SRX` with `MCSM0.FS_AUTOCAL=1` for each new frequency. That is, VCO current and VCO capacitance calibration is done, but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from 712/724 µs to 145/157 µs (26 MHz crystal and `TEST0 =` 0x09/0B, see Table 27). The blanking interval between each frequency hop is then 220/232 µs.

There is a trade-off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. This solution also requires that the supply voltage and temperature do not vary much in order to have a robust solution. Solution 3) gives 567 µs smaller blanking interval than solution 1).

The recommended settings for `TEST0.VCO_SEL_CAL_EN` change with frequency. This means that one should always use SmartRF Studio [4] to get the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is being used.

Note: The content in the `TEST0` register is not retained in SLEEP state, thus it is necessary to re-write this register when returning from the SLEEP state.

26 Configuration Registers

The configuration of CC113L is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF Studio software [4]. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 8 command strobe registers, listed in Table 30. Accessing these registers will initiate the change of an internal state or mode. There are 43 normal 8-bit configuration registers listed in Table 31, and SmartRF Studio [4] will provide recommended settings for these registers[2].

There are also 8 status registers that are listed in Table 32. These registers, which are read-only, contain information about the status of CC113L.

The RX FIFO is accessed through one 8-bit register. During the header byte transfer and while writing data to a register, a status byte is returned on the SO line. This status byte is described in Table 16 on page 23.

Table 33 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

[2] Addresses marked as "Not Used" can be part of a burst access and one can write a dummy value to them. Addresses marked as "Reserved" must be configured according to SmartRF Studio

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	Reserved	
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode (MCSM0.FS_AUTOCAL=0)
0x34	SRX	In IDLE state: Enable RX. Perform calibration first if MCSM0.FS_AUTOCAL=1.
0x35	Reserved	
0x36	SIDLE	Enter IDLE state
0x37 - 0x38	Reserved	
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B - 0x3C	Reserved	
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Table 30: Command Strobes

Address	Register	Description	Preserved in SLEEP State	Details on Page Number
0x00	IOCFG2	GDO2 output pin configuration	Yes	49
0x01	IOCFG1	GDO1 output pin configuration	Yes	49
0x02	IOCFG0	GDO0 output pin configuration	Yes	49
0x03	FIFOTHR	RX FIFO threshold	Yes	50
0x04	SYNC1	Sync word, high byte	Yes	51
0x05	SYNC0	Sync word, low byte	Yes	51
0x06	PKTLEN	Packet length	Yes	51
0x07	PKTCTRL1	Packet automation control	Yes	51
0x08	PKTCTRL0	Packet automation control	Yes	52
0x09	ADDR	Device address	Yes	52
0x0A	CHANNR	Channel number	Yes	52
0x0B	FSCTRL1	Frequency synthesizer control	Yes	52
0x0C	FSCTRL0	Frequency synthesizer control	Yes	53
0x0D	FREQ2	Frequency control word, high byte	Yes	53
0x0E	FREQ1	Frequency control word, middle byte	Yes	53
0x0F	FREQ0	Frequency control word, low byte	Yes	53
0x10	MDMCFG4	Modem configuration	Yes	53
0x11	MDMCFG3	Modem configuration	Yes	53
0x12	MDMCFG2	Modem configuration	Yes	54
0x13	MDMCFG1	Modem configuration	Yes	55
0x14	MDMCFG0	Modem configuration	Yes	55
0x15	DEVIATN	Modem deviation setting	Yes	55
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	55
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	55
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	56
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	57
0x1A	BSCFG	Bit Synchronization configuration	Yes	58
0x1B	AGCTRL2	AGC control	Yes	59
0x1C	AGCTRL1	AGC control	Yes	60
0x1D	AGCTRL0	AGC control	Yes	61
0x1E - 0x1F	Not Used			
0x20	RESERVED		Yes	61
0x21	FREND1	Front end RX configuration	Yes	62
0x22	Not Used			
0x23	FSCAL3	Frequency synthesizer calibration	Yes	62
0x24	FSCAL2	Frequency synthesizer calibration	Yes	62
0x25	FSCAL1	Frequency synthesizer calibration	Yes	62
0x26	FSCAL0	Frequency synthesizer calibration	Yes	62
0x27 - 0x28	Not Used			
0x29 - 0x2B	RESERVED		No	63
0x2C	TEST2	Various test settings	No	63
0x2D	TEST1	Various test settings	No	63
0x2E	TEST0	Various test settings	No	63

Table 31: Configuration Registers Overview

Address	Register	Description	Details on page number
0x30 (0xF0)	PARTNUM	Part number for CC113L	64
0x31 (0xF1)	VERSION	Current version number	64
0x32 (0xF2)	FREQEST	Frequency Offset Estimate	64
0x33 (0xF3)	CRC_REG	CRC OK	64
0x34 (0xF4)	RSSI	Received signal strength indication	64
0x35 (0xF5)	MARCSTATE	Control state machine state	65
0x36 - 0x37 (0xF6 - 0xF7)	Reserved		
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	66
0x39 - 0x3A (0xF9 - 0xFA)	Reserved		
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	66
0x3C - 0x3D (0xFC - 0xFD)	Reserved		

Table 32: Status Registers Overview

	Write		Read		
	Single Byte	Burst	Single Byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	Not Used				
0x1F	Not Used				
0x20	RESERVED				
0x21	FREND1				
0x22	Not Used				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	Not Used				
0x28	Not Used				
0x29	RESERVED				
0x2A	RESERVED				
0x2B	RESERVED				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F	Not Used				
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	Reserved		Reserved	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	CRC_REG	
0x34	SRX		SRX	RSSI	
0x35	Reserved		Reserved	MARCSTATE	
0x36	SIDLE		SIDLE	Reserved	
0x37	Reserved		Reserved	Reserved	
0x38	Reserved		Reserved	PKTSTATUS	
0x39	SPWD		SPWD	Reserved	
0x3A	SFRX		SFRX	Reserved	
0x3B	Reserved		Reserved	RXBYTES	
0x3C	Reserved		Reserved	Reserved	
0x3D	SNOP		SNOP	Reserved	
0x3E	Reserved		Reserved	Reserved	
0x3F	Reserved		RX FIFO	RX FIFO	

Table 33: SPI Address Space

26.1 Configuration Register Details - Registers with preserved values in SLEEP state

0x00: IOCFG2 - GDO2 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (101001)	R/W	Default is CHP_RDYn (See Table 29 on page 42).

0x01: IOCFG1 - GDO1 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (101110)	R/W	Default is 3-state (See Table 29 on page 42).

0x02: IOCFG0 - GDO0 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7		0	R/W	Use setting from SmartRF Studio [4]
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (See Table 29 on page 42). It is recommended to disable the clock output in initialization, in order to optimize RF performance.

0x03: FIFOTHR - RX FIFO Thresholds

Bit	Field Name	Reset	R/W	Description	
7		0	R/W	Use setting from SmartRF Studio [4]	
6	ADC_RETENTION	0	R/W	0: TEST1 = 0x31 and TEST2= 0x88 when waking up from SLEEP 1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode will always be the reset value. The ADC_RETENTION bit should be set to 1before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.	
5:4	CLOSE_IN_RX[1:0]	0 (00)	R/W	For more details, please see DN010 [5]	
				Setting	RX Attenuation, Typical Values
				0 (00)	0 dB
				1 (01)	6 dB
				2 (10)	12 dB
				3 (11)	18 dB
3:0	FIFO_THR[3:0]	7 (0111)	R/W	Set the threshold for the RX FIFO. The threshold is exceeded when the number of bytes in the RX FIFO is equal to or higher than the threshold value.	
				Setting	Bytes in RX FIFO
				0 (0000)	4
				1 (0001)	8
				2 (0010)	12
				3 (0011)	16
				4 (0100)	20
				5 (0101)	24
				6 (0110)	28
				7 (0111)	32
				8 (1000)	36
				9 (1001)	40
				10 (1010)	44
				11 (1011)	48
				12 (1100)	52
				13 (1101)	56
				14 (1110)	60
				15 (1111)	64

0x04: SYNC1 - Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 - Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN - Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed. This value must be different from 0.

0x07: PKTCTRL1 - Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7:5		0 (000)	R/W	Use setting from SmartRF Studio [4]
4		0	R0	Not Used.
3	CRC_AUTOFLUSH	0	R/W	Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RX FIFO and that packet length is limited to the RX FIFO size.
2	APPEND_STATUS	1	R/W	When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain the RSSI value, as well as CRC OK.
1:0	ADR_CHK[1:0]	0 (00)	R/W	Controls address check configuration of received packages. Setting: Address check configuration 0 (00): No address check 1 (01): Address check, no broadcast 2 (10): Address check and 0 (0x00) broadcast 3 (11): Address check and 0 (0x00) and 255 (0xFF) broadcast

0x08: PKTCTRL0 - Packet Automation Control

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used	
6		1	R/W	Use setting from SmartRF Studio [4]	
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX data	
				Setting	Packet format
				0 (00)	Normal mode, use RX FIFO
				1 (01)	Synchronous serial mode, Data out on either of the GDOx pins
				2 (10)	Reserved
				3 (11)	Asynchronous serial mode, Data out on either of the GDOx pins
3		0	R0	Not used	
2	CRC_EN	1	R/W	1: CRC calculation enabled 0: CRC calculation disabled	
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length	
				Setting	Packet length configuration
				0 (00)	Fixed packet length mode. Length configured in `PKTLEN` register
				1 (01)	Variable packet length mode. Packet length configured by the first byte received after sync word
				2 (10)	Infinite packet length mode
				3 (11)	Reserved

0x09: ADDR - Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR - Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5		0	R/W	Use setting from SmartRF Studio [4]
4:0	FREQ_IF[4:0]	15 (01111)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 381kHz, assuming a 26.0 MHz crystal.

0x0C: FSCTRL0 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer. (2s-complement). Resolution is $F_{XTAL}/2^{14}$ (1.59 kHz - 1.65kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency.

0x0D: FREQ2 - Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0 (00)	R	`FREQ[23:22]` is always 0 (the `FREQ2` register is less than 36 with 26 - 27 MHz crystal)
5:0	FREQ[21:16]	30 (011110)	R/W	`FREQ[23:0]` is the base frequency for the frequency synthesiser in increments of $f_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 - Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. `FREQ2` register

0x0F: FREQ0 - Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. `FREQ2` register

0x10: MDMCFG4 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (10)	R/W	
5:4	CHANBW_M[1:0]	0 (00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ The default values give 203 kHz channel filter bandwidth, assuming a 26.0 MHz crystal.
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7	DEM_DCFILT_OFF	0	R/W	Disable digital DC blocking filter before demodulator. 0 = Enable (better sensitivity) 1 = Disable (current optimized). Only for data rates ≤ 250 kBaud The recommended IF frequency changes when the DC blocking is disabled. Please use SmartRF Studio [4] to calculate correct register setting.
6:4	MOD_FORMAT[2:0]	0 (000)	R/W	The modulation format of the radio signal Setting — Modulation format 0 (000) — 2-FSK 1 (001) — GFSK 2 (010) — Reserved 3 (011) — OOK 4 (100) — 4-FSK 5 (101) — Reserved 6 (110) — Reserved 7 (111) — Reserved 4-FSK modulation cannot be used together with Manchester encoding
3	MANCHESTER_EN	0	R/W	Enables Manchester decoding. 0 = Disable 1 = Enable Manchester encoding cannot be used when using asynchronous serial mode or 4-FSK modulation
2:0	SYNC_MODE[2:0]	2 (010)	R/W	Combined sync-word qualifier mode. The values 0 and 4 disables preamble and sync word detection The values 1, 2, 5, and 6 enables 16-bit sync word detection. Only 15 of 16 bits need to match when using setting 1 or 5. The values 3 and 7 enables 32-bits sync word detection (only 30 of 32 bits need to match). Setting — Sync-word qualifier mode 0 (000) — No preamble/sync 1 (001) — 15/16 sync word bits detected 2 (010) — 16/16 sync word bits detected 3 (011) — 30/32 sync word bits detected 4 (100) — No preamble/sync, carrier-sense above threshold 5 (101) — 15/16 + carrier-sense above threshold 6 (110) — 16/16 + carrier-sense above threshold 7 (111) — 30/32 + carrier-sense above threshold

0x13: MDMCFG1 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7		0	R/W	Use setting from SmartRF Studio [4]
6:2			R0	Not used
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

0x14: MDMCFG0 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number `CHAN` and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E}$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN - Modem Deviation Setting

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used.	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent.	
3			R0	Not used.	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	2-FSK/ GFSK/ 4-FSK	Specifies the expected frequency deviation of incoming signal, must be approximately right for demodulation to be performed reliably and robustly.
				OOK	This setting has no effect.

0x16: MCSM2 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:5			R0	Not used
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3:0		7 (0111)	R/W	Use setting from SmartRF Studio [4]

0x17: MCSM1 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description	
7:6			R0	Not used	
5:4		3 (11)	R/W	Use setting from SmartRF Studio [4]	
3:2	RXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been received.	
				Setting	Next state after finishing packet reception
				0 (00)	IDLE
				1 (01)	Reserved
				2 (10)	Reserved
				3 (11)	Stay in RX
1:0		0 (00)	R/W	Use setting from SmartRF Studio [4]	

0x18: MCSM0 - Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td colspan="3">Not used</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">FS_AUTOCAL[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="3">Automatically calibrate when going to to/from RX mode</td></tr>
<tr><td>Setting</td><td colspan="2">When to perform automatic calibration</td></tr>
<tr><td>0 (00)</td><td colspan="2">Never (manually calibrate using SCAL strobe)</td></tr>
<tr><td>1 (01)</td><td colspan="2">When going from IDLE to RX</td></tr>
<tr><td>2 (10)</td><td colspan="2">When going from RX back to IDLE automatically</td></tr>
<tr><td>3 (11)</td><td colspan="2">Every 4th time when going from RX to IDLE automatically</td></tr>
<tr><td rowspan="7">3:2</td><td rowspan="7">PO_TIMEOUT</td><td rowspan="7">1 (01)</td><td rowspan="7">R/W</td><td colspan="3">Programs the number of times the six-bit ripple counter must expire after the XOSC has settled before CHP_RDYn goes low. [3]

If XOSC is on (stable) during power-down, PO_TIMEOUT shall be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 µs.

For robust operation it is recommended to use PO_TIMEOUT = 2 or 3 when XOSC is off during power-down.</td></tr>
<tr><td>Setting</td><td>Expire count</td><td>Timeout after XOSC start</td></tr>
<tr><td>0 (00)</td><td>1</td><td>Approx. 2.3 - 2.4 µs</td></tr>
<tr><td>1 (01)</td><td>16</td><td>Approx. 37 - 39 µs</td></tr>
<tr><td>2 (10)</td><td>64</td><td>Approx. 149 - 155 µs</td></tr>
<tr><td>3 (11)</td><td>256</td><td>Approx. 597 - 620 µs</td></tr>
<tr><td colspan="3">Exact timeout depends on crystal frequency.</td></tr>
<tr><td>1</td><td></td><td>0</td><td>R/W</td><td colspan="3">Use setting from SmartRF Studio [4]</td></tr>
<tr><td>0</td><td>XOSC_FORCE_ON</td><td>0</td><td>R/W</td><td colspan="3">Force the XOSC to stay on in the SLEEP state.</td></tr>
</table>

[3] Note that the XOSC_STABLE signal will be asserted at the same time as the CHIP_RDYn signal; i.e. the PO_TIMEOUT delays both signals and does not insert a delay between the signals.

0x19: FOCCFG - Frequency Offset Compensation Configuration

Bit	Field Name	Reset	R/W	Description	
7:6			R0	Not used	
5	FOC_BS_CS_GATE	1	R/W	If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CS signal goes high.	
4:3	FOC_PRE_K[1:0]	2 (10)	R/W	The frequency compensation loop gain to be used before a sync word is detected.	
				Setting	Freq. compensation loop gain before sync word
				0 (00)	*K*
				1 (01)	2*K*
				2 (10)	3*K*
				3 (11)	4*K*
2	FOC_POST_K	1	R/W	The frequency compensation loop gain to be used after a sync word is detected.	
				Setting	Freq. compensation loop gain after sync word
				0	Same as FOC_PRE_K
				1	*K*/2
1:0	FOC_LIMIT[1:0]	2 (10)	R/W	The saturation point for the frequency offset compensation algorithm:	
				Setting	Saturation point (max compensated offset)
				0 (00)	±0 (no frequency offset compensation)
				1 (01)	$\pm BW_{CHAN}/8$
				2 (10)	$\pm BW_{CHAN}/4$
				3 (11)	$\pm BW_{CHAN}/2$
				Frequency offset compensation is not supported for OOK. Always use FOC_LIMIT=0 with this modulation format.	

0x1A: BSCFG - Bit Synchronization Configuration

Bit	Field Name	Reset	R/W	Description	
7:6	BS_PRE_KI[1:0]	1 (01)	R/W	The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):	
				Setting	Clock recovery loop integral gain before sync word
				0 (00)	K_I
				1 (01)	$2K_I$
				2 (10)	$3K_I$
				3 (11)	$4K_I$
5:4	BS_PRE_KP[1:0]	2 (10)	R/W	The clock recovery feedback loop proportional gain to be used before a sync word is detected.	
				Setting	Clock recovery loop proportional gain before sync word
				0 (00)	K_P
				1 (01)	$2K_P$
				2 (10)	$3K_P$
				3 (11)	$4K_P$
3	BS_POST_KI	1	R/W	The clock recovery feedback loop integral gain to be used after a sync word is detected.	
				Setting	Clock recovery loop integral gain after sync word
				0	Same as BS_PRE_KI
				1	$K_I/2$
2	BS_POST_KP	1	R/W	The clock recovery feedback loop proportional gain to be used after a sync word is detected.	
				Setting	Clock recovery loop proportional gain after sync word
				0	Same as BS_PRE_KP
				1	K_P
1:0	BS_LIMIT[1:0]	0 (00)	R/W	The saturation point for the data rate offset compensation algorithm:	
				Setting	Data rate offset saturation (max data rate difference)
				0 (00)	±0 (No data rate offset compensation performed)
				1 (01)	±3.125 % data rate offset
				2 (10)	±6.25 % data rate offset
				3 (11)	±12.5 % data rate offset

0x1B: AGCCTRL2 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7:6	MAX_DVGA_GAIN[1:0]	0 (00)	R/W	Reduces the maximum allowable DVGA gain.	
				Setting	Allowable DVGA settings
				0 (00)	All gain settings can be used
				1 (01)	The highest gain setting cannot be used
				2 (10)	The 2 highest gain settings cannot be used
				3 (11)	The 3 highest gain settings cannot be used
5:3	MAX_LNA_GAIN[2:0]	0 (000)	R/W	Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.	
				Setting	Maximum allowable LNA + LNA 2 gain
				0 (000)	Maximum possible LNA + LNA 2 gain
				1 (001)	Approx. 2.6 dB below maximum possible gain
				2 (010)	Approx. 6.1 dB below maximum possible gain
				3 (011)	Approx. 7.4 dB below maximum possible gain
				4 (100)	Approx. 9.2 dB below maximum possible gain
				5 (101)	Approx. 11.5 dB below maximum possible gain
				6 (110)	Approx. 14.6 dB below maximum possible gain
				7 (111)	Approx. 17.1 dB below maximum possible gain
2:0	MAGN_TARGET[2:0]	3 (011)	R/W	These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).	
				Setting	Target amplitude from channel filter
				0 (000)	24 dB
				1 (001)	27 dB
				2 (010)	30 dB
				3 (011)	33 dB
				4 (100)	36 dB
				5 (101)	38 dB
				6 (110)	40 dB
				7 (111)	42 dB

0x1C: AGCCTRL1 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used	
6	AGC_LNA_PRIORITY	1	R/W	Selects between two different strategies for LNA and LNA 2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA 2 gain is decreased to minimum before decreasing LNA gain.	
5:4	CARRIER_SENSE_REL_THR[1:0]	0 (00)	R/W	Sets the relative change threshold for asserting carrier sense	
				Setting	Carrier sense relative threshold
				0 (00)	Relative carrier sense threshold disabled
				1 (01)	6 dB increase in RSSI value
				2 (10)	10 dB increase in RSSI value
				3 (11)	14 dB increase in RSSI value
3:0	CARRIER_SENSE_ABS_THR[3:0]	0 (0000)	R/W	Sets the absolute RSSI threshold for asserting carrier sense. The 2-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.	
				Setting	Carrier sense absolute threshold (Equal to channel filter amplitude when AGC has not decreased gain)
				-8 (1000)	Absolute carrier sense threshold disabled
				-7 (1001)	7 dB below `MAGN_TARGET` setting
				…	…
				-1 (1111)	1 dB below `MAGN_TARGET` setting
				0 (0000)	At `MAGN_TARGET` setting
				1 (0001)	1 dB above `MAGN_TARGET` setting
				…	…
				7 (0111)	7 dB above `MAGN_TARGET` setting

0x1D: AGCCTRL0 - AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">HYST_LEVEL[1:0]</td><td rowspan="6">2 (10)</td><td rowspan="6">R/W</td><td colspan="3">Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determine gain changes).</td></tr>
<tr><td>Setting</td><td colspan="2">Description</td></tr>
<tr><td>0 (00)</td><td colspan="2">No hysteresis, small symmetric dead zone, high gain</td></tr>
<tr><td>1 (01)</td><td colspan="2">Low hysteresis, small asymmetric dead zone, medium gain</td></tr>
<tr><td>2 (10)</td><td colspan="2">Medium hysteresis, medium asymmetric dead zone, medium gain</td></tr>
<tr><td>3 (11)</td><td colspan="2">Large hysteresis, large asymmetric dead zone, low gain</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">WAIT_TIME[1:0]</td><td rowspan="6">1 (01)</td><td rowspan="6">R/W</td><td colspan="3">Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.</td></tr>
<tr><td>Setting</td><td colspan="2">Channel filter samples</td></tr>
<tr><td>0 (00)</td><td colspan="2">8</td></tr>
<tr><td>1 (01)</td><td colspan="2">16</td></tr>
<tr><td>2 (10)</td><td colspan="2">24</td></tr>
<tr><td>3 (11)</td><td colspan="2">32</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">AGC_FREEZE[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="3">Control when the AGC gain should be frozen.</td></tr>
<tr><td>Setting</td><td colspan="2">Function</td></tr>
<tr><td>0 (00)</td><td colspan="2">Normal operation. Always adjust gain when required.</td></tr>
<tr><td>1 (01)</td><td colspan="2">The gain setting is frozen when a sync word has been found.</td></tr>
<tr><td>2 (10)</td><td colspan="2">Manually freeze the analogue gain setting and continue to adjust the digital gain.</td></tr>
<tr><td>3 (11)</td><td colspan="2">Manually freezes both the analogue and the digital gain setting. Used for manually overriding the gain.</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">FILTER_LENGTH[1:0]</td><td rowspan="6">1 (01)</td><td rowspan="6">R/W</td><td colspan="3">2-FSK and 4-FSK: Sets the averaging length for the amplitude from the channel filter.
OOK: Sets the OOK decision boundary for OOK reception.</td></tr>
<tr><td>Setting</td><td>Channel filter samples</td><td>OOK decision boundary</td></tr>
<tr><td>0 (00)</td><td>8</td><td>4 dB</td></tr>
<tr><td>1 (01)</td><td>16</td><td>8 dB</td></tr>
<tr><td>2 (10)</td><td>32</td><td>12 dB</td></tr>
<tr><td>3 (11)</td><td>64</td><td>16 dB</td></tr>
</table>

0x20: RESERVED

Bit	Field Name	Reset	R/W	Description
7:3		31 (11111)	R/W	Use setting from SmartRF Studio [4]
2			R0	Not used
1:0		0 (00)	R/W	Use setting from SmartRF Studio [4]

0x21: FREND1 - Front End RX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

0x23: FSCAL3 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (10)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF Studio software [4].
5:4	CHP_CURR_CAL_EN[1:0]	2 (10)	R/W	Disable charge pump calibration stage when 0.
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $I\_OUT = I_0 \cdot 2^{FSCAL3[3:0]/4}$ Please see Section 25.2 for more details.

0x24: FSCAL2 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (01010)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value. Please see Section 25.2 for more details.

0x25: FSCAL1 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Please see Section 25.2 for more details.

0x26: FSCAL0 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF Studio software [4].

26.2 Configuration Register Details - Registers that Loose Programming in SLEEP State

0x29: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		89 (0x59)	R/W	Use setting from SmartRF Studio [4]

0x2A: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		127 (0x7F)	R/W	Use setting from SmartRF Studio [4]

0x2B: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		63 (0x3F)	R/W	Use setting from SmartRF Studio [4]

0x2C: TEST2 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	136 (0x88)	R/W	Use setting from SmartRF Studio [4] This register will be forced to 0x88 or 0x81 when it wakes up from SLEEP mode, depending on the configuration of `FIFOTHR.ADC_RETENTION`. Note that the value read from this register when waking up from SLEEP always is the reset value (0x88) regardless of the `ADC_RETENTION` setting. The inverting of some of the bits due to the `ADC_RETENTION` setting is only seen INTERNALLY in the analog part.

0x2D: TEST1 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	Use setting from SmartRF Studio [4] This register will be forced to 0x31 or 0x35 when it wakes up from SLEEP mode, depending on the configuration of `FIFOTHR.ADC_RETENTION`. Note that the value read from this register when waking up from SLEEP always is the reset value (0x31) regardless of the `ADC_RETENTION` setting. The inverting of some of the bits due to the `ADC_RETENTION` setting is only seen INTERNALLY in the analog part.

0x2E: TEST0 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (000010)	R/W	Use setting from SmartRF Studio [4]
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	Use setting from SmartRF Studio [4]

26.3 Status Register Details

0x30 (0xF0): PARTNUM - Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	0 (0x00)	R	Chip part number

0x31 (0xF1): VERSION - Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	8 (0x08)	R	Chip version number.

0x32 (0xF2): FREQEST - Frequency Offset Estimate from Demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (2's complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is ±202 kHz to ±210 kHz, depending on XTAL frequency. Frequency offset compensation is only supported for 2-FSK, GFSK, and 4-FSK modulation. This register will read 0 when using OOK modulation.

0x33 (0xF3): CRC_REG - CRC OK

Bit	Field Name	Reset	R/W	Description
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0			R	Reserved

0x34 (0xF4): RSSI - Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE - Main Radio Control State Machine State

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7:5</td><td></td><td></td><td>R0</td><td colspan="3">Not used</td></tr>
<tr><td rowspan="22">4:0</td><td rowspan="22">MARC_STATE[4:0]</td><td rowspan="22"></td><td rowspan="22">R</td><td colspan="3">Main Radio Control FSM State</td></tr>
<tr><td>Value</td><td>State name</td><td>State (Figure 21, page 35)</td></tr>
<tr><td>0 (0x00)</td><td>SLEEP</td><td>SLEEP</td></tr>
<tr><td>1 (0x01)</td><td>IDLE</td><td>IDLE</td></tr>
<tr><td>2 (0x02)</td><td>XOFF</td><td>XOFF</td></tr>
<tr><td>3 (0x03)</td><td>VCOON_MC</td><td>MANCAL</td></tr>
<tr><td>4 (0x04)</td><td>REGON_MC</td><td>MANCAL</td></tr>
<tr><td>5 (0x05)</td><td>MANCAL</td><td>MANCAL</td></tr>
<tr><td>6 (0x06)</td><td>VCOON</td><td>FS_WAKEUP</td></tr>
<tr><td>7 (0x07)</td><td>REGON</td><td>FS_WAKEUP</td></tr>
<tr><td>8 (0x08)</td><td>STARTCAL</td><td>CALIBRATE</td></tr>
<tr><td>9 (0x09)</td><td>BWBOOST</td><td>SETTLING</td></tr>
<tr><td>10 (0x0A)</td><td>FS_LOCK</td><td>SETTLING</td></tr>
<tr><td>11 (0x0B)</td><td>IFADCON</td><td>SETTLING</td></tr>
<tr><td>12 (0x0C)</td><td>ENDCAL</td><td>CALIBRATE</td></tr>
<tr><td>13 (0x0D)</td><td>RX</td><td>RX</td></tr>
<tr><td>14 (0x0E)</td><td>RX_END</td><td>RX</td></tr>
<tr><td>15 (0x0F)</td><td>RX_RST</td><td>RX</td></tr>
<tr><td>16 (0x10)</td><td>Reserved</td><td></td></tr>
<tr><td>17 (0x11)</td><td>RXFIFO_OVERFLOW</td><td>RXFIFO_OVERFLOW</td></tr>
<tr><td>18 (0x12)
-
22 (0x16)</td><td>Reserved</td><td></td></tr>
<tr><td colspan="3">Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.</td></tr>
</table>

0x38 (0xF8): PKTSTATUS - Current GDOx Status and Packet Status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense. Cleared when entering IDLE mode.
5			R	Reserved
4			R	Reserved
3	SFD		R	Start of Frame Delimiter. This bit is asserted when sync word has been received and de-asserted at the end of the packet. It will also de-assert when a packet is discarded due to address or maximum length filtering or the radio enters RXFIFO_OVERFLOW state.
2	GDO2		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG2.GDO2_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS[2]` with `GDO2_CFG=0x0A`.
1			R0	Not used
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG0.GDO0_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS[0]` with `GDO0_CFG=0x0A`.

0x3B (0xFB): RXBYTES - Overflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

27 Development Kit Ordering Information

Orderable Evaluation Module	Description	Minimum Order Quantity
CC11xLDK-868-915	CC11xL Development Kit, 868/915 MHz	1
CC11xLEMK-433	CC11xL Evaluation Module Kit, 433 MHz	1

Figure 26: Development Kit Ordering Information

28 References

[1] Characterization Design 315 - 433 MHz

(Identical to the CC1101EM 315 - 433 MHz Reference Design (swrr046.zip))

[2] Characterization Design 868 - 915 MHz

(Identical to the CC1101EM 868 - 915 MHz Reference Design (swrr045.zip))

[3] CC113L Errata Notes (swrz038.pdf)

[4] SmartRF Studio (swrc176.zip)

[5] DN010 Close-in Reception with CC1101 (swra147.pdf)

[6] DN015 Permanent Frequency Offset Compensation (swra159.pdf)

[7] DN505 RSSI Interpretation and Timing (swra114.pdf)

[8] DN022 CC11xx OOK/ASK register settings (swra215.pdf)

[9] DN005 CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (swra122.pdf)

[10] CC113LEM 433 MHz Reference Design (swrr083.zip)

[11] CC113LEM 868 - 915 MHz Reference Design (swrr084.zip)

29 General Information

29.1 Document History

Revision	Date	Description/Changes
SWRS108	05.24.2011	Initial Release
SWRS108A	08.09.2011	Added three registers (CHANNR, MDMCFG1, and MDMCFG0). Changes made to Section 20. Hyperlinks added to the CC113LEM 433 MHz Reference Design and the CC113LEM 868 - 915 MHz Reference Design

Table 34: Document History

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CC113LRTKR	ACTIVE	VQFN	RTK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CC113LRTKT	ACTIVE	VQFN	RTK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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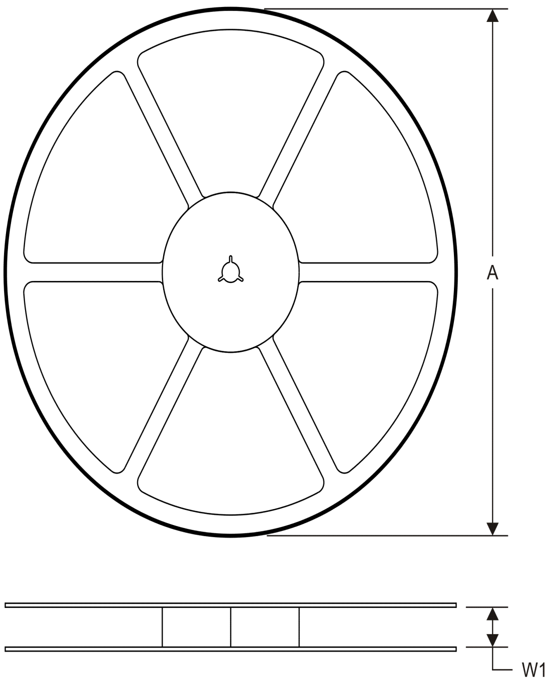
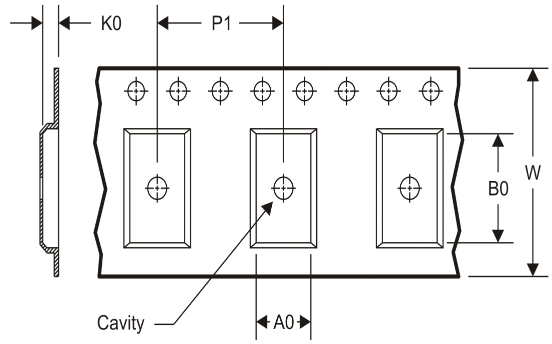
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



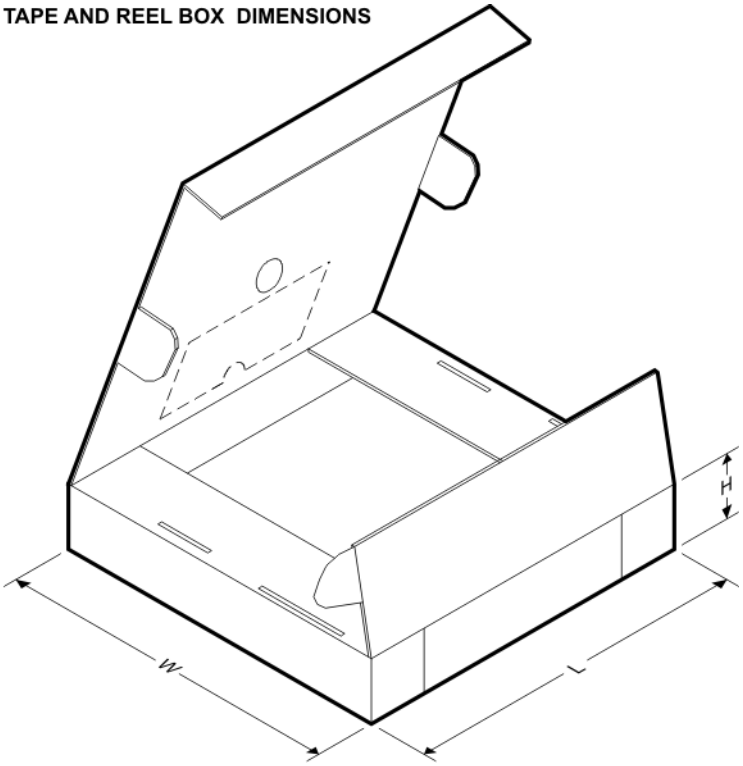
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC113LRTKR	VQFN	RTK	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CC113LRTKT	VQFN	RTK	20	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

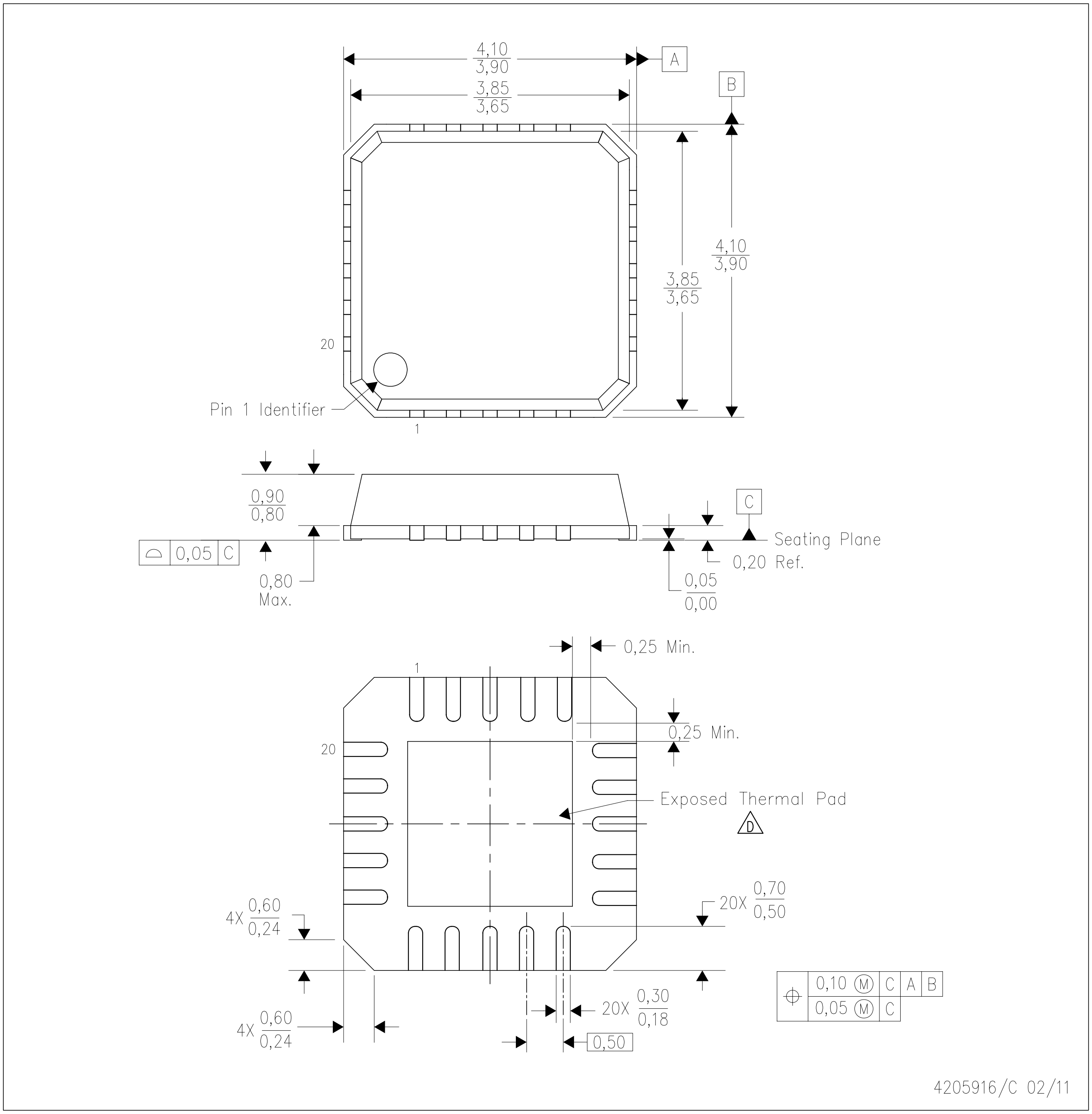
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC113LRTKR	VQFN	RTK	20	3000	338.1	338.1	20.6
CC113LRTKT	VQFN	RTK	20	250	338.1	338.1	20.6

RTK (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5—1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

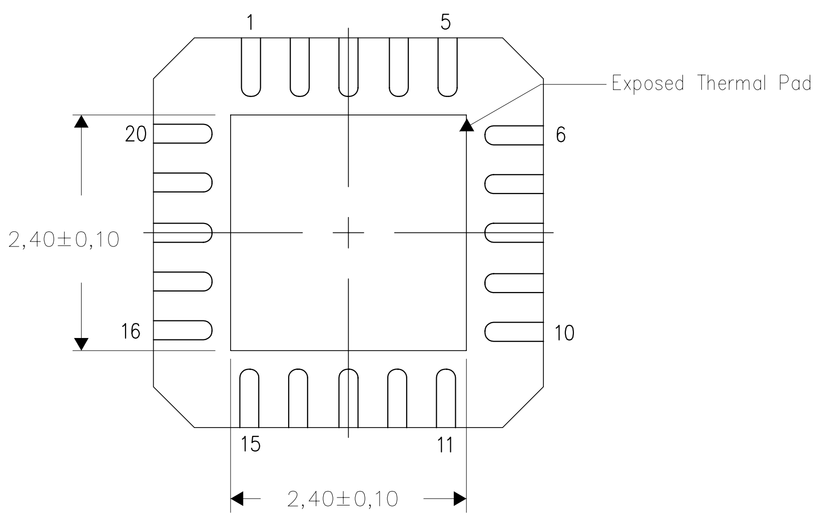
RTK (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



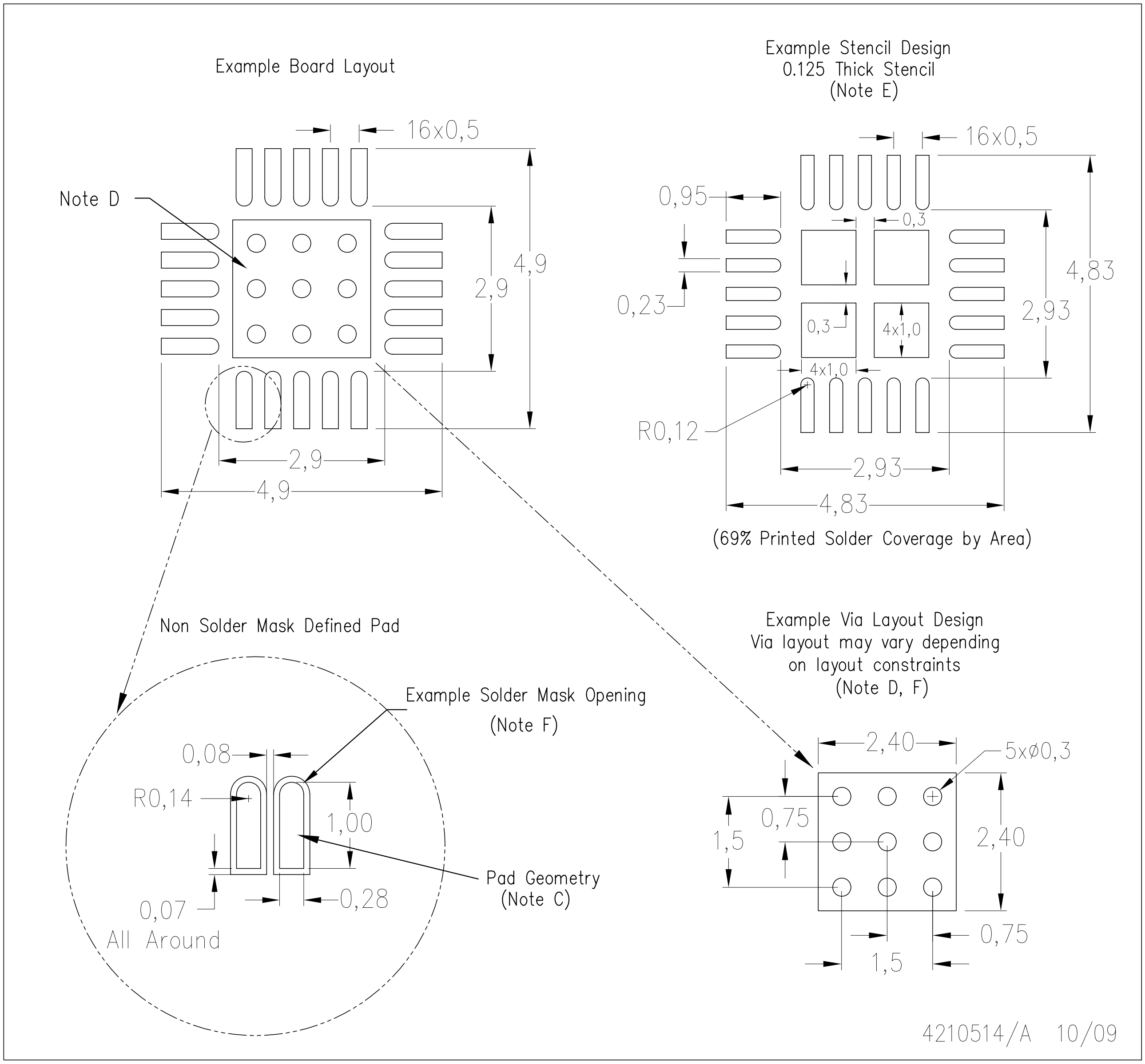
Bottom View

Exposed Thermal Pad Dimensions

4208000-3/G 02/11

NOTE: A. All linear dimensions are in millimeters

RTK (S-PVQFN-N20)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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