

Designing for Flexibility around eMMC

When choosing non-volatile storage memory for your design, Embedded MultiMediaCard (eMMC) technology provides many advantages over standard Secure Digital (SD) cards in terms of performance, reliability and form factor. However, there can be supply constraints when sourcing eMMC devices as a design moves into manufacturing. This application note walks through some simple steps to take, during the design process, to create flexibility in the design to accept various revisions of eMMC. These steps will help to mitigate supply issues by enabling multiple existing revisions of eMMC to work with your design as well as future-proof your design for new revisions of eMMC.

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Table of Contents

Designing for Flexibility around eMMC	1
1 eMMC Versions	3
2 Schematics	4
3 Layout	8
4 Conclusion	10

1 eMMC Versions

The JEDEC Solid State Technology Association is an independent semiconductor engineering trade organization and standardization body. JEDEC defines the [eMMC standard](#) and has released a number of versions of this standard. When the Texas Instruments Sitara ARM® Cortex®-A8 [AM335x](#) Processor within the OSD335x System-In-Package Family was designed the released eMMC standard was version 4.3 (v4.3). Therefore, the OSD335x SiP supports the standard v4.3 command and response set. However, the newest eMMC memory devices available on the market (at this writing) support the standard v5.1 command and response set. *Fortunately, the newer eMMC devices are backward compatible with the older eMMC specifications.*

Therefore, it is straightforward to create designs around the OSD335x Family of devices that utilize the newest eMMC memory devices. The main caveat being that product designs need to comprehend the changes in schematics and layout between the eMMC v4.3 and eMMC v5.1 standards. Designing to the JEDEC standard itself rather than following a particular eMMC vendor data-sheet will give the most flexibility when sourcing eMMC devices.

2 Schematics

When starting a design, the first step normally involves creating or obtaining a schematic symbol based on the datasheet of the part. However, in the case of eMMC, some pins within the standard are optional and may not be implemented by a given device, such as vendor specific function pins (VSF). This can lead a design to mistakenly consider these pins as unimportant which can then limit the design to only using parts that implement a particular subset of the standard. Therefore, the schematic symbol should instead reflect the eMMC v5.1 standard. It should also include all “Reserve for Future Use” (RFU) pins so that it is clear which pins are “No Connect” (NC) vs RFU. The NC pins can be routed through while the RFU pins should be avoided during routing.

Unfortunately, many datasheets do not mark all of the pins that are defined / reserved by the eMMC standard. For example, Figure 1 shows a current ball map for a eMMC v5.1 part.

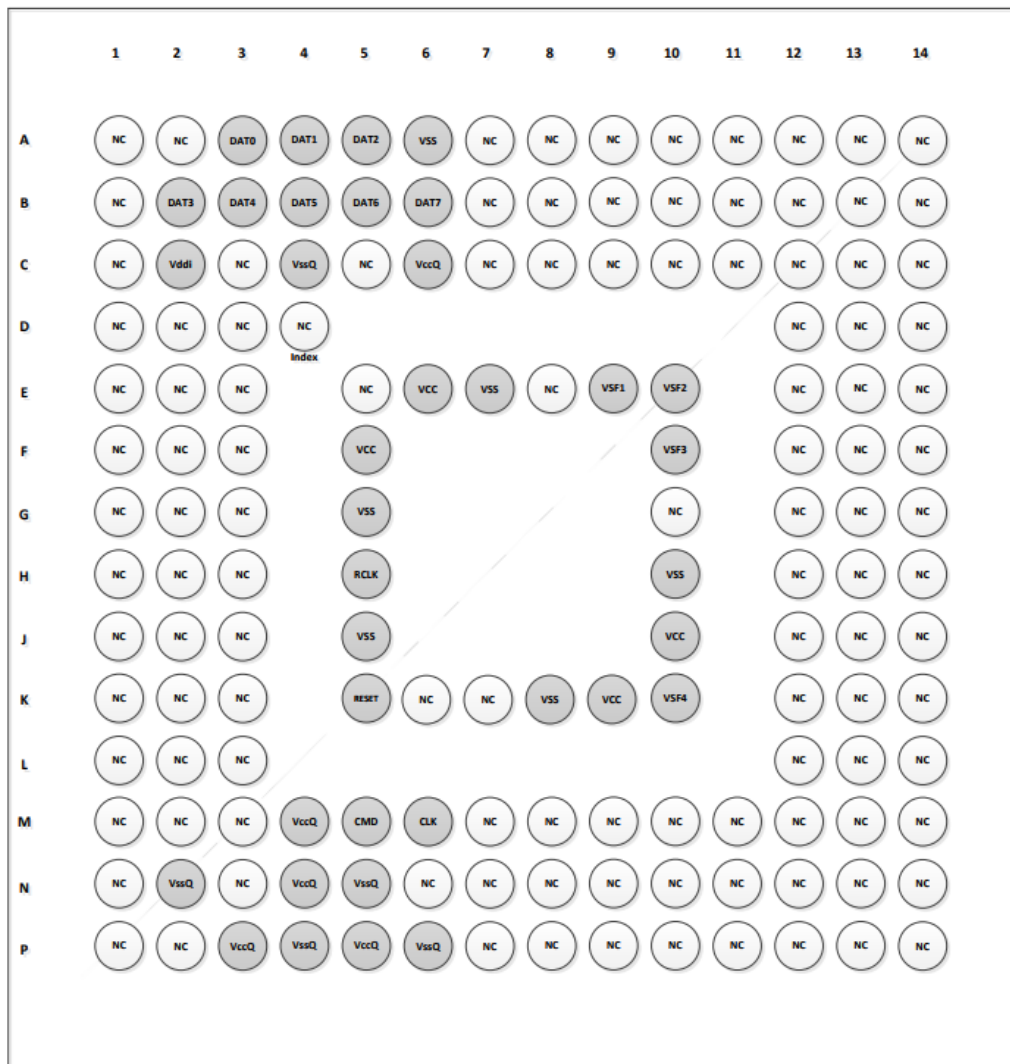


Figure 1 - eMMC v5.x Ball Map from a vendor Datasheet

However, when looking at the JEDEC standard pin layout (see yellow and orange pins) in Figure 2 below, there are a number of pins that differ from our example in Figure 1. For example, there are several pins that are marked as “NC” in the Figure 1 ball map that are actually used by the standard. This includes the “RFU” pins as well as some additional “VSF” pins. See examples highlighted in Figure 3.

153-Ball eMMC V5.0 / e2MMC Ballout - Ball-side down view

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	D-VDDQ	D-VSSQ	D-VSS	D-VDD	D-VSSQ	NC	NC	
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	D-VDDQ	NC	
C	D-VSS	VDDI	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	D-VDDQ	
D	NC	NC	NC	NC index									NC	NC	D-VSSQ
E	NC	NC	NC		RFU	VCC	VSS	VSF	VSF	VSF			NC	NC	NC
F	D-VDD	NC	NC		VCC					VSF			NC	NC	D-VSSQ
G	NC	NC	D-VDD2		VSS					VSF			NC	D-VDDQ	D-VDD
H	D-VDDQ	NC	NC		DS					VSS			NC	D-VDDQ	D-VSS
J	NC	NC	NC		VSS					VCC			NC	NC	D-VSSQ
K	NC	D-VSS	NC		RST_n	RFU	RFU	VSS	VCC	VSF			NC	NC	NC
L	NC	NC	NC										NC	NC	D-VSSQ
M	D-VSS	D-VDD	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	D-VDDQ
N	NC	VSSQ	NC	VCCQ	VSSQ	D-VSSQ	NC	NC	NC	NC	NC	NC	NC	D-VDDQ	NC
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	D-VDDQ	D-VDDQ	D-VSSQ	VSF	D-VDD	D-VSSQ	NC	NC	

eMMC Version 5.0

e2MMC, otherwise NC

RFU

Figure 2 - eMMC 5.x JEDEC Standard Pin Layout

You can find the standard layout of eMMC pins in [JEDEC Standard No. 21-C, Figure 3.12.1-49](#).

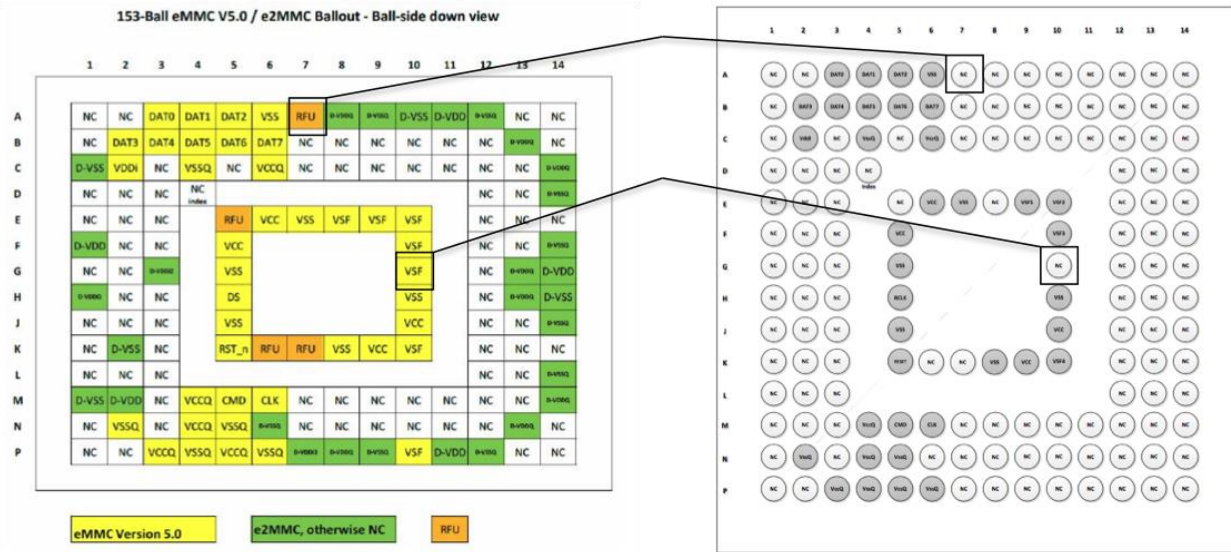


Figure 3 - Examples of pins specified in eMMC specification vs vendor datasheet

You can see above in Figure 3, two examples of pins that are utilized in the vendor’s datasheet as NC that are reserved differently in the standard.

Figure 4 shows the eMMC v4.3 interface of the OSD335x Family connected to an eMMC v5.x component. All of the reserved and additional pins are designated on the schematic symbol so it is easier to understand and avoid those pins in layout.

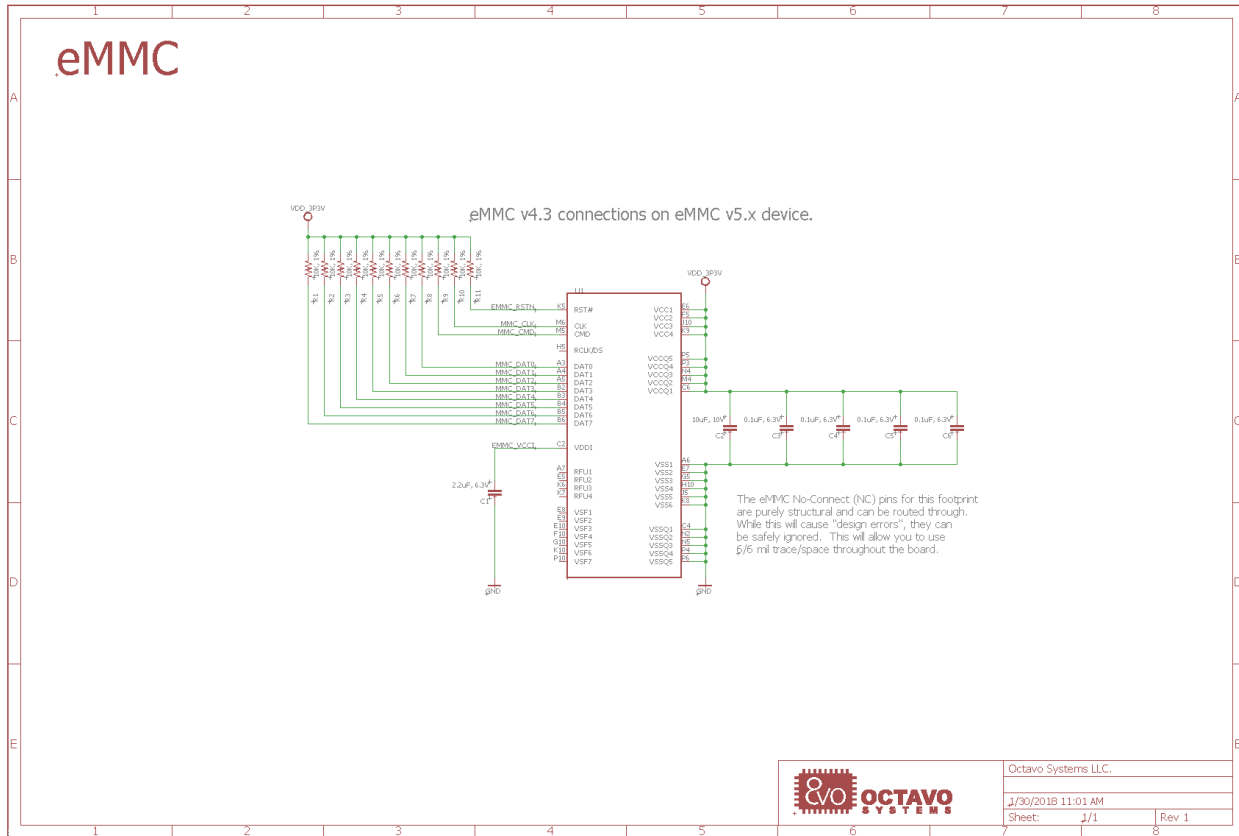


Figure 4 - eMMC v5.x symbol connected to eMMC v4.3 interface

3 Layout

The 153 ball eMMC footprint is very standard and supports a broad range of devices from many manufacturers. While, there may be smaller footprints, for maximum flexibility it is best to use the 11.5mm x 13mm outline for the size of eMMC device. All pins marked “NC” in the JEDEC standard (i.e. all the white and green pins in Figure 2) are purely structural (i.e. not electrically connected) and may be routed through, according to the standard.

Figure 5 shows an example escape routing of a v5.x eMMC device using 6 mil trace / 6 mil space routing and 12 mil drill / 24 mil finished vias. One thing to note is that due to the eMMC ball spacing, the traces may need to be adjusted $\frac{1}{4}$ or $\frac{1}{2}$ a mil to center the trace through the “NC” balls.

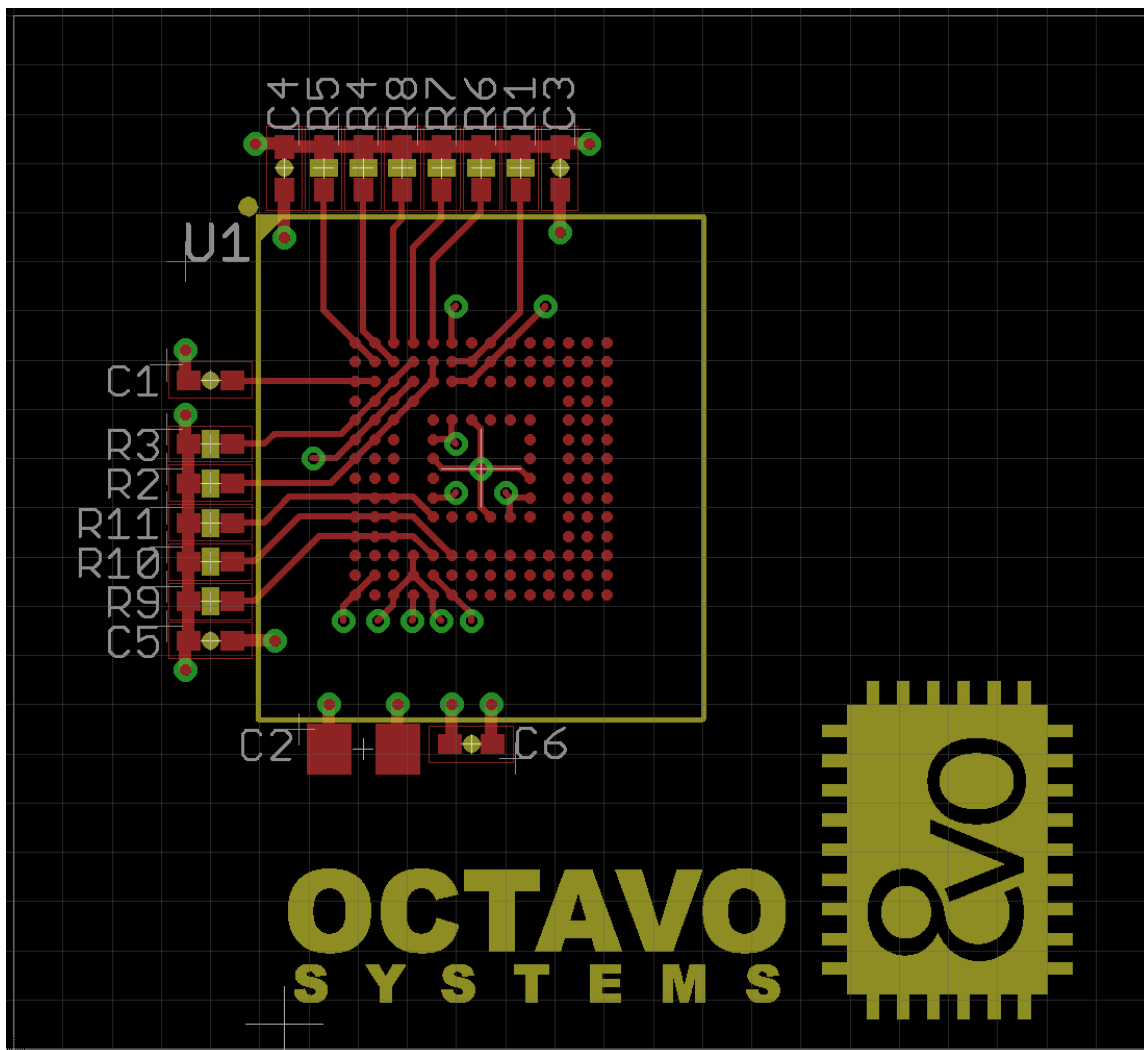


Figure 5 - Example Layout of eMMC v5.x device avoiding reserved pins

When routing through “NC” pins, this will create overlap errors in design tools like EAGLE. Figure 6 shows the overlap design errors that are created from the example BGA escape shown in Figure 5. While these errors can be ignored, it is important to make sure that none of the reserved or otherwise specified pins of the eMMC v5.x standard have been routed through. Also, there should be no clearance errors. If clearance errors exist, then the traces should be adjusted accordingly to center them through the eMMC ball.

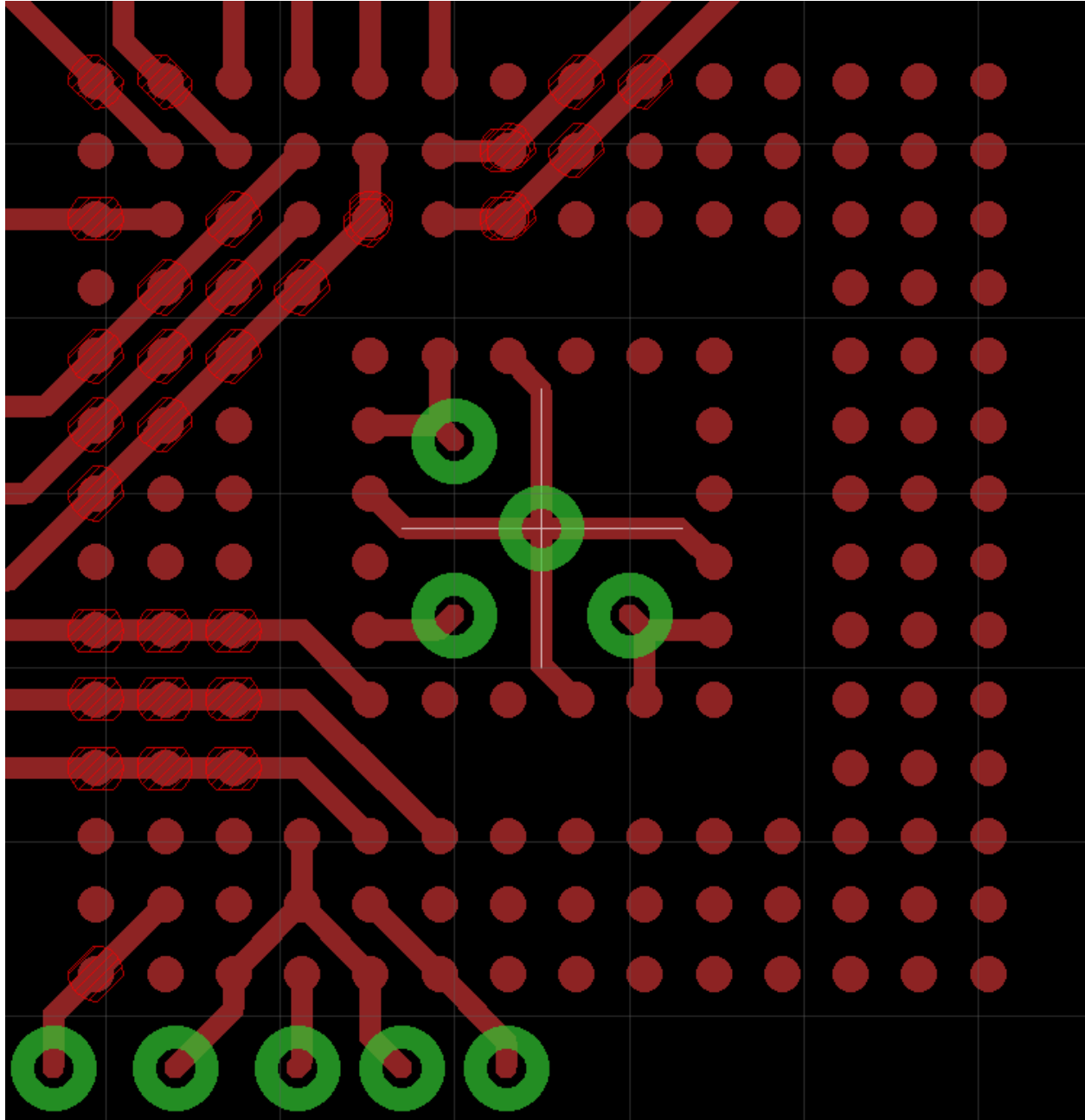


Figure 6 - EAGLE design "overlap" errors that can be ignored

4 Conclusion

From the example above, it is clear that by observing a few simple schematic and layout rules, new designs can take advantage of both the newer eMMC v5.x as well as the older eMMC v4.x parts when sourcing eMMC for an OSD335x Family design.

For additional assistance laying out your design using the OSD335x Family of devices, please connect directly to our engineers on the forums at www.octavosystems.com/forums