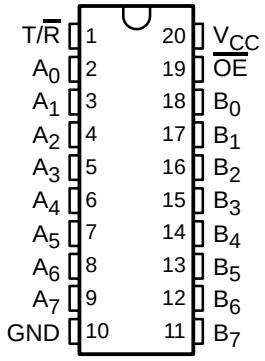
- **Function and Pinout Compatible With FCT and F Logic**
- **25-Ω Output Series Resistors to Reduce Transmission-Line Reflection Noise**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **12-mA Output Sink Current**
  15-mA Output Source Current
- **3-State Outputs**

P, Q, OR SO PACKAGE
(TOP VIEW)



description

The CY74FCT2245T contains eight noninverting, bidirectional buffers with 3-state outputs intended for bus-oriented applications. On-chip termination resistors at the outputs reduce system noise caused by reflections. For this reason, the CY74FCT2245T can replace the CY74FCT245T in an existing design. The CY74FCT2245T current-sinking capability is 12 mA at the A and B ports.

The transmit/receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active high) enables data from A ports to B ports; receive (active low) enables data from B ports to A ports. The output-enable ($\overline{OE}$) input, when high, disables both the A and B ports by putting them in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT2245CTQCT	FCT2245
	SOIC – SO	Tube	4.1	CY74FCT2245CTSOC	FCT2245
		Tape and reel	4.1	CY74FCT2245CTSOCT	
	DIP – P	Tube	4.6	CY74FCT2245ATPC	74FCT2245ATPC
	QSOP – Q	Tape and reel	4.6	CY74FCT2245ATQCT	FCT2245A
	SOIC – SO	Tube	4.6	CY74FCT2245ATSOC	FCT2245A
		Tape and reel	4.6	CY74FCT2245ATSOCT	
	QSOP – Q	Tape and reel	7.0	CY74FCT2245TQCT	FCT2245
	SOIC – SO	Tube	7.0	CY74FCT2245TSOC	FCT2245
		Tape and reel	7.0	CY74FCT2245TSOCT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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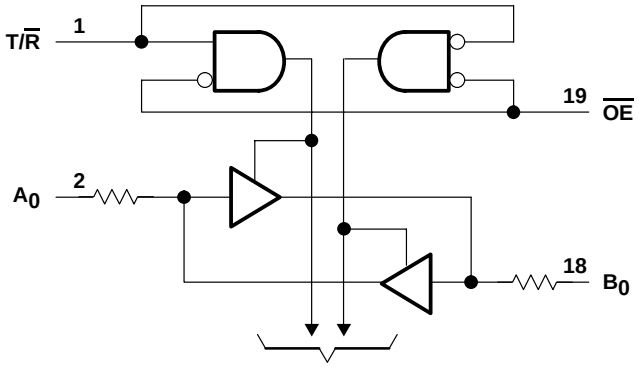
FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to bus A
L	H	Bus A data to bus B
H	X	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . . 69°C/W
Q package . . . . . 68°C/W
SO package . . . . . 58°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75,	I_{IN} = –18 mA			–0.7	–1.2	V
V_{OH}	V_{CC} = 4.75,	I_{OH} = –15 mA		2.4	3.3		V
V_{OL}	V_{CC} = 4.75,	I_{OL} = 12 mA			0.3	0.55	V
R_{out}	V_{CC} = 4.75,	I_{OL} = 12 mA		20	25	40	Ω
V_{hys}	All inputs				0.2		V
I_I	V_{CC} = 5.25 V,	V_{IN} = V_{CC}				5	µA
I_{IH}	V_{CC} = 5.25 V,	V_{IN} = 2.7 V				±1	µA
I_{IL}	V_{CC} = 5.25 V,	V_{IN} = 0.5 V				±1	µA
I_{OZH}	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V				10	µA
I_{OZL}	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V				–10	µA
I_{OS}‡	V_{CC} = 5.25 V,	V_{OUT} = 0 V		–60	–120	–225	mA
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1	µA
I_{CC}	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2	mA
ΔI_{CC}	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2	mA
I_{CCD}¶	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{T/R}$ = $\overline{OE}$ = GND, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V				0.06	0.12	mA/ MHz
I_C#	V_{CC} = 5.25 V, Outputs open, $\overline{T/R}$ = $\overline{OE}$ = GND	One input switching at f_1 = 10 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		0.7	1.4	mA
			V_{IN} = 3.4 V or GND		1	2.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V		1.3	2.6‖	
			V_{IN} = 3.4 V or GND		3.3	10.6‖	
C_i					5	10	pF
C_o					9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

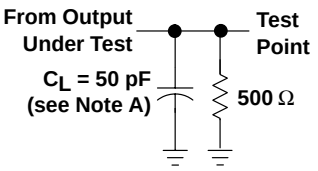
All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

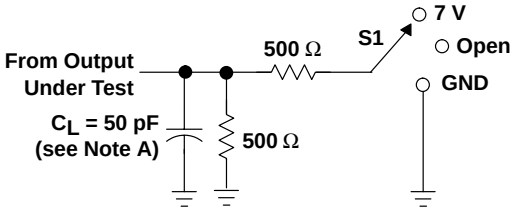
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2245T		CY74FCT2245AT		CY74FCT2245CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A_n or B_n	B_n or A_n	1.5	7	1.5	4.6	1.5	4.1	ns
t_{PHL}			1.5	7	1.5	4.6	1.5	4.1	
t_{PZH}	$\overline{OE}$	A or B	1.5	9.5	1.5	6.2	1.5	5.8	ns
t_{PZL}			1.5	9.5	1.5	6.2	1.5	5.8	
t_{PHZ}	$\overline{OE}$	A or B	1.5	7.5	1.5	5	1.5	4.5	ns
t_{PLZ}			1.5	7.5	1.5	5	1.5	4.5	

PARAMETER MEASUREMENT INFORMATION

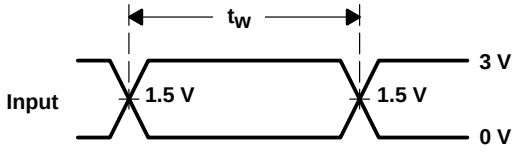


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

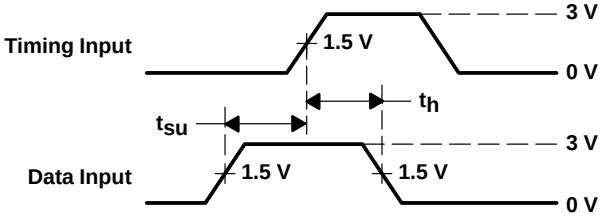


LOAD CIRCUIT FOR
3-STATE OUTPUTS

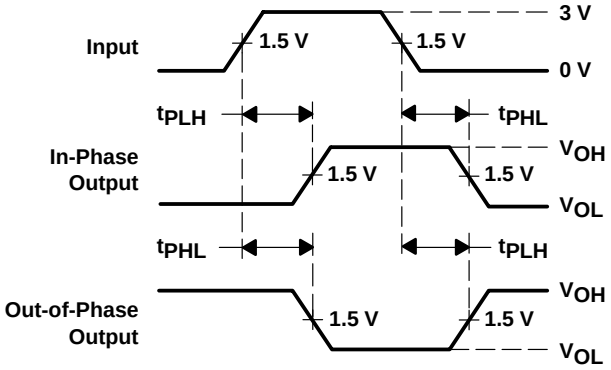
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



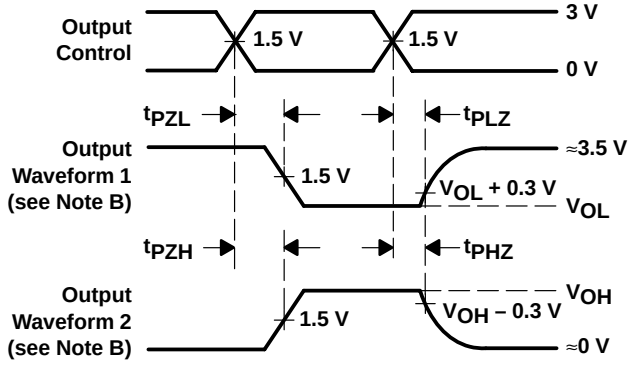
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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