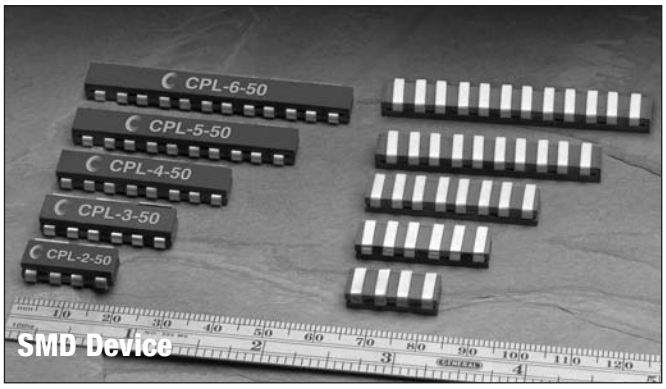
COILTRONICS®

# Multi-Phase Power Inductors

## CPL, CPLA & CPLE Series




### Description

- Halogen Free
- ***CPLA Series*** *features acoustic noise dampening properties*
- ***CPLE Series*** *features optimized core material for enhanced light load efficiency*

- Designed exclusively for use with Volterra® VPR-Devices [A]
- High current multi-phase inductor applications
- Ferrite core material
- 50nH per phase coupled inductor
- 125°C maximum temperature operation
- Frequency range up to 2MHz
- Patents pending
- RoHS compliant

### Applications

- For exclusive use with Volterra® VPR-Devices

### Environmental Data

- Storage temperature range: -40°C to +125°C
- Operating temperature range: -40°C to +125°C (Range is application specific)
- Solder reflow temperature: J-STD-020D compliant

### Packaging

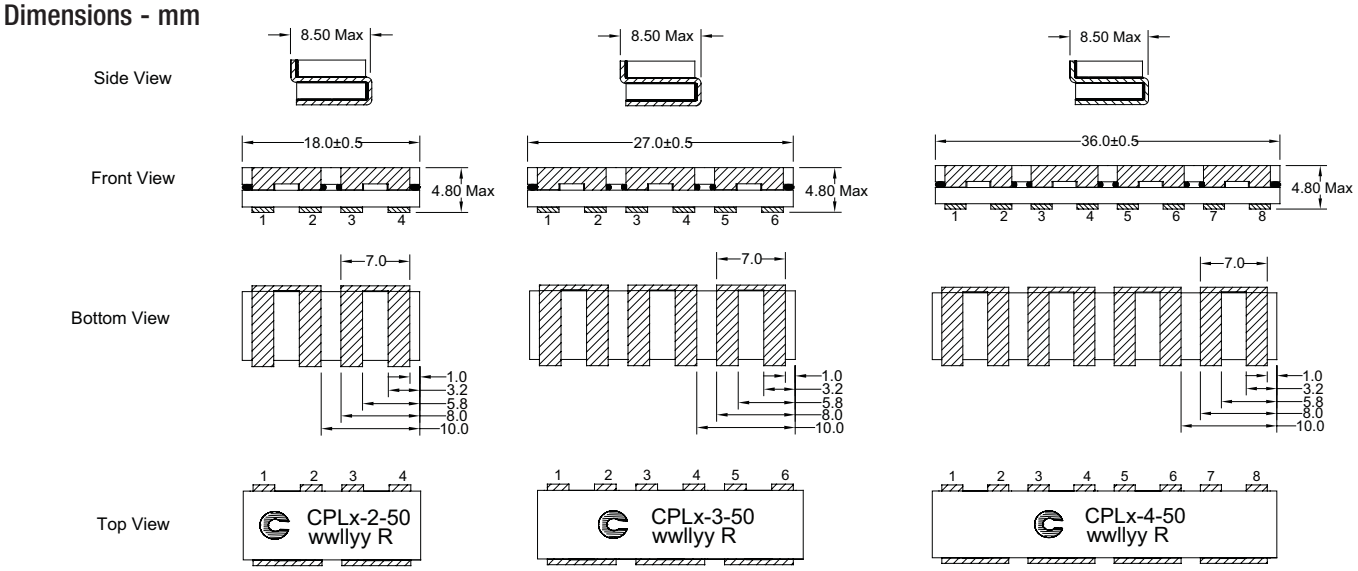
- Supplied in tape and reel packaging, 750 parts per reel, 13" diameter reel

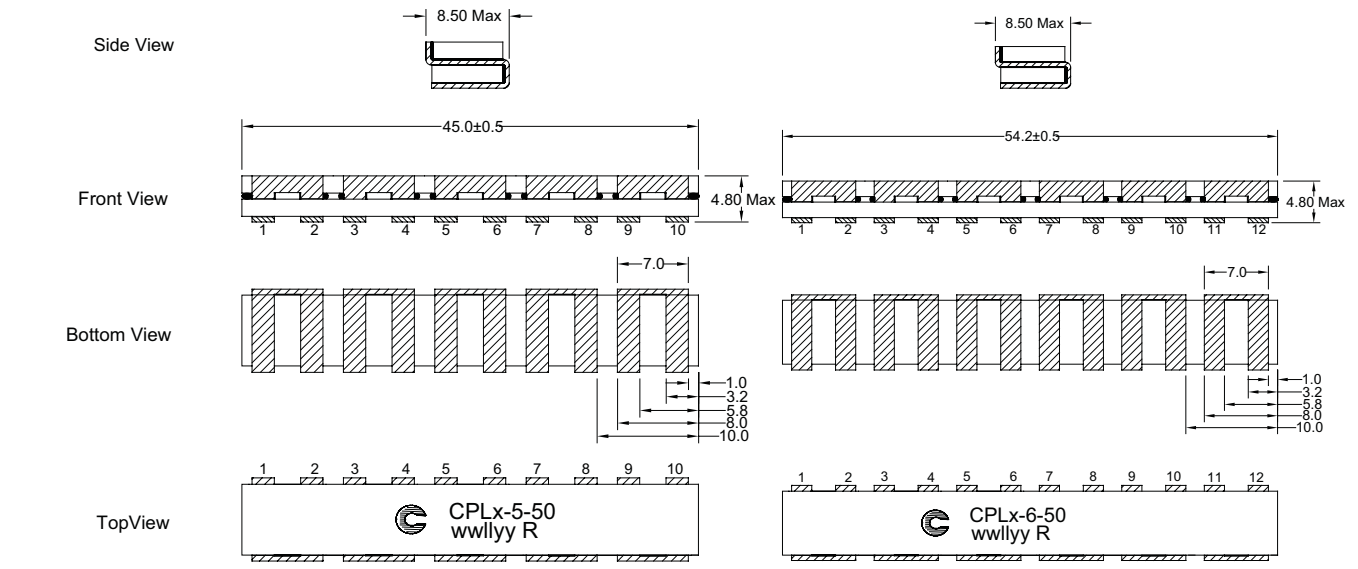
| Function Specifications | | | | | | Test Specifications | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Part Number | Inductor Phases | DCR (Ω) Nom. @25°C | DCR (Ω) Max. @25°C | Rated Inductance per Phase (nH) [3] | I Rated per Phase (Adc) [3] | Pin Numbers | OCL (nH)[1,2] | Pin Numbers | OCL (nH)[1,2] | Magnetizing Inductance @ 5Adc (25°C) |
| **CPL Series** | | | | | | | | | | |
| CPL-2-50TR-R | 2 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (1-2) | 365 ±18% | (3-4) | 365 ±18% | 300 |
| CPL-3-50TR-R | 3 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4) | 490 ±20% | (1-2), (5-6) | 365 ±18% | 400 |
| CPL-4-50TR-R | 4 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6) | 490 ±20% | (1-2), (7-8) | 365 ±18% | 400 |
| CPL-5-50TR-R | 5 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6), (7-8) | 490 ±20% | (1-2), (9-10) | 365 ±18% | 400 |
| CPL-6-50TR-R | 6 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6), (7-8), (9-10) | 490 ±20% | (1-2), (11-12) | 365 ±18% | 400 |
| **CPLA Series - Acoustic Noise Dampening** | | | | | | | | | | |
| CPLA-2-50TR-R | 2 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (1-2) | 365 ±18% | (3-4) | 365 ±18% | 300 |
| CPLA-3-50TR-R | 3 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4) | 490 ±20% | (1-2), (5-6) | 365 ±18% | 400 |
| CPLA-4-50TR-R | 4 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6) | 490 ±20% | (1-2), (7-8) | 365 ±18% | 400 |
| CPLA-5-50TR-R | 5 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6), (7-8) | 490 ±20% | (1-2), (9-10) | 365 ±18% | 400 |
| **CPLE Series - Low Core Loss for Light Load Efficiency** | | | | | | | | | | |
| CPLE-2-50TR-R | 2 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (1-2) | 365 ±18% | (3-4) | 365 ±18% | 300 |
| CPLE-3-50TR-R | 3 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4) | 490 ±20% | (1-2) , (5-6) | 365 ±18% | 400 |
| CPLE-4-50TR-R | 4 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6) | 490 ±20% | (1-2) , (7-8) | 365 ±18% | 400 |
| CPLE-5-50TR-R | 5 | 0.0005 | 0.0006 | 50 ± 20% | 40 | (3-4), (5-6), (7-8) | 490 ±20% | (1-2) , (9-10) | 365 ±18% | 400 |

1 OCL (Open Circuit Inductance)
2 Test parameters: 1MHz, 0.1$V_{rms}$, 0.0Adc.
3 The rated current and rated inductance per phase is determined by Volterra's testing and circuit design. Additional information can be provided by contacting Volterra.
4 Part Number Definition: CPLx-y-50TR-R-50TR-R
- CPLx= Product code and size - CPL (standard)/CPLA (acoustic dampening)/CPLE (low core loss)
- -y= number of phases • -50 = rated inductance value per phase in nH
- TR= Tape and reel • -R suffix= RoHS compliant

A This device is licensed for use only when incorporated within a voltage regulator employing power regulating devices manufactured by Volterra® Semiconductor Corporation. No license is granted expressly or by implication to use this device with power regulating devices manufactured by any company other than Volterra.

## Dimensions - mm



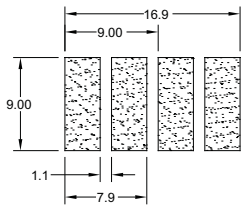




Part Marking: Coiltronics logo CPL/CPLA/CPLE = Product Code and Size -y (-2, -3, -4 & -5, -6) = Number of Phases -50 = Inductance value per phase wwllyy = Date code R = Revision level

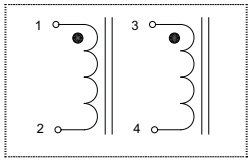
## Pad Layouts & Schematics - mm

CPL-2-50-R

Recommended Pad Layout

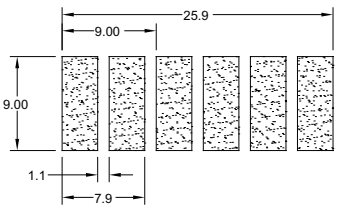



Schematic

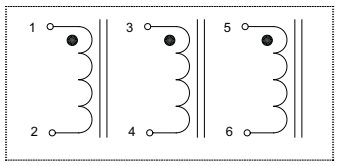



CPL-3-50-R

Recommended Pad Layout

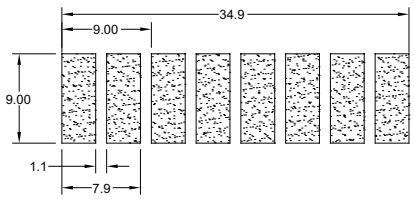



Schematic

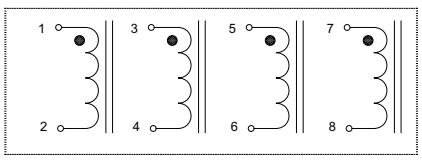



CPL-4-50-R

Recommended Pad Layout

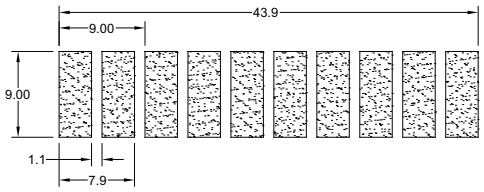



Schematic




CPL-5-50-R

Recommended Pad Layout

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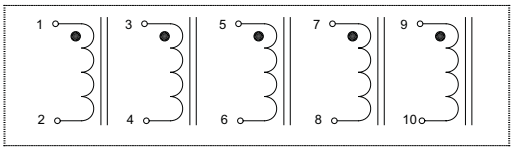
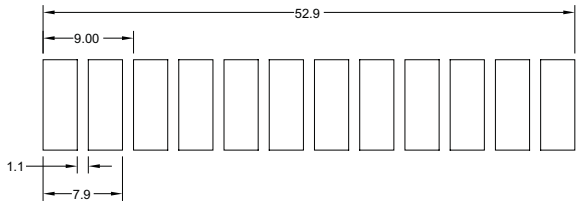
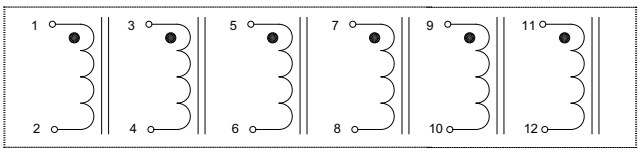



CPL-6-50-R

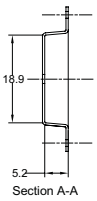


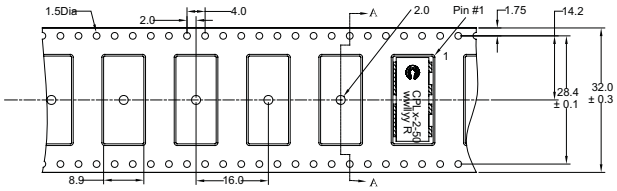




All dimensions ±0.2mm unless otherwise specified.

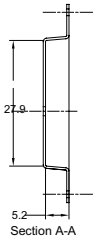
## Packaging Information - mm

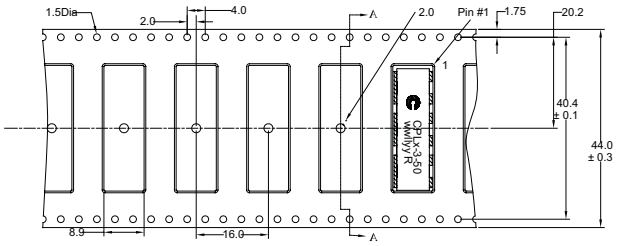
CPLx-2-50



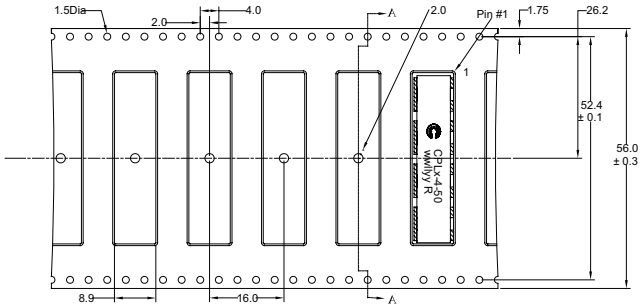




CPLx-3-50

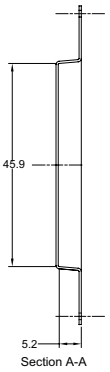


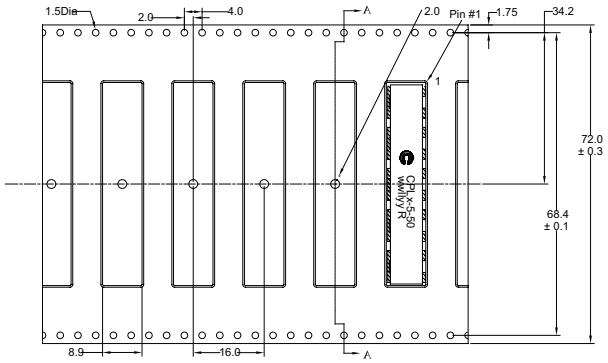




CPLx-4-50

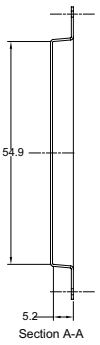



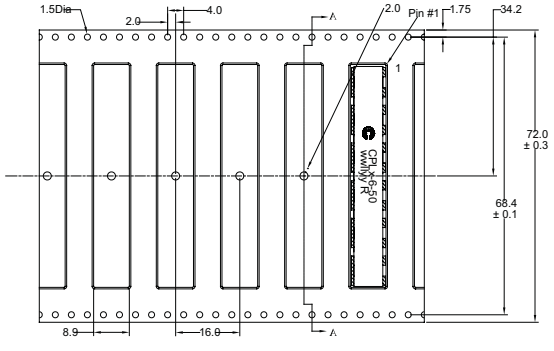

CPLx-5-50




CPLx-6-50

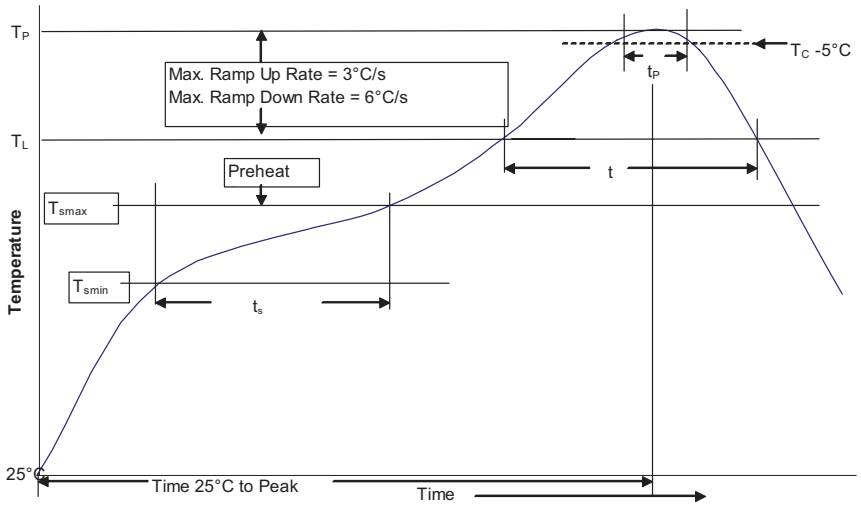



Supplied in tape-and-reel packaging, 750 parts per reel, 13” diameter reel.

User direction of feed

## Solder Reflow Profile




### Table 1 - Standard SnPb Solder ($T_C$)

| Package Thickness | Volume mm³ <350 | Volume mm³ ≥350 |
|---|---|---|
| <2.5mm | 235°C | 220°C |
| ≥2.5mm | 220°C | 220°C |

### Table 2 - Lead (Pb) Free Solder ($T_C$)

| Package Thickness | Volume mm³ <350 | Volume mm³ 350 - 2000 | Volume mm³ >2000 |
|---|---|---|---|
| <1.6mm | 260°C | 260°C | 260°C |
| 1.6 – 2.5mm | 260°C | 250°C | 245°C |
| >2.5mm | 250°C | 245°C | 245°C |

## Reference JDEC J-STD-020D

| Profile Feature | | Standard SnPb Solder | Lead (Pb) Free Solder |
|---|---|---|---|
| Preheat and Soak | • Temperature min. ($T_{smin}$) | 100°C | 150°C |
| | • Temperature max. ($T_{smax}$) | 150°C | 200°C |
| | • Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | 60-120 Seconds | 60-120 Seconds |
| Average ramp up rate $T_{smax}$ to $T_p$ | | 3°C/ Second Max. | 3°C/ Second Max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | | 183°C<br>60-150 Seconds | 217°C<br>60-150 Seconds |
| Peak package body temperature ($T_P$)* | | Table 1 | Table 2 |
| Time ($t_p$)** within 5 °C of the specified classification temperature ($T_C$) | | 20 Seconds** | 30 Seconds** |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | | 6°C/ Second Max. | 6°C/ Second Max. |
| Time 25°C to Peak Temperature | | 6 Minutes Max. | 8 Minutes Max. |

* Tolerance for peak profile temperature ($T_p$) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum.

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