DAC121C081/ DAC121C085 12-Bit Micro Power Digital-to-Analog Converter with an I²C-Compatible Interface

Check for Samples: DAC121C081, DAC121C085

FEATURES

- **Guaranteed Monotonicity to 12-Bits**
- **Low Power Operation: 156 µA Max @ 3.3V**
- **Extended Power Supply Range (+2.7V to +5.5V)**
- **I²C-Compatible 2-Wire Interface Which Supports Standard (100kHz), Fast (400kHz), and High Speed (3.4MHz) Modes**
- **Rail-to-Rail Voltage Output**
- **Very Small Package**

APPLICATIONS

- **Industrial Process Control**
- **Portable Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage & Current Sources**
- **Test Equipment**

KEY SPECIFICATIONS

- **Resolution: 12 bits**
- **INL: ±8 LSB (max)**
- **DNL: +0.6 / -0.5 LSB (max)**
- **Settling Time: 8.5 µs (max)**
- **Zero Code Error: +10 mV (max)**
- **Full-Scale Error: −0.7 %FS (max)**
- **Supply Power**
  - **Normal: 380 µW (3V) / 730 µW (5V) typ**
  - **Power Down: 0.5 µW (3V) / 0.9 µW (5V) typ**

DESCRIPTION

The DAC121C081 is a 12-bit, single channel, voltage-output digital-to-analog converter (DAC) that operates from a +2.7V to 5.5V supply. The output amplifier allows rail-to-rail output swing and has an 8.5µsec settling time. The DAC121C081 uses the supply voltage as the reference to provide the widest dynamic output range and typically consumes 132µA while operating at 5.0V. It is available in 6-lead SOT and WSON packages and provides three address options (pin selectable).

As an alternative, the DAC121C085 provides nine I²C addressing options and uses an external reference. It has the same performance and settling time as the DAC121C081. It is available in an 8-lead VSSOP.

The DAC121C081 and DAC121C085 use a 2-wire, I²C-compatible serial interface that operates in all three speed modes, including high speed mode (3.4MHz). An external address selection pin allows up to three DAC121C081 or nine DAC121C085 devices per 2-wire bus. Pin compatible alternatives to the DAC121C081 are available that provide additional address options.

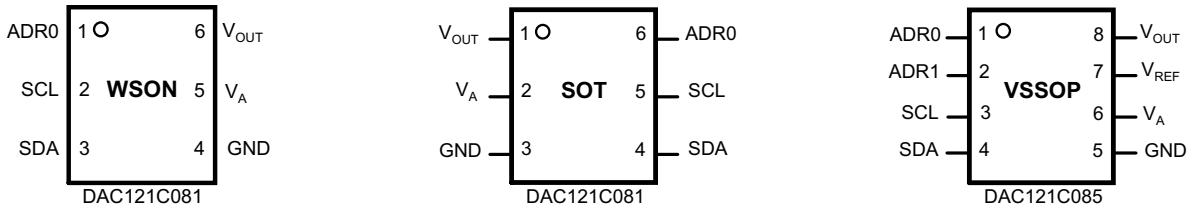
The DAC121C081 and DAC121C085 each have a 16-bit register that controls the mode of operation, the power-down condition, and the output voltage. A power-on reset circuit ensures that the DAC output powers up to zero volts. A power-down feature reduces power consumption to less than a microWatt. Their low power consumption and small packages make these DACs an excellent choice for use in battery operated equipment. Each DAC operates over the extended industrial temperature range of −40°C to +125°C.

The DAC121C081 and DAC121C085 are each part of a family of pin compatible DACs that also provide 8 and 10 bit resolution. For 8-bit DACs see the DAC081C081 and DAC081C085. For 10-bit DACs see the DAC101C081 and DAC101C085.

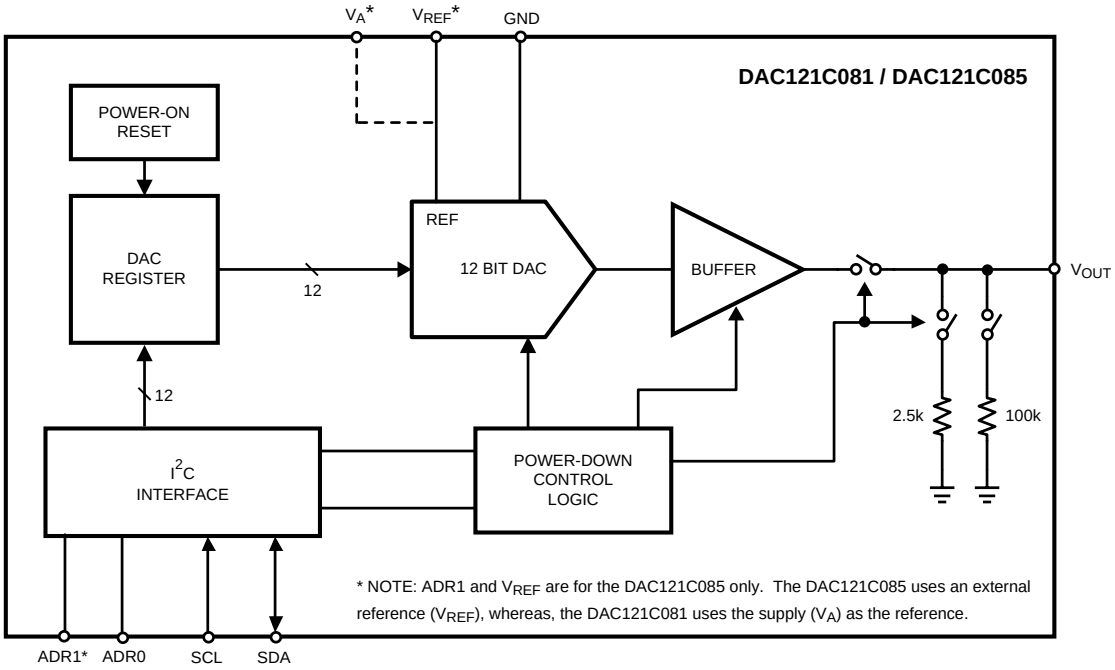
Pin-Compatible Alternatives
All devices are fully pin and function compatible.

Resolution	SOT-6 and WSONP-6 Packages	VSSOP-8 Package w/ External Reference
12-bit	DAC121C081	DAC121C085
10-bit	DAC101C081	DAC101C085
8-bit	DAC081C081	DAC081C085

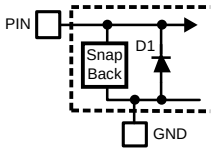
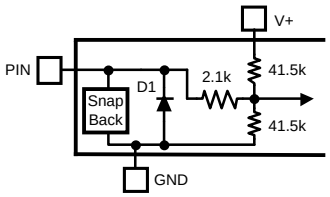
Connection Diagrams



Block Diagram



PIN DESCRIPTIONS

Symbol	Type	Equivalent Circuit	Description
V_{OUT}	Analog Output		Analog Output Voltage.
V_A	Supply		Power supply input. For the SOT and WSON versions, this supply is used as the reference. Must be decoupled to GND.
GND	Ground		Ground for all on-chip circuitry.
SDA	Digital Input/Output		Serial Data bi-directional connection. Data is clocked into or out of the internal 16-bit register relative to the clock edges of SCL. This is an open drain data line that must be pulled to the supply (V_A) by an external pull-up resistor.
SCL	Digital Input		Serial Clock Input. SCL is used together with SDA to control the transfer of data in and out of the device.
ADR0	Digital Input, three levels		Tri-state Address Selection Input. Sets the two Least Significant Bits (A1 & A0) of the 7-bit slave address. (see Table 1)
ADR1	Digital Input, three levels		Tri-state Address Selection Input. Sets Bits A6 & A3 of the 7-bit slave address. (see Table 1)
V_{REF}	Supply		Unbufferred reference voltage. For the VSSOP, this supply is used as the reference. V_{REF} must be free of noise and decoupled to GND.
PAD (LLP only)	Ground		Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

Package Pinouts

	V_{OUT}	V_A	GND	SDA	SCL	ADR0	ADR1	V_{REF}	PAD (WSON only)
SOT	1	2	3	4	5	6	N/A	N/A	N/A
WSON	6	5	4	3	2	1	N/A	N/A	7
VSSOP	8	6	5	4	3	1	2	7	N/A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

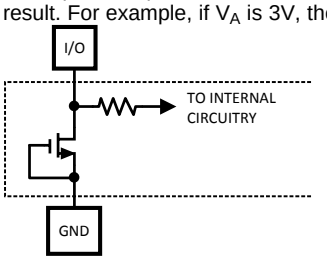
Supply Voltage, V_A			−0.3V to +6.5V
Voltage on any Input Pin			−0.3V to +6.5V
Input Current at Any Pin(4)			±10 mA
Package Input Current(4)			±20 mA
Power Consumption at T_A = 25°C			See(5)
ESD Susceptibility(6)	V_A, GND, V_{REF}, V_{OUT}, ADR0, ADR1 pins	Human Body Model	2500V
		Machine Model	250V
		Charged Device Model (CDM)	1000V
	SDA, SCL pins	Human Body Model	5000V
		Machine Model	350V
		Charged Device Model (CDM)	1000V
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5V or is less than GND, the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).
(6) Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is a 220 pF capacitor discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings(1)(2)

Operating Temperature Range	$-40°C \le T_A \le +125°C$
Supply Voltage, V_A	+2.7V to 5.5V
Reference Voltage, V_{REFIN}	+1.0V to V_A
Digital Input Voltage(3)	0.0V to 5.5V
Output Load	0 to 1500 pF

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) The inputs are protected as shown below. Input voltage magnitudes up to 5.5V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3V, the digital input pins can be driven with a 5V logic device.



Package Thermal Resistances[1][2]

Package	θ_{JA}
6-Lead SOT	250°C/W
6-Lead WSON	190°C/W
8-Lead VSSOP	240°C/W

(1) *Soldering process must comply with Texas Instruments' Reflow Temperature Profile specifications. Refer to* http://www.ti.com/packaging (SNOA549)
(2) Reflow temperature profiles are different for lead-free packages.

Electrical Characteristics

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = +2.7V to +5.5V, $V_{REF} = V_A$, C_L = 200 pF to GND, input code range 48 to 4047. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Typical[1]	Limits[1]	Units (Limits)
STATIC PERFORMANCE					
	Resolution			**12**	Bits (min)
	Monotonicity			**12**	Bits (min)
INL	Integral Non-Linearity		+2.2	**+8**	LSB (max)
			−1.5	**−8**	LSB (min)
DNL	Differential Non-Linearity		+0.18	**+0.6**	LSB (max)
			−0.12	**−0.5**	LSB (min)
ZE	Zero Code Error	I_{OUT} = 0	+1.1	**+10**	mV (max)
FSE	Full-Scale Error	I_{OUT} = 0	−0.1	**−0.7**	%FSR (max)
GE	Gain Error	All ones Loaded to DAC register	−0.2	**−0.7**	%FSR (max)
ZCED	Zero Code Error Drift		−20		µV/°C
TC GE	Gain Error Tempco	V_A = 3V	−0.7		ppm FSR/°C
		V_A = 5V	−1.0		ppm FSR/°C
ANALOG OUTPUT CHARACTERISTICS (V_{OUT})					
	Output Voltage Range[2]	DAC121C085		**0** **V_{REF}**	V (min) V (max)
		DAC121C081		**0** **V_A**	V (min) V (max)
ZCO	Zero Code Output	V_A = 3V, I_{OUT} = 200 µA	1.3		mV
		V_A = 5V, I_{OUT} = 200 µA	7.0		mV
FSO	Full Scale Output	V_A = 3V, I_{OUT} = 200 µA	2.984		V
		V_A = 5V, I_{OUT} = 200 µA	4.989		V
I_{OS}	Output Short Circuit Current (I_{SOURCE})	V_A = 3V, V_{OUT} = 0V, Input Code = FFFh.	56		mA
		V_A = 5V, V_{OUT} = 0V, Input Code = FFFh.	69		mA
I_{OS}	Output Short Circuit Current (I_{SINK})	V_A = 3V, V_{OUT} = 3V, Input Code = 000h.	−52		mA
		V_A = 5V, V_{OUT} = 5V, Input Code = 000h.	−75		mA
I_O	Continuous Output Current[2]	Available on the DAC output		**11**	mA (max)
C_L	Maximum Load Capacitance	R_L = ∞	1500		pF
		R_L = 2kΩ	1500		pF
Z_{OUT}	DC Output Impedance		7.5		Ω
REFERENCE INPUT CHARACTERISTICS- (DAC121C085 only)					
V_{REF}	Input Range Minimum		0.2	**1.0**	V (min)
	Input Range Maximum			**V_A**	V (max)
	Input Impedance		120		kΩ

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = +2.7V to +5.5V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 48 to 4047. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Typical(1)	Limits(1)	Units (Limits)
LOGIC INPUT CHARACTERISTICS (SCL, SDA)						
V_{IH}	Input High Voltage				**0.7 x V_A**	V (min)
V_{IL}	Input Low Voltage				**0.3 x V_A**	V (max)
I_{IN}	Input Current				**±1**	µA (max)
C_{IN}	Input Pin Capacitance(3)				**3**	pF (max)
V_{HYST}	Input Hysteresis				**0.1 x V_A**	V (min)
LOGIC INPUT CHARACTERISTICS (ADR0, ADR1)						
V_{IH}	Input High Voltage				**V_A- 0.5V**	V (min)
V_{IL}	Input Low Voltage				**0.5**	V (max)
I_{IN}	Input Current				**±1**	µA (max)
LOGIC OUTPUT CHARACTERISTICS (SDA)						
V_{OL}	Output Low Voltage	I_{SINK} = 3 mA			**0.4**	V (max)
		I_{SINK} = 6 mA			**0.6**	V (max)
I_{OZ}	High-Impedence Output Leakage Current				**±1**	µA (max)
POWER REQUIREMENTS						
V_A	Supply Voltage Minimum				**2.7**	V (min)
	Supply Voltage Maximum				**5.5**	V (max)
Normal -- V_{OUT} set to midscale. 2-wire interface quiet (SCL = SDA = V_A). (output unloaded)						
I_{ST_VA-1}	V_A**DAC121C081** Supply Current		V_A = 2.7V to 3.6V	105	**156**	µA (max)
			V_A = 4.5V to 5.5V	132	**214**	µA (max)
I_{ST_VA-5}	V_A**DAC121C085** Supply Current		V_A = 2.7V to 3.6V	86	**118**	µA (max)
			V_A = 4.5V to 5.5V	98	**152**	µA (max)
I_{ST_VREF}	V_{REF} Supply Current (DAC121C085 only)		V_A = 2.7V to 3.6V	37	**43**	µA (max)
			V_A = 4.5V to 5.5V	53	**61**	µA (max)
P_{ST}	Power Consumption (V_A & V_{REF} for DAC121C085)(4)		V_A = 3.0V	380		µW
			V_A = 5.0V	730		µW
Continuous Operation -- 2-wire interface actively addressing the DAC and writing to the DAC register. (output unloaded)						
I_{CO_VA-1}	V_A**DAC121C081** Supply Current	f_{SCL}=400kHz	V_A = 2.7V to 3.6V	134	**220**	µA (max)
			V_A = 4.5V to 5.5V	192	**300**	µA (max)
		f_{SCL}=3.4MHz	V_A = 2.7V to 3.6V	225	**320**	µA (max)
			V_A = 4.5V to 5.5V	374	**500**	µA (max)
I_{CO_VA-5}	V_A**DAC121C085** Supply Current	f_{SCL}=400kHz	V_A = 2.7V to 3.6V	101	**155**	µA (max)
			V_A = 4.5V to 5.5V	142	**220**	µA (max)
		f_{SCL}=3.4MHz	V_A = 2.7V to 3.6V	193	**235**	µA (max)
			V_A = 4.5V to 5.5V	325	**410**	µA (max)
I_{CO_VREF}	V_{REF} Supply Current (DAC121C085 only)		V_A = 2.7V to 3.6V	33.5	**55**	µA (max)
			V_A = 4.5V to 5.5V	49.5	**71.4**	µA (max)
P_{CO}	Power Consumption (V_A & V_{REF} for DAC121C085)	f_{SCL}=400kHz	V_A = 3.0V	480		µW
			V_A = 5.0V	1.06		mW
		f_{SCL}=3.4MHz	V_A = 3.0V	810		µW
			V_A = 5.0V	2.06		mW

(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) To ensure accuracy, it is required that V_A and V_{REF} be well bypassed.

Electrical Characteristics (continued)

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = +2.7V to +5.5V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 48 to 4047. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Typical[1]	Limits[1]	Units (Limits)
Power Down -- 2-wire interface quiet (SCL = SDA = V_A) after PD mode written to DAC register. (output unloaded)						
I_{PD}	Supply Current (V_A & V_{REF} for DAC121C085)	All Power Down Modes	V_A = 2.7V to 3.6V	0.13	**1.52**	µA (max)
			V_A = 4.5V to 5.5V	0.15	**3.25**	µA (max)
P_{PD}	Power Consumption (V_A & V_{REF} for DAC121C085)	All Power Down Modes	V_A = 3.0V	0.5		µW
			V_A = 5.0V	0.9		µW

A.C. and Timing Characteristics

Values shown in this table are design targets and are subject to change before product release.
The following specifications apply for V_A = +2.7V to +5.5V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions[1]	Typical[2]	Limits[1][2]	Units (Limits)
t_s	Output Voltage Settling Time[3]	400h to C00h code change R_L = 2kΩ, C_L = 200 pF	6	**8.5**	µs (max)
SR	Output Slew Rate		1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh	12		nV-sec
	Digital Feedthrough		0.5		nV-sec
	Multiplying Bandwidth[4]	V_{REF} = 2.5V ± 0.1Vpp	160		kHz
	Total Harmonic Distortion[4]	V_{REF} = 2.5V ± 0.1Vpp input frequency = 10kHz	70		dB
t_{WU}	Wake-Up Time	V_A = 3V	0.8		µsec
		V_A = 5V	0.5		µsec
DIGITAL TIMING SPECS (SCL, SDA)					
f_{SCL}	Serial Clock Frequency	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**100** **400** **3.4** **1.7**	kHz (max) kHz (max) MHz (max) MHz (max)
t_{LOW}	SCL Low Time	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**4.7** **1.3** **160** **320**	µs (min) µs (min) ns (min) ns (min)
t_{HIGH}	SCL High Time	Standard Mode Fast Mode High Speed Mode, C_b = 100pF High Speed Mode, C_b = 400pF		**4.0** **0.6** **60** **120**	µs (min) µs (min) ns (min) ns (min)
$t_{SU;DAT}$	Data Setup Time	Standard Mode Fast Mode High Speed Mode		**250** **100** **10**	ns (min) ns (min) ns (min)

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.
(2) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) Applies to the Multiplying DAC configuration. In this configuration, the reference is used as the analog input. The value loaded in the DAC Register will digitally attenuate the signal at Vout.

A.C. and Timing Characteristics (continued)

Values shown in this table are design targets and are subject to change before product release.

The following specifications apply for V_A = +2.7V to +5.5V, $V_{REF} = V_A$, R_L = Infinity, C_L = 200 pF to GND. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions[1]	Typical[2]	Limits[1][2]	Units (Limits)
$t_{HD;DAT}$	Data Hold Time	Standard Mode		**0** **3.45**	µs (min) µs (max)
		Fast Mode		**0** **0.9**	µs (min) µs (max)
		High Speed Mode, C_b = 100pF		**0** **70**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**0** **150**	ns (min) ns (max)
$t_{SU;STA}$	Setup time for a start or a repeated start condition	Standard Mode Fast Mode High Speed Mode		**4.7** **0.6** **160**	µs (min) µs (min) ns (min)
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard Mode Fast Mode High Speed Mode		**4.0** **0.6** **160**	µs (min) µs (min) ns (min)
t_{BUF}	Bus free time between a stop and start condition	Standard Mode Fast Mode		**4.7** **1.3**	µs (min) µs (min)
$t_{SU;STO}$	Setup time for a stop condition	Standard Mode Fast Mode High Speed Mode		**4.0** **0.6** **160**	µs (min) µs (min) ns (min)
t_{rDA}	Rise time of SDA signal	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)
t_{fDA}	Fall time of SDA signal	Standard Mode		**250**	ns (max)
		Fast Mode		**20+0.1C_b** **250**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)
t_{rCL}	Rise time of SCL signal	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **40**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **80**	ns (min) ns (max)
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit.	Standard Mode		**1000**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **80**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **160**	ns (min) ns (max)

A.C. and Timing Characteristics (continued)

Values shown in this table are design targets and are subject to change before product release.

The following specifications apply for V_A = +2.7V to +5.5V, $V_{REF} = V_A$, R_L = Infinity, C_L = 200 pF to GND. **Boldface limits apply for $T_{MIN} \le T_A \le T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions[1]	Typical[2]	Limits[1][2]	Units (Limits)
t_{fCL}	Fall time of a SCL signal	Standard Mode		**300**	ns (max)
		Fast Mode		**20+0.1C_b** **300**	ns (min) ns (max)
		High Speed Mode, C_b = 100pF		**10** **40**	ns (min) ns (max)
		High Speed Mode, C_b = 400pF		**20** **80**	ns (min) ns (max)
C_b	Capacitive load for each bus line (SCL and SDA)			**400**	pF (max)
t_{SP}	Pulse Width of spike suppressed[5][6]	Fast Mode High Speed Mode		**50** **10**	ns (max) ns (max)
t_{outz}	SDA output delay (see the ADDITIONAL TIMING INFORMATION: toutz section)	Fast Mode High Speed Mode	87 38	**270** **60**	ns (max) ns (max)

(5) Spike suppression filtering on SCL and SDA will supress spikes that are less than 50ns for standard-fast mode and less than 10ns for hs-mode.

(6) This parameter is specified by design and/or characterization and is not tested in production.

Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 4096 = V_A / 4096.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC output is not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (FFFh) loaded into the DAC and the value of V_A x 4095 / 4096.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Characteristics.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n \quad (1)$$

where V_{REF} is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 12 for the DAC121C081.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

MULTIPLYING BANDWIDTH is the frequency at which the output amplitude falls 3dB below the input sine wave on V_{REFIN} with a full-scale code loaded into the DAC.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

TOTAL HARMONIC DISTORTION (THD) is the measure of the harmonics present at the output of the DACs with an ideal sine wave applied to V_{REFIN}. THD is measured in dB.

WAKE-UP TIME is the time for the output to exit power-down mode. This time is measured from the rising edge of SCL during the ACK bit of the lower data byte to the time the output voltage deviates from the power-down voltage of 0V.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

Transfer Characteristic

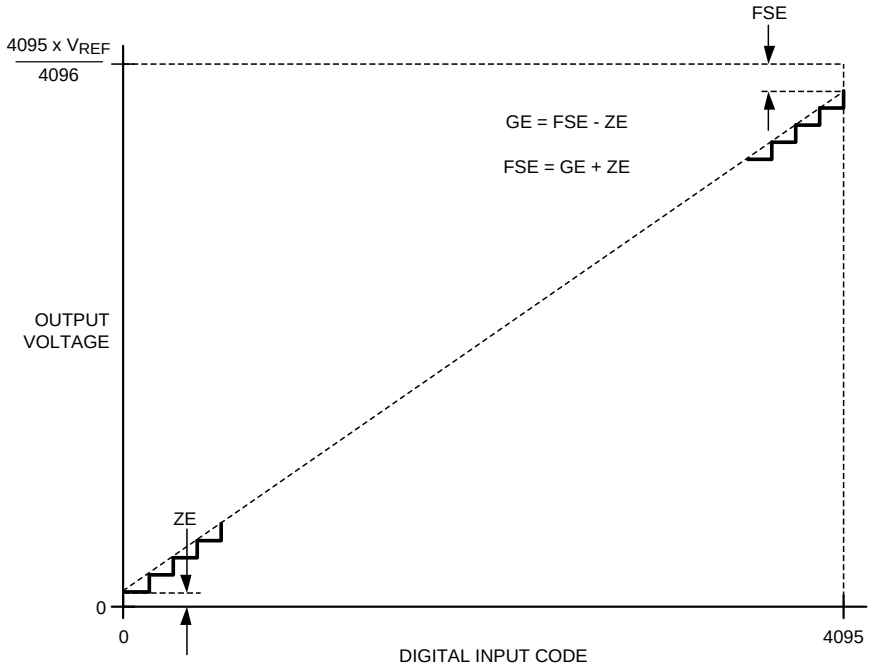


Figure 1. Input / Output Transfer Characteristic

Timing Diagrams

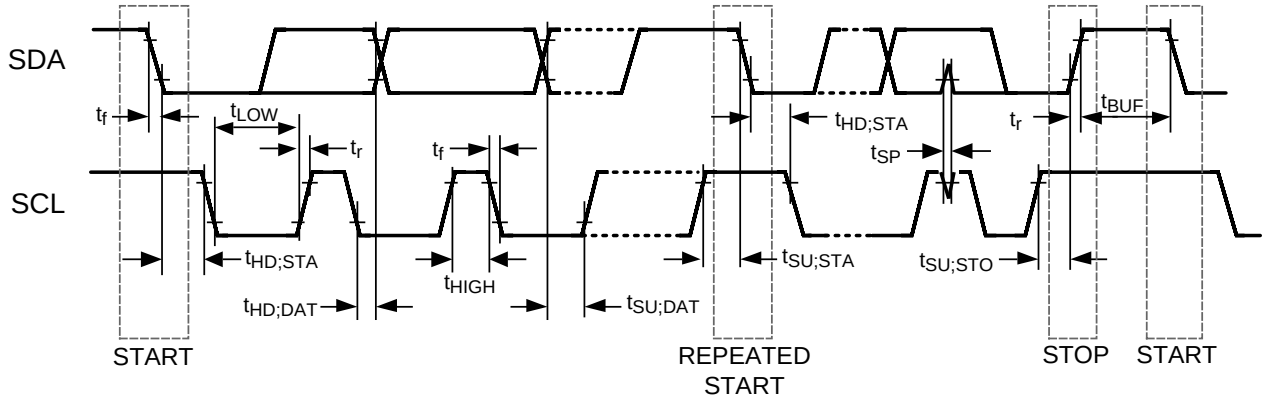


Figure 2. Serial Timing Diagram

Typical Performance Characteristics

$V_{REF} = V_A$, f_{SCL} = 3.4MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

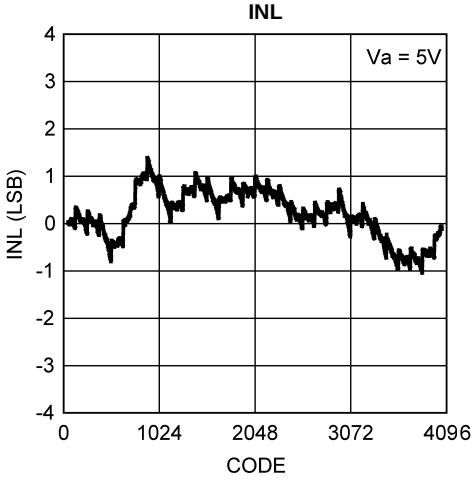


Figure 3.

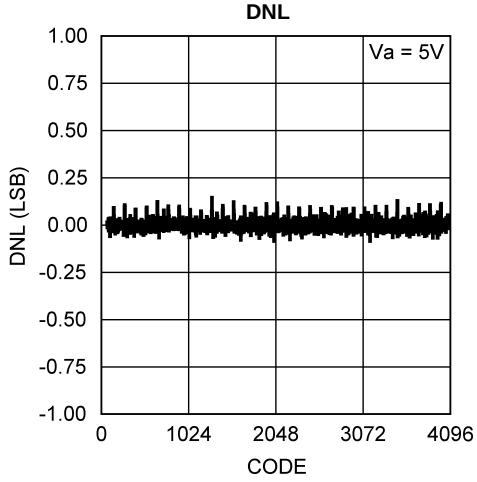


Figure 4.

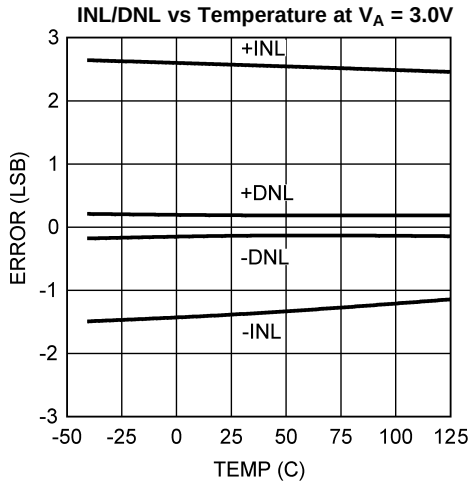


Figure 5.

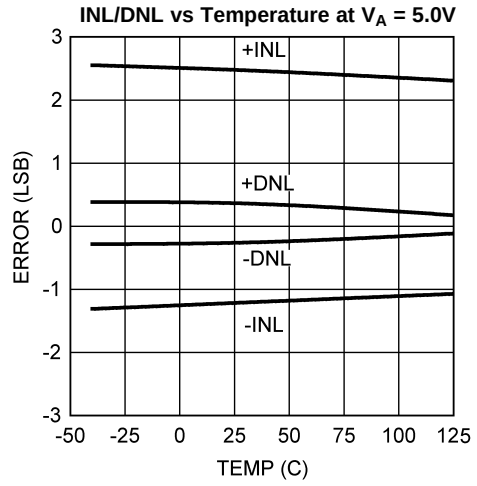


Figure 6.

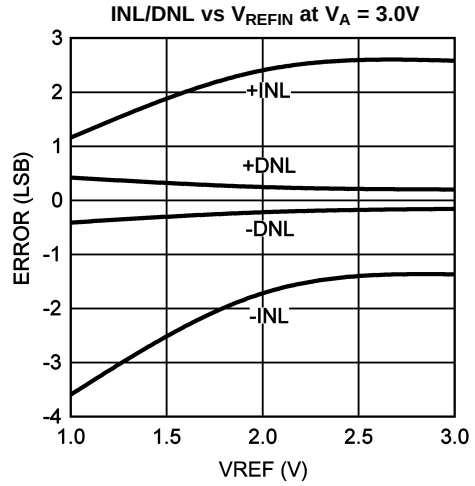


Figure 7.

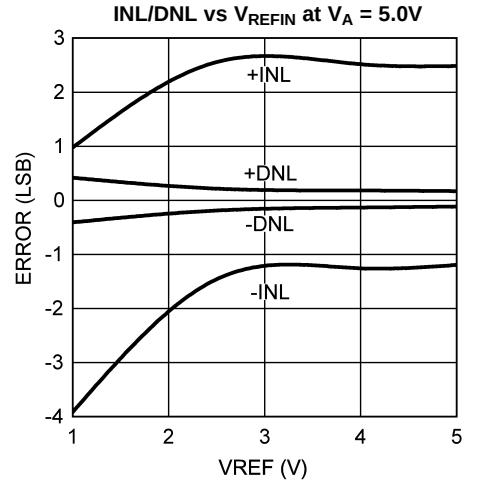


Figure 8.

Typical Performance Characteristics (continued)

$V_{REF} = V_A$, f_{SCL} = 3.4MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

INL/DNL vs V_A

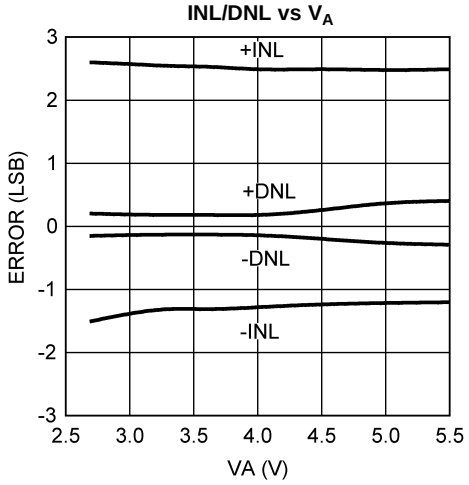


Figure 9.

Zero Code Error vs. V_A

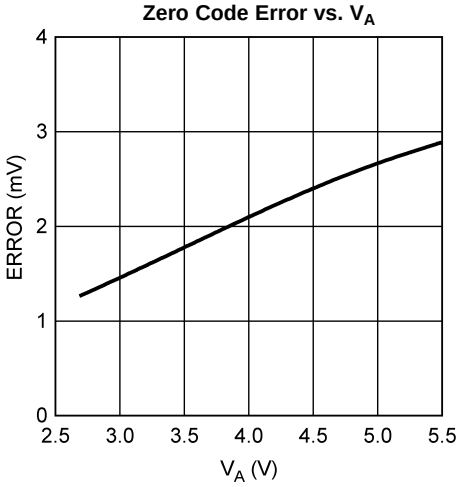


Figure 10.

Zero Code Error vs. Temperature

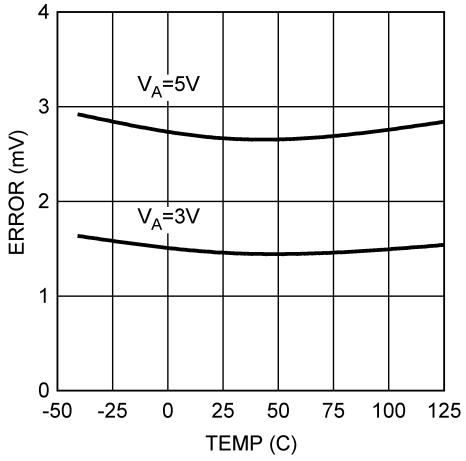


Figure 11.

Full Scale Error vs. V_A

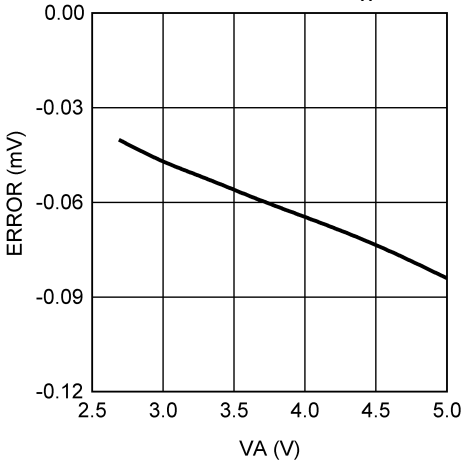


Figure 12.

Full Scale Error vs. Temperature

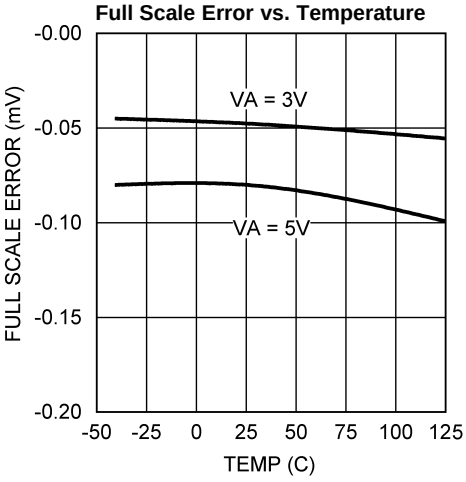


Figure 13.

Total Supply Current vs. V_A

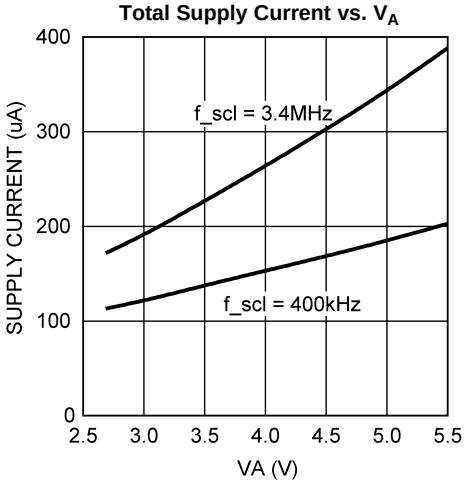


Figure 14.

Typical Performance Characteristics (continued)

V_{REF} = V_A, f_{SCL} = 3.4MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

V_{REF} Supply Current vs. V_A

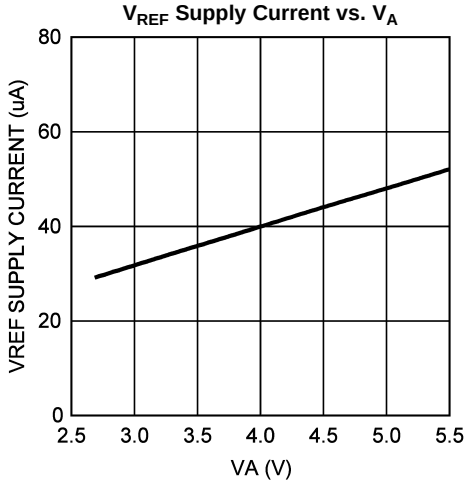


Figure 15.

Total Supply Current vs. Temperature @ V_A = 3V

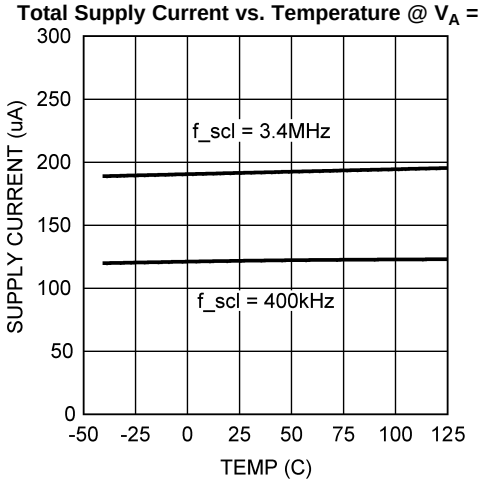


Figure 16.

Total Supply Current vs. Temperature @ V_A = 5V

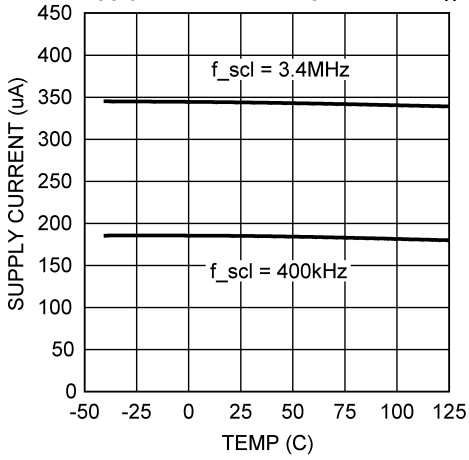


Figure 17.

5V Glitch Response

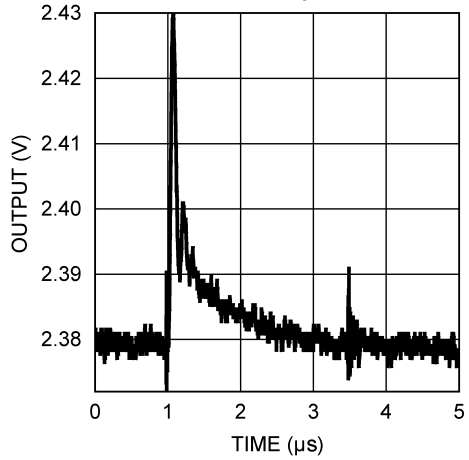


Figure 18.

Power-On Reset

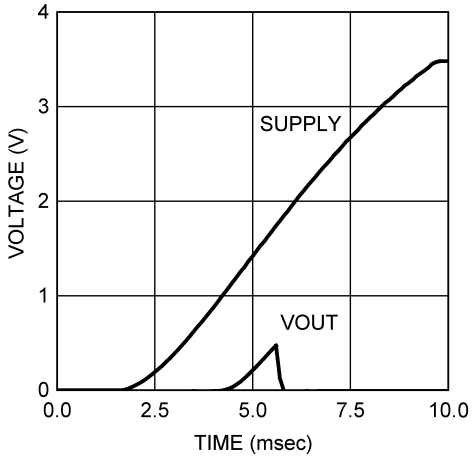


Figure 19.

FUNCTIONAL DESCRIPTION

DAC SECTION

The DAC121C081 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

For simplicity, a single resistor string is shown in Figure 20. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_{REF} \times (D / 4096) \quad (2)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register. D can take on any integer value between 0 and 4095. This configuration ensures that the DAC is monotonic.

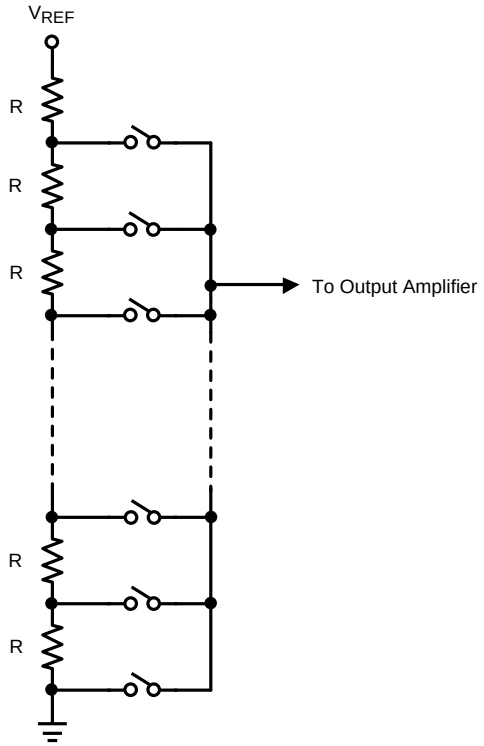


Figure 20. DAC Resistor String

OUTPUT AMPLIFIER

The output amplifier is rail-to-rail, providing an output voltage range of 0V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in the Electrical Characteristics.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the Electrical Characteristics.

REFERENCE VOLTAGE

The DAC121C081 uses the supply (V_A) as the reference. With that said, V_A must be treated as a reference. The Analog output will only be as clean as the reference (V_A). It is recommended that the reference be driven by a voltage source with low output impedance.

The DAC121C085 comes with an external reference supply pin (V_{REF}). For the DAC121C085, it is important that V_{REF} be kept as clean as possible.

The Applications Information section describes a handful of ways to drive the reference appropriately. Refer to the USING REFERENCES AS POWER SUPPLIES section for details.

SERIAL INTERFACE

The I^2C-compatible interface operates in all three speed modes. Standard mode (100kHz) and Fast mode (400kHz) are functionally the same and will be referred to as Standard-Fast mode in this document. High-Speed mode (3.4MHz) is an extension of Standard-Fast mode and will be referred to as Hs-mode in this document. The following diagrams describe the timing relationships of the clock (SCL) and data (SDA) signals. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed.

Basic I^2C Protocol

The I^2C interface is bi-directional and allows multiple devices to operate on the same bus. To facilitate this bus configuration, each device has a unique hardware address which is referred to as the "slave address." To communicate with a particular device on the bus, the controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit. If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a Stop condition on the bus.

All communication on the bus begins with either a Start condition or a Repeated Start condition. The protocol for starting the bus varies between Standard-Fast mode and Hs-mode. In Standard-Fast mode, the master generates a Start condition by driving SDA from high to low while SCL is high. In Hs-mode, starting the bus is more complicated. Please refer to the High-Speed (Hs) Mode section for the full details of a Hs-mode Start condition. A Repeated Start is generated to either address a different device, or switch between read and write modes. The master generates a Repeated Start condition by driving SDA low while SCL is high. Following the Repeated Start, the master sends out the slave address and a read/write bit as shown in Figure 21. The bus continues to operate in the same speed mode as before the Repeated Start condition.

All communication on the bus ends with a Stop condition. In either Standard-Fast mode or Hs-Mode, a Stop condition occurs when SDA is pulled from low to high while SCL is high. After a Stop condition, the bus remains idle until a master generates a Start condition.

Please refer to the Phillips $I^2C^{®}$ Specification (Version 2.1 Jan, 2000) for a detailed description of the serial interface.

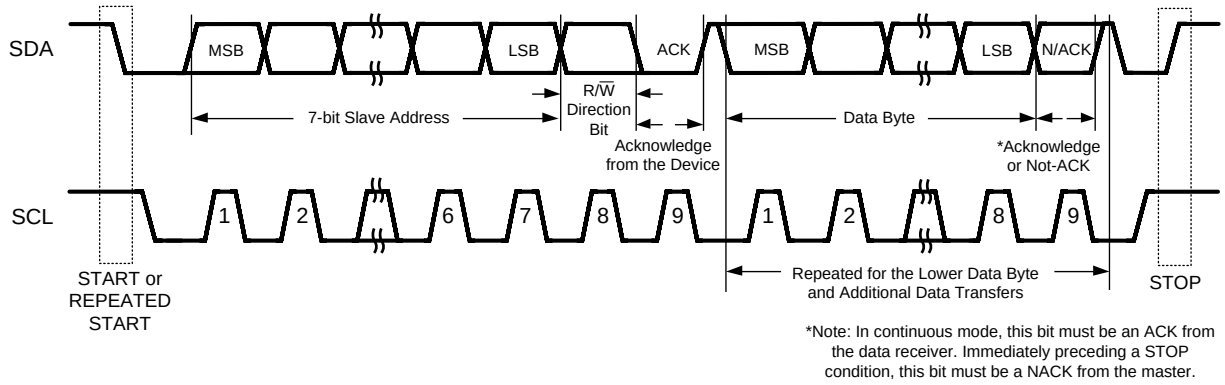


Figure 21. Basic Operation.

Standard-Fast Mode

In Standard-Fast mode, the master generates a start condition by driving SDA from high to low while SCL is high. The Start condition is always followed by a 7-bit slave address and a Read/Write bit. After these eight bits have been transmitted by the master, SDA is released by the master and the DAC121C081 either ACKs or NACKs the address. If the slave address matches, the DAC121C081 ACKs the master. If the address doesn't match, the DAC121C081 NACKs the master.

For a **write** operation, the master follows the ACK by sending the upper eight data bits to the DAC121C081. Then the DAC121C081 ACKs the transfer by driving SDA low. Next, the lower eight data bits are sent by the master. The DAC121C081 then ACKs the transfer. At this point, the DAC output updates to reflect the contents of the 16-bit DAC register. Next, the master either sends another pair of data bytes, generates a Stop condition to end communication, or generates a Repeated Start condition to communicate with another device on the bus.

For a **read** operation, the DAC121C081 sends out the upper eight data bits of the DAC register. This is followed by an ACK by the master. Next, the lower eight data bits of the DAC register are sent to the master. The master then produces a NACK by letting SDA be pulled high. The NACK is followed by a master-generated Stop condition to end communication on the bus, or a Repeated Start to communicate with another device on the bus.

High-Speed (Hs) Mode

For Hs-mode, the sequence of events to begin communication differ slightly from Standard-Fast mode. Figure 22 describes this in further detail. Initially, the bus begins running in Standard-Fast mode. The master generates a Start condition and sends the 8-bit Hs master code (00001XXX) to the DAC121C081. Next, the DAC121C081 responds with a NACK. Once the SCL line has been pulled to a high level, the master switches to Hs-mode by increasing the bus speed and generating a Repeated Start condition (driving SDA low while SCL is pulled high). At this point, the master sends the slave address to the DAC121C081, and communication continues as shown above in the "Basic Operation" Diagram (see Figure 21).

When the master generates a Repeated Start condition while in Hs-mode, the bus stays in Hs-mode awaiting the slave address from the master. The bus continues to run in Hs-mode until a Stop condition is generated by the master. When the master generates a Stop condition on the bus, the bus must be started in Standard-Fast mode again before increasing the bus speed and switching to Hs-mode. ns16705

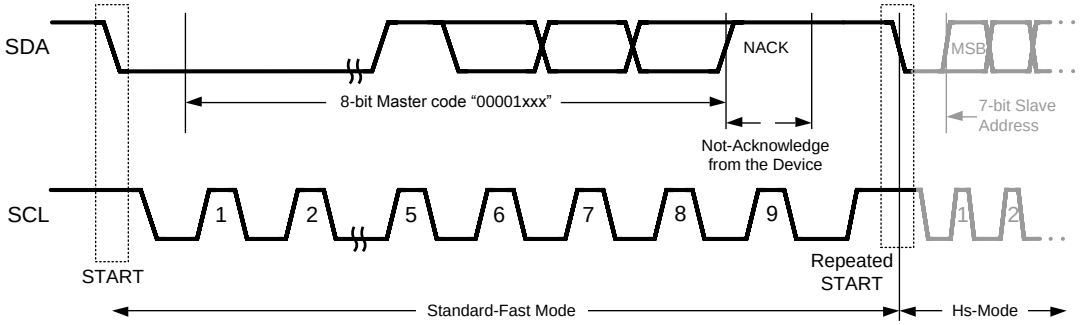


Figure 22. Beginning Hs-Mode Communication

I²C Slave (Hardware) Address

The DAC has a seven-bit I²C slave address. For the VSSOP version of the DAC, this address is configured by the ADR0 and ADR1 address selection inputs. For the DAC121C081, the address is configured by the ADR0 address selection input. ADR0 and ADR1 can be grounded, left floating, or tied to V_A. If desired, the address selection inputs can be set to $V_A/2$ rather than left floating. The state of these inputs sets the address the DAC responds to on the I²C bus (see Table 1). In addition to the selectable slave address, there is also a broadcast address (1001000) for all DAC121C081's and DAC121C085's on the 2-wire bus. When the bus is addressed by the broadcast address, all the DAC121C081's and DAC121C085's will respond and update synchronously. Figure 23 and Figure 24 describe how the master device should address the DAC via the I²C-Compatible interface.

Keep in mind that the address selection inputs (ADR0 and ADR1) are only sampled until the DAC is correctly addressed with a non-broadcast address. At this point, the ADR0 and ADR1 inputs TRI-STATE and the slave address is "locked". Changes to ADR0 and ADR1 will not update the selected slave address until the device is power-cycled.

Table 1. Slave Addresses

Slave Address [A6 - A0]	DAC121C085 (VSSOP)		DAC121C081 (SOT & WSON) *
	ADR1	ADR0	ADR0
0001100	Floating	Floating	Floating
0001101	Floating	GND	GND
0001110	Floating	V_A	V_A
0001000	GND	Floating	----------
0001001	GND	GND	----------
0001010	GND	V_A	----------
1001100	V_A	Floating	----------
1001101	V_A	GND	----------
1001110	V_A	V_A	----------
1001000	---------- Broadcast Address ----------		

* Pin-compatible alternatives to the DAC121C081 options are available with additional address options.

Writing to the DAC Register

To write to the DAC, the master addresses the part with the correct slave address (A6-A0) and writes a "zero" to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. The master then sends out the upper data byte. The DAC responds by sending an ACK to the master. Next, the master sends the lower data byte to the DAC. The DAC responds by sending an ACK again. At this point, the master either sends the upper byte of the next data word to be converted by the DAC, generates a Stop condition to end communication, or generates a Repeated Start condition to begin communication with another device on the bus. Until generating a Stop condition, the master can continuously write the upper and lower data bytes to the DAC register. This allows for a maximum DAC conversion rate of 188.9 kilo-conversions per second in Hs-mode.

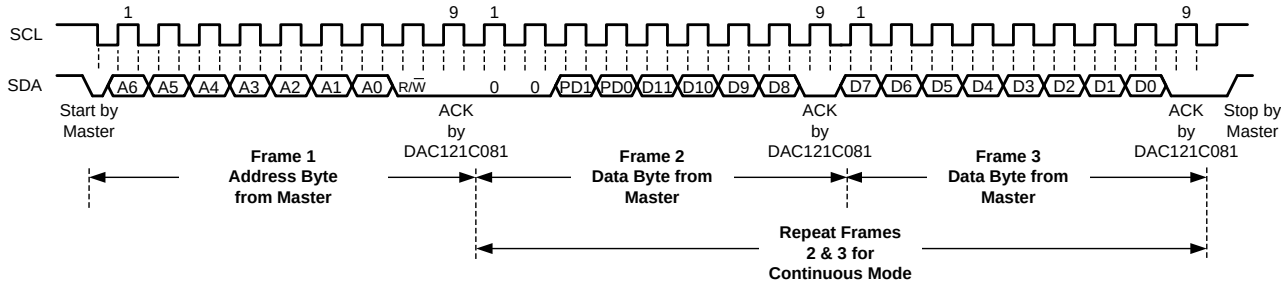


Figure 23. Typical Write to the DAC Register

Reading from the DAC Register

To read from the DAC register, the master addresses the part with the correct slave address (A6-A0) and writes a "one" to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. Next, the DAC sends out the upper data byte. The master responds by sending an ACK to the DAC to indicate that it wants to receive another data byte. Then the DAC sends the lower data byte to the master. Assuming only one 16-bit data word is read, the master sends a NACK after receiving the lower data byte. At this point, the master either generates a Stop condition to end communication, or a Repeated Start condition to begin communication with another device on the bus.

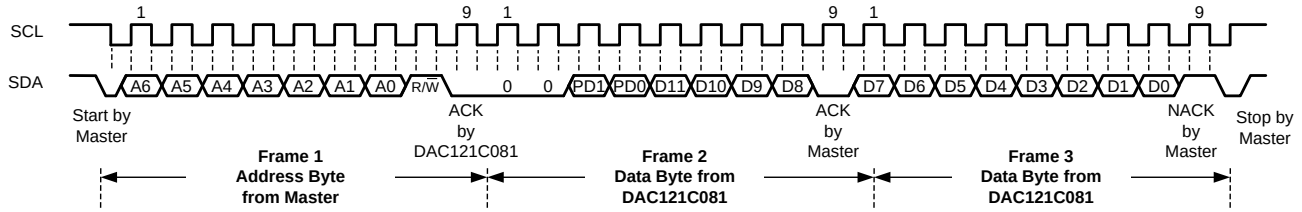


Figure 24. Typical Read from the DAC Register

DAC REGISTER

The DAC register, Figure 25, has sixteen bits. The first two bits are always zero. The next two bits determine the mode of operation (normal mode or one of three power-down modes). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with twelve 0's corresponding to an output of 0V and twelve 1's corresponding to a full-scale output of V_A - 1 LSB. When writing to the DAC Register, V_{OUT} will update on the rising edge of the ACK following the lower data byte.

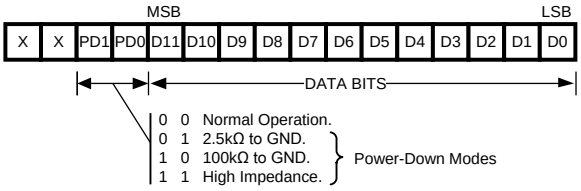


Figure 25. DAC Register Contents

POWER-ON RESET

The power-on reset circuit controls the output voltage of the DAC during power-up. Upon application of power, the DAC register is filled with zeros and the output voltage is 0 Volts. The output remains at 0V until a valid write sequence is made to the DAC.

When resetting the device, it is crutial that the V_A supply be lowered to a maximum of 200mV before the supply is raised again to power-up the device. Dropping the supply to within 200mV of GND during a reset will ensure the ADC performs as specified.

SIMULTANEOUS RESET

The broadcast address allows the I^2C master to write a single word to multiple DACs simultaneously. Provided that all of the DACs exist on a single I^2C bus, every DAC will update when the broadcast address is used to address the bus. This feature allows the master to reset all of the DACs on a shared I^2C bus to a specific digital code. For instance, if the master writes a power-down code to the bus with the broadcast address, all of the DACs will power-down simultaneously.

POWER-DOWN MODES

The DAC121C081 has three power-down modes. In power-down mode, the supply current drops to 0.13µA at 3V and 0.15µA at 5V (typ). The DAC121C081 is put into power-down mode by writing a one to PD1 and/or PD0. The outputs can be set to high impedance, terminated by 2.5 kΩ to GND, or terminated by 100 kΩ to GND (see Figure 25).

The bias generator, output amplifier, resistor string, and other linear circuitry are all shut down in any of the power-down modes. When the DAC121C081 is powered down, the value written to the DAC register, including the power-down bits, is saved. While the DAC is in power-down, the saved DAC register contents can be read back. When the DAC is brought out of power-down mode, the DAC register contents will be overwritten and V_{OUT} will be updated with the new 12-bit data value.

The time to exit power-down (Wake-Up Time) is typically 0.8µsec at 3V and 0.5µsec at 5V.

ADDITIONAL TIMING INFORMATION: t_{outz}

The t_{outz} specification is provided to aid the design of the I^2C bus. After the SCL bus is driven low by the I^2C master, the SDA bus will be held for a short time by the DAC121C081. This time is referred to as t_{outz}. The following figure illustrates the relationship between the fall of SCL, at the 30% threshold, to the time when the DAC begins to transition the SDA bus. The t_{outz} specification only applies when the DAC is in control of the SDA bus. The DAC is only in control of the bus during an ACK by the DAC121C081 or a data byte read from the DAC (see Figure 24).

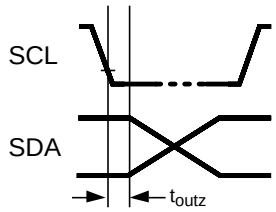


Figure 26. Data Output Timing

The t_{outz} specification is typically 87nsec in Standard-Fast Mode and 38nsec in Hs-Mode.

Applications Information

USING REFERENCES AS POWER SUPPLIES

While the simplicity of the DAC121C081 implies ease of use, it is important to recognize that the path from the reference input (V_A for the DAC121C081 & V_{REF} for the DAC121C085) to V_{OUT} will have essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to the reference. In order to use the full dynamic range of the DAC121C085, the supply pin (V_A) and V_{REF} can be connected together and share the same supply voltage. Since the DAC121C081 consumes very little power, a reference source may be used as the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC121C081. When using the DAC121C081, it is important to treat the analog supply (V_A) as the reference.

LM4132

The LM4132, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC121C081. The 4.096V version is useful if a 0 to 4.095V output range is desirable or acceptable. Bypassing the LM4132 V_{IN} pin with a 0.1µF capacitor and the V_{OUT} pin with a 2.2µF capacitor will improve stability and reduce output noise. The LM4132 comes in a space-saving 5-pin SOT-23.

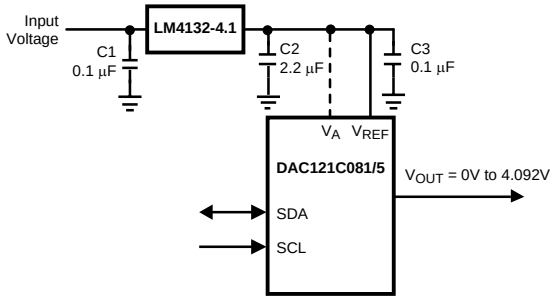


Figure 27. The LM4132 as a power supply

LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC121C081. It is available in 4.096V and 5V versions and comes in a space-saving 3-pin SOT-23.

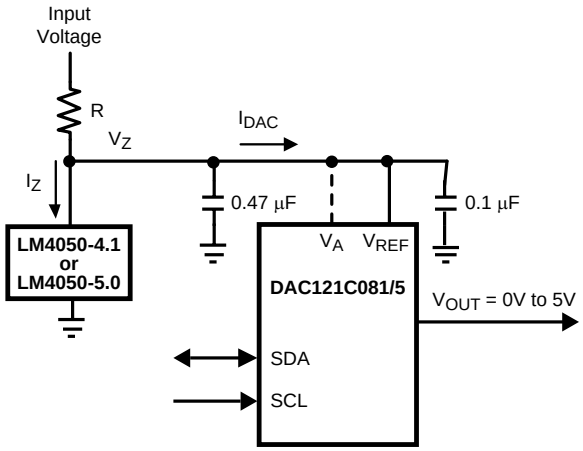


Figure 28. The LM4050 as a power supply

The minimum resistor value in the circuit of Figure 28 must be chosen such that the maximum current through the LM4050 does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC121C081 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC121C081 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC121C081 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max) \quad (3)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min)) \quad (4)$$

where $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature, $I_Z(max)$ is the maximum allowable current through the LM4050, $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation, and $I_{DAC}(max)$ is the maximum DAC121C081 supply current.

LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC121C081. It comes in 3.0V, 3.3V and 5V versions, among others, and sports a low 30 µV noise specification at low frequencies. Since low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

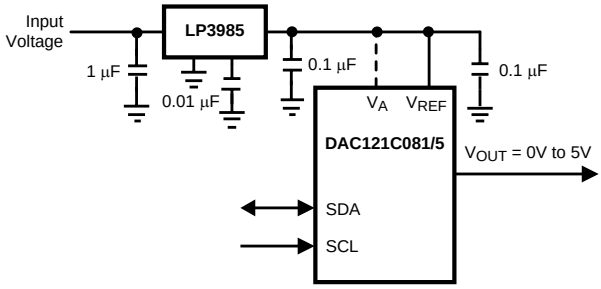


Figure 29. Using the LP3985 regulator

An input capacitance of 1.0µF without any ESR requirement is required at the LP3985 input, while a 1.0µF ceramic capacitor with an ESR requirement of 5mΩ to 500mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3.0V, 3.3V and 5V versions, among others.

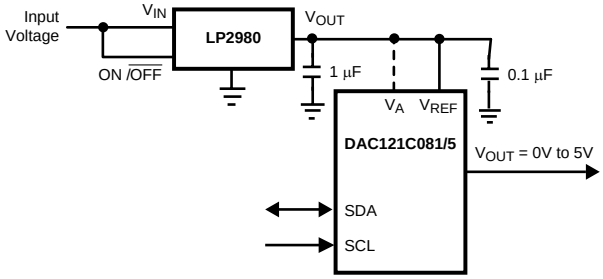


Figure 30. Using the LP2980 regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0µF over temperature, but values of 2.2µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

BIPOLAR OPERATION

The DAC121C081 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 31. This circuit will provide an output voltage range of ±5 Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5V.

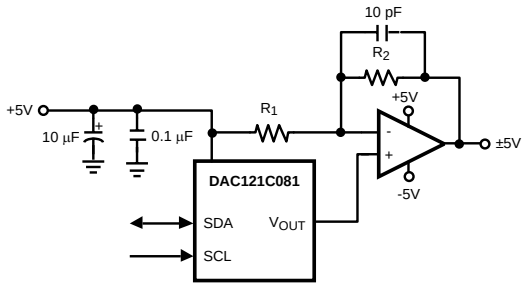


Figure 31. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R1) \quad (5)$$

where D is the input code in decimal form. With V_A = 5V and R1 = R2,

$$V_O = (10 \times D / 4096) - 5V \quad (6)$$

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 2.

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMP7701	SOT-23	37 uV	0.79 mA
LMV841	SC70-5	50 uV	1 mA
LMC7111	SOT-23	0.9 mV	25 µA
LM7301	SO-8, SOT-23	0.03 mV	620 µA
LM8261	SOT-23	0.7 mV	1 mA

DSP/MICROPROCESSOR INTERFACING

Interfacing the DAC121C081 to microprocessors and DSPs is quite simple. The following guidelines are offered to simplify the design process.

Interfacing to the 2-wire Bus

Figure 32 shows a microcontroller interfacing to the DAC121C081 via the 2-wire bus. Pull-up resistors (Rp) should be chosen to create an appropriate bus rise time and to limit the current that will be sunk by the open-drain outputs of the devices on the bus. Please refer to the $I^2C^®$ Specification for further details. Typical pull-up values to use in Standard-Fast mode bus applications are 2kΩ to 10kΩ. SCL and SDA series resisters (R_S) near the DAC121C081 are optional. If high-voltage spikes are expected on the 2-wire bus, series resistors should be used to filter the voltage on SDA and SCL. The value of the series resistance must be picked to ensure the V_{IL} threshold can be achieved. If used, R_S is typically 51Ω.

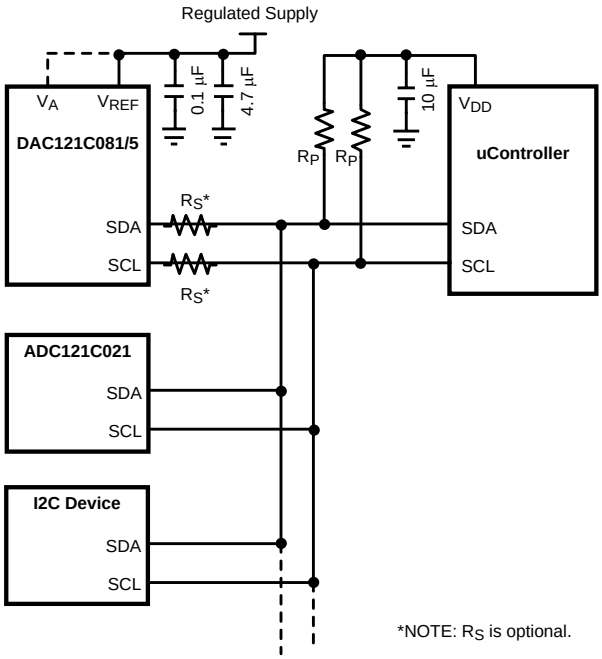


Figure 32. Serial Interface Connection Diagram

Interfacing to a Hs-mode Bus

Interfacing to a Hs-mode bus is very similar to interfacing to a Standard-Fast mode bus. In Hs-mode, the specified rise time of SCL is shortened. To create a faster rise time, the master device (microcontroller) can drive the SCL bus high and low. In other words, the microcontroller can drive the line high rather than leaving it to the pull-up resistor. It is also possible to decrease the value of the pull-up resistors or increase the pull-up current to meet the tighter timing specs. Please refer to the $I^2C^®$ Specification for further details.

LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC121C081 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located on the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC121C081. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC121C081 power supply should be bypassed with a 4.7µF and a 0.1µF capacitor as close as possible to the device with the 0.1µF right at the device supply pin. The 4.7µF capacitor should be a tantalum type and the 0.1µF capacitor should be a low ESL, low ESR type. The power supply for the DAC121C081 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. These clock and data lines should have controlled impedances.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC121C081CIMK/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C	Samples
DAC121C081CIMKX/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	X84C	Samples
DAC121C081CISD/NOPB	ACTIVE	WSON	NGF	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X87	Samples
DAC121C081CISDX/NOPB	ACTIVE	WSON	NGF	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X87	Samples
DAC121C085CIMM	NRND	VSSOP	DGK	8		TBD	Call TI	Call TI	-40 to 125	X90C	
DAC121C085CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X90C	Samples
DAC121C085CIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	X90C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

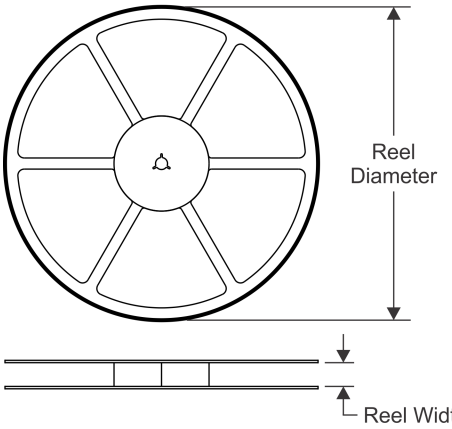
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

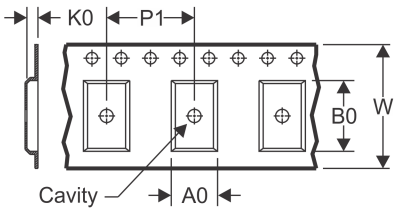
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

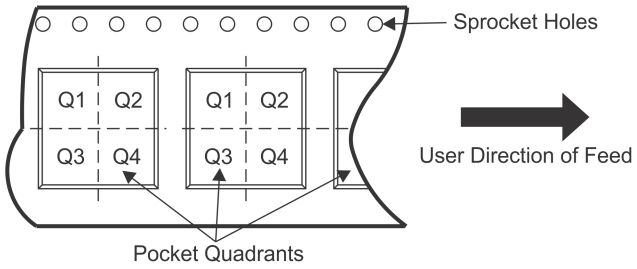


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

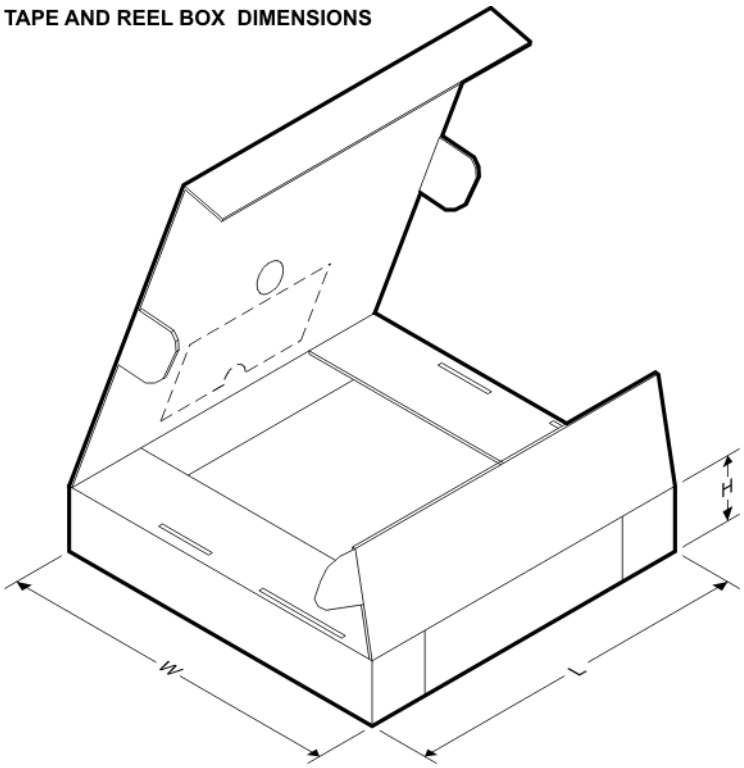
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC121C081CIMK/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121C081CIMKX/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC121C081CISD/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC121C081CISDX/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC121C085CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC121C085CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

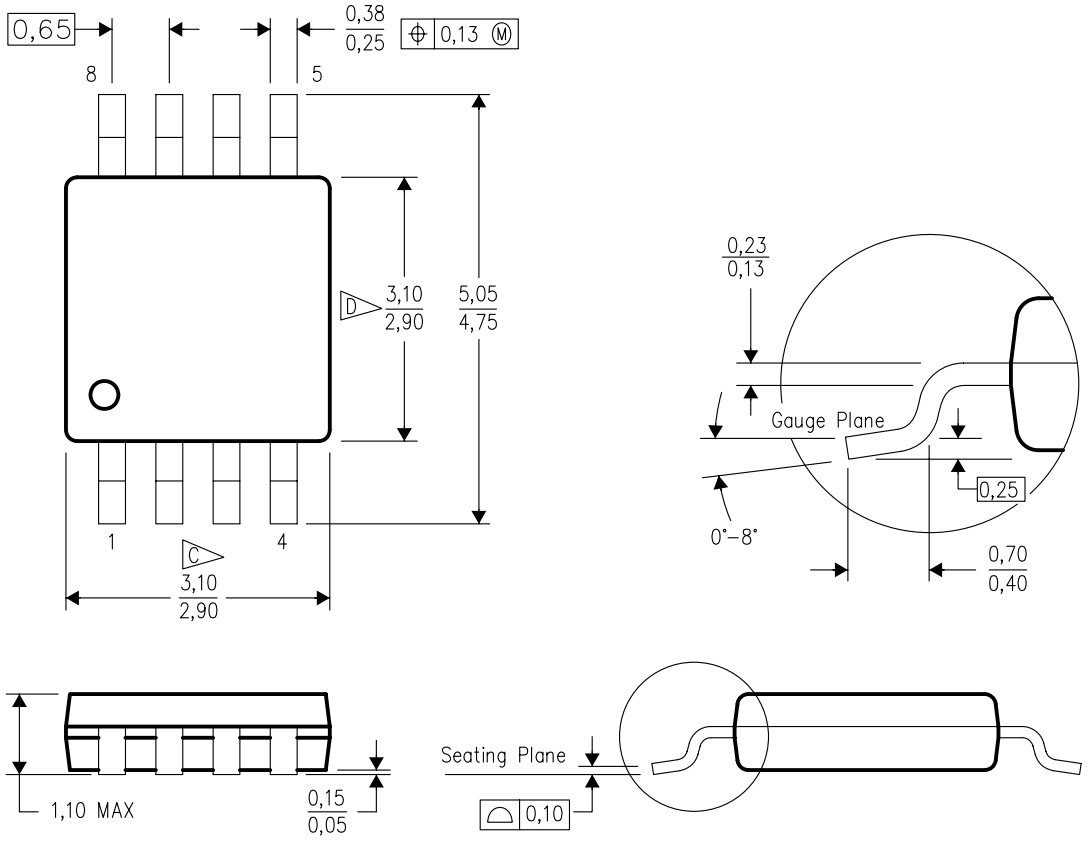
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC121C081CIMK/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
DAC121C081CIMKX/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0
DAC121C081CISD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
DAC121C081CISDX/NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
DAC121C085CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
DAC121C085CIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

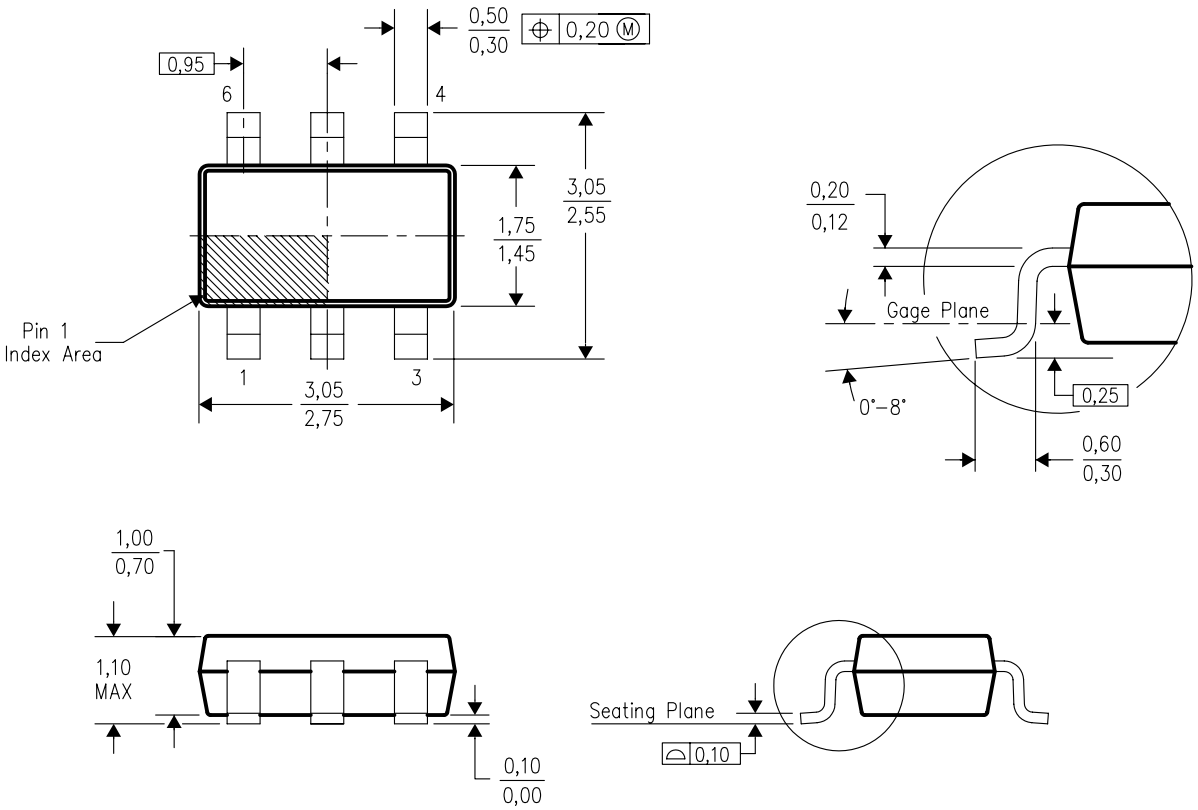
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

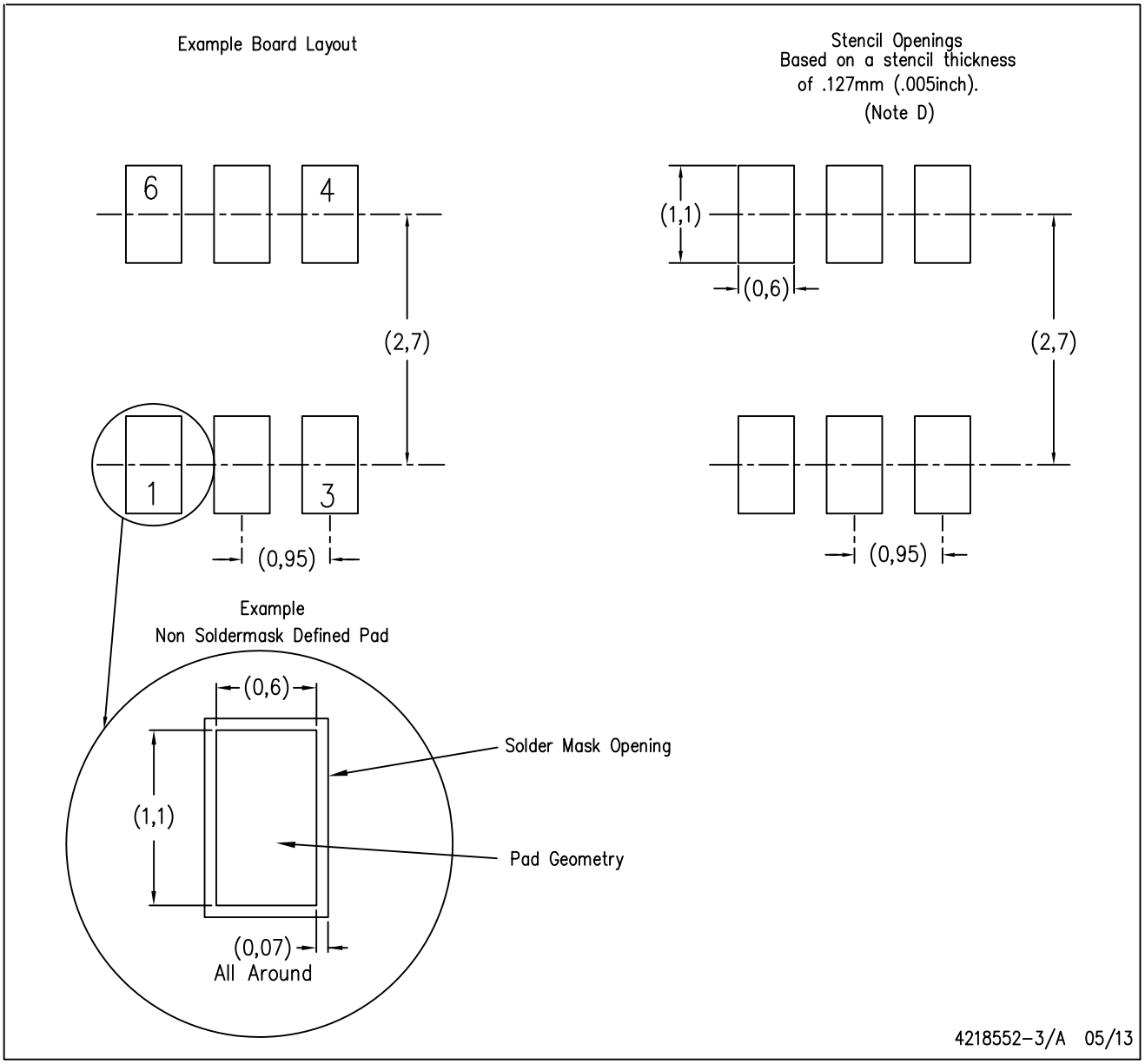
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

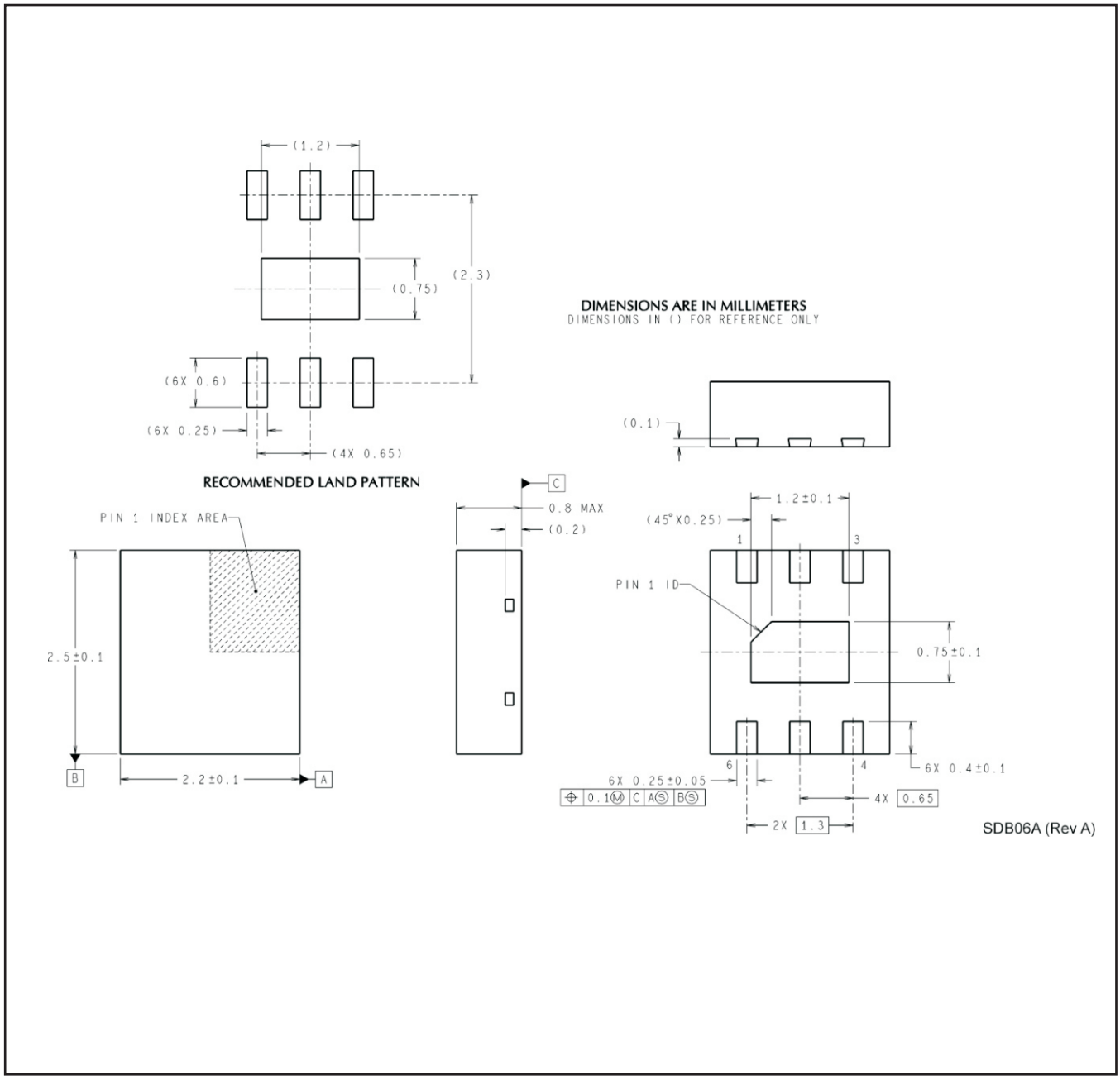
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

NGF0006A


(1.2)
(2.3)
(0.75)
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
2.5±0.1
2.2±0.1
B
A
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
6X 0.4±0.1
6X 0.25±0.05
0.10 M C A S B S
4X 0.65
2X 1.3
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DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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