Jameco Part Number 1759238

Coulomb Counter/ Battery Gas Gauge

FEATURES

- **Indicates Charge Quantity and Polarity**
- **±50mV Sense Voltage Range**
- Precision Timer Capacitor or Crystal Not Required
- 2.7V to 8.5V Operation
- High Side Sense
- 32.55Hz/V Charge Count Frequency
- 1.5µA Shutdown Current
- 10-Pin MSOP Package

APPLICATIONS

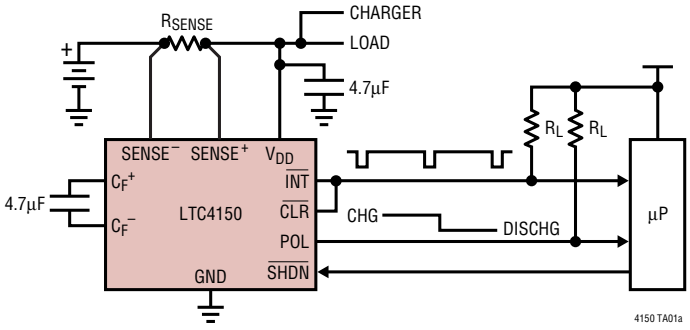
- Battery Chargers
- Palmtop Computers and PDAs
- Cellular Telephones and Wireless Modems

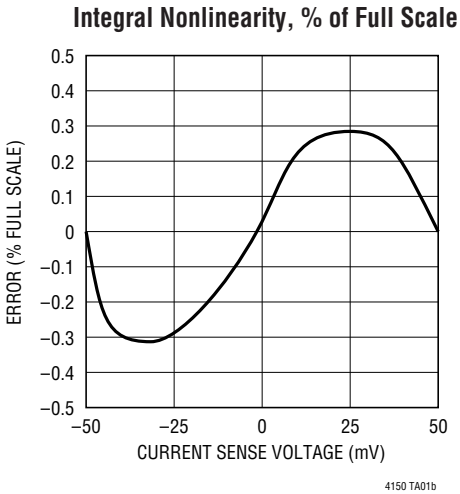
DESCRIPTION

The LTC®4150 measures battery depletion and charging in handheld PC and portable product applications. The device monitors current through an external sense resistor between the battery's positive terminal and the battery's load or charger. A voltage-to-frequency converter transforms the current sense voltage into a series of output pulses at the interrupt pin. These pulses correspond to a fixed quantity of charge flowing into or out of the battery. The part also indicates charge polarity as the battery is depleted or charged.

The LTC4150 is intended for 1-cell or 2-cell Li-Ion and 3-cell to 6-cell NiCd or NiMH applications.

TYPICAL APPLICATION



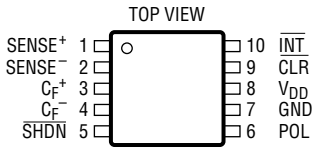


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{DD}) ..... –0.3V to 9V
Input Voltage Range
  Digital Inputs ($\overline{CLR}$, $\overline{SHDN}$) ..... –0.3V to (V_{DD} + 0.3)
  SENSE$^-$, SENSE$^+$, C_F^-, C_F^+ ..... –0.3V to (V_{DD} + 0.3)
Output Voltage Range
  Digital Outputs ($\overline{INT}$, POL) ..... –0.3V to 9V
Operating Temperature Range
  LTC4150CMS ..... 0°C to 70°C
  LTC4150IMS ..... –40°C TO 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LTC4150CMS LTC4150IMS
MS PART MARKING
LTQW

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 2.7V and 8.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	Digital Input Low Voltage, $\overline{CLR}$, $\overline{SHDN}$		●			0.7	V
V_{IH}	Digital Input High Voltage, $\overline{CLR}$, $\overline{SHDN}$		●	1.9			V
V_{OL}	Digital Output Low Voltage, $\overline{INT}$, POL	I_{OL} = 1.6mA, V_{DD} = 2.7V	●			0.5	V
I_{LEAK}	Digital Output Leakage Current, $\overline{INT}$, POL	V_{INT} = V_{POL} = 8.5V	●		0.01	1	µA
V_{OS}	Differential Offset Voltage (Note 4)	V_{DD} = 4.0V	 ●			±100 ±150	µV µV
		V_{DD} = 8.0V	 ●			±100 ±150	µV µV
		V_{DD} = 2.7V to 8.5V	 ●			±150 ±200	µV µV
$V_{SENSE(CM)}$	Sense Voltage Common Mode Input Range		●	V_{DD} – 0.06		V_{DD} + 0.06	V
V_{SENSE}	Sense Voltage Differential Input Range	SENSE$^+$ – SENSE$^-$	●	–0.05		0.05	V
R_{IDR}	Average Differential Input Resistance, Across SENSE$^+$ and SENSE$^-$	V_{DD} = 4.1V (Note 3)		155	270	390	kΩ
V_{UVLO}	Undervoltage Lockout Threshold	V_{DD} Rising	●		2.5	2.7	V
Power Supply Current							
I_{DD}	Supply Current, Operating	V_{DD} = 8.5V V_{DD} = 2.7V	● ●		115 80	140 100	µA µA
$I_{DD(SD)}$	Supply Current, Shutdown	V_{DD} = 8.5V V_{DD} = 2.7V	● ●			10 1.5	µA µA
AC Characteristics							
G_{VF}	Voltage to Frequency Gain	V_{SENSE} = 50mV to –50mV, 2.7V ≤ V_{DD} ≤ 8.5V	 ●	32.0 31.8	32.55	33.1 33.3	Hz/V Hz/V
$\Delta G_{VF}(V_{DD})$	Gain Variation with Supply	2.7V ≤ V_{DD} ≤ 8.5V		0		0.5	%/V
$\Delta G_{VF}(TEMP)$	Gain Variation with Temperature	(Note 2)	●	–0.03		0.03	%/ °C
INL	Integral Nonlinearity		 ●	–0.4 –0.5		0.4 0.5	% %
t_{CLR}	$\overline{CLR}$ Pulse Width to Reset $\overline{INT}$, $\overline{INT}$ and $\overline{CLR}$ Not Connected	Figure 2		20			µs
t_{INT}	$\overline{INT}$ Low Time, $\overline{INT}$ Connected to $\overline{CLR}$	Figure 3, C_L = 15pF	●	1			µs

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by design and not tested in production.

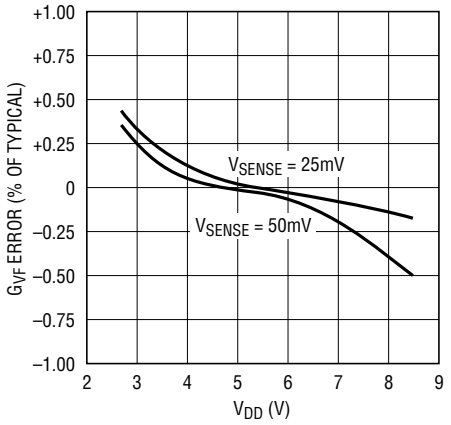
Note 3: Measured at least 20ms after power on.

Note 4: Tested in feedback loop to $SENSE^+$ and $SENSE^-$.

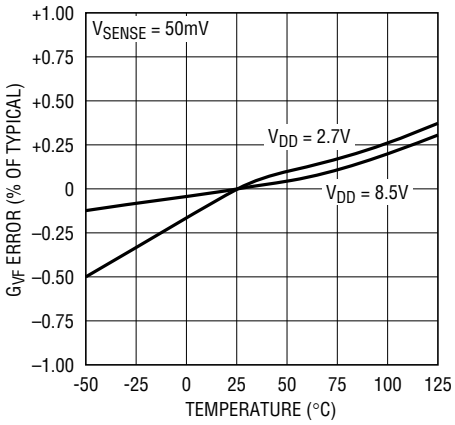
TYPICAL PERFORMANCE CHARACTERISTICS

(Specifications are at T_A = 25°C, unless otherwise noted.)

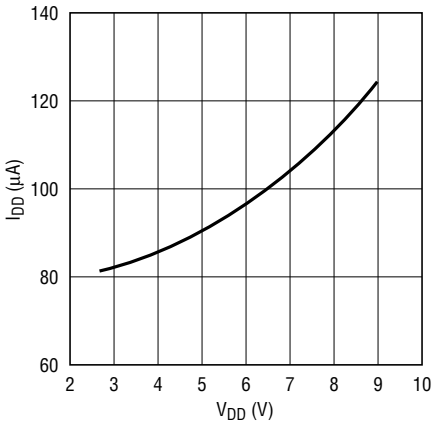
Voltage to Frequency Gain vs Supply Voltage



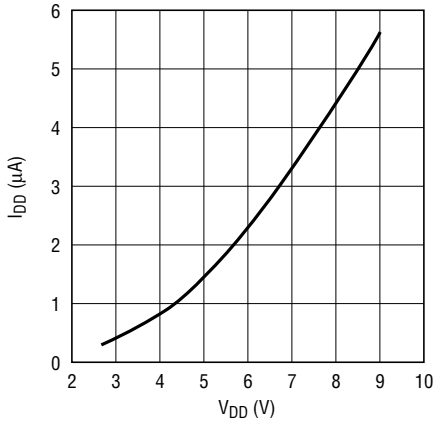
Voltage to Frequency Gain vs Temperature



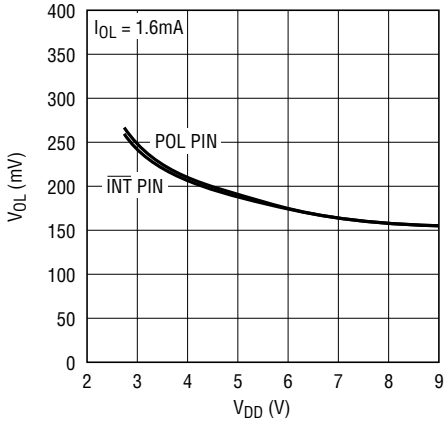
Operating I_{DD} vs V_{DD}



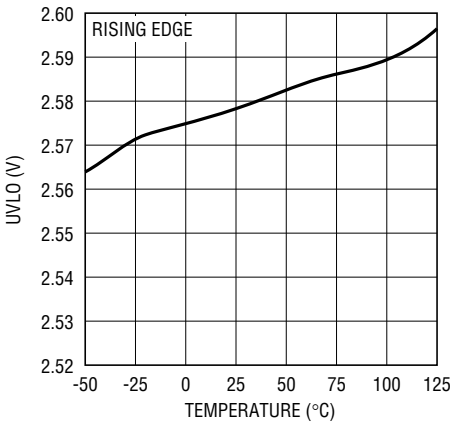
Shutdown I_{DD} vs V_{DD}



Digital Output Low Voltage vs V_{DD}



Undervoltage Lockout Threshold vs Temperature



PIN FUNCTIONS

SENSE+ (Pin 1): Positive Sense Input. This is the noninverting current sense input. Connect SENSE+ to the load and charger side of the sense resistor. Full-scale current sense input is 50mV. SENSE+ must be within 60mV of V_{DD} for proper operation.

SENSE– (Pin 2): Negative Sense Input. This is the inverting current sense input. Connect SENSE– to the positive battery terminal side of the sense resistor. Full-scale current sense input is 50mV. SENSE– must be within 60mV of V_{DD} for proper operation.

C_F^+ (Pin 3): Filter Capacitor Positive Input. A capacitor connected between C_F^+ and C_F^- filters and averages noise and fast battery current variations. A 4.7µF value is recommended. If filtering is not desired, leave C_F^+ and C_F^- unconnected.

C_F^- (Pin 4): Filter Capacitor Negative Input. A capacitor connected between C_F^+ and C_F^- filters and averages noise and fast battery current variations. A 4.7µF value is recommended. If filtering is not desired, leave C_F^+ and C_F^- unconnected.

$\overline{SHDN}$ (Pin 5): Shutdown Digital Input. When asserted low, $\overline{SHDN}$ forces the LTC4150 into its low current consumption power-down mode and resets the part. In applications with logic supply $V_{CC} > V_{DD}$, a resistive divider must be used between $\overline{SHDN}$ and the logic which drives it. See the Applications Information section.

POL (Pin 6): Battery Current Polarity Open-Drain Output. POL indicates the most recent battery current polarity when $\overline{INT}$ is high. A low state indicates the current is flowing out of the battery while high impedance means the current is going into the battery. POL latches its state when $\overline{INT}$ is asserted low. POL is an open-drain output and can be pulled up to any logic supply up to 9V. In shutdown, POL is high impedance.

GND (Pin 7): Ground. Connect directly to the negative battery terminal.

V_{DD} (Pin 8): Positive Power Supply. Connect to the load and charger side of the sense resistor. SENSE+ also connects to V_{DD}. V_{DD} operating range is 2.7V to 8.5V. Bypass V_{DD} with 4.7µF capacitor.

$\overline{CLR}$ (Pin 9): Clear Interrupt Digital Input. When asserted low for more than 20µs, $\overline{CLR}$ resets $\overline{INT}$ high. Charge counting is *unaffected*. $\overline{INT}$ may be directly connected to $\overline{CLR}$. In this case the LTC4150 will capture each assertion of $\overline{INT}$ and wait at least 1µs before resetting it. This ensures that $\overline{INT}$ pulses low for at least 1µs but gives automatic $\overline{INT}$ reset. In applications with a logic supply $V_{CC} > V_{DD}$, a resistive divider must be used between $\overline{INT}$ and $\overline{CLR}$. See the Applications Information section.

$\overline{INT}$ (Pin 10): Charge Count Interrupt Open-Drain Output. $\overline{INT}$ latches low every $1/(V_{SENSE} \bullet G_{VF})$ seconds and is reset by a low pulse at $\overline{CLR}$. $\overline{INT}$ is an open-drain output and can be pulled up to any logic supply of up to 9V. In shutdown $\overline{INT}$ is high impedance.

BLOCK DIAGRAM

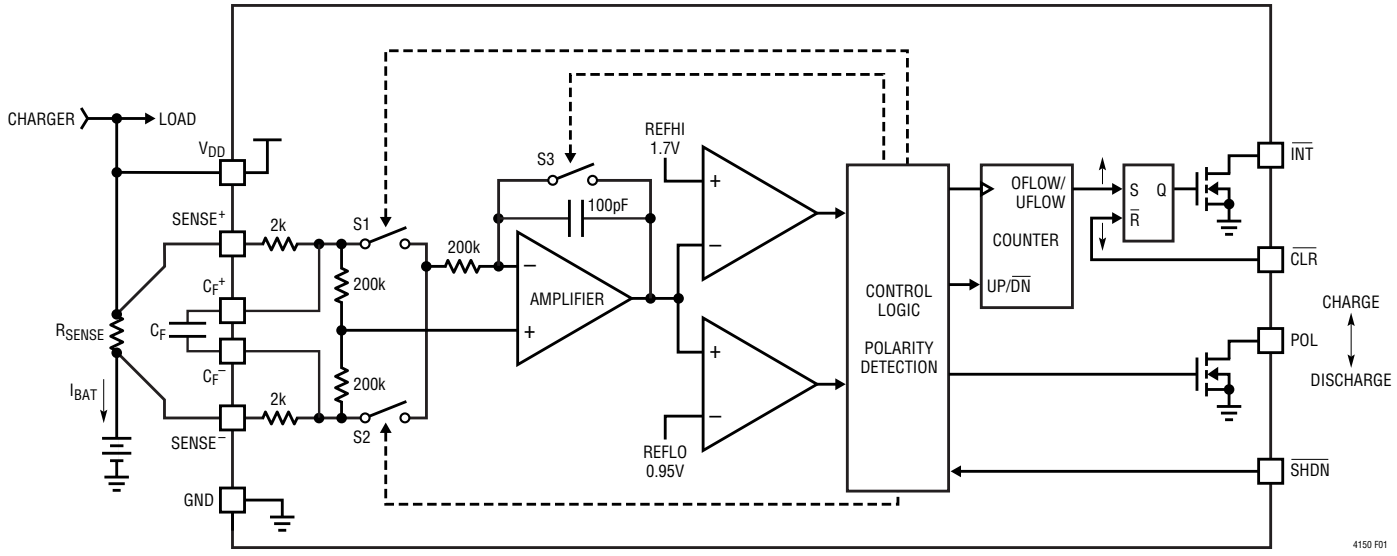


Figure 1. Block Diagram

TIMING DIAGRAMS

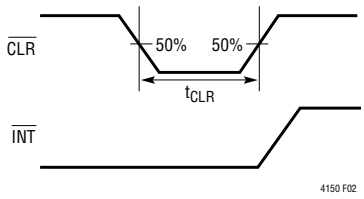


Figure 2. $\overline{CLR}$ Pulse Width to Reset $\overline{INT}$, $\overline{CLR}$ and $\overline{INT}$ Not Connected

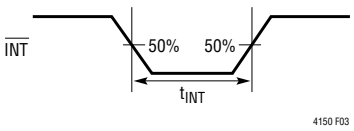


Figure 3. $\overline{INT}$ Minimum Pulse Width, $\overline{CLR}$ and $\overline{INT}$ Connected

OPERATION

Charge is the time integral of current. The LTC4150 measures battery current by monitoring the voltage developed across a sense resistor and then integrates this information in several stages to infer charge. The Block Diagram shows the stages described below. As each unit of charge passes into or out of the battery, the LTC4150 $\overline{INT}$ pin interrupts an external microcontroller and the POL pin reports the polarity of the charge unit. The external microcontroller then resets $\overline{INT}$ with the $\overline{CLR}$ input in preparation for the next interrupt issued by the LTC4150. The value of each charge unit is determined by the sense resistor value and the sense voltage to interupt frequency gain G_{VF} of the LTC4150.

Power-On and Start-Up Initialization

When power is first applied to the LTC4150, all internal circuitry is reset. After an initialization interval, the LTC4150 begins counting charge. This interval depends on V_{DD} and the voltage across the sense resistor but will be at least 5ms. It may take an additional 80ms for the LTC4150 to accurately track the sense voltage. An internal undervoltage lockout circuit monitors V_{DD} and resets all circuitry when V_{DD} falls below 2.5V.

Asserting $\overline{SHDN}$ low also resets the LTC4150's internal circuitry and reduces the supply current to 1.5μA. In this condition, POL and $\overline{INT}$ outputs are high impedance. The LTC4150 resumes counting after another initialization interval. Shutdown minimizes battery drain when both the charger and load are off.

CHARGE COUNTING

First, the current measurement is filtered by capacitor C_F connected across pins C_F^+ and C_F^-. This averages fast changes in current arising from ripple, noise and spikes in the load or charging current.

Second, the filter's output is applied to an integrator with the amplifier and 100pF capacitor at its core. When the integrator output ramps to REFHI or REFLO levels, switches S1 and S2 reverse the ramp direction. By observing the condition of S1 and S2 and the ramp direction, polarity is determined. The integrating interval is trimmed to 600μs at 50mV full-scale sense voltage.

Third, a counter is incremented or decremented every time the integrator changes ramp direction. The counter effectively increases integration time by a factor of 1024, greatly reducing microcontroller overhead required to service interrupts from the LTC4150.

At each counter under or overflow, the $\overline{INT}$ output latches low, flagging a microcontroller. Simultaneously, the POL output is latched to indicate the polarity of the observed charge. With this information, the microcontroller can total the charge over long periods of time, developing an accurate estimate of the battery's condition. Once the interrupt is recognized, the microcontroller resets $\overline{INT}$ with a low going pulse on $\overline{CLR}$ and awaits the next interrupt. Alternatively, $\overline{INT}$ can drive $\overline{CLR}$.

APPLICATIONS INFORMATION

SENSE VOLTAGE INPUT AND FILTERS

Since the overall integration time is set by internally trimming the LTC4150, no external timing capacitor or trimming is necessary. The only external component that affects the transfer function of interrupts per coulomb of charge is the sense resistor, R_{SENSE}. The common mode range for the SENSE$^+$ and SENSE$^-$ pins is V_{DD} ±60mV, with a maximum differential voltage range of ±50mV. SENSE$^+$ is normally tied to V_{DD}, so there is no common mode issue when SENSE$^-$ operates within the 50mV differential limit relative to SENSE$^+$.

Choose R_{SENSE} to provide 50mV drop at maximum charge or discharge current, whichever is greater. Calculate R_{SENSE} from:

$$R_{SENSE} = \frac{50mV}{I_{MAX}} \quad (1)$$

The sense input range is small (±50mV) to minimize the loss across R_{SENSE}. To preserve accuracy, use Kelvin connections at R_{SENSE}.

The external filter capacitor C_F operates against a total on-chip resistance of 4k to form a lowpass filter that averages battery current and improves accuracy in the presence of noise, spikes and ripple. 4.7µF is recommended for general applications but can be extended to higher values as long as the capacitor's leakage is low. A 10nA leakage is roughly equivalent to the input offset error of the integrator. Ceramic capacitors are suitable for this use.

Switching regulators are a particular concern because they generate high levels of current ripple which may flow through the battery. The V_{DD} and SENSE$^+$ connection to the charger and load should be bypassed by at least 4.7µF at the LTC4150 if a switching regulator is present.

The LTC4150 maintains high accuracy even when Burst Mode® switching regulators are used. Burst pulse "on" levels must be within the specified differential input voltage range of 50mV as measured at C_F^+ and C_F^-. To retain accurate charge information, the LTC4150 must remain enabled during Burst Mode operation. If the LTC4150 shuts down or V_{DD} drops below 2.5V, the part resets and charge information is lost.

Coulomb Counting

The LTC4150's transfer function is quantified as a voltage to frequency gain G_{VF}, where output frequency is the number of interrupts per second and input voltage is the differential drive V_{SENSE} across SENSE$^+$ and SENSE$^-$. The number of interrupts per second will be:

$$f = G_{VF} \bullet |V_{SENSE}| \quad (2)$$

where

$$V_{SENSE} = I_{BATTERY} \bullet R_{SENSE} \quad (3)$$

Therefore,

$$f = G_{VF} \bullet |I_{BATTERY} \bullet R_{SENSE}| \quad (4)$$

Since I • t = Q, coulombs of battery charge per $\overline{INT}$ pulse can be derived from Equation 4:

$$\text{One } \overline{INT} = \frac{1}{G_{VF} \bullet R_{SENSE}} \text{ Coulombs} \quad (5)$$

Battery capacity is most often expressed in ampere-hours.

$$1Ah = 3600 \text{ Coulombs} \quad (6)$$

Combining Equations 5 and 6:

$$\text{One } \overline{INT} = \frac{1}{3600 \bullet G_{VF} \bullet R_{SENSE}} \text{ [Ah]} \quad (7)$$

or

$$1Ah = 3600 \bullet G_{VF} \bullet R_{SENSE} \text{ Interrupts} \quad (8)$$

The charge measurement may be further scaled within the microcontroller. However, the number of interrupts, coulombs or Ah all represent battery charge.

The LTC4150's transfer function is set only by the value of the sense resistor and the gain G_{VF}. Once R_{SENSE} is selected using Equation 1, the charge per interrupt can be determined from Equation 5 or 7.

Note that R_{SENSE} is not chosen to set the relationship between ampere-hours of battery charge and number of interrupts issued by the LTC4150. Rather, R_{SENSE} is chosen to keep the maximum sense voltage equal to or less than the LTC4150's 50mV full-scale sense input.

Burst Mode is registered trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

$\overline{INT}$, POL and $\overline{CLR}$

$\overline{INT}$ asserts low each time the LTC4150 measures a unit of charge. At the same time, POL is latched to indicate the polarity of the charge unit. The integrator and counter continue running, so the microcontroller must service and clear the interrupt before another unit of charge accumulates. Otherwise, one measurement will be lost. The time available between interrupts is the reciprocal of Equation 2:

$$\text{Time per } \overline{INT} \text{ Assertion} = \frac{1}{G_{VF} \bullet |V_{SENSE}|} \quad (9)$$

At 50mV full scale, the minimum time available is 596ms. To be conservative and accommodate for small, unexpected excursions above the 50mV sense voltage limit, the microcontroller should process the interrupt and polarity information and clear $\overline{INT}$ within 500ms.

Toggling $\overline{CLR}$ low for at least 20µs resets $\overline{INT}$ high and unlatches POL. Since the LTC4150's integrator and counter operate independently of the $\overline{INT}$ and POL latches, no charge information is lost during the latched period or while $\overline{CLR}$ is low. Charge/discharge information continues to accumulate during those intervals and accuracy is unaffected.

Once cleared, $\overline{INT}$ idles in a high state and POL indicates real-time polarity of the battery current. POL high indicates charge flowing into the battery and low indicates charge flowing out. Indication of a polarity change requires at least:

$$t_{POL} = \frac{2}{G_{VF} \bullet 1024 \bullet |V_{SENSE}|} \quad (10)$$

where V_{SENSE} is the smallest sense voltage magnitude before and after the polarity change.

Open-drain outputs POL and $\overline{INT}$ can sink I_{OL} = 1.6mA at V_{OL} = 0.5V. The minimum pull-up resistance for these pins should be:

$$R_L > (V_{CC} - 0.5) / 1.6mA \quad (11)$$

where V_{CC} is the logic supply voltage. Because speed isn't an issue, pull-up resistors of 10k or higher are adequate.

Interfacing to $\overline{INT}$, POL, $\overline{CLR}$ and $\overline{SHDN}$

The LTC4150 operates directly from the battery, while in most cases the microcontroller supply comes from some separate, regulated source. This poses no problem for $\overline{INT}$ and POL because they are open-drain outputs and can be pulled up to any voltage 9V or less, regardless of the voltage applied to the LTC4150's V_{DD}.

$\overline{CLR}$ and $\overline{SHDN}$ inputs require special attention. To drive them, the microcontroller or external logic must generate a minimum logic high level of 1.9V. The maximum input level for these pins is V_{DD} + 0.3V. If the microcontroller's supply is more than this, resistive dividers must be used on $\overline{CLR}$ and $\overline{SHDN}$. The schematic in Figure 6 shows an application with $\overline{INT}$ driving $\overline{CLR}$ and microcontroller V_{CC} > V_{DD}. The resistive dividers on $\overline{CLR}$ and $\overline{SHDN}$ keep the voltages at these pins within the LTC4150's V_{DD} range. Choose R2 and R1 so that:

$$(R1 + R2) \geq 50R_L \quad (12)$$

$$1.9V \leq \frac{R1}{R1+R2} V_{CC} \leq V_{DD} \text{ (Minimum)} \quad (13)$$

Equation 13 also applies to the selection of R3 and R4. The minimum V_{DD} is the lowest supply to the LTC4150 when the battery powering it is at its lowest discharged voltage.

When the battery is removed in any application, the $\overline{CLR}$ and $\overline{SHDN}$ inputs are unpredictable. $\overline{INT}$ and POL outputs may be erratic and should be ignored until after the battery is replaced.

If desired, the simple logic of Figure 4 may be used to derive separate charge and discharge pulse trains from $\overline{INT}$ and POL.

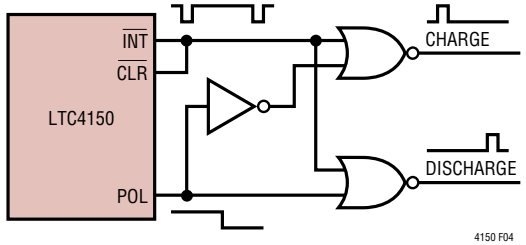


Figure 4. Unravelling Polarity—Separate Charge and Discharge Outputs

APPLICATIONS INFORMATION

AUTOMATIC CHARGE COUNT INTERRUPT AND CLEAR

In applications where a $\overline{CLR}$ pulse is unavailable, it's easy to make the LTC4150 run autonomously, as shown in Figures 5 and 6. If the microcontroller V_{CC} is less than or equal to the battery V_{DD}, $\overline{INT}$ may be directly connected to $\overline{CLR}$, as in Figure 5. The only requirement is that the microcontroller should be able to provide a high logic level of 1.9V to $\overline{SHDN}$. If the microcontroller V_{CC} is greater than the battery V_{DD}, use Figure 6. The resistor dividers on $\overline{CLR}$ and $\overline{SHDN}$ keep the voltages at these pins within the LTC4150's V_{DD} range. Choose an R_L value using Equation 11 and R1-R4 values using Equation 13. In either application, the LTC4150 will capture the first assertion of $\overline{INT}$ and wait at least 1µs before resetting it. This insures that $\overline{INT}$ pulses low for at least 1µs but gives automatic $\overline{INT}$ reset.

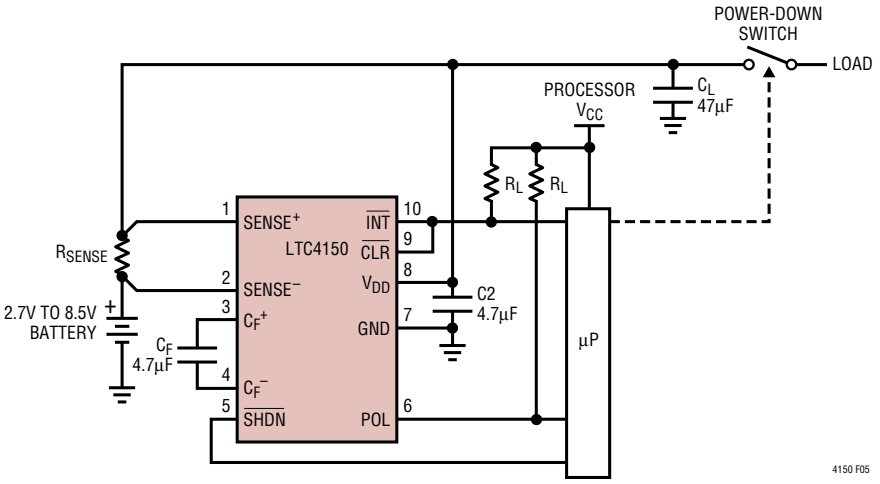


Figure 5. Application with $\overline{INT}$ Direct Drive of $\overline{CLR}$ and Separate Microprocessor Supply $V_{CC} \leq V_{DD}$

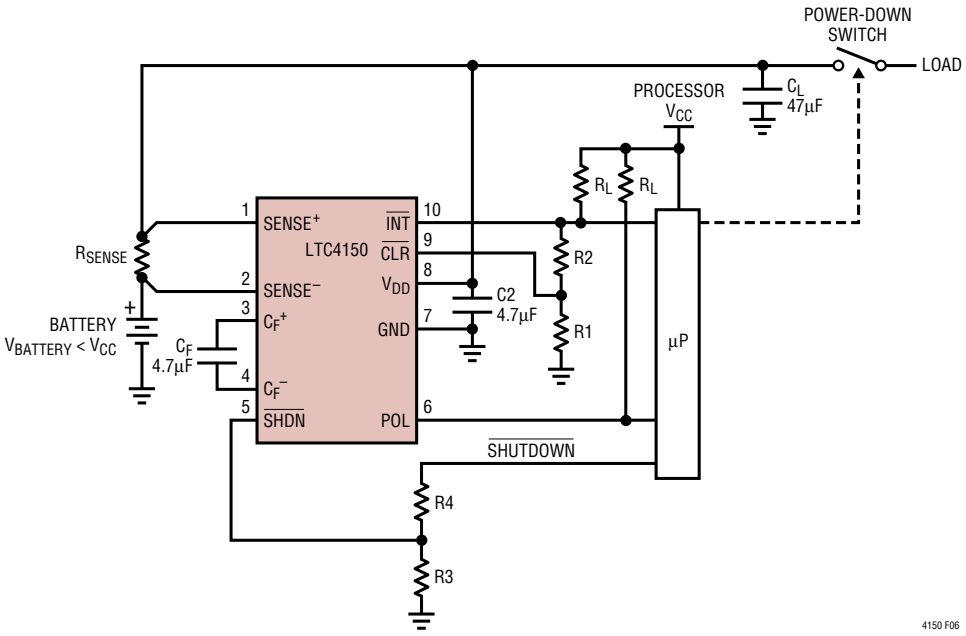


Figure 6. Application with $\overline{INT}$ Driving $\overline{CLR}$ and Separate Microprocessor Supply $V_{CC} > V_{DD}$

APPLICATIONS INFORMATION

PC BOARD LAYOUT SUGGESTIONS

Keep all traces as short as possible to minimize noise and inaccuracy. The supply bypass capacitor C2 should be placed close to the LTC4150. The 4.7µF filter capacitor C_F should be placed close the C_F^+ and C_F^- pins and should be a low leakage, unpolarized type. Use a 4-wire Kelvin sense connection for the sense resistor, locating it close to the LTC4150 with short sense traces to the $SENSE^+$ and $SENSE^-$ pins and longer force lines to the battery pack and powered load, see Figure 7.

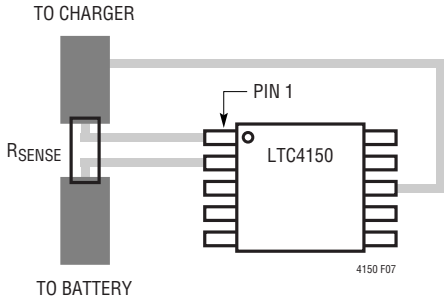


Figure 7. Kelvin Connection on SENSE Resistor

TYPICAL APPLICATIONS

Figure 8 shows a typical application designed for a single cell lithium-ion battery and 500mA maximum load current. Use Equation 1 to calculate R_{SENSE} = 0.05V / 0.5A = 0.1Ω.

With R_{SENSE} = 0.1Ω, Equation 7 shows that each interrupt corresponds to 0.085mAh. Equation 14, derived from Equation 2, gives the number of $\overline{INT}$ assertions for average battery current, I_{BATT}, over a time, t, in seconds:

$$\overline{INT}\ \text{Assertions} = G_{VF} \bullet I_{BATT} \bullet R_{SENSE} \bullet t \qquad (14)$$

Loading the battery so that 51.5mA is drawn from it over 600 seconds results in 100 $\overline{INT}$ assertions. For an 800mAh battery, this is (51.5mA • 1/6h) / 800mAh = 11% of the battery's capacity.

With a microcontroller supply = 5V, Equation 11 gives R_L > 2.875k. The nearest standard value is 3k.

From Equation 12, R_L = 3k gives R1 + R2 equal to 150.5k. A single cell lithium-ion battery can discharge as low as 2.7V.

From Equation 13, select R1 = 75k; the nearest standard value for R2 is 76.8k.

Also from Equation 13, we choose R3 = 75k and R4 = 76.8k.

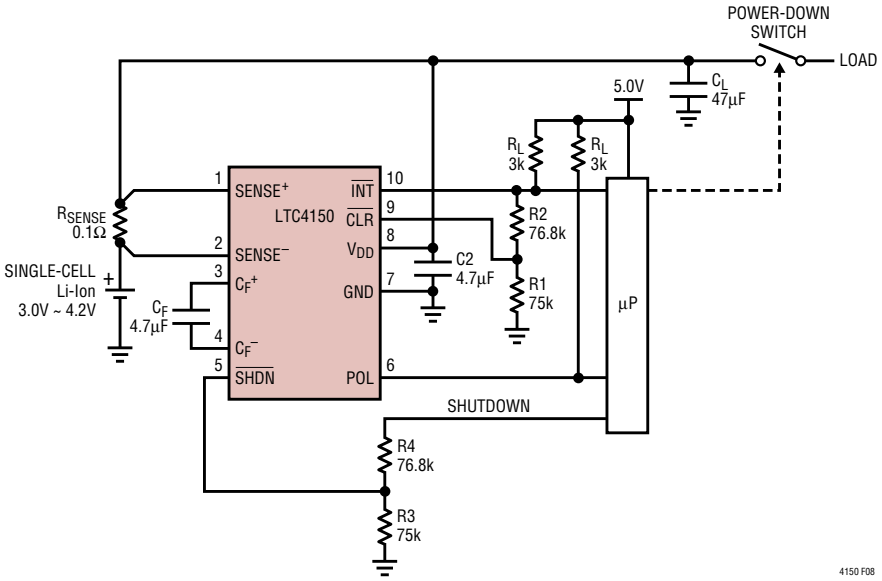
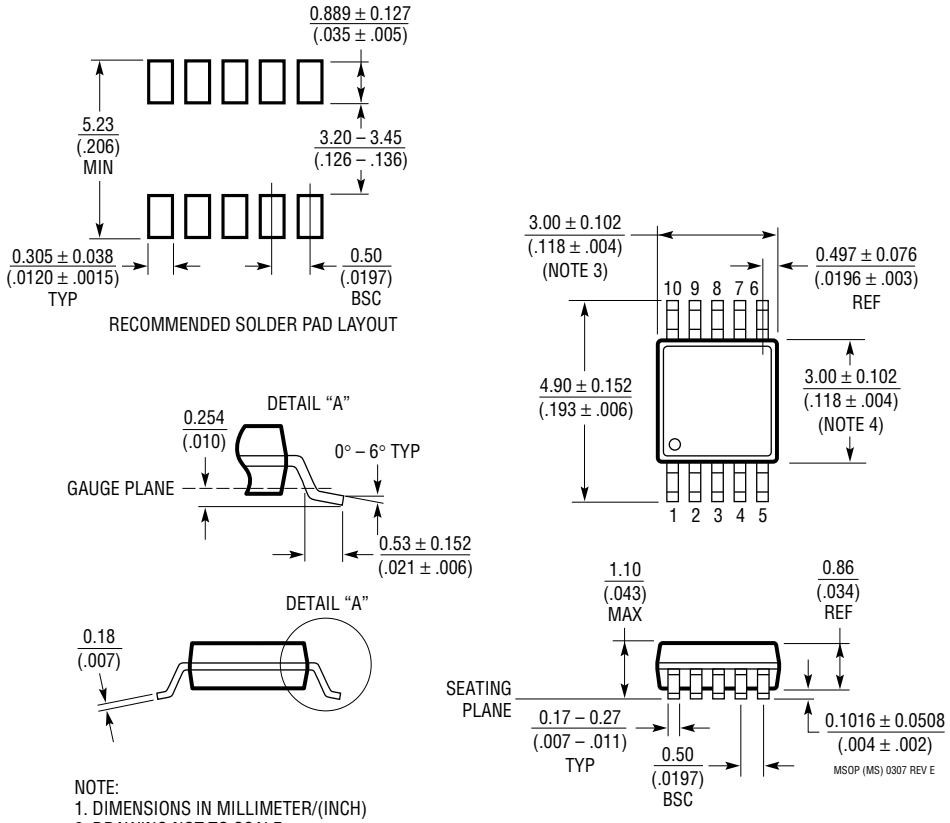


Figure 8. Typical Application, Single Cell Lithium-Ion Battery

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATIONS

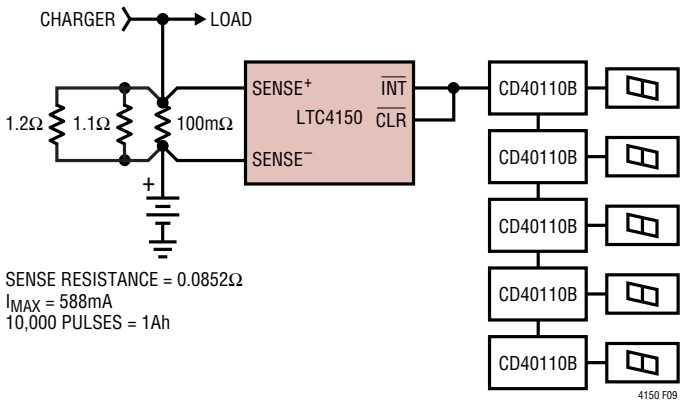


Figure 9. Ampere-Hour Gauge

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1732	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Features Preset Voltages, C/10 Charger Detection and Programmable Timer, Input Power Good Indication
LTC1733	Monolithic Lithium-Ion Linear Battery Charger	Standalone Charger with Programmable Timer, Up to 1.5A Charge Current
LTC1734	Lithium-Ion Linear Battery Charger in ThinSOT™	Simple ThinSOT Charger, No Blocking Diode, No Sense Resistor Needed
LTC1734L	Lithium-Ion Linear Battery Charger in ThinSOT	Low Current Version of LTC1734
LTC1998	Lithium-Ion Low Battery Detector	1% Accurate 2.5μA Quiescent Current, SOT-23
LTC4006	Small, High Efficiency, Fixed Voltage, Lithium-Ion Battery Charger	Constant-Current/Constant Voltage Switching Regulator with Termination Timer, AC Adapter Current Limit and Thermistor Sensor in a Small 16-Pin Package
LTC4050	Lithium-Ion Linear Battery Charger Controller	Simple Charger uses External FET, Features Preset Voltages, C/10 Charger Detection and Programmable Timer, Input Power Good Indication, Thermistor Interface
LTC4052	Monolithic Lithium-Ion Battery Pulse Charger	No Blocking Diode or External Power FET Required, Safety Current Limit
LTC4053	USB Compatible Monolithic Lithium-Ion Battery Charger	Standalone Charger with Programmable Timer, Up to 1.25A Charge Current
LTC4054	800mA Standalone Linear Lithium-Ion Battery Charger with Thermal Regulation in ThinSOT	No External MOSFET, Sense Resistor or Blocking Diode Required, Charge Current Monitor for Gas Gauging, C/10 Charge Termination
LTC4410	USB Power Manager	For Simultaneous Operation of USB Peripheral and Battery Charging from USB Port, Keeps Current Drawn from USB Port Constant, Keeps Battery Fresh, Use with the LTC4053, LTC1733, LTC4054
LTC4412	PowerPath™ Controller in ThinSOT	More Efficient Diode OR'ing, Automatic Switching Between DC Sources, Simplified Load Sharing, $3V \le V_{IN} \le 28V$

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