

Description

The 9ZX21200 is a small-footprint 12-output differential buffer that meets all the performance requirements of the Intel DB1200Z specification. The 9ZX21200 is backwards compatible to PCIe Gen1 and Gen2 applications. A fixed, internal feedback path maintains low drift for critical QPI applications. In bypass mode, the 9ZX21200 can provide outputs up to 150MHz.

Recommended Application

12-output PCIe Gen3/ QPI differential buffer for Romley and newer platforms

Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew < 65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- QPI 9.6GT/s 12UI phase jitter < 0.2ps RMS

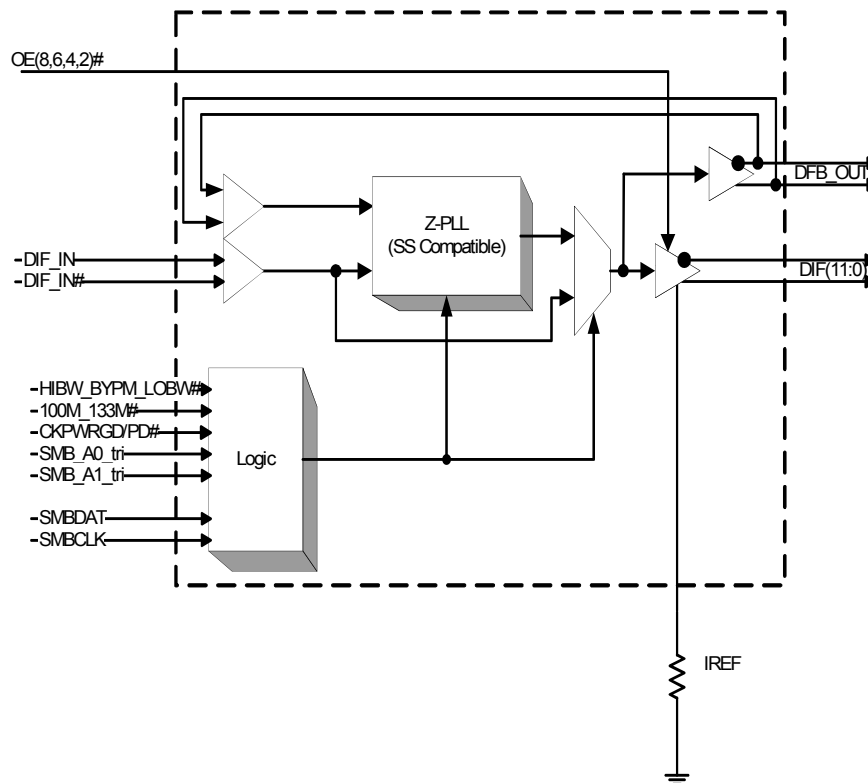
Features/Benefits

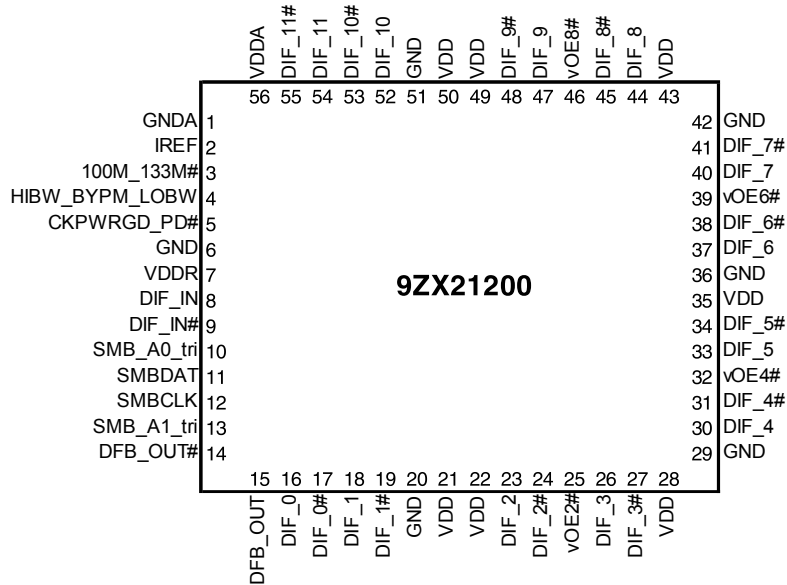
- Space-saving 56-pin package
- Fixed feedback path for 0ps input-to-output delay
- 9 Selectable SMBus Addresses; Multiple devices can share the same SMBus Segment
- 4 OE# pins; Hardware control of four outputs
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation; supports PCIe and QPI applications
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI
- Software control of PLL Bandwidth and Bypass Settings/PLL can dejitter incoming clock (B Rev only)

Output Features

- 12 - 0.7V differential HCSL output pairs

Block Diagram





Notes: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldown.
Even though the feedback path is fixed, the DFB_OUT pair still needs a termination network for the part to function.

Power Management Table

| CKPWRGD_PD# | DIF_IN/ DIF_IN# | SMBus EN bit | DIF(11:0) DIF(1:0)# | PLL STATE IF NOT IN BYPASS MODE |
|-------------|--------------------|-----------------|------------------------|--|
| 0 | X | X | Low/Low | OFF |
| 1 | Running | 0 1 | Low/Low Running | ON ON |

PLL Operating Mode Table

| HiBW_BypM_LoBW# | MODE |
|-----------------|-----------|
| Low | PLL Lo BW |
| Mid | Bypass |
| High | PLL Hi BW |

NOTE: PLL is OFF in Bypass Mode

MLF Power Connections

| Pin Number | | | Description |
|------------|-------------|--------------------|--------------|
| VDD | VDD | GND | |
| 56 | | 1 | Analog PLL |
| 7 | | 6 | Analog Input |
| 21,35,50 | 22,28,43,49 | 20,29,36,42, 51 | DIF clocks |

Tri-Level Input Thresholds

| Level | Voltage |
|-------|--------------|
| Low | <0.8V |
| Mid | 1.2<Vin<1.8V |
| High | Vin > 2.2V |

9ZX21200 SMBus Addressing

| Pin | | SMBus Address |
|------------|------------|---------------|
| SMB_A1_tri | SMB_A0_tri | |
| 0 | 0 | D8 |
| 0 | M | DA |
| 0 | 1 | DE |
| M | 0 | C2 |
| M | M | C4 |
| M | 1 | C6 |
| 1 | 0 | CA |
| 1 | M | CC |
| 1 | 1 | CE |

Functionality at Power-up (PLL mode)

| 100M_133M# | DIF_IN MHz | DIF(11:0) |
|------------|---------------|-----------|
| 1 | 100.00 | DIF_IN |
| 0 | 133.33 | DIF_IN |

PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW) | 0 | 0 |
| Mid (Bypass) | 0 | 1 |
| High (High BW) | 1 | 1 |

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|-----------------|------|---|
| 1 | GNDA | PWR | Ground pin for the PLL core. |
| 2 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 3 | 100M_133M# | IN | 3.3V Input to select operating frequency See Functionality Table for Definition |
| 4 | HIBW_BYPM_LOBW# | IN | Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details. |
| 5 | CKPWRGD_PD# | IN | Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode. |
| 6 | GND | PWR | Ground pin. |
| 7 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 8 | DIF_IN | IN | 0.7 V Differential TRUE input |
| 9 | DIF_IN# | IN | 0.7 V Differential Complementary Input |
| 10 | SMB_A0_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses. |
| 11 | SMBDAT | I/O | Data pin of SMBUS circuitry, 5V tolerant |
| 12 | SMBCLK | IN | Clock pin of SMBUS circuitry, 5V tolerant |
| 13 | SMB_A1_tri | IN | SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses. |
| 14 | DFB_OUT# | OUT | Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. |
| 15 | DFB_OUT | OUT | True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. |
| 16 | DIF_0 | OUT | 0.7V differential true clock output |
| 17 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 18 | DIF_1 | OUT | 0.7V differential true clock output |
| 19 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 20 | GND | PWR | Ground pin. |
| 21 | VDD | PWR | Power supply, nominal 3.3V |
| 22 | VDD | PWR | Power supply, nominal 3.3V |
| 23 | DIF_2 | OUT | 0.7V differential true clock output |
| 24 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 25 | voE2# | IN | Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs |
| 26 | DIF_3 | OUT | 0.7V differential true clock output |
| 27 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 28 | VDD | PWR | Power supply, nominal 3.3V |
| 29 | GND | PWR | Ground pin. |
| 30 | DIF_4 | OUT | 0.7V differential true clock output |
| 31 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 32 | voE4# | IN | Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs |
| 33 | DIF_5 | OUT | 0.7V differential true clock output |
| 34 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 35 | VDD | PWR | Power supply, nominal 3.3V |
| 36 | GND | PWR | Ground pin. |
| 37 | DIF_6 | OUT | 0.7V differential true clock output |
| 38 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 39 | voE6# | IN | Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs |
| 40 | DIF_7 | OUT | 0.7V differential true clock output |
| 41 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 42 | GND | PWR | Ground pin. |
| 43 | VDD | PWR | Power supply, nominal 3.3V |
| 44 | DIF_8 | OUT | 0.7V differential true clock output |
| 45 | DIF_8# | OUT | 0.7V differential Complementary clock output |
| 46 | voE8# | IN | Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs |
| 47 | DIF_9 | OUT | 0.7V differential true clock output |
| 48 | DIF_9# | OUT | 0.7V differential Complementary clock output |
| 49 | VDD | PWR | Power supply, nominal 3.3V |
| 50 | VDD | PWR | Power supply, nominal 3.3V |
| 51 | GND | PWR | Ground pin. |
| 52 | DIF_10 | OUT | 0.7V differential true clock output |
| 53 | DIF_10# | OUT | 0.7V differential Complementary clock output |
| 54 | DIF_11 | OUT | 0.7V differential true clock output |
| 55 | DIF_11# | OUT | 0.7V differential Complementary clock output |
| 56 | VDDA | PWR | 3.3V power for the PLL core. |

Stresses above the ratings listed below can cause permanent damage to the 9ZX21200. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage | VDD, VDDA | VDD for core logic and PLL | | | 4.6 | V | 1,2 |
| IO Supply Voltage | VDD | VDD for differential IO | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | Except for SMBus interface | | | V _{DD} +0.5V | V | 1 |
| Input High Voltage | V _{IHSMB} | SMBus clock and data pins | | | 5.5V | V | 1 |
| Storage Temperature | T _S | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _J | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–Clock Input Parameters

T_A = T_{COM}; Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d _{in} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFIn} | Differential Measurement | 0 | | 125 | ps | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through +/-75mV window centered around differential zero

T_A = T_{COM}; Supply Voltage V_{DD} = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|--|-----------|--------|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | 2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, except SMBus, low threshold and tri-level inputs | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = V _{DD} | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = V _{DD} ; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | 33 | | 150 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 100MHz PLL mode | 90 | 100.00 | 110 | MHz | 2 |
| | F _{ipll} | V _{DD} = 3.3 V, 133.33MHz PLL mode | 120 | 133.33 | 147 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | T _{STAB} | From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.300 | 1 | ms | 1,2 |
| Input SS Modulation Frequency | f _{MODIN} | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 4 | | 12 | clocks | 1,3 |
| Tdrive_PD# | t _{DRVPD} | DIF output enable after PD# de-assertion | | 16 | 300 | us | 1,3 |
| Tfall | t _F | Fall time of control inputs | | | 10 | ns | 1,2 |
| Trise | t _R | Rise time of control inputs | | | 10 | ns | 1,2 |
| SMBus Input Low Voltage | V _{ILSMB} | | | | 0.8 | V | 1 |
| SMBus Input High Voltage | V _{IHSMB} | | 2.1 | | V _{DD} SMB | V | 1 |
| SMBus Output Low Voltage | V _{OLSMB} | @ I _{PULLUP} | | | 0.4 | V | 1 |
| SMBus Sink Current | I _{PULLUP} | @ V _{OL} | 4 | | | mA | 1 |
| Nominal Bus Voltage | V _{DD} SMB | 3V to 5V +/- 10% | 2.7 | | 5.5 | V | 1 |
| SCLK/SDATA Rise Time | t _{RSMB} | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | t _{FSMB} | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | f _{MAXSMB} | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴DIF_IN input

⁵The differential input clock must be running for the SMBus to be active

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------|---|------|------|------|-------|---------|
| Slew rate | Trf | Scope averaging on | 1 | 2 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔTrf | Slew rate matching, Scope averaging on | | 8 | 20 | % | 1, 2, 4 |
| Voltage High | VHigh | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 705 | 850 | mV | 1 |
| Voltage Low | VLow | | -150 | 1 | 150 | | 1 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 725 | 1150 | mV | 1 |
| Min Voltage | Vmin | | -300 | -22 | | | 1 |
| Vswing | Vswing | Scope averaging off | 300 | 1407 | | mV | 1, 2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 309 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 22 | 140 | mV | 1, 6 |

¹Guaranteed by design and characterization, not 100% tested in production. I_{REF} = VDD/(3xR_R). For R_R = 412Ω (1%), I_{REF} = 2.7mA. I_{OH} = 6.4 x I_{REF} and V_{OH} = 0.7V @ Z_O=85Ω differential impedance.

² Measured from differential waveform

³ Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

⁵ Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_cross_min/max (V_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V_cross_delta to be smaller than V_cross absolute.

Electrical Characteristics–Current Consumption

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------|-----------------------|---|-----|-----|-----|-------|-------|
| Operating Current | I _{DDVDD} | 133MHz, C _L = Full load; VDD rail, Z _O =85Ω | | 260 | 275 | mA | 1 |
| | I _{DDVDDA} | 133MHz, C _L = Full load; VDD rail, Z _O =85Ω | | 13 | 20 | mA | 1 |
| Powerdown Current | I _{DDVDDPD} | Power Down, VDD rail, Z _O =85Ω | | 2 | 6 | mA | 1 |
| | I _{DDVDDAPD} | Power Down, VDD rail, Z _O =85Ω | | 1.3 | 2 | mA | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|-----|------------|-----------|
| CLK_IN, DIF[x:0] | t _{SPO_PLL} | Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V | -100 | 29 | 100 | ps | 1,2,4,5,8 |
| CLK_IN, DIF[x:0] | t _{PD_BYP} | Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V | 2.5 | 3.7 | 4.5 | ns | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_PLL} | Input-to-Output Skew Variation in PLL mode across voltage and temperature | -50 | | 50 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSPO_BYP} | Input-to-Output Skew Variation in Bypass mode across voltage and temperature | -250 | | 250 | ps | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DTE} | Random Differential Tracking error between two 9ZX devices in Hi BW Mode | | 2.9 | 5 | ps (ms) | 1,2,3,5,8 |
| CLK_IN, DIF[x:0] | t _{DSSTE} | Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode | | 14 | 75 | ps | 1,2,3,5,8 |
| DIF{x:0} | t _{SKEW_ALL} | Output-to-Output Skew across all outputs (Common to Bypass and PLL mode) | | 32 | 65 | ps | 1,2,3,8 |
| PLL Jitter Peaking | j _{peak-hibw} | LOBW#_BYPASS_HIBW = 1 | 0 | 1.8 | 2.5 | dB | 7,8 |
| PLL Jitter Peaking | j _{peak-lobw} | LOBW#_BYPASS_HIBW = 0 | 0 | 0.7 | 2 | dB | 7,8 |
| PLL Bandwidth | p _{llHIBW} | LOBW#_BYPASS_HIBW = 1 | 2 | 3.1 | 4 | MHz | 8,9 |
| PLL Bandwidth | p _{llLOBW} | LOBW#_BYPASS_HIBW = 0 | 0.7 | 1.1 | 1.4 | MHz | 8,9 |
| Duty Cycle | t _{DC} | Measured differentially, PLL Mode | 45 | 49.6 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCCD} | Measured differentially, Bypass Mode @100MHz | -2 | -0.2 | 2 | % | 1,10 |
| Jitter, Cycle to cycle | t _{jcy-cyc} | PLL mode | | 15.7 | 50 | ps | 1,11 |
| | | Additive Jitter in Bypass Mode | | 0.1 | 50 | ps | 1,11 |

Notes for preceding table:

- ¹ Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
- ² Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.
- ³ All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
- ⁴ This parameter is deterministic for a given device
- ⁵ Measured with scope averaging on to find mean value.
- ⁶ t is the period of the input clock
- ⁷ Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
- ⁸ Guaranteed by design and characterization, not 100% tested in production.
- ⁹ Measured at 3 db down or half power point.
- ¹⁰ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.
- ¹¹ Measured from differential waveform

T_A = T_{COM}; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|---------------------------------------|-------------------------|--|-----|------|-----|----------|---------|
| Phase Jitter, PLL Mode | t _{jphPCleG1} | PCle Gen 1 | | 32 | 86 | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCle Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.8 | 3 | ps (rms) | 1,2 |
| | | PCle Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 1.9 | 3.1 | ps (rms) | 1,2 |
| | t _{jphPCleG3} | PCle Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.45 | 1 | ps (rms) | 1,2,4 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.20 | 0.5 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.14 | 0.3 | ps (rms) | 1,5 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.12 | 0.2 | ps (rms) | 1,5 |
| Additive Phase Jitter, Bypass mode | t _{jphPCleG1} | PCle Gen 1 | | 0.10 | 10 | ps (p-p) | 1,2,3 |
| | t _{jphPCleG2} | PCle Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.13 | 0.1 | ps (rms) | 1,2,6 |
| | | PCle Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.10 | 0.5 | ps (rms) | 1,2,6 |
| | t _{jphPCleG3} | PCle Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.10 | 0.2 | ps (rms) | 1,2,4,6 |
| | t _{jphQPI_SMI} | QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI) | | 0.09 | 0.1 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 8.0Gb/s, 12UI) | | 0.09 | 0.1 | ps (rms) | 1,5,6 |
| | | QPI & SMI (100MHz, 9.6Gb/s, 12UI) | | 0.09 | 0.1 | ps (rms) | 1,5,6 |

¹ Applies to all outputs.

² See <http://www.pcisig.com> for complete specs

³ Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴ Subject to final radification by PCI SIG.

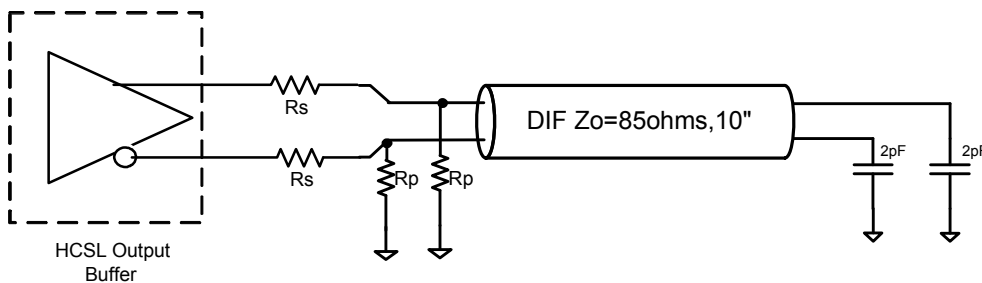
⁵ Calculated from Intel-supplied Clock Jitter Tool v 1.6.4

⁶ For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)² = (total jitter)² - (input jitter)²

Differential Output Terminations

| DIF Zo (Ω) | Iref (Ω) | Rs (Ω) | Rp (Ω) |
|------------|----------|--------|--------------|
| 100 | 475 | 33 | 50 |
| 85 | 412 | 27 | 42.2 or 43.2 |

9ZX21200 Differential Test Loads



| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 100.00 | 9.94900 | | 9.99900 | 10.00000 | 10.00100 | | 10.05100 | ns | 1,2,3 |
| | 133.33 | 7.44925 | | 7.49925 | 7.50000 | 7.50075 | | 7.55075 | ns | 1,2,4 |

Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| DIF | 99.75 | 9.94906 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.10107 | ns | 1,2,3 |
| | 133.00 | 7.44930 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.58830 | ns | 1,2,4 |

Notes:

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZX21200 itself does not contribute to ppm error.

³ Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

⁴ Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host) | | | IDT (Slave/Receiver) |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| ACK | | X Byte | |
| ACK | | | Beginning Byte N |
| O | | | O |
| O | | | O |
| | | | O |
| | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBusTable: PLL Mode, and Frequency Select Register

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|--|-------------------|-------------------------------------|-----------|--|--------------------|----------|
| Bit 7 | 3 | PLL Mode 1 | PLL Operating Mode Rd back 1 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 6 | 3 | PLL Mode 0 | PLL Operating Mode Rd back 0 | R | See PLL Operating Mode Readback Table | | Latch |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | These bits available in B rev only. | PLL_SW_EN | Enable S/W control of PLL BW | RW | HW Latch | S/W Control | 0 |
| Bit 2 | | PLL Mode 1 | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 1 |
| Bit 1 | | PLL Mode 0 | PLL Operating Mode 1 | RW | See PLL Operating Mode Readback Table | | 1 |
| Bit 0 | 2 | 100M_133M# | Frequency Select Readback | R | 133MHz | 100MHz | Latch |

SMBusTable: Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|----------|----------------------------------|------|---------|--------|---------|
| Bit 7 | 42/41 | DIF 7_En | Output Control overrides OE# pin | RW | Low/Low | Enable | 1 |
| Bit 6 | 38/37 | DIF 6_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 5 | 34/35 | DIF 5_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 4 | 30/29 | DIF 4_En | Output Control overrides OE# pin | RW | | | 1 |
| Bit 3 | 25/26 | DIF 3_En | Output Control | RW | | | 1 |
| Bit 2 | 23/24 | DIF 2_En | Output Control | RW | | | 1 |
| Bit 1 | 18/19 | DIF 1_En | Output Control | RW | | | 1 |
| Bit 0 | 16/17 | DIF 0_En | Output Control | RW | | | 1 |

SMBusTable: Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-----------|------------------|------|---------|--------|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | 55/54 | DIF 11_En | Output Control | RW | Low/Low | Enable | 1 |
| Bit 2 | 53/52 | DIF 10_En | Output Control | RW | | | 1 |
| Bit 1 | 48/47 | DIF 9_En | Output Control | RW | | | 1 |
| Bit 0 | 46/45 | DIF 8_En | Output Control | RW | | | 1 |

SMBusTable: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Reserved Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

SMBusTable: Vendor & Revision ID Register

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|------------------------------|---|---------|
| Bit 7 | - | RID3 | REVISION ID | R | A rev = 0000 B rev = 0001 | | X |
| Bit 6 | - | RID2 | | R | | | X |
| Bit 5 | - | RID1 | | R | | | X |
| Bit 4 | - | RID0 | | R | | | X |
| Bit 3 | - | VID3 | VENDOR ID | R | 0001 for IDT/ICS | | 0 |
| Bit 2 | - | VID2 | | R | | | 0 |
| Bit 1 | - | VID1 | | R | | | 0 |
| Bit 0 | - | VID0 | | R | | | 1 |

SMBusTable: DEVICE ID

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|-------------------|------------------|------|-------------------------------|---|---------|
| Bit 7 | - | Device ID 7 (MSB) | | R | 1200 is 200 decimal or C8 hex | | 1 |
| Bit 6 | - | Device ID 6 | | R | | | 1 |
| Bit 5 | - | Device ID 5 | | R | | | 0 |
| Bit 4 | - | Device ID 4 | | R | | | 0 |
| Bit 3 | - | Device ID 3 | | R | | | 1 |
| Bit 2 | - | Device ID 2 | | R | | | 0 |
| Bit 1 | - | Device ID 1 | | R | | | 0 |
| Bit 0 | - | Device ID 0 | | R | | | 0 |

SMBusTable: Byte Count Register

| Byte 7 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|---|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default. | | 0 |
| Bit 3 | - | BC3 | | RW | | | 1 |
| Bit 2 | - | BC2 | | RW | | | 0 |
| Bit 1 | - | BC1 | | RW | | | 0 |
| Bit 0 | - | BC0 | | RW | | | 0 |

SMBusTable: Reserved Register

| Byte 8 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7 | | | Reserved | | | | 0 |
| Bit 6 | | | Reserved | | | | 0 |
| Bit 5 | | | Reserved | | | | 0 |
| Bit 4 | | | Reserved | | | | 0 |
| Bit 3 | | | Reserved | | | | 0 |
| Bit 2 | | | Reserved | | | | 0 |
| Bit 1 | | | Reserved | | | | 0 |
| Bit 0 | | | Reserved | | | | 0 |

DIF Reference Clock

| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
|---|--------------------|------|--------|
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs (100 ohm differential traces) | 33 | ohm | 1 |
| Rs (85 ohm differential traces) | 27 | ohm | 1 |

| Down Device Differential Routing | Dimension or Value | Unit | Figure |
|--|---------------------|------|--------|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | Dimension or Value | Unit | Figure |
|--|-----------------------|------|--------|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

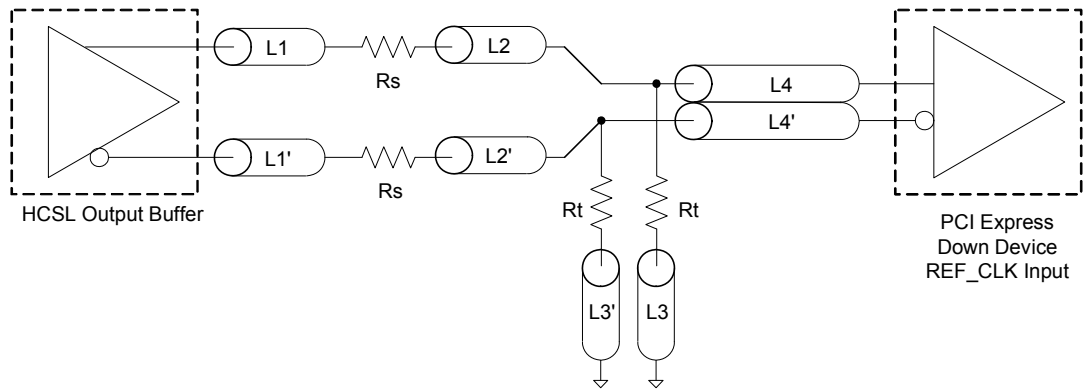
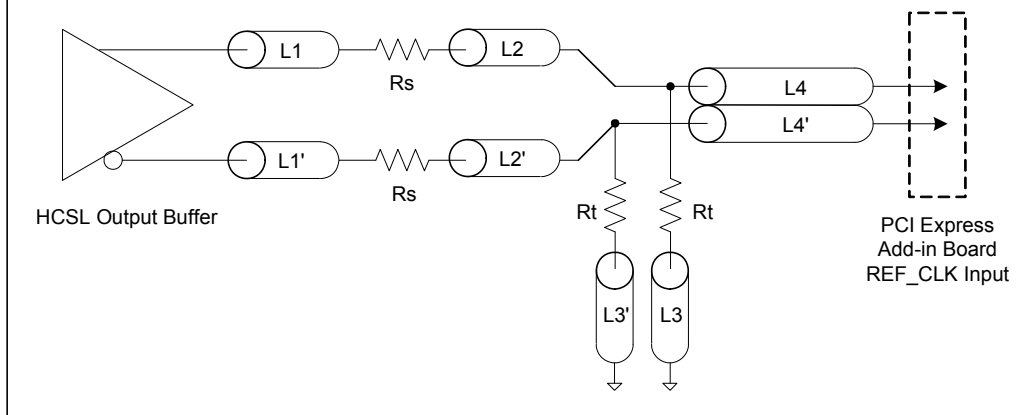


Figure 2: PCI Express Connector Routing

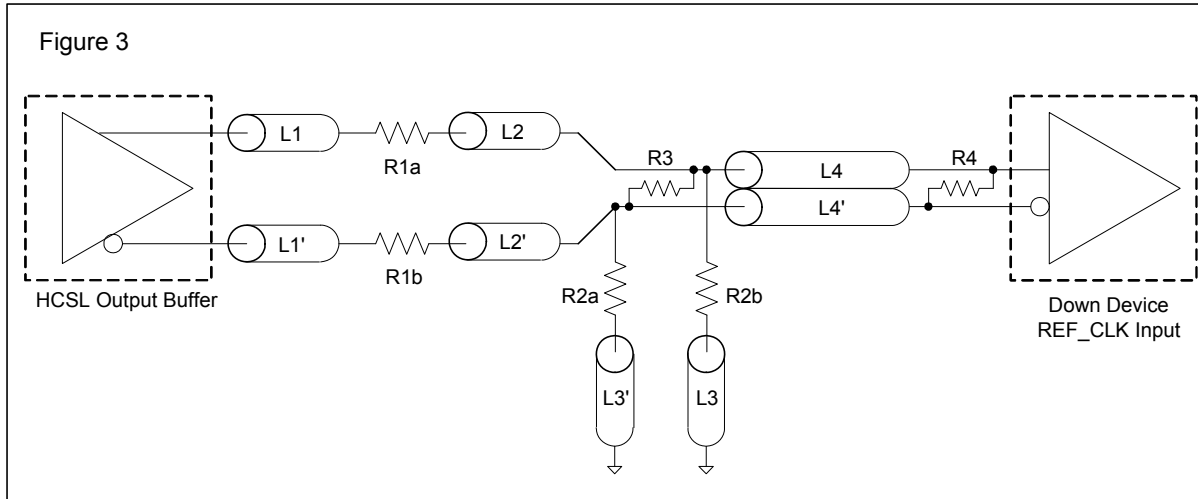


Alternative Termination for LVDS and other Common Differential Signals (figure 3)

| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
|-------|-------|------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

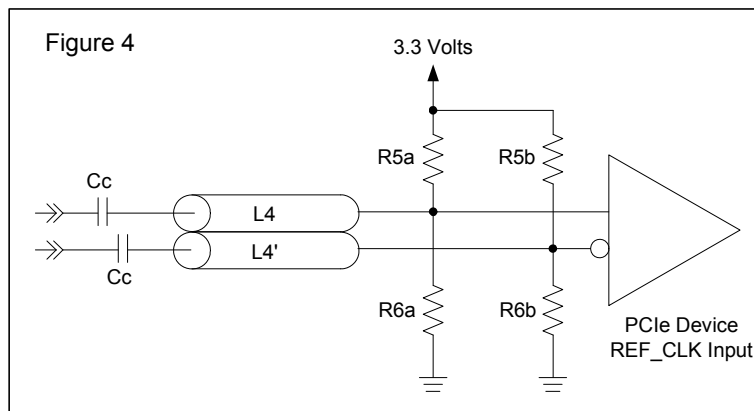
R1a = R1b = R1

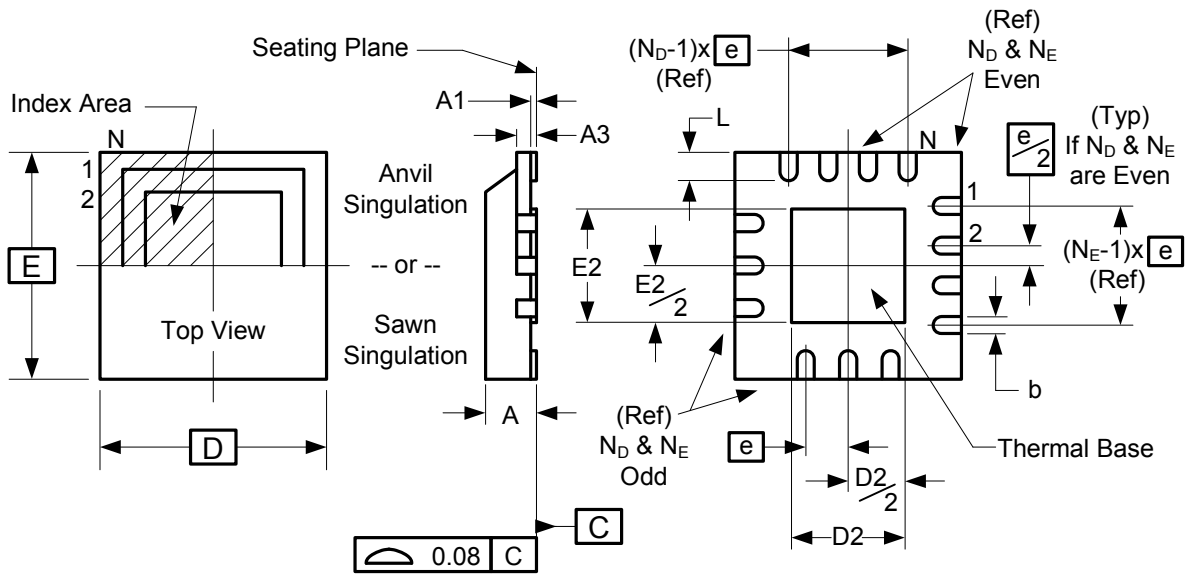
R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)

| Component | Value | Note |
|-----------|-------------|------|
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |





| Dimensions (mm) | | |
|-----------------|----------------|------|
| Symbol | Min | Max |
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.3 |
| e | 0.50 BASIC | |
| D x E BASIC | 8.00 x 8.00 | |
| D2 MIN./MAX. | 4.35 | 4.65 |
| E2 MIN./MAX. | 5.05 | 5.35 |
| L MIN./MAX. | 0.3 | 0.5 |
| N | 56 | |
| N_D | 14 | |
| N_E | 14 | |

Ordering Information

| Part / Order Number | Shipping Package | Package | Temperature | Difference |
|---------------------|------------------|---------------|-------------|------------------------------|
| 9ZX21200AKLF | Trays | 56-pin VFQFPN | 0 to +70°C | W/O Byte 0 PLL Control |
| 9ZX21200AKLFT | Tape and Reel | 56-pin VFQFPN | 0 to +70°C | |
| 9ZX21200BKLF | Trays | 56-pin VFQFPN | 0 to +70°C | With Byte 0 PLL Mode Control |
| 9ZX21200BKLFT | Tape and Reel | 56-pin VFQFPN | 0 to +70°C | |

"LF" suffix to the part number designates Pb-Free configuration, RoHS compliant.

"A" and "B" are the device revision designators (will not correlate with the datasheet revision).

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| Rev. | Issue Date | Issuer | Description | Page # |
|------|------------|--------|--|-----------|
| A | 9/13/2011 | RDW | <ol style="list-style-type: none"> 1. Updated electrical tables with char data 2. Fixed minor typographical errors 3. Moved to final | Various |
| B | 12/8/2011 | RDW | <ol style="list-style-type: none"> 1. Added B rev functionality description to Features, Benefits 2. Updated tDSPO_BYP parameter from +/-350ps to +/-250ps 3. Updated SMBus Byte 0 with B rev functionality 4. Updated ordering information to include B rev | 1,7,11,15 |
| C | 4/18/2012 | RDW | <ol style="list-style-type: none"> 1. Updated Power Connections table to be consistent with 9ZXL1230 2. Updated Rp values on Output Terminations Table from 43.2 ohms to 42.2 or 43.2 ohms to be consistent with Intel. | 2,8 |
| D | 4/15/2013 | RDW | Corrected typo in OE# Latency parameter; changed 1 min. to 3 max. cycles to 4 min. to 12 max. clocks. | 5 |

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