# ISL22323

Dual Digitally Controlled Potentiometer (XDCP)
Low Noise, Low Power, $I^2C$ Bus, 256 Taps

FN6422
Rev.2.00
Aug 17, 2015

The ISL22323 integrates two digitally controlled potentiometers (DCP), control logic and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the $I^2C$ bus interface. The potentiometer has an associated volatile Wiper Register (WRi) and a non-volatile Initial Value Register (IVRi) that can be directly written to and read by the user. The contents of the WRi control the position of the corresponding wiper. At power up the device recalls the contents of the DCP's IVRi to the correspondent WRi.

The ISL22323 also has 13 general purpose non-volatile registers that can be used as storage of lookup table for multiple wiper position or any other valuable information.

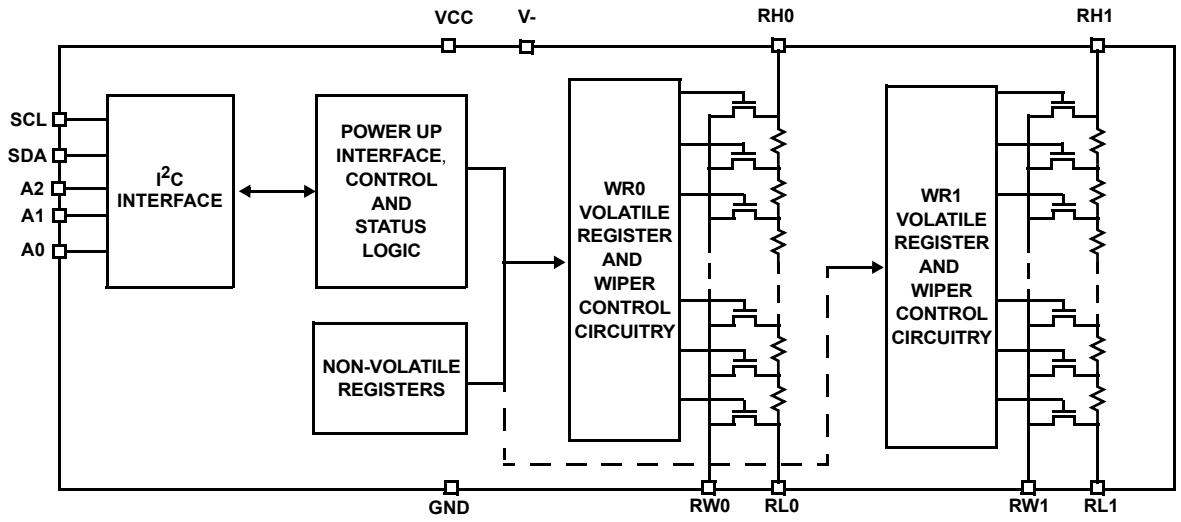
The ISL22323 features a dual supply, that is beneficial for applications requiring a bipolar range for DCP terminals between V- and VCC.

Each DCP can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

## Features

- Two potentiometers in one package
- 256 resistor taps
- $I^2C$ serial interface
  - Three address pins, up to eight devices per bus
- Non-volatile EEPROM storage of wiper position
- 13 General Purpose non-volatile registers
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ T ≤ +55°C
- Wiper resistance: 70Ω typical @ 1mA
- Standby current <4µA max
- Shut-down current <4µA max
- Dual power supply
  - $V_{CC}$ = 2.25V to 5.5V
  - V- = -2.25V to -5.5V
- 10kΩ, 50kΩ or 100kΩ total resistance
- Extended industrial temperature range: -40 to +125°C
- 14 Ld TSSOP or 16 Ld QFN
- Pb-free (RoHS compliant)

## Block Diagram



## Ordering Information

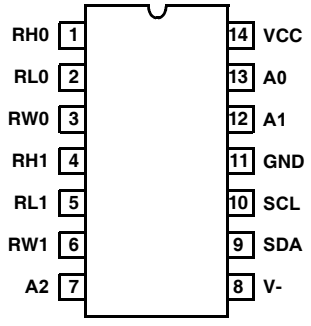
| PART NUMBER (Notes 1, 2) | PART MARKING | RESISTANCE OPTION (kΩ) | TEMPERATURE RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL22323TFV14Z | 22323 TFVZ | 100 | -40 to +125 | 14 Ld TSSOP | M14.173 |
| ISL22323TFR16Z | 223 23TFRZ | 100 | -40 to +125 | 16 Ld QFN | L16.4x4A |
| ISL22323UFV14Z **(No longer available, recommended replacement: ISL22323TFV14Z-TK)** | 22323 UFVZ | 50 | -40 to +125 | 14 Ld TSSOP | M14.173 |
| ISL22323UFR16Z **(No longer available, recommended replacement: ISL22323TFV14Z-TK)** | 223 23UFRZ | 50 | -40 to +125 | 16 Ld QFN | L16.4x4A |
| ISL22323WFV14Z **(No longer available, recommended replacement: ISL22323TFV14Z-TK)** | 22323 WFVZ | 10 | -40 to +125 | 14 Ld TSSOP | M14.173 |
| ISL22323WFR16Z **(No longer available, recommended replacement: ISL22323TFV14Z-TK)** | 223 23WFRZ | 10 | -40 to +125 | 16 Ld QFN | L16.4x4A |

NOTES:

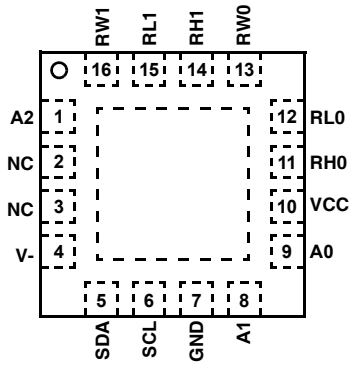
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

## Pinouts

**ISL22323**
**(14 LD TSSOP)**
TOP VIEW




**ISL22323**
**(16 LD QFN)**
TOP VIEW



## Pin Descriptions

| TSSOP PIN | QFN PIN | SYMBOL | DESCRIPTION |
|---|---|---|---|
| 1 | 11 | RH0 | “High” terminal of DCP0 |
| 2 | 12 | RL0 | “Low” terminal of DCP0 |
| 3 | 13 | RW0 | “Wiper” terminal of DCP0 |
| 4 | 14 | RH1 | “High” terminal of DCP1 |
| 5 | 15 | RL1 | “Low” terminal of DCP1 |
| 6 | 16 | RW1 | “Wiper” terminal of DCP1 |
| 7 | 1 | A2 | Device address input for the $I^2C$ interface |
| 8 | 4 | V- | Negative power supply pin |
| 9 | 5 | SDA | Open drain Serial data I/O for the $I^2C$ interface |
| 10 | 6 | SCL | $I^2C$ interface clock input |
| 11 | 7 | GND | Device ground pin |
| 12 | 8 | A1 | Device address input for the $I^2C$ interface |
| 13 | 9 | A0 | Device address input for the $I^2C$ interface |
| 14 | 10 | VCC | Positive power supply pin |
| | 2, 3 | NC | No connection |
| | EPAD* | | Exposed Die Pad internally connected to V- |

NOTE: *PCB thermal land for QFN EPAD should be connected to V- plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf

## Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to $V_{CC}$+0.3
$V_{CC}$ . . . . . -0.3V to +6V
V- . . . . . -6V to 0.3V
Voltage at any DCP Pin with
respect to GND. . . . . V- to $V_{CC}$
$I_W$ (10s) . . . . . ±6mA
Latchup . . . . . Class II, Level A at +125°C
ESD
Human Body Model . . . . . 3.5kV
Machine Model . . . . . .350V

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 14 Lead TSSOP | 105 | N/A |
| 16 Lead QFN (Note 4) | 39 | 3.0 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Temperature Range (Full Industrial) . . . . . -40°C to +125°C
Power Rating . . . . . 15mW
$V_{CC}$ . . . . . 2.25V to 5.5V
V- . . . . . -2.25V to -5.5V
Max Wiper Current Iw . . . . . ±3.0mA

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

## Analog Specifications

Over recommended operating conditions unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| $R_{TOTAL}$ | RHi to RLi Resistance | W option | | 10 | | kΩ |
| | | U option | | 50 | | kΩ |
| | | T option | | 100 | | kΩ |
| | RHi to RLi Resistance Tolerance | | -20 | | +20 | % |
| | End-to-End Temperature Coefficient | W option | | ±85 | | ppm/°C |
| | | U, T option | | ±45 | | ppm/°C |
| $V_{RHi}$, $V_{RLi}$ | DCP Terminal Voltage | $V_{RH}$ and $V_{RL}$ to GND | V- | | $V_{CC}$ | V |
| $R_W$ | Wiper Resistance | RH - floating, $V_{RL}$ = V-, force Iw current to the wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$ | | 70 | 250 | Ω |
| $C_H/C_L/C_W$ (Note 19) | Potentiometer Capacitance | See Macro Model below. | | 10/10/25 | | pF |
| $I_{LkgDCP}$ | Leakage on DCP Pins | Voltage at pin from V- to $V_{CC}$ | | 0.1 | 1 | µA |
| **VOLTAGE DIVIDER MODE** (V- @ RLi; $V_{CC}$ @ RHi; measured at RWi, unloaded) | | | | | | |
| INL (Note 10) | Integral Non-linearity Monotonic Over All Tap Positions | W option | -1.5 | ±0.5 | 1.5 | LSB (Note 6) |
| | | U, T option | -1.0 | ±0.2 | 1.0 | LSB (Note 6) |
| DNL (Note 9) | Differential Non-linearity Monotonic Over All Tap Positions | W option | -1.0 | ±0.4 | 1.0 | LSB (Note 6) |
| | | U, T option | -0.5 | ±0.15 | 0.5 | LSB (Note 6) |
| ZSerror (Note 7) | Zero-scale Error | W option | 0 | 1 | 5 | LSB (Note 6) |
| | | U, T option | 0 | 0.5 | 2 | |
| FSerror (Note 8) | Full-scale Error | W option | -5 | -1 | 0 | LSB (Note 6) |
| | | U, T option | -2 | -1 | 0 | |
| $V_{MATCH}$ (Note 11, 19) | DCP-to-DCP Matching | Wipers at the same tap position, the same voltage at all RH terminals and the same voltage at all RL terminals | -2 | | 2 | LSB (Note 6) |

## Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| $TC_V$ (Note 12, 19) | Ratiometric Temperature Coefficient | DCP register set to 80 hex | | ±4 | | ppm/°C |
| $f_{cutoff}$ (Note 19) | -3dB Cut Off Frequency | Wiper at midpoint (80hex) W option (10k) | | 1000 | | kHz |
| | | Wiper at midpoint (80hex) U option (50k) | | 250 | | kHz |
| | | Wiper at midpoint (80hex) T option (100k) | | 120 | | kHz |
| **RESISTOR MODE** (Measurements between RWi and RLi with RHi not connected, or between RWi and RHi with RLi not connected) | | | | | | |
| RINL (Note 16) | Integral Non-linearity | W option | -3 | ±1.5 | 3 | MI (Note 13) |
| | | U, T option | -1 | ±0.4 | 1 | MI (Note 13) |
| RDNL (Note 15) | Differential Non-linearity | W option | -1.5 | ±0.5 | 1.5 | MI (Note 13) |
| | | U, T option | -0.5 | ±0.15 | 0.5 | MI (Note 13) |
| Roffset (Note 14) | Offset | W option | 0 | 1 | 5 | MI (Note 13) |
| | | U, T option | 0 | 0.5 | 2 | MI (Note 13) |
| $R_{MATCH}$ (Note 17) | DCP-to-DCP Matching | Wipers at the same tap position with the same terminal voltages | -2 | | 2 | MI (Note 13) |
| $TC_R$ (Notes 18, 19) | Resistance Temperature Coefficient | DCP register set between 32hex and FF hex | | ±40 | | ppm/°C |

## Operating Specifications

Over the recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | $V_{CC}$ Supply Current (Volatile Write/Read) | $V_{CC}$ = 5.5V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Volatile Write states only) | | 0.01 | 0.2 | mA |
| | | $V_{CC}$ = 2.25V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Volatile Write states only) | | 0.005 | 0.1 | mA |
| $I_{V-1}$ | V- Supply Current (Volatile Write/Read) | V- = -5.5V, $V_{CC}$ = 5.5V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Volatile Write states only) | -0.2 | -0.05 | | mA |
| | | V- = -2.25V, $V_{CC}$ = 2.25V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Volatile Write states only) | -0.1 | -0.02 | | mA |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Non-volatile Write/Read) | $V_{CC}$ = 5.5V, V- = 5.5V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Non-volatile Write states only) | | 1.0 | 2.0 | mA |
| | | $V_{CC}$ = 2.25V, V- = -2.25V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Non-volatile Write states only) | | 0.3 | 1.0 | mA |
| $I_{V-2}$ | V- Supply Current (Non-volatile Write/Read) | V- = -5.5V, $V_{CC}$ = 5.5V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Non-volatile Write states only) | -2.0 | -1.2 | | mA |
| | V- Supply Current (Non-volatile Write/Read) | V- = -2.25V, $V_{CC}$ = 2.25V, $f_{SCL}$ = 400kHz; (for $I^2C$ Active, Read and Non-volatile Write states only) | -1.0 | -0.4 | | mA |

**Operating Specifications** Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| $I_{SB}$ | $V_{CC}$ Current (Standby) | $V_{CC}$ = +5.5V, V- = -5.5V @ +85°C, $I^2C$ interface in standby state | | 0.5 | 2.0 | µA |
| | | $V_{CC}$ = +5.5V, V- = -5.5V @ +125°C, $I^2C$ interface in standby state | | 1.0 | 4.0 | µA |
| | | $V_{CC}$ = +2.25V, V- = -2.25V @ +85°C, $I^2C$ interface in standby state | | 0.2 | 1.0 | µA |
| | | $V_{CC}$ = +2.25V, V- = -2.25V @ +125°C, $I^2C$ interface in standby state | | 0.5 | 2.0 | µA |
| $I_{V-SB}$ | V- Current (Standby) | V- = -5.5V, $V_{CC}$ = +5.5V @ +85°C, $I^2C$ interface in standby state | -3.0 | -0.7 | | µA |
| | | V- = -5.5V, $V_{CC}$ = +5.5V @ +125°C, $I^2C$ interface in standby state | -5.0 | -1.5 | | µA |
| | | V- = -2.25V, $V_{CC}$ = +2.25V @ +85°C, $I^2C$ interface in standby state | -2.0 | -0.3 | | µA |
| | | V- = -2.25V, $V_{CC}$ = +2.25V @ +125°C, $I^2C$ interface in standby state | -3.0 | -0.4 | | µA |
| $I_{SD}$ | $V_{CC}$ Current (Shut-down) | $V_{CC}$ = +5.5V, V- = -5.5V @ +85°C, $I^2C$ interface in standby state | | 0.5 | 2.0 | µA |
| | | $V_{CC}$ = +5.5V, V- = -5.5V @ +125°C, $I^2C$ interface in standby state | | 1.0 | 4.0 | µA |
| | | $V_{CC}$ = +2.25V, V- = -2.25V @ +85°C, $I^2C$ interface in standby state | | 0.2 | 1.0 | µA |
| | | $V_{CC}$ = +2.25V, V- = -2.25V @ +125°C, $I^2C$ interface in standby state | | 0.5 | 2.0 | µA |
| $I_{V-SB}$ | V- Current (Standby) | V- = -5.5V, $V_{CC}$ = +5.5V @ +85°C, $I^2C$ interface in standby state | -3.0 | -0.7 | | µA |
| | | V- = -5.5V, $V_{CC}$ = +5.5V @ +125°C, $I^2C$ interface in standby state | -5.0 | -1.5 | | µA |
| | | V- = -2.25V, $V_{CC}$ = +2.25V @ +85°C, $I^2C$ interface in standby state | -2.0 | -0.3 | | µA |
| | | V- = -2.25V, $V_{CC}$ = +2.25V @ +125°C, $I^2C$ interface in standby state | -3.0 | -0.4 | | µA |
| $I_{LkgDig}$ | Leakage Current, at Pins A0, A1, A2, SDA, and SCL | Voltage at pin from GND to $V_{CC}$ | -1 | | 1 | µA |
| $t_{WRT}$ (Note 19) | DCP Wiper Response Time | SCL falling edge of last bit of DCP data byte to wiper new position | | 1.5 | | µs |
| $t_{ShdnRec}$ (Note 19) | DCP Recall Time from Shut-down Mode | SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection | | 1.5 | | µs |
| Vpor | Power-on Recall Voltage | Minimum $V_{CC}$ at which memory recall occurs | 1.9 | | 2.1 | V |
| VCCRamp | $V_{CC}$ Ramp Rate | | 0.2 | | | V/ms |
| $t_D$ | Power-up Delay | $V_{CC}$ above Vpor, to DCP Initial Value Register recall completed, and $I^2C$ Interface in standby state | | | 5 | ms |

**Operating Specifications** Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| **EEPROM SPECIFICATION** | | | | | | |
| | EEPROM Endurance | | 1,000,000 | | | Cycles |
| | EEPROM Retention | Temperature T ≤ +55°C | 50 | | | Years |
| $t_{WC}$ (Note 20) | Non-volatile Write Cycle Time | | | 12 | 20 | ms |
| **SERIAL INTERFACE SPECS** | | | | | | |
| $V_{IL}$ | A0, A1, A2, SDA, and SCL Input Buffer LOW Voltage | | | | $0.3*V_{CC}$ | V |
| $V_{IH}$ | A0, A1, A2, SDA, and SCL Input Buffer HIGH Voltage | | $0.7*V_{CC}$ | | | V |
| Hysteresis (Note 19) | SDA and SCL Input Buffer Hysteresis | | $0.05*V_{CC}$ | | | V |
| $V_{OL}$ (Note 19) | SDA Output Buffer LOW Voltage, Sinking 4mA | | 0 | | 0.4 | V |
| Cpin (Note 19) | A0, A1, A2, SDA, and SCL Pin Capacitance | | | | 10 | pF |
| $f_{SCL}$ | SCL Frequency | | | | 400 | kHz |
| $t_{sp}$ | Pulse Width Suppression Time at SDA and SCL Inputs | Any pulse narrower than the max spec is suppressed | | | 50 | ns |
| $t_{AA}$ (Note 19) | SCL Falling Edge to SDA Output Data Valid | SCL falling edge crossing 30% of $V_{CC}$, until SDA exits the 30% to 70% of $V_{CC}$ window | | | 900 | ns |
| $t_{BUF}$ (Note 19) | Time the Bus Must be Free Before The Start of a New Transmission | SDA crossing 70% of $V_{CC}$ during a STOP condition, to SDA crossing 70% of $V_{CC}$ during the following START condition | 1300 | | | ns |
| $t_{LOW}$ | Clock LOW Time | Measured at the 30% of $V_{CC}$ crossing | 1300 | | | ns |
| $t_{HIGH}$ | Clock HIGH Time | Measured at the 70% of $V_{CC}$ crossing | 600 | | | ns |
| $t_{SU:STA}$ | START Condition Setup Time | SCL rising edge to SDA falling edge; both crossing 70% of $V_{CC}$ | 600 | | | ns |
| $t_{HD:STA}$ | START Condition Hold Time | From SDA falling edge crossing 30% of $V_{CC}$ to SCL falling edge crossing 70% of $V_{CC}$ | 600 | | | ns |
| $t_{SU:DAT}$ | Input Data Setup Time | From SDA exiting the 30% to 70% of $V_{CC}$ window, to SCL rising edge crossing 30% of $V_{CC}$ | 100 | | | ns |
| $t_{HD:DAT}$ | Input Data Hold Time | From SCL rising edge crossing 70% of $V_{CC}$ to SDA entering the 30% to 70% of $V_{CC}$ window | 0 | | | ns |
| $t_{SU:STO}$ | STOP Condition Setup Time | From SCL rising edge crossing 70% of $V_{CC}$, to SDA rising edge crossing 30% of $V_{CC}$ | 600 | | | ns |
| $t_{HD:STO}$ | STOP Condition Hold Time for Read, or Volatile Only Write | From SDA rising edge to SCL falling edge; both crossing 70% of $V_{CC}$ | 1300 | | | ns |
| $t_{DH}$ (Note 19) | Output Data Hold Time | From SCL falling edge crossing 30% of $V_{CC}$, until SDA enters the 30% to 70% of $V_{CC}$ window | 0 | | | ns |
| $t_R$ (Note 19) | SDA and SCL Rise Time | From 30% to 70% of $V_{CC}$ | 20 + 0.1*Cb | | 250 | ns |
| $t_F$ (Note 19) | SDA and SCL Fall Time | From 70% to 30% of $V_{CC}$ | 20 + 0.1*Cb | | 250 | ns |

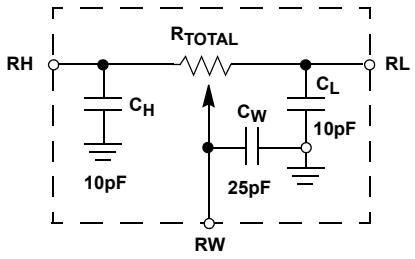
**Operating Specifications** Over the recommended operating conditions unless otherwise specified. **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 21) | TYP (Note 5) | MAX (Note 21) | UNIT |
|---|---|---|---|---|---|---|
| Cb (Note 19) | Capacitive Loading of SDA or SCL | Total on-chip and off-chip | 10 | | 400 | pF |
| Rpu (Note 19) | SDA and SCL Bus Pull-up Resistor Off-chip | Maximum is determined by $t_R$ and $t_F$<br>For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ<br>For Cb = 40pF, max is about 15kΩ ~ 20kΩ | 1 | | | kΩ |
| $t_{SU:A}$ | A0, A1, and A2 Setup Time | Before START condition | 600 | | | ns |
| $t_{HD:A}$ | A0, A1, and A2 Hold Time | After STOP condition | 600 | | | ns |

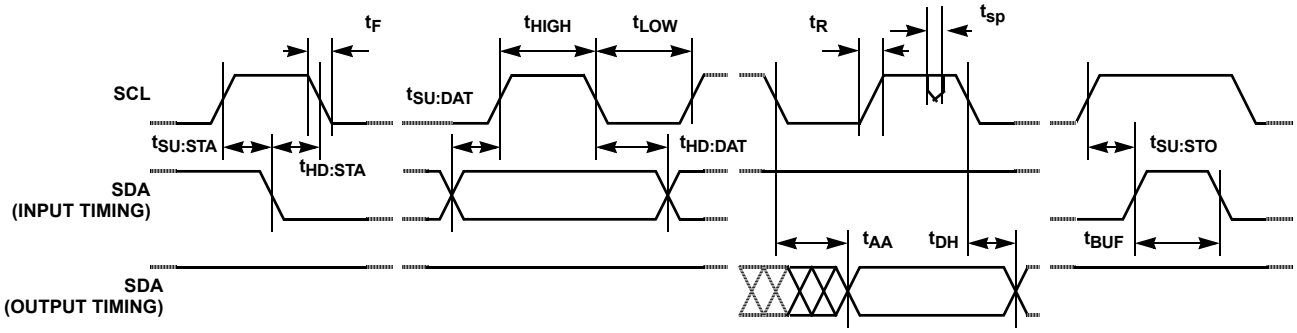
NOTES:

5. Typical values are for $T_A$ = +25°C and 3.3V supply voltage.
6. LSB: $[V(R_W)_{255} – V(R_W)_0]/255$. $V(R_W)_{255}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.
8. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
10. INL = $[V(RW)_i – i • LSB – V(RW)_0]$/LSB for i = 1 to 255
11. $V_{MATCH}$= [V(RWx)i -V(RWy)i]/LSB, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
12. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
13. MI = $|RW_{255} – RW_0|/255$. MI is a minimum increment. $RW_{255}$ and $RW_0$ are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
14. $R_{OFFSET} = RW_0$/MI, when measuring between RW and RL.
    $R_{OFFSET} = RW_{255}$/MI, when measuring between RW and RH.
15. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 16 to 255.
16. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 16 to 255.
17. $R_{MATCH}$= [(Rx)i -(Ry)i]/MI, for i = 0 to 255, x = 0 to 1, y = 0 to 1.
18. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 240, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
19. This parameter is not 100% tested.
20. $t_{WC}$ is the time from a valid STOP condition at the end of a Write sequence of $I^2C$ serial interface, to the end of the self-timed internal non-volatile write cycle.
21. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

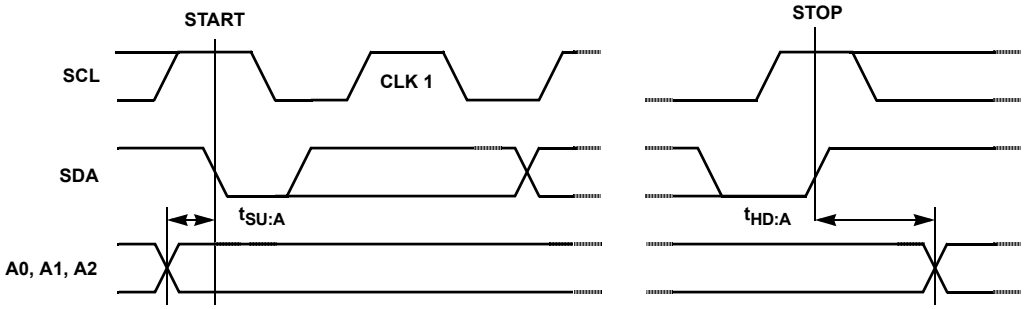
### DCP Macro Model




### SDA vs SCL Timing




### A0, A1 and A2 Pin Timing




## Typical Performance Curves

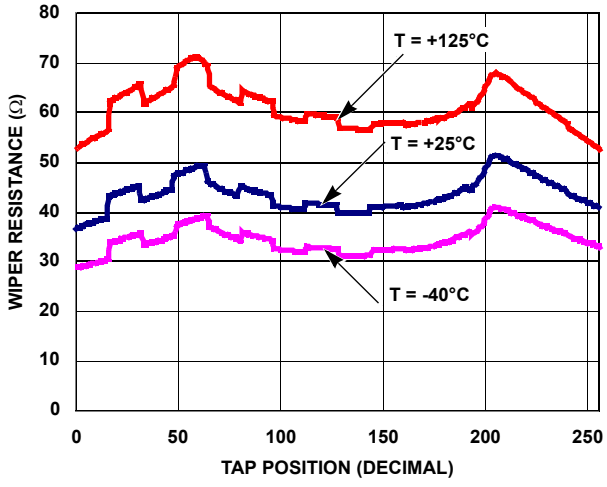



FIGURE 1. WIPER RESISTANCE vs TAP POSITION [ I(RW) = $V_{CC}/R_{TOTAL}$ ] FOR 10kΩ (W)

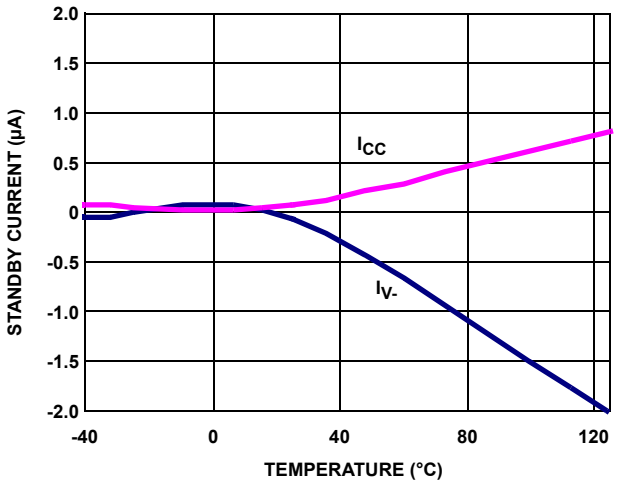



FIGURE 2. STANDBY $I_{CC}$ and $I_{V-}$ vs TEMPERATURE

## *Typical Performance Curves* (Continued)

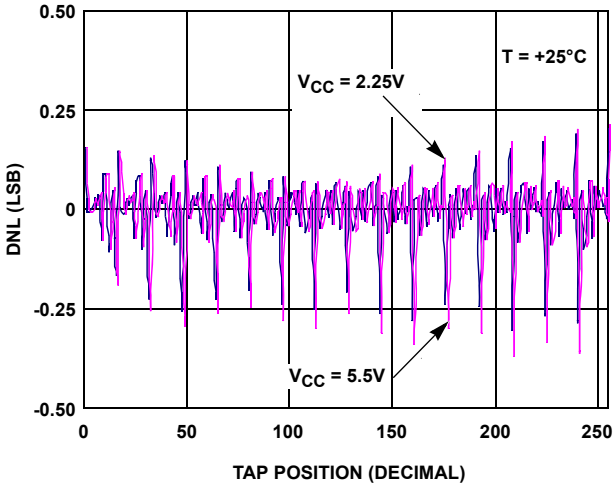



FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

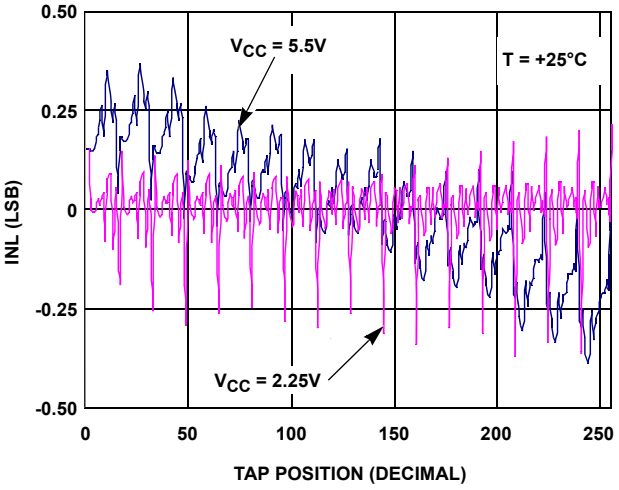



FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

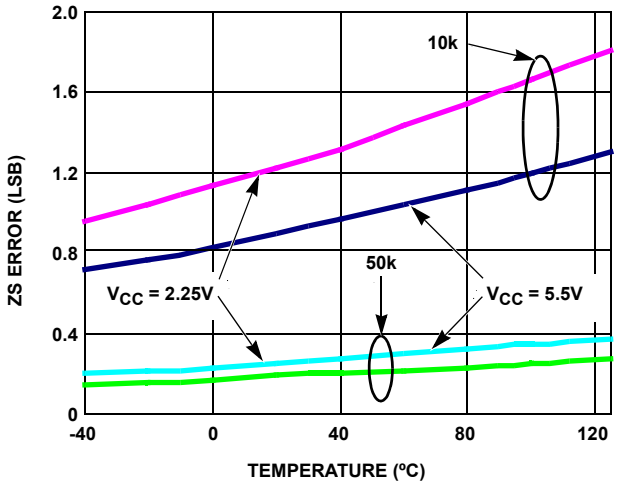



FIGURE 5. ZS ERROR vs TEMPERATURE

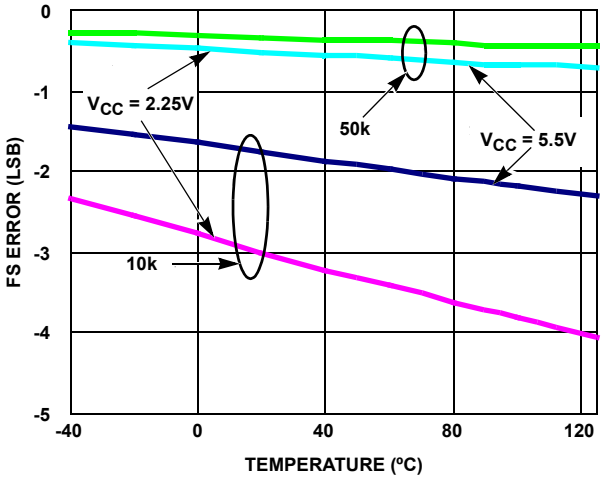



FIGURE 6. FS ERROR vs TEMPERATURE

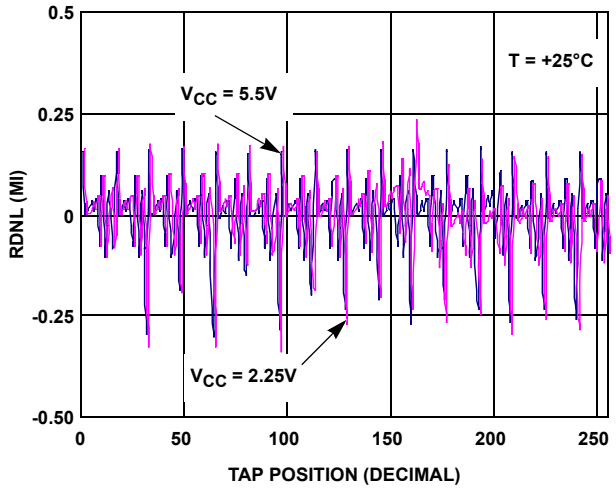



FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

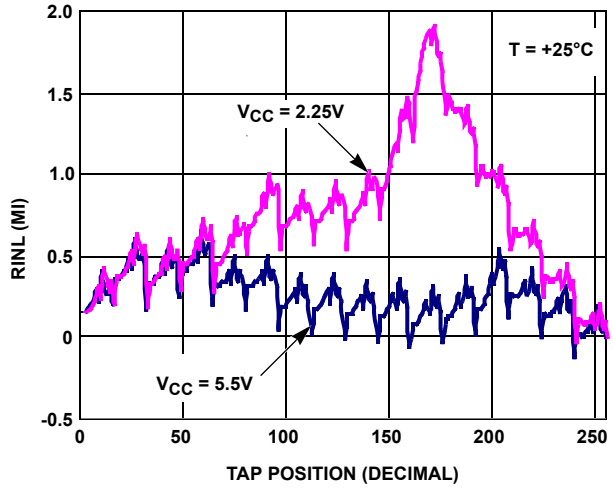



FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

## *Typical Performance Curves* (Continued)

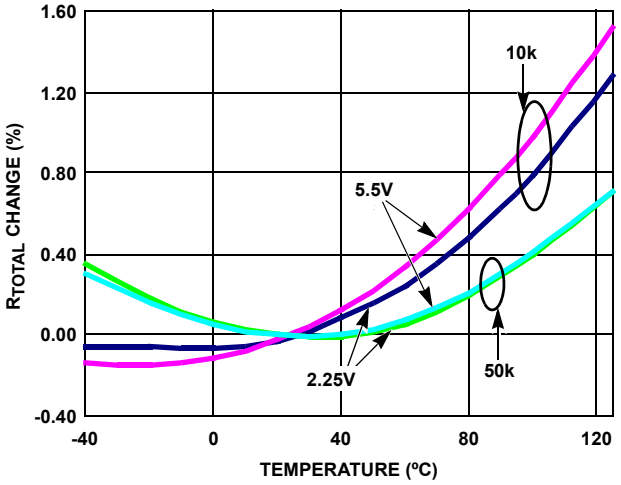



FIGURE 9. END TO END $R_{TOTAL}$ % CHANGE vs TEMPERATURE

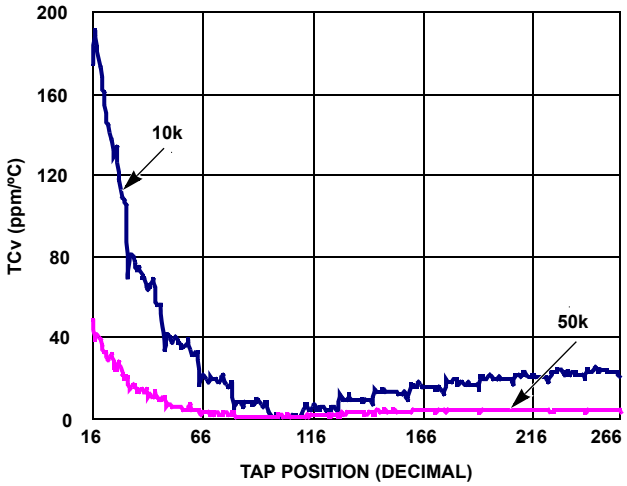



FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

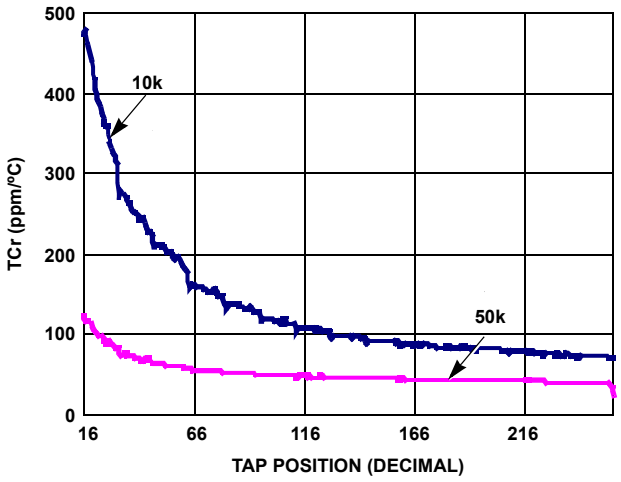



FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

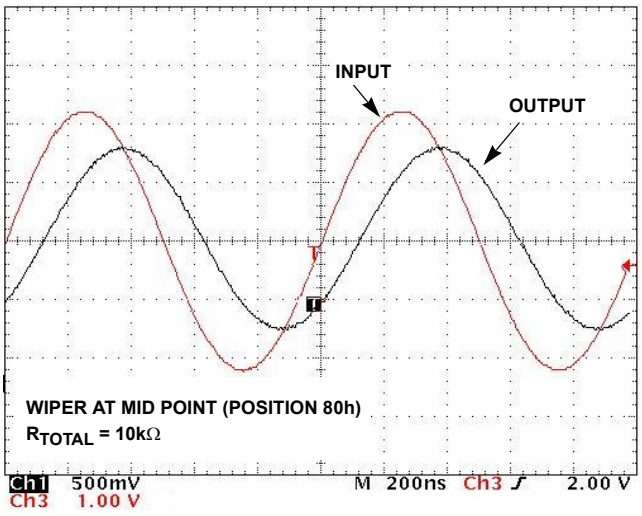



FIGURE 12. FREQUENCY RESPONSE (1MHz)

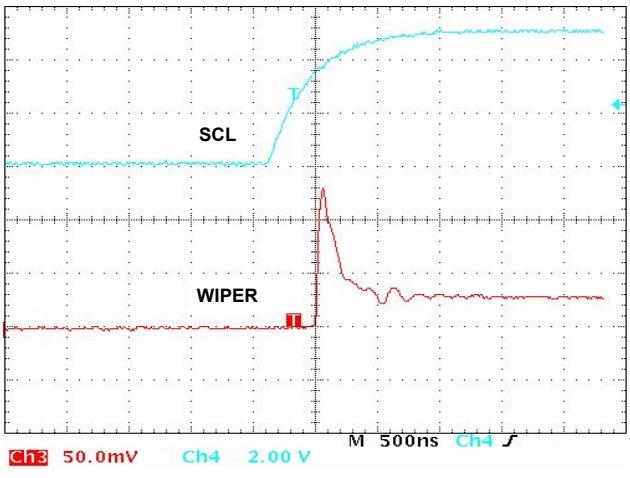



FIGURE 13. MIDSCALE GLITCH, CODE 7Fh TO 80h

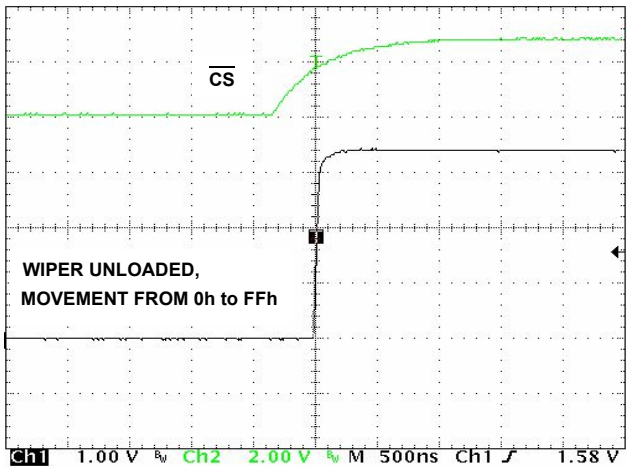



FIGURE 14. LARGE SIGNAL SETTLING TIME

## Pin Description

### Potentiometers Pins

#### RHI AND RLi

The high (RHi) and low (RLi) terminals of the ISL22323 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 255 decimal, the wiper will be closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

#### RWi

RWi is the wiper terminal, and it is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

### Bus Interface Pins

#### SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for $I^2C$ interface. It receives device address, operation code, wiper address and data from an $I^2C$ external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

#### SERIAL CLOCK (SCL)

This input is the serial clock of the $I^2C$ serial interface. SCL requires an external pull-up resistor.

#### DEVICE ADDRESS (A2, A1, A0)

The address inputs are used to set the least significant 3 bits of the 7-bit $I^2C$ interface slave address. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22323. A maximum of eight ISL22323 devices may occupy the $I^2C$ serial bus (See Table 3).

## Principles of Operation

The ISL22323 is an integrated circuit incorporating two DCPs with its associated registers, non-volatile memory and an $I^2C$ serial interface providing direct communication between a host and the potentiometer and memory. The resistor arrays are comprised of individual resistors connected in a series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi will be maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to their initial positions.

### DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RHi and RLi pins). The RWi pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WRi). When the WRi of a DCP contains all zeroes (WRi[7:0]= 00h), its wiper terminal (RWi) is closest to its “Low” terminal (RLi). When the WRi register of a DCP contains all ones (WRi[7:0] = FFh), its wiper terminal (RWi) is closest to its “High” terminal (RHi). As the value of the WRi increases from all zeroes (0) to all ones (255 decimal), the wiper moves monotonically from the position closest to RLi to the position closest to RHi. At the same time, the resistance between RWi and RLi increases monotonically, while the resistance between RHi and RWi decreases monotonically.

While the ISL22323 is being powered up, the WRi is reset to 80h (128 decimal), which locates RWi roughly at the center between RLi and RHi. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WRi will be reloaded with the value stored in corresponding non-volatile Initial Value Register (IVRi).

The WRi and IVRi can be read or written to directly using the $I^2C$ serial interface as described in the following sections.

### Memory Description

The ISL22323 contains two non-volatile 8-bit Initial Value Register (IVRi), thirteen General Purpose non-volatile 8-bit registers and three volatile 8-bit registers: two Wiper Registers (WRi) and Access Control Register (ACR). Memory map of ISL22323 is in Table 1. The non-volatile registers (IVRi) at address 0 and 1, contain initial wiper position and volatile registers (WRi) contain current wiper position.

**TABLE 1. MEMORY MAP**

| ADDRESS (hex) | NON-VOLATILE | VOLATILE |
|---|---|---|
| 10 | N/A | ACR |
| F | Reserved | |
| E | General Purpose | N/A |
| D | General Purpose | N/A |
| C | General Purpose | N/A |
| B | General Purpose | N/A |
| A | General Purpose | N/A |
| 9 | General Purpose | N/A |
| 8 | General Purpose | N/A |
| 7 | General Purpose | N/A |

**TABLE 1. MEMORY MAP (Continued)**

| ADDRESS (hex) | NON-VOLATILE | VOLATILE |
|---|---|---|
| 6 | General Purpose | N/A |
| 5 | General Purpose | N/A |
| 4 | General Purpose | N/A |
| 3 | General Purpose | N/A |
| 2 | General Purpose | N/A |
| 1 | IVR1 | WR1 |
| 0 | IVR0 | WR0 |

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2.

The VOL bit (ACR[7]) determines whether the access to wiper registers WRi or initial value registers IVRi.

**TABLE 2. ACCESS CONTROL REGISTER (ACR)**

| BIT # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| NAME | VOL | $\overline{SHDN}$ | WIP | 0 | 0 | 0 | 0 | 0 |

If VOL bit is 0, the non-volatile IVRi registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. Note: value is written to IVRi register also is written to the corresponding WRi. The default value of this bit is 0.

The $\overline{SHDN}$ bit (ACR[6]) disables or enables Shut-down mode. When this bit is 0, DCPs are in Shut-down mode. Default value of the $\overline{SHDN}$ bit is 1.

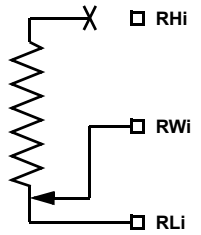



**FIGURE 15. DCP CONNECTION IN SHUT-DOWN MODE**

The WIP bit (ACR[5]) is a read-only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WRi or ACR while WIP bit is 1.

## *I²C Serial Interface*

The ISL22323 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22323 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

### *Protocol Conventions*

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 16). On power-up of the ISL22323, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22323 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 16). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 16). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK (Acknowledge) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 17).

The ISL22323 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22323 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1 and A0. The LSB is the Read/$\overline{Write}$ bit. Its value is “1” for a Read operation and “0” for a Write operation (See Table 3).

**TABLE 3. IDENTIFICATION BYTE FORMAT**

| | | | | LOGIC VALUES AT PINS A2, A1 AND A0, RESPECTIVELY | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | A2 | A1 | A0 | R/$\overline{W}$ |
| (MSB) | | | | | | | (LSB) |

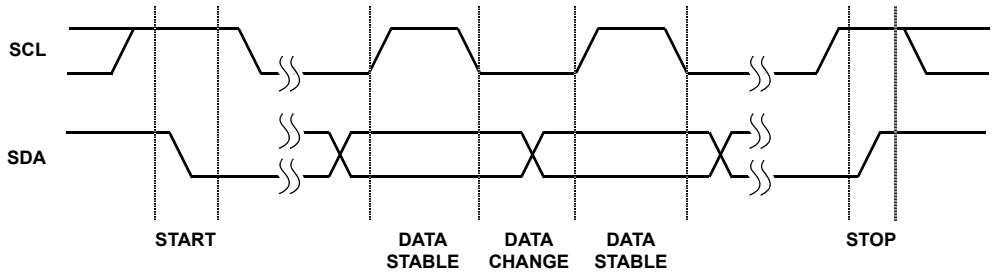



FIGURE 16. VALID DATA CHANGES, START AND STOP CONDITIONS

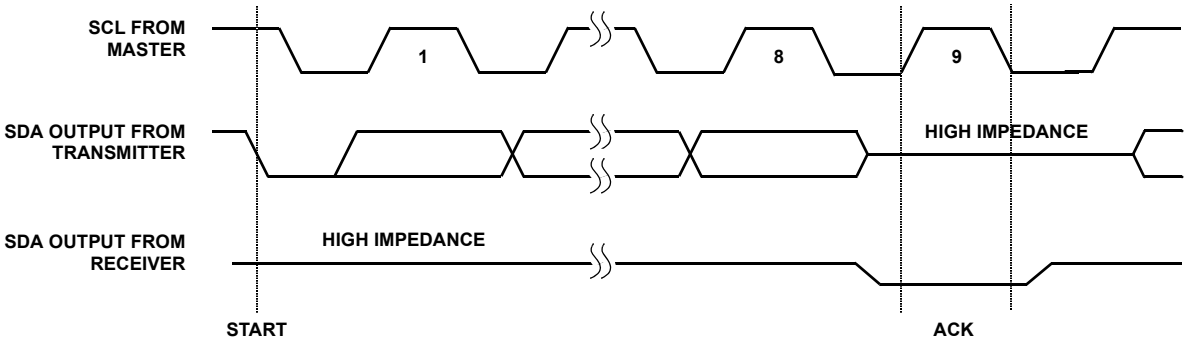



FIGURE 17. ACKNOWLEDGE RESPONSE FROM RECEIVER

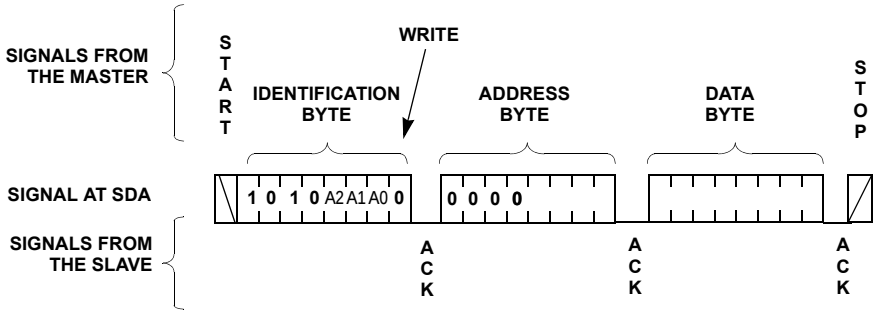



FIGURE 18. BYTE WRITE SEQUENCE

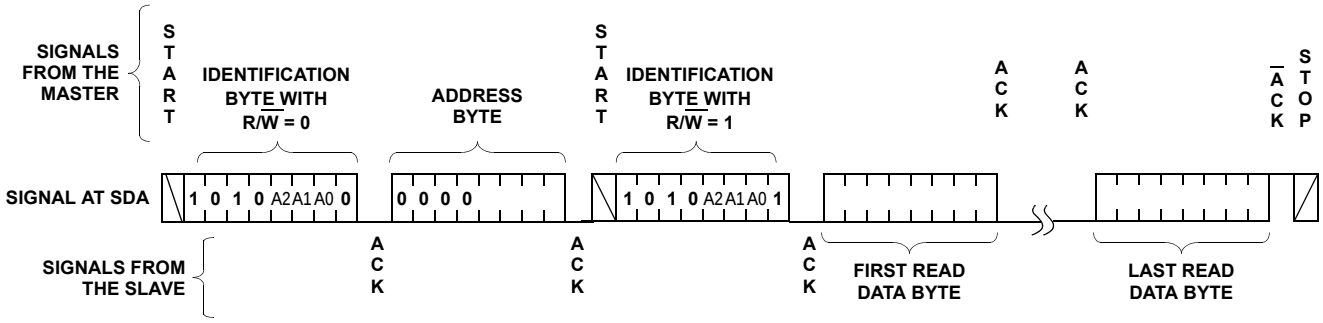



FIGURE 19. READ SEQUENCE

### *Write Operation*

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22323 responds with an ACK. At this time, the device enters its standby state (See Figure 18).

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

### *Read Operation*

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 19). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22323 responds with an ACK. Then the ISL22323 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The Data Bytes are from the registers indicated by an internal pointer. This pointers initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 0Fh, the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.The master terminates the read operation issuing a NACK ($\overline{ACK}$) and a STOP condition following the last bit of the last Data Byte (See Figure 19).

## *Applications Information*

### *Wiper Transition*

When stepping up through each tap in voltage divider mode, some tap transition points can result in noticeable voltage transients (or overshoot/undershoot) resulting from the sudden transition from a very low impedance “make” to a much higher impedance “break within an extremely short period of time (<50ns). Two such code transitions are EFh to F0h, and 0Fh to 10h. Note that all switching transients will settle well within the settling time as stated on the datasheet. A small capacitor can be added externally to reduce the amplitude of these voltage transients, but that will also reduce the useful bandwidth of the circuit, thus this may not be a good solution for some applications. It may be a good idea, in that case, to use fast amplifiers in a signal chain for fast recovery.

### *Application Example*

Figure 20 shows an example of using ISL22323 for gain setting and offset correction in high side current measurement application. DCP0 applies a programmable offset voltage of ±25mV to the FB+ pin of the Instrumentation Amplifier EL8173 to adjust output offset to zero voltages. DCP1 programs the gain of the EL8173 from 90 to 110 with 5V output for 10A current through current sense resistor.

More application examples can be found at:
http://www.intersil.com/data/an/AN1145.pdf

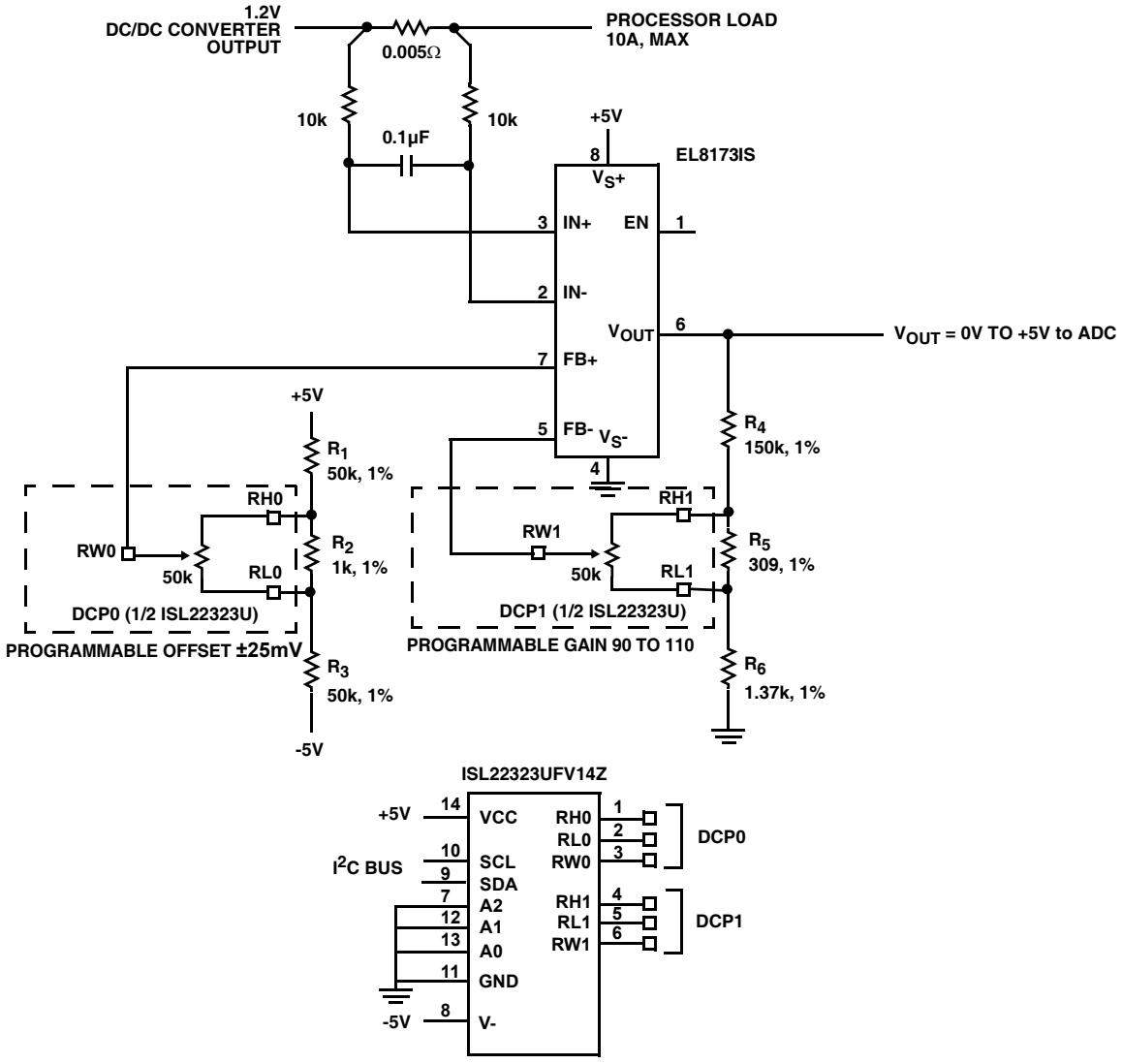



FIGURE 20. CURRENT SENSING WITH GAIN AND OFFSET CONTROL

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| August 17, 2015 | FN6422.2 | - Ordering Information Table on page 2.<br>- Added Revision History<br>- Added About Intersil Verbiage.<br>- Updated POD L16.4X4A to latest revision changes are as follow:<br>Updated to new POD format by removing table listing dimensions and moving dimensions onto drawing.<br>Added Typical Recommended Land Pattern. Removed package option.<br>- Updated POD M14.173 to most current version changes are as follow:<br>Updated drawing to remove table and added land pattern. |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

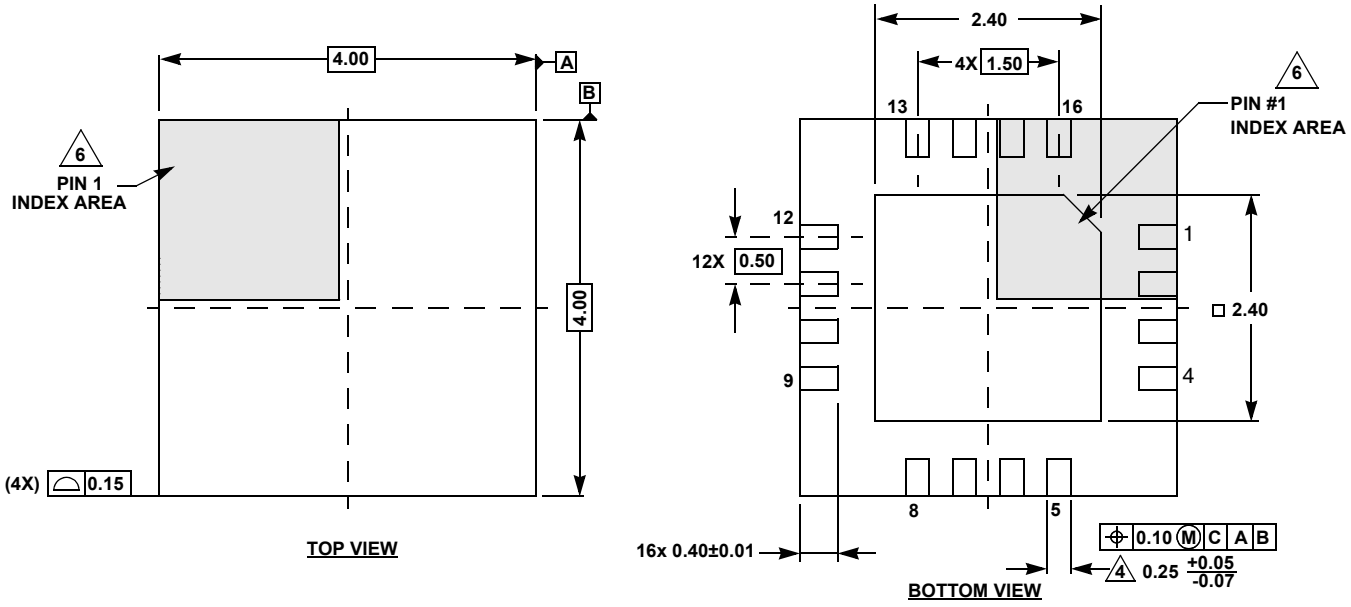
Reliability reports are also available from our website at www.intersil.com/support

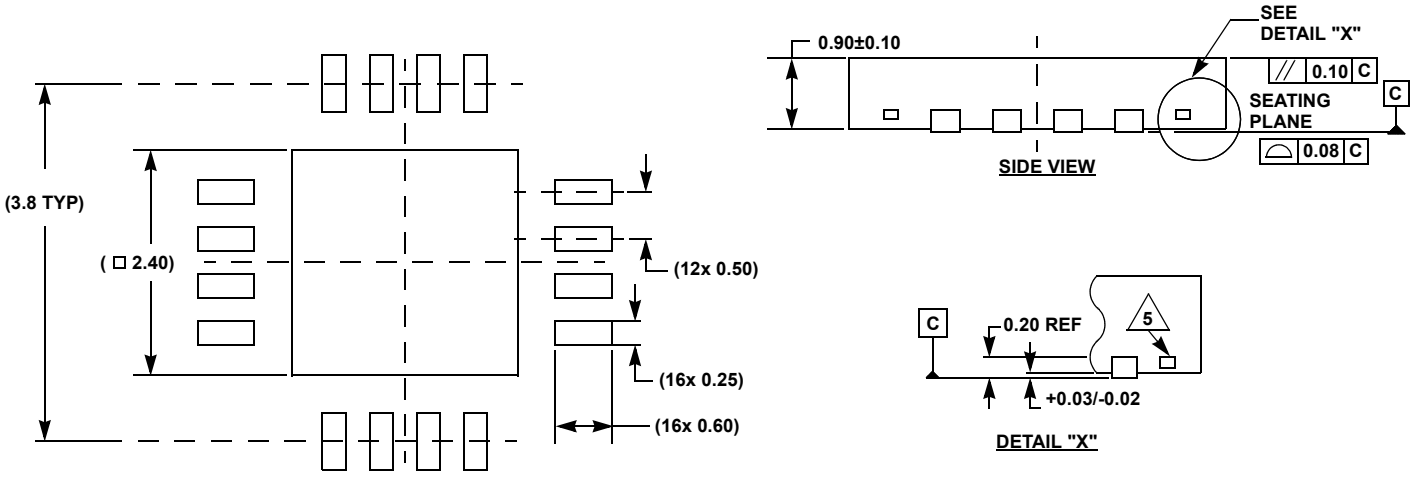
# Package Outline Drawing

## L16.4x4A

**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**

**Rev 3, 03/15**



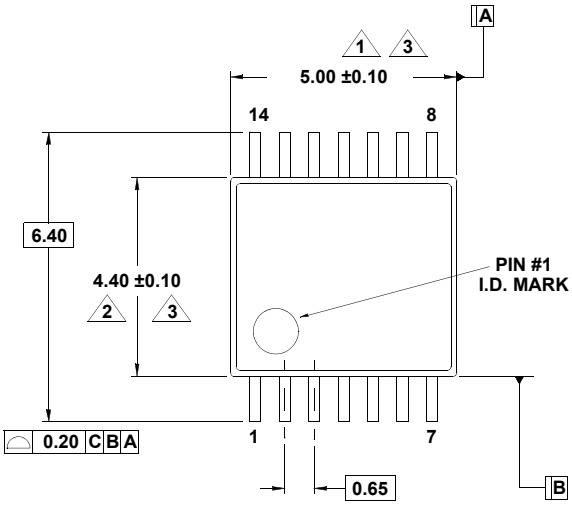

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

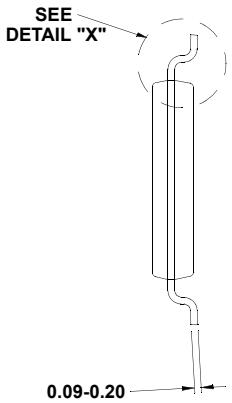
# Package Outline Drawing

## M14.173

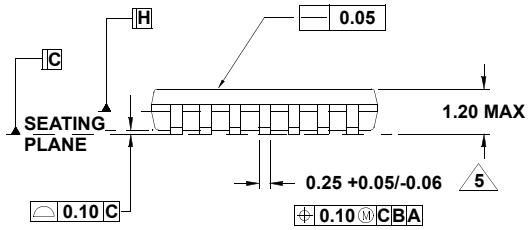
**14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**
**Rev 3, 10/09**



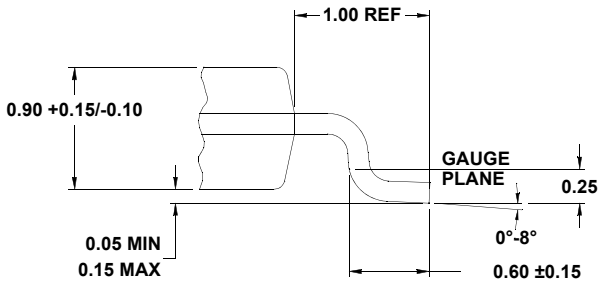

TOP VIEW



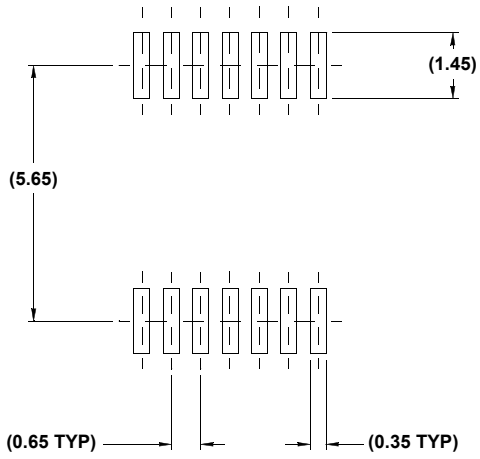

END VIEW




SIDE VIEW




DETAIL "X"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.