



DMOS

400mA Low-Dropout Regulator

FEATURES

- **CAP-FREE DMOS TOPOLOGY:**
Ultra Low Dropout Voltage:
250mV typ at 400mA
Output Capacitor *not* Required for Stability
- UP TO 500mA PEAK, TYPICAL
- FAST TRANSIENT RESPONSE
- VERY LOW NOISE: 28 μ Vrms
- HIGH ACCURACY: $\pm 1.5\%$ max
- HIGH EFFICIENCY:
 $I_{GND} = 850\mu A$ at $I_{OUT} = 400mA$
Not Enabled: $I_{GND} = 0.01\mu A$
- 2.5V, 2.85V, 3.0V, 3.3V, AND 5.0V OUTPUT VERSIONS
- OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST
- FOLDBACK CURRENT LIMIT
- THERMAL PROTECTION
- SMALL SURFACE-MOUNT PACKAGES:
SOT23-5 and MSOP-8

APPLICATIONS

- PORTABLE COMMUNICATION DEVICES
- BATTERY-POWERED EQUIPMENT
- PERSONAL DIGITAL ASSISTANTS
- MODEMS
- BAR-CODE SCANNERS
- BACKUP POWER SUPPLIES

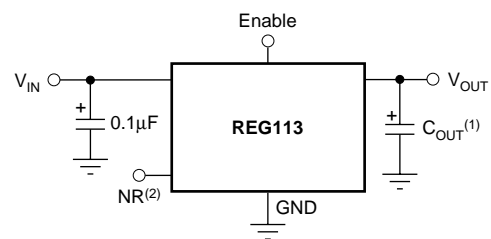
DESCRIPTION

The REG113 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 250mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1 μ F.

Typical ground pin current is only 850 μ A (at $I_{OUT} = 400mA$) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG113 has very low output noise (typically 28 μ Vrms for $V_{OUT} = 3.3V$ with $C_{NR} = 0.01\mu F$), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range ($-40^{\circ}C$ to $+85^{\circ}C$).

The REG113 is well protected—internal circuitry provides a current limit which protects the load from damage, furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG113 is available in SOT23-5 and MSOP-8 packages.



NOTES: (1) Optional. (2) NR = Noise Reduction.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Input Voltage, V_{IN}	-0.3V to 12V
Enable Input Voltage, V_{EN}	-0.3V to V_{IN}
NR Pin Voltage, V_{NR}	-0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	-55°C to +125°C
Storage Temperature Range (T_A)	-65°C to +150°C
Lead Temperature (soldering, 3s)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

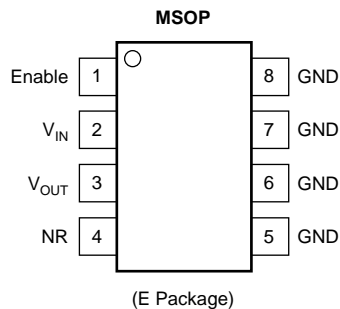
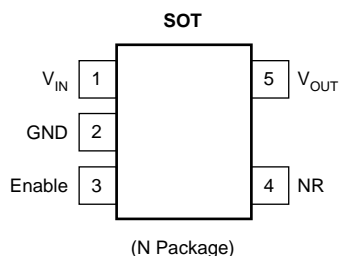
PRODUCT	V_{OUT} ⁽²⁾
REG113xx-yyyy/zzz	<p>XX is package designator.</p> <p>YYYY is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable).</p> <p>ZZZ is package quantity.</p>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

PIN CONFIGURATIONS

Top View



NOTE: Leads 5 through 8 are fused to the lead frame and can be used for improved thermal dissipation.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, $T_J = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

At $T_J = +25^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 1\text{V}$, $V_{ENABLE} = 1.8\text{V}$, $I_{OUT} = 5\text{mA}$, $C_{NR} = 0.01\mu\text{F}$, and $C_{OUT} = 0.1\mu\text{F}^{(1)}$, unless otherwise noted.

PARAMETER	CONDITION	REG113NA REG113EA			UNITS
		MIN	TYP	MAX	
OUTPUT VOLTAGE					
Output Voltage Range	V_{OUT}		2.5		V
REG113-2.5			2.85		V
REG113-2.85			3.0		V
REG113-3			3.3		V
REG113-3.3			5.0		V
REG113-5			± 0.5	± 1.5	%
Accuracy				± 2.3	%
Over Temperature vs Temperature	dV_{OUT}/dT		50	± 2.3	ppm/ $^{\circ}\text{C}$
vs Line and Load		$I_{OUT} = 5\text{mA to } 400\text{mA}$, $V_{IN} = (V_{OUT} + 0.4\text{V})$ to 10V	± 1	± 2.3	%
Over Temperature		$I_{OUT} = 5\text{mA to } 400\text{mA}$, $V_{IN} = (V_{OUT} + 0.6\text{V})$ to 10V		± 3.0	%
DC DROPOUT VOLTAGE⁽²⁾	V_{DROP}		4	10	mV
For all models		$I_{OUT} = 5\text{mA}$	250	325	mV
Over Temperature		$I_{OUT} = 400\text{mA}$		410	mV
VOLTAGE NOISE					
$f = 10\text{Hz to } 100\text{kHz}$	V_n				
Without C_{NR}		$C_{NR} = 0$, $C_{OUT} = 0$	$23\mu\text{Vrms/V} \cdot V_{OUT}$		μVrms
With C_{NR}		$C_{NR} = 0.01\mu\text{F}$, $C_{OUT} = 10\mu\text{F}$	$7\mu\text{Vrms/V} \cdot V_{OUT}$		μVrms
OUTPUT CURRENT					
Current Limit ⁽³⁾	I_{CL}		425	500	575
Over Temperature					600
Short-Circuit Current Limit	I_{SC}			200	
RIPPLE REJECTION				65	dB
$f = 120\text{Hz}$					
ENABLE CONTROL					
V_{ENABLE} HIGH (output enabled)	V_{ENABLE}		1.8		V_{IN}
V_{ENABLE} LOW (output disabled)			-0.2		0.5
I_{ENABLE} HIGH (output enabled)	I_{ENABLE}	$V_{ENABLE} = 1.8\text{V to } V_{IN}$, $V_{IN} = 1.8\text{V to } 6.5^{(4)}$		1	100
I_{ENABLE} LOW (output disabled)		$V_{ENABLE} = 0\text{V to } 0.5\text{V}$		2	100
Output Disable Time		$C_{OUT} = 1.0\mu\text{F}$, $R_{LOAD} = 13\Omega$		50	μs
Output Enable Softstart Time		$C_{OUT} = 1.0\mu\text{F}$, $R_{LOAD} = 13\Omega$		1.5	ms
THERMAL SHUTDOWN					
Junction Temperature				160	$^{\circ}\text{C}$
Shutdown				140	$^{\circ}\text{C}$
Reset from Shutdown					
GROUND PIN CURRENT					
Ground Pin Current	I_{GND}	$I_{OUT} = 5\text{mA}$		400	500
		$I_{OUT} = 400\text{mA}$		850	1000
Enable Pin LOW		$V_{ENABLE} \leq 0.5\text{V}$		0.01	0.2
					μA
INPUT VOLTAGE					
Operating Input Voltage Range ⁽⁵⁾	V_{IN}		1.8		10
Specified Input Voltage Range		$V_{IN} > 1.8\text{V}$	$V_{OUT} + 0.4$		10
Over Temperature		$V_{IN} > 1.8\text{V}$	$V_{OUT} + 0.6$		10
					V
TEMPERATURE RANGE					
Specified Range	T_J		-40		+85
Operating Range	T_J		-55		+125
Storage Range	T_A		-65		+150
Thermal Resistance					
SOT23-5 Surface-Mount	θ_{JA}	Junction-to-Ambient		200	$^{\circ}\text{C/W}$
MSOP-8 Surface-Mount	θ_{JC}	Junction-to-Case		35 ⁽⁶⁾	$^{\circ}\text{C/W}$
	θ_{JA}	Junction-to-Ambient		160 ⁽⁶⁾	$^{\circ}\text{C/W}$

NOTES: (1) The REG113 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.

(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at $V_{IN} = V_{OUT} + 1\text{V}$ at fixed load.

(3) Current limit is the output current that produces a 10% change in output voltage from $V_{IN} = V_{OUT} + 1\text{V}$ and $I_{OUT} = 5\text{mA}$.

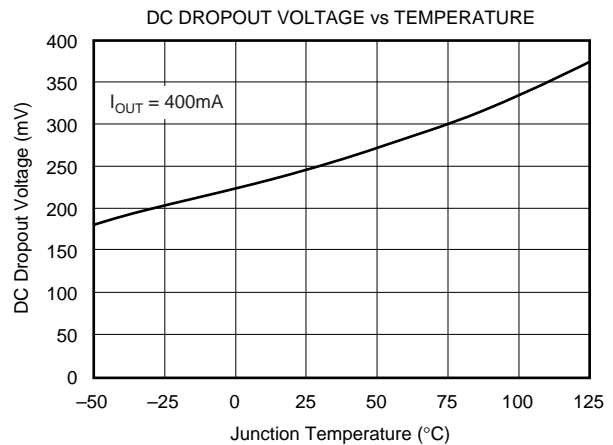
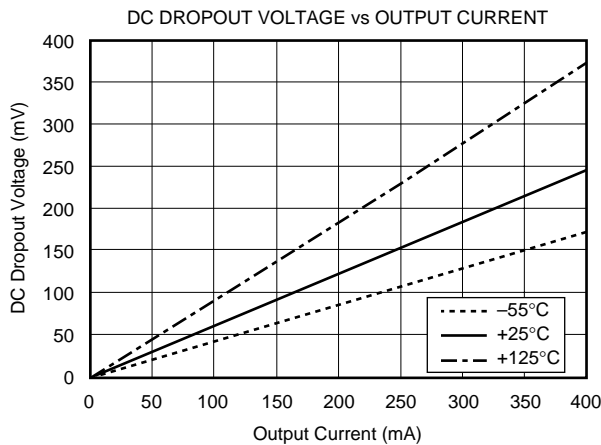
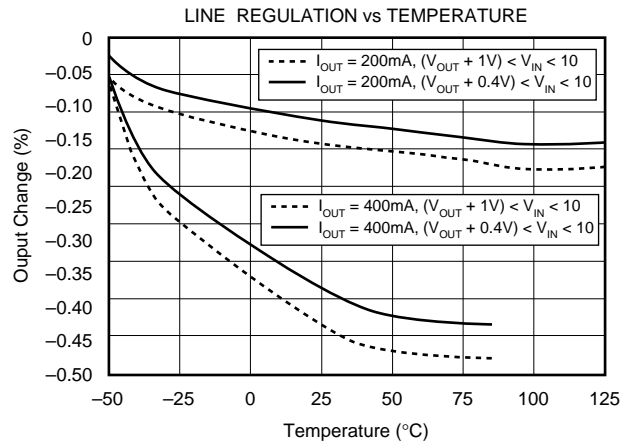
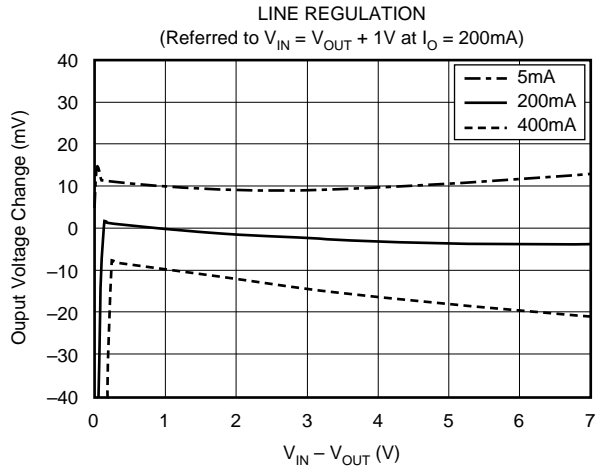
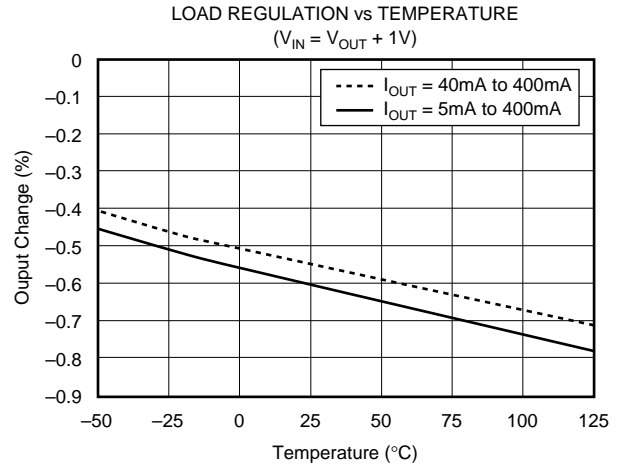
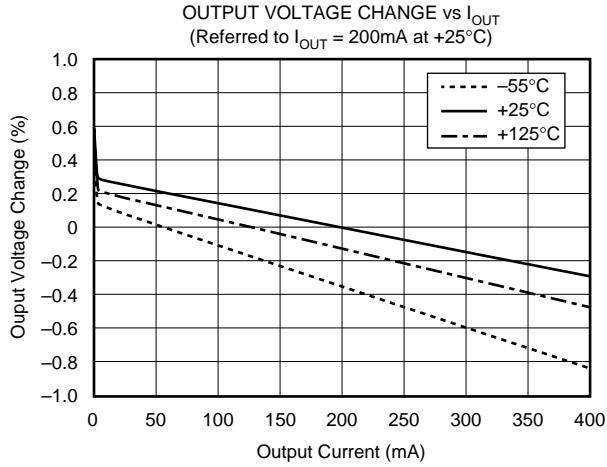
(4) For $V_{ENABLE} > 6.5\text{V}$, see typical characteristic I_{ENABLE} vs V_{ENABLE} .

(5) The REG113 no longer regulates when $V_{IN} < V_{OUT} + V_{DROP(MAX)}$. In dropout, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at $T_J = +25^{\circ}\text{C}$.

(6) See Figure 7.

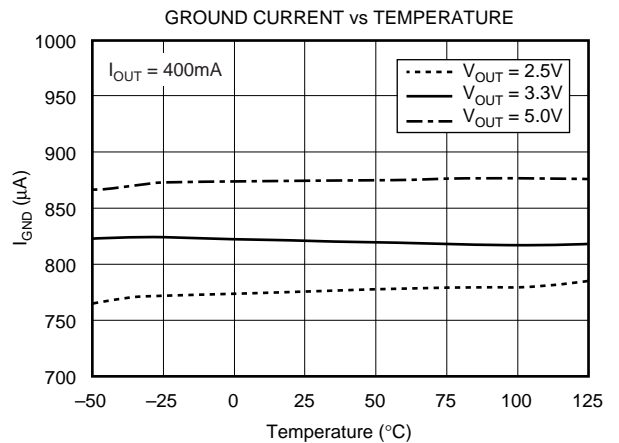
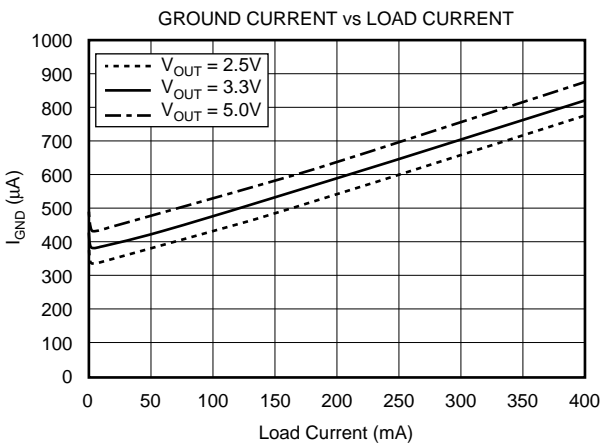
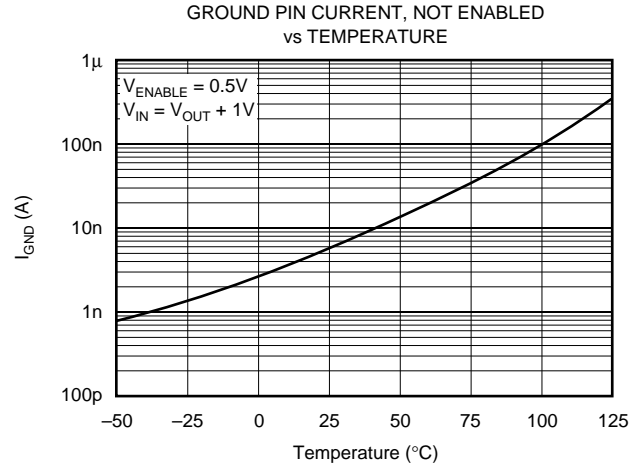
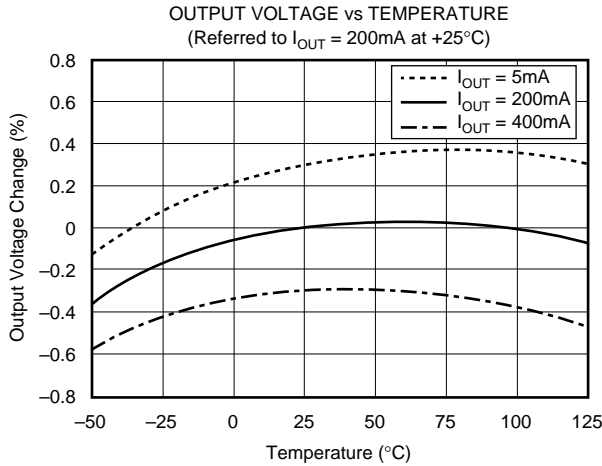
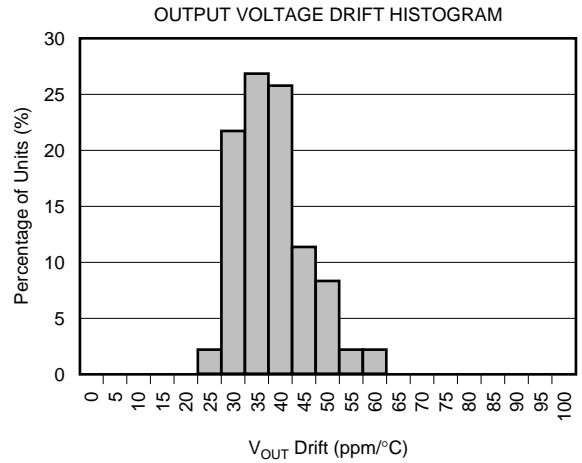
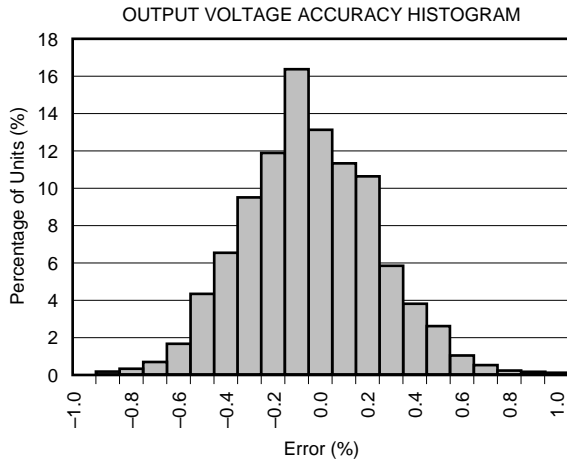
TYPICAL CHARACTERISTICS

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



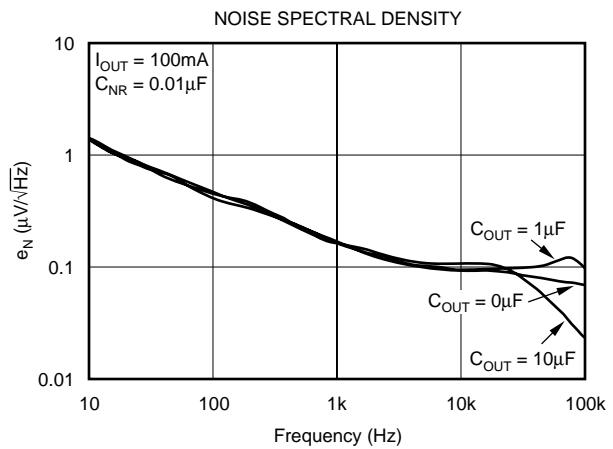
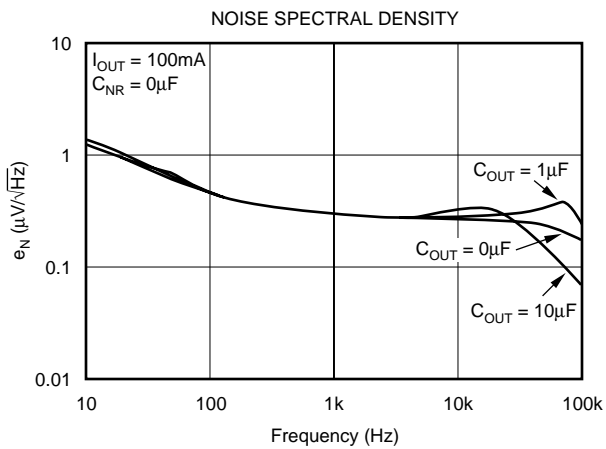
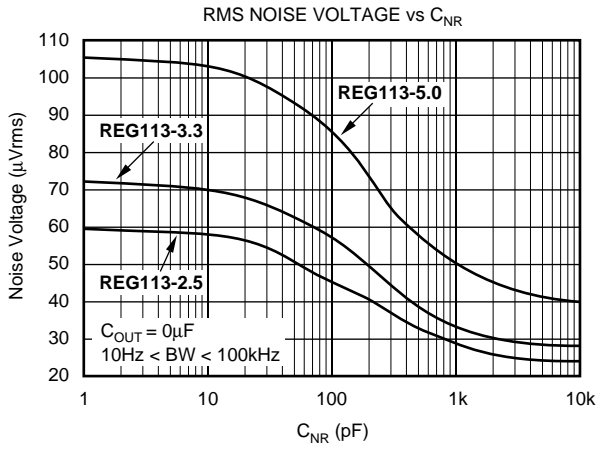
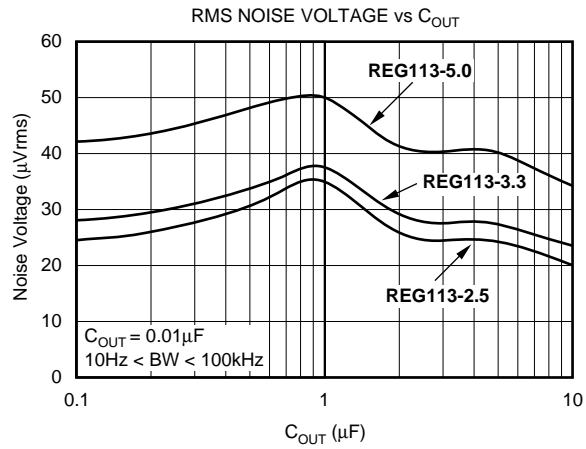
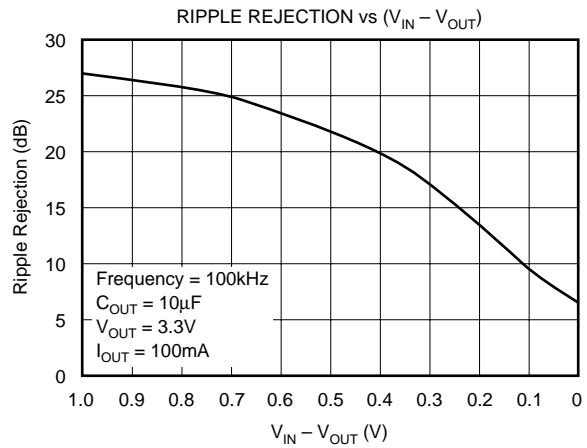
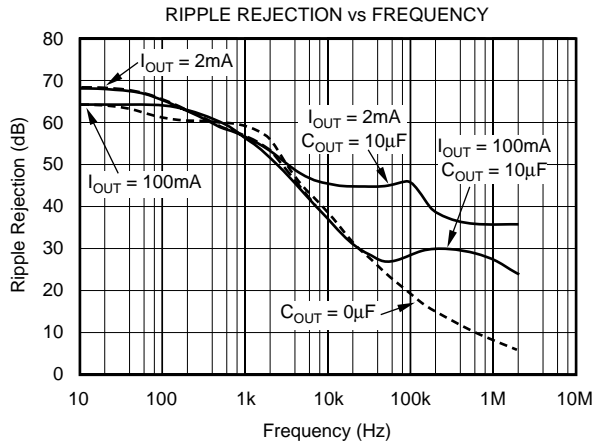
TYPICAL CHARACTERISTICS (Cont.)

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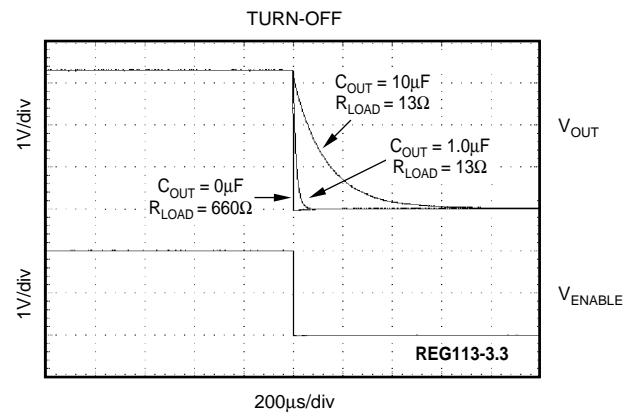
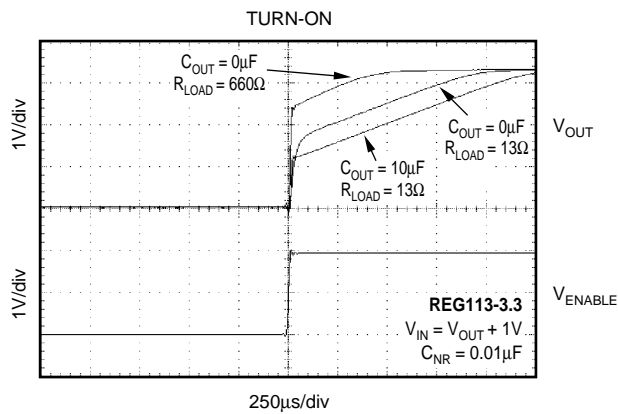
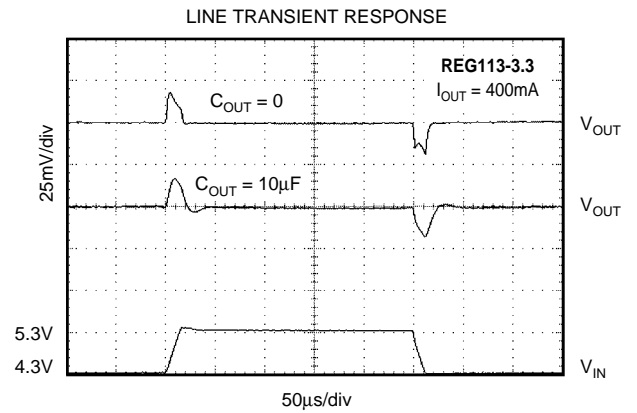
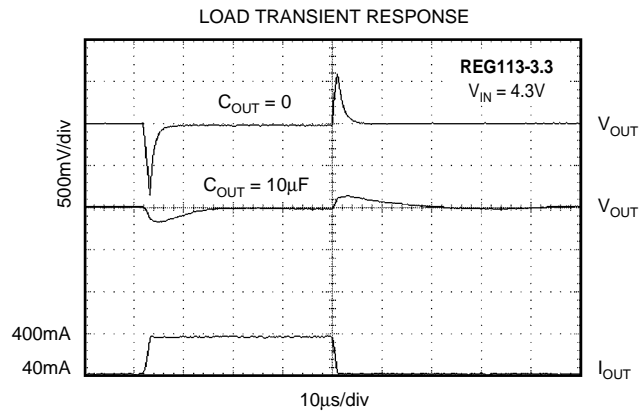
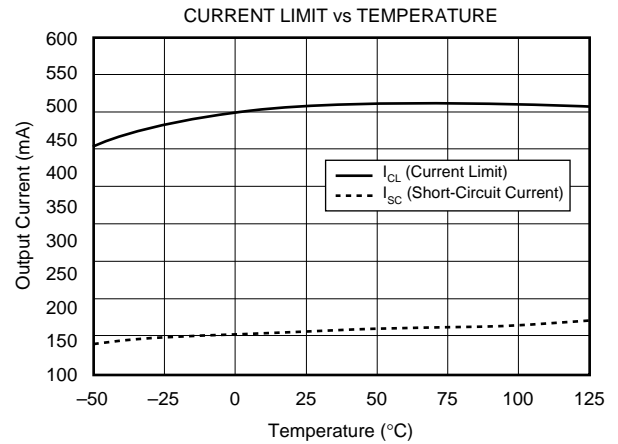
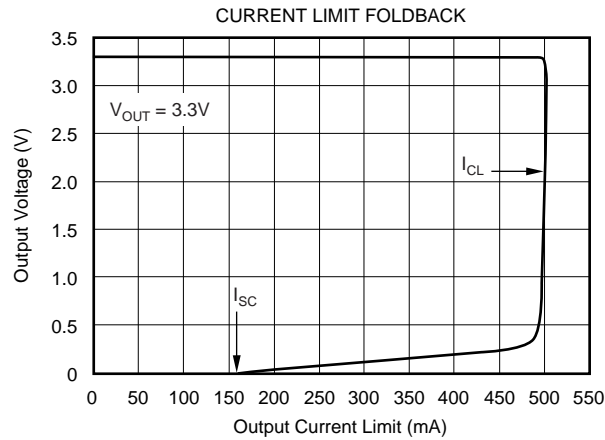
TYPICAL CHARACTERISTICS (Cont.)

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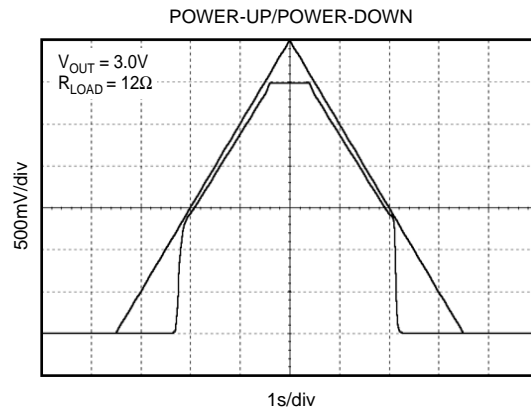
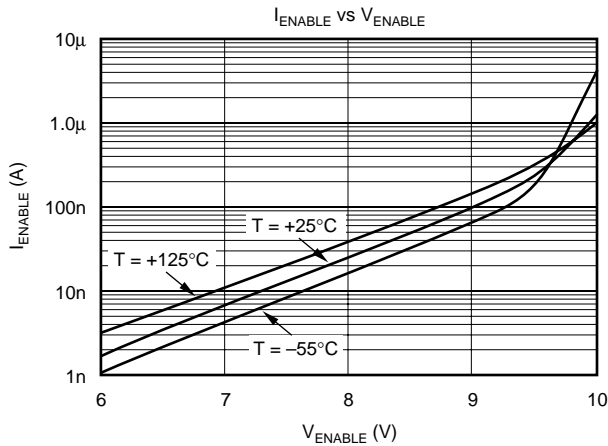
TYPICAL CHARACTERISTICS (Cont.)

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TYPICAL CHARACTERISTICS (Cont.)

For all models, at $T_J = +25^\circ\text{C}$ and $V_{\text{ENABLE}} = 1.8\text{V}$, unless otherwise noted.



BASIC OPERATION

The REG113 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG113 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG113 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10 μF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a 1k Ω to 2k Ω load resistor, using capacitance values smaller than 10 μF , or keeping the effective series resistance greater than 0.05 Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a 0.1 μF low ESR capacitor across the input supply voltage; this is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple. Figure 1 shows the basic circuit connections for the fixed voltage models.

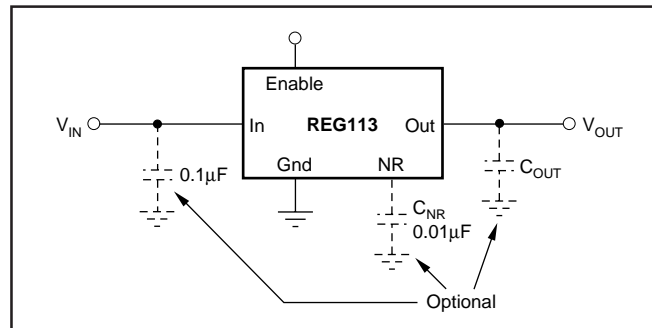


FIGURE 1. Fixed Voltage Nominal Circuit for the REG113.

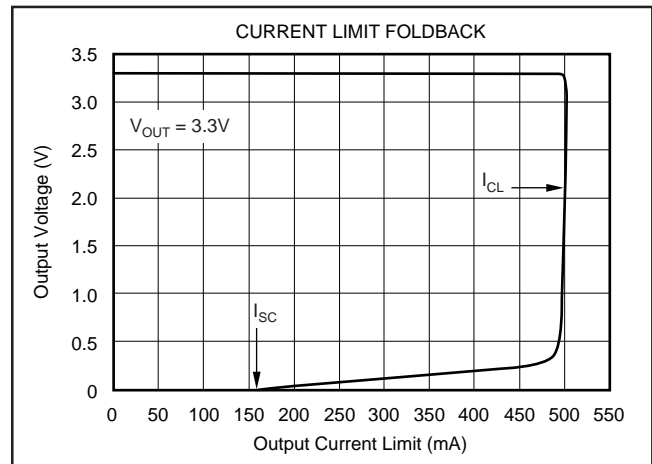


FIGURE 2. Foldback Current Limit of the REG113-3.3 at 25 $^\circ\text{C}$.

INTERNAL CURRENT LIMIT

The REG113 internal current limit has a typical value of 500mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 200mA. A curve of V_{OUT} versus I_{OUT} is given in Figure 2, and in the Typical Characteristics section.

ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to V_{IN} .

OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the REG113 and generates approximately $29\mu\text{V}_{\text{rms}}$ in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu\text{V}_{\text{rms}} \frac{R_1 + R_2}{R_2} = 29\mu\text{V}_{\text{rms}} \cdot \frac{V_{\text{OUT}}}{V_{\text{REF}}} \quad (1)$$

Since the value of V_{REF} is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu\text{V}_{\text{rms}}}{\text{V}} \cdot V_{\text{OUT}} \quad (2)$$

Connecting a capacitor, C_{NR} , from the Noise Reduction (NR) pin to ground (as shown in Figure 3) forms a low-pass filter for the voltage reference. For $C_{NR} = 10\text{nF}$, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for $V_{\text{OUT}} = 3.3\text{V}$. This noise reduction effect is shown in Figure 4, and as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT} . Best overall noise performance is achieved with very low ($< 0.22\mu\text{F}$) or very high ($> 2.2\mu\text{F}$) values of C_{OUT} (see the *RMS Noise Voltage vs C_{OUT}* typical characteristic).

The REG113 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN} . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of I_{OUT} and C_{OUT} .

DROPOUT VOLTAGE

The REG113 uses an N-channel DMOS as the pass element. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DROPOUT}), the DMOS pass device behaves like a resistor; therefore, for low values of $(V_{\text{IN}} - V_{\text{OUT}})$, the regulator input-to-output resistance is the $R_{\text{ds(ON)}}$ of the DMOS pass element (typically $600\text{m}\Omega$). For static (DC) loads, the REG113 will

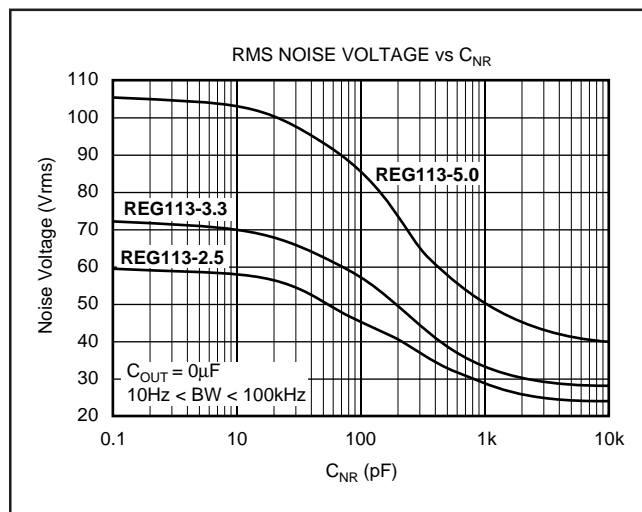


FIGURE 4. Output Noise versus Noise Reduction Capacitor.

typically maintain regulation down to a $(V_{\text{IN}} - V_{\text{OUT}})$ voltage drop of 250mV at full rated output current. In Figure 5, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

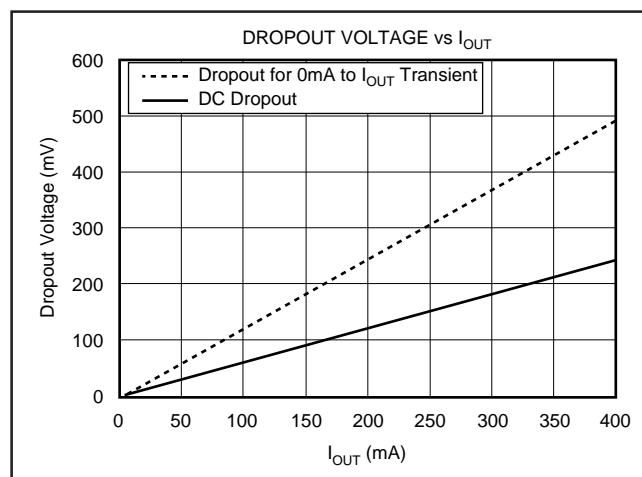


FIGURE 5. Transient and DC Dropout.

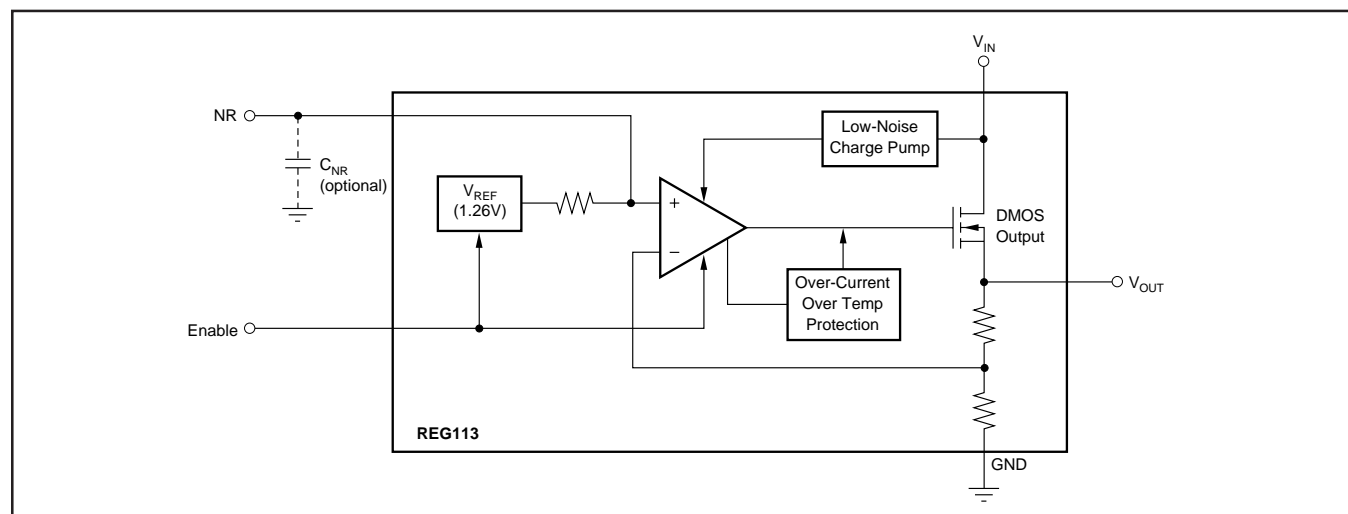


FIGURE 3. Block Diagram.

For large step changes in load current, the REG113 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient dropout region is shown as the top line in Figure 5. Values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with $(V_{IN} - V_{OUT})$ voltage drop close to DC dropout levels), the REG113 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG113 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value $0.47\mu\text{F}$) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin also improves the transient response.

THERMAL PROTECTION

Power dissipated within the REG113 can cause the junction temperature to rise, however, the REG113 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C , allowing the device to cool. When the junction temperature cools to approximately 140°C , the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C , maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG113 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG113 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG113 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. On the MSOP-8 package, leads 5 through 8 are fused to the lead frame and may be used to improve the thermal performance of the package. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult or impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 6. In all cases the PCB copper area is bare copper, free of solder resist mask, and not solder plated. All examples are for 1-ounce copper and in the case of the MSOP-8, the copper area is connected to fused leads 5 to 8. See Figure 7 for thermal resistance for varying areas of copper. Using heavier copper can increase the effectiveness in removing the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

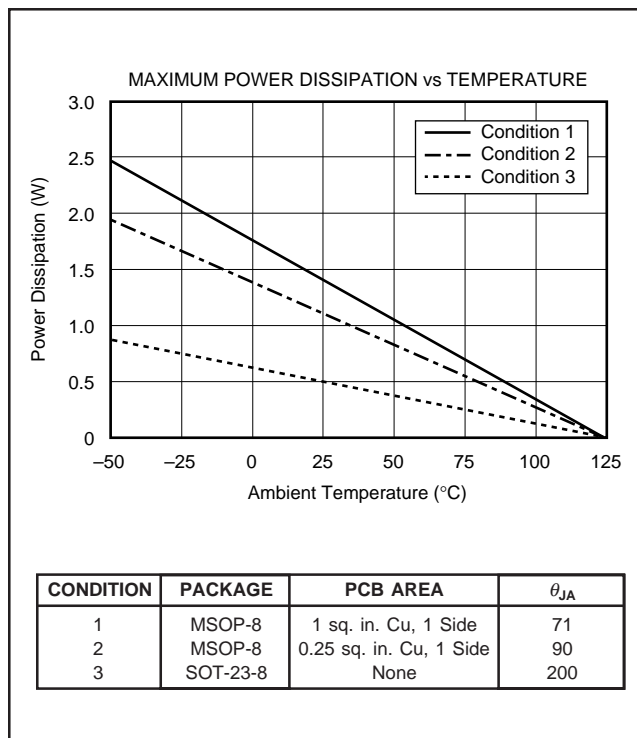


FIGURE 6. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element (V_{IN} to V_{OUT} voltage drop):

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

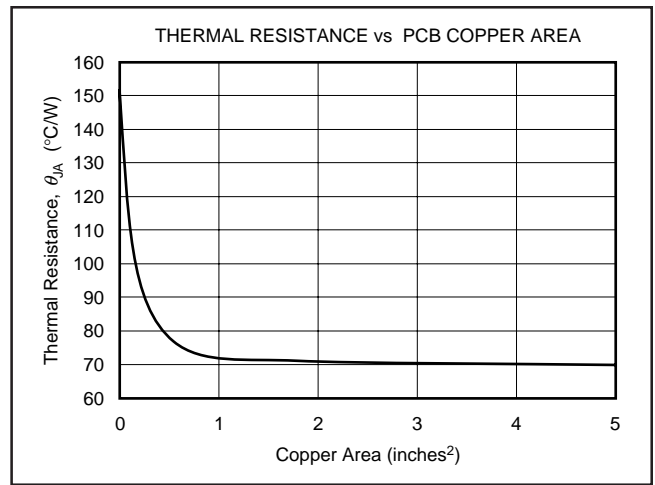



FIGURE 7. Thermal Resistance versus PCB Area for the MSOP-8.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
REG113EA-2.5/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-2.5/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-2.5/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-2.5/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13G	Samples
REG113EA-3.3/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113EA-3.3/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113EA-3/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13D	Samples
REG113EA-3/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13D	Samples
REG113EA-3/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13D	Samples
REG113EA-3/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13D	Samples
REG113EA-5/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA-5/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA-5/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA-5/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13B	Samples
REG113EA33250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113EA332K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	R13C	Samples
REG113NA-2.5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
REG113NA-2.5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples
REG113NA-2.5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples
REG113NA-2.5/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13G	Samples
REG113NA-2.85/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	Samples
REG113NA-2.85/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	Samples
REG113NA-2.85/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	Samples
REG113NA-3.3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3.3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3.3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3.3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13C	Samples
REG113NA-3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13D	Samples
REG113NA-5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples
REG113NA-5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples
REG113NA-5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples
REG113NA-5/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
REG113NA2.85/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R13N	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

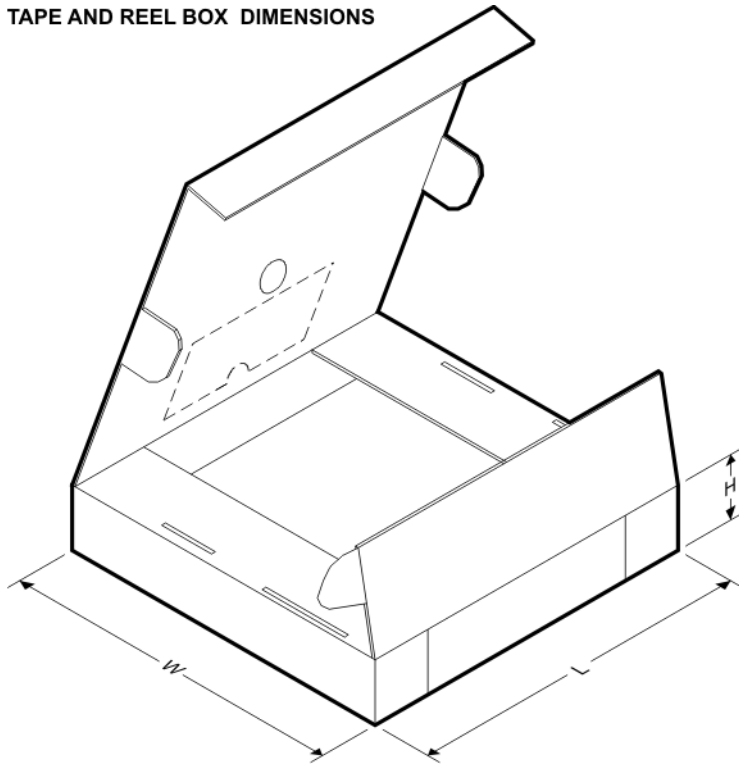


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG113EA-2.5/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-2.5/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3.3/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3.3/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-3/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-5/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113EA-5/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
REG113NA-2.5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.85/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-2.85/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3.3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3.3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG113NA-5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


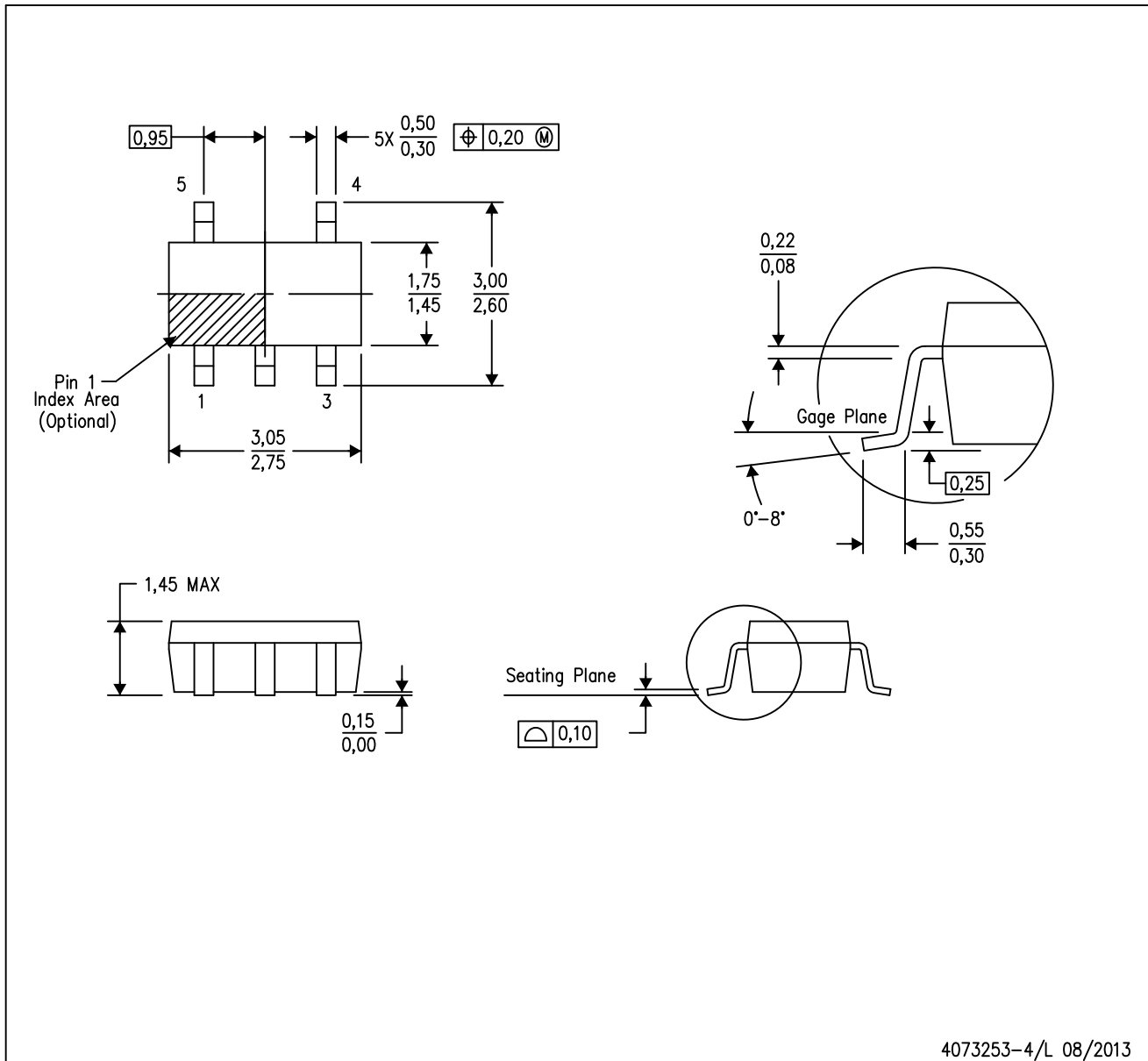
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG113EA-2.5/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-2.5/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
REG113EA-3.3/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-3.3/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
REG113EA-3/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-3/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
REG113EA-5/250	VSSOP	DGK	8	250	210.0	185.0	35.0
REG113EA-5/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
REG113NA-2.5/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG113NA-2.5/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG113NA-2.85/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG113NA-2.85/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG113NA-3.3/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG113NA-3.3/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG113NA-3/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG113NA-3/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG113NA-5/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG113NA-5/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0

MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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