

# LMC7101/LMC7101Q Tiny Low Power Operational Amplifier with Rail-to-Rail Input and Output

 Check for Samples: [LMC7101](#), [LMC7101Q](#)

## FEATURES

- Tiny 5-Pin SOT-23 Package Saves Space—Typical Circuit Layouts Take Half the Space of 8-Pin SOIC Designs
- Guaranteed Specs at 2.7V, 3V, 5V, 15V Supplies
- Typical Supply Current 0.5 mA at 5V
- Typical Total Harmonic Distortion of 0.01% at 5V
- 1.0 MHz Gain-Bandwidth
- Similar to Popular LMC6482/LMC6484

- Rail-to-Rail Input and Output
- Temperature Range  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (LMC7101Q)

## APPLICATIONS

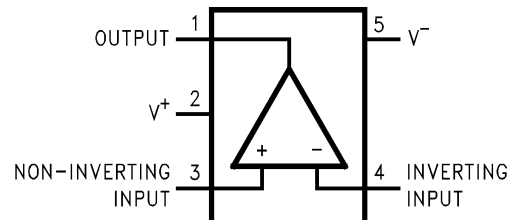
- Mobile Communications
- Notebooks and PDAs
- Battery Powered Products
- Sensor Interface
- Automotive Applications (LMC7101Q)

## DESCRIPTION

The LMC7101 is a high performance CMOS operational amplifier available in the space saving 5-Pin SOT-23 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/LMC6484 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

## Connection Diagram



**Figure 1. 5-Pin SOT-23  
Top View**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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**Absolute Maximum Ratings<sup>(1)(2)</sup>**

ESD Tolerance <sup>(3)</sup>	
Human Body Model	1000V
Machine Model	200V
Charged Device Model	1000V
Difference Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V <sup>+</sup> ) + 0.3V, (V <sup>-</sup> ) - 0.3V
Supply Voltage (V <sup>+</sup> - V <sup>-</sup> )	16V
Current at Input Pin	±5 mA
Current at Output Pin <sup>(4)</sup>	±35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature <sup>(5)</sup>	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model is 1.5 kΩ in series with 100 pF.
- (4) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
- (5) The maximum power dissipation is a function of T<sub>J(MAX)</sub>, θ<sub>JA</sub> and T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/θ<sub>JA</sub>. All numbers apply for packages soldered directly into a PC board.

**Recommended Operating Conditions<sup>(1)</sup>**

Supply Voltage	2.7V ≤ V <sup>+</sup> ≤ 15.5V
Temperature Range	
LMC7101AI, LMC7101BI	-40°C to 85°C
LMC7101Q	-40°C to 125°C
Thermal Resistance (θ <sub>JA</sub> )	
5-Pin SOT-23	325°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**2.7V Electrical Characteristics**

Unless otherwise specified, all limits guaranteed for T<sub>J</sub> = 25°C, V<sup>+</sup> = 2.7V, V<sup>-</sup> = 0V, V<sub>CM</sub> = V<sub>O</sub> = V<sup>+</sup>/2 and R<sub>L</sub> > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	LMC7101AI Limit <sup>(2)</sup>	LMC7101BI Limit <sup>(2)</sup>	LMC7101Q Limit <sup>(2)(3)</sup>	Units
V <sub>OS</sub>	Input Offset Voltage Average Drift	V <sup>+</sup> = 2.7V	0.11	6	9	9	mV max
TCV <sub>OS</sub>	Input Offset Voltage		1				µV/°C
I <sub>B</sub>	Input Bias Current		1.0	<b>64</b>	<b>64</b>	<b>1000</b>	pA max
I <sub>OS</sub>	Input Offset Current		0.5	<b>32</b>	<b>32</b>	<b>2000</b>	pA max
R <sub>IN</sub>	Input Resistance		>1				Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V <sub>CM</sub> ≤ 2.7V V <sup>+</sup> = 2.7V	70	55	50	50	dB min
V <sub>CM</sub>	Input Common Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	0.0	V min
			3.0	2.7	2.7	2.7	V max

- (1) Typical Values represent the most likely parametric norm.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) When operated at temperature between -40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.

## 2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
PSRR	Power Supply Rejection Ratio	$V^+ = 1.35\text{V to } 1.65\text{V}$ $V^- = -1.35\text{V to } -1.65\text{V}$ $V_{\text{CM}} = 0$	60	50	45	45	dB min
$C_{\text{IN}}$	Common-Mode Input Capacitance		3				pF
$V_O$	Output Swing	$R_L = 2\text{ k}\Omega$	2.45	2.15	2.15	2.15	V min
			0.25	0.5	0.5	0.5	V max
		$R_L = 10\text{ k}\Omega$	2.68	2.64	2.64	2.64	V min
			0.025	0.06	0.06	0.06	V max
$I_S$	Supply Current		0.5	0.81 <b>0.95</b>	0.81 <b>0.95</b>	0.81 <b>0.95</b>	mA max
SR	Slew Rate <sup>(4)</sup>		0.7				V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product		0.6				MHz

(4)  $V^+ = 15\text{V}$ . Connected as a voltage follower with a 10V step input. Number specified is the slower of the positive and negative slew rates.  
 $R_L = 100\text{ k}\Omega$  connected to 7.5V. Amp excited with 1 kHz to produce  $V_O = 10\text{ V}_{\text{PP}}$ .

## 3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 3\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = V^+/2$  and  $R_L = 1\text{M}\Omega$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
$V_{\text{OS}}$	Input Offset Voltage		0.11	4 <b>6</b>	7 <b>9</b>	7	mV max
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1				$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Current		1.0	<b>64</b>	<b>64</b>	<b>1000</b>	pA max
$I_{\text{OS}}$	Input Offset Current		0.5	<b>32</b>	<b>32</b>	<b>2000</b>	pA max
$R_{\text{IN}}$	Input Resistance		>1				Tera $\Omega$
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 3\text{V}$ $V^+ = 3\text{V}$	74	64	60	60	db min
$V_{\text{CM}}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	0.0	0.0	0.0	0.0	V min
			3.3	3.0	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.5\text{V to } 7.5\text{V}$ $V^- = -1.5\text{V to } -7.5\text{V}$ $V_O = V_{\text{CM}} = 0$	80	68	60	60	dBmin
$C_{\text{IN}}$	Common-Mode Input Capacitance		3				pF
$V_O$	Output Swing	$R_L = 2\text{ k}\Omega$	2.8	2.6	2.6	2.6	V min
			0.2	0.4	0.4	0.4	V max
		$R_L = 600\Omega$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
$I_S$	Supply Current		0.5	0.81 <b>0.95</b>	0.81 <b>0.95</b>	0.81 <b>0.95</b>	mA max

(1) Typical Values represent the most likely parametric norm.

(2) All limits are guaranteed by testing or statistical analysis.

(3) When operated at temperature between  $-40^\circ\text{C}$  and  $85^\circ\text{C}$ , the LMC7101Q will meet LMC7101BI specifications.

### 5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.5\text{V}$ ,  $V_O = V^+/2$  and  $R_L = 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units	
$V_{OS}$	Input Offset Voltage	$V^+ = 5\text{V}$	0.11	3 <b>5</b>	7 <b>9</b>	7 <b>9</b>	mV max	
$TCV_{OS}$	Input Offset Voltage Average Drift		1.0				$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Current		1	<b>64</b>	<b>64</b>	<b>1000</b>	pA max	
$I_{OS}$	Input Offset Current		0.5	<b>32</b>	<b>32</b>	<b>2000</b>	pA max	
$R_{IN}$	Input Resistance		>1				Tera $\Omega$	
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 5\text{V}$ LMC7101Q @ $125^\circ\text{C}$ $0.2\text{V} \leq V_{CM} \leq 4.8\text{V}$	82	65 <b>60</b>	60 <b>55</b>	60 <b>55</b>	db min	
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to $15\text{V}$ $V^- = 0\text{V}$ , $V_O = 1.5\text{V}$	82	70 <b>65</b>	65 <b>62</b>	65 <b>62</b>	db min	
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -5\text{V}$ to $-15\text{V}$ $V^+ = 0\text{V}$ , $V_O = -1.5\text{V}$	82	70 <b>65</b>	65 <b>62</b>	65 <b>62</b>	db min	
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{ dB}$	-0.3	-0.20 <b>0.00</b>	-0.20 <b>0.00</b>	-0.2 <b>0.2</b>	V min	
			5.3	5.20 <b>5.00</b>	5.20 <b>5.00</b>	5.2 <b>4.8</b>	V max	
$C_{IN}$	Common-Mode Input Capacitance		3				pF	
$V_O$	Output Swing	$R_L = 2\text{ k}\Omega$	4.9	4.7 <b>4.6</b>	4.7 <b>4.6</b>	4.7 <b>4.54</b>	V min	
			0.1	0.18 <b>0.24</b>	0.18 <b>0.24</b>	0.18 <b>0.28</b>	V max	
		$R_L = 600\Omega$	4.7	4.5 <b>4.24</b>	4.5 <b>4.24</b>	4.5 <b>4.28</b>	V min	
			0.3	0.5 <b>0.65</b>	0.5 <b>0.65</b>	0.5 <b>0.8</b>	V max	
$I_{SC}$	Output Short Circuit Current	$V_O = 0\text{V}$ 24	Sourcing	24	16 <b>11</b>	16 <b>11</b>	16 <b>9</b>	mA min
		$V_O = 5\text{V}$	Sinking	19	11 <b>7.5</b>	11 <b>7.5</b>	11 <b>5.8</b>	mA min
$I_S$	Supply Current		0.5	0.85 <b>1.0</b>	0.85 <b>1.0</b>	0.85 <b>1.0</b>	mA max	

- (1) Typical Values represent the most likely parametric norm.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) When operated at temperature between  $-40^\circ\text{C}$  and  $85^\circ\text{C}$ , the LMC7101Q will meet LMC7101BI specifications.

### 5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.5\text{V}$ ,  $V_O = V^+/2$  and  $R_L = 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	Units
THD	Total Harmonic Distortion	$f = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 4.0\text{ V}_{PP}$	0.01			%
SR	Slew Rate		1.0			V/ $\mu\text{s}$
GBW	Gain Bandwidth Product		1.0			MHz

- (1) Typical Values represent the most likely parametric norm.
- (2) All limits are guaranteed by testing or statistical analysis.

## 15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 15\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$ ,  $V_O = V^+/2$  and  $R_L = 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units	
$V_{\text{OS}}$	Input Offset Voltage		0.11				mV max	
$\text{TCV}_{\text{OS}}$	Input Offset Voltage Average Drift		1.0				$\mu\text{V}/^\circ\text{C}$	
$I_B$	Input Current		1.0	<b>64</b>	<b>64</b>	<b>1000</b>	pA max	
$I_{\text{OS}}$	Input Offset Current		0.5	<b>32</b>	<b>32</b>	<b>2000</b>	pA max	
$R_{\text{IN}}$	Input Resistance		>1				Tera $\Omega$	
CMRR	Common-Mode Rejection Ratio	$0\text{V} \leq V_{\text{CM}} \leq 15\text{V}$ LMC7101Q @ $^\circ 125\text{C}$ $0.2\text{V} \leq V_{\text{CM}} \leq 14.8\text{V}$	82	70 <b>65</b>	65 <b>60</b>	65 <b>60</b>	dB min	
+PSRR	Positive Power Supply Rejection Ratio	$V^+ = 5\text{V}$ to $15\text{V}$ $V^- = 0\text{V}$ , $V_O = 1.5\text{V}$	82	70 <b>65</b>	65 <b>62</b>	65 <b>62</b>	dB min	
-PSRR	Negative Power Supply Rejection Ratio	$V^- = -5\text{V}$ to $-15\text{V}$ $V^+ = 0\text{V}$ , $V_O = -1.5\text{V}$	82	70 <b>65</b>	65 <b>62</b>	65 <b>62</b>	dB min	
$V_{\text{CM}}$	Input Common-Mode Voltage Range	$V^+ = 5\text{V}$ For CMRR $\geq 50\text{ dB}$	-0.3	-0.20 <b>0.00</b>	-0.20 <b>0.00</b>	-0.2 <b>0.2</b>	V min	
			15.3	15.20 <b>15.00</b>	15.20 <b>15.00</b>	15.2 <b>14.8</b>	V max	
$A_V$	Large Signal Voltage Gain (4)	$R_L = 2\text{ k}\Omega$	Sourcing	340	80 <b>40</b>	80 <b>40</b>	80 <b>30</b>	V/mV
			Sinking	24	15 <b>10</b>	15 <b>10</b>	15 <b>4</b>	
		$R_L = 600\Omega$	Sourcing	300	34	34	34	V/mV
			Sinking	15	6	6	6	
$C_{\text{IN}}$	Input Capacitance		3				pF	
$V_O$	Output Swing	$V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$		14.7	14.4 <b>14.2</b>	14.4 <b>14.2</b>	14.4 <b>14.2</b>	V min
				0.16	0.32 <b>0.45</b>	0.32 <b>0.45</b>	0.32 <b>0.45</b>	V max
		$V^+ = 15\text{V}$ $R_L = 600\Omega$		14.1	13.4 <b>13.0</b>	13.4 <b>13.0</b>	13.4 <b>12.85</b>	V min
				0.5	1.0 <b>1.3</b>	1.0 <b>1.3</b>	1.0 <b>1.5</b>	V max
$I_{\text{SC}}$	Output Short Circuit Current (5)	$V_O = 0\text{V}$	Sourcing	50	30 <b>20</b>	30 <b>20</b>	30 <b>20</b>	mA min
		$V_O = 12\text{V}$	Sinking	50	30 <b>20</b>	30 <b>20</b>	30 <b>20</b>	
$I_S$	Supply Current		0.8	1.50 <b>1.71</b>	1.50 <b>1.71</b>	1.50 <b>1.75</b>	mA max	

(1) Typical Values represent the most likely parametric norm.

(2) All limits are guaranteed by testing or statistical analysis.

(3) When operated at temperature between  $-40^\circ\text{C}$  and  $85^\circ\text{C}$ , the LMC7101Q will meet LMC7101BI specifications.

(4)  $V^+ = 15\text{V}$ ,  $V_{\text{CM}} = 1.5\text{V}$  and  $R_L$  connect to  $7.5\text{V}$ . For sourcing tests,  $7.5\text{V} \leq V_O \leq 12.5\text{V}$ . For sinking tests,  $2.5\text{V} \leq V_O \leq 7.5\text{V}$ .

(5) Do not short circuit output to  $V^+$  when  $V^+$  is greater than  $12\text{V}$  or reliability will be adversely affected.

### 15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 15\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 1.5\text{V}$ ,  $V_O = V^+/2$  and  $R_L = 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
SR	Slew Rate (4)	$V^+ = 15\text{V}$	1.1	0.5 <b>0.4</b>	0.5 <b>0.4</b>	0.5 <b>0.4</b>	V/ $\mu\text{s}$ min
GBW	Gain-Bandwidth Product	$V^+ = 15\text{V}$	1.1				MHz
$\phi_m$	Phase Margin		45				deg
$G_m$	Gain Margin		10				dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$ , $V_{CM} = 1\text{V}$	37				$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	1.5				$\frac{\text{fA}}{\sqrt{\text{Hz}}}$
THD	Total Harmonic Distortion	$f = 10\text{ kHz}$ , $A_V = -2$ $R_L = 10\text{ k}\Omega$ , $V_O = 8.5\text{ V}_{PP}$	0.01				%

- (1) Typical Values represent the most likely parametric norm.
- (2) All limits are guaranteed by testing or statistical analysis.
- (3) When operated at temperature between  $-40^\circ\text{C}$  and  $85^\circ\text{C}$ , the LMC7101Q will meet LMC7101BI specifications.
- (4)  $V^+ = 15\text{V}$ . Connected as a voltage follower with a 10V step input. Number specified is the slower of the positive and negative slew rates.  $R_L = 100\text{ k}\Omega$  connected to 7.5V. Amp excited with 1 kHz to produce  $V_O = 10\text{ V}_{PP}$ .

### 2.7V Typical Performance Characteristics

$V^+ = 2.7V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

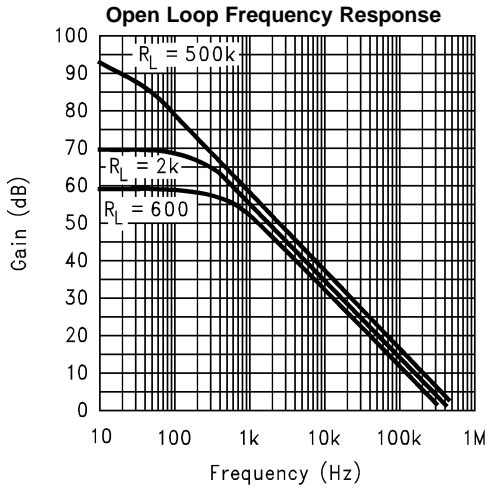


Figure 2.

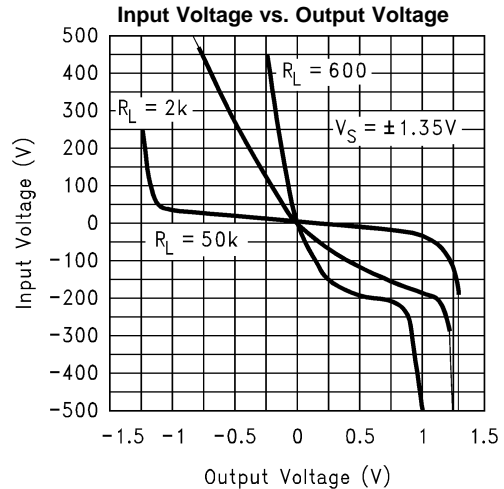


Figure 3.

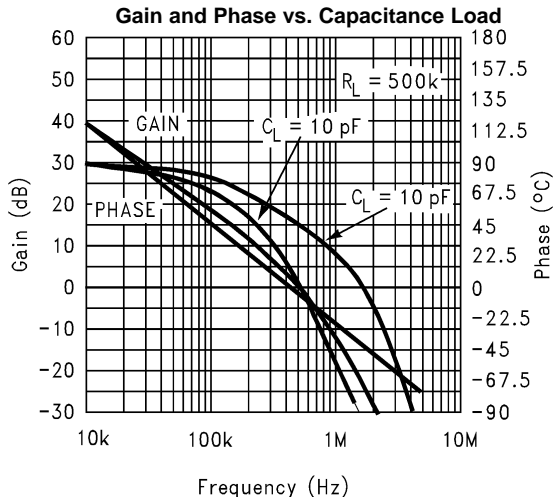


Figure 4.

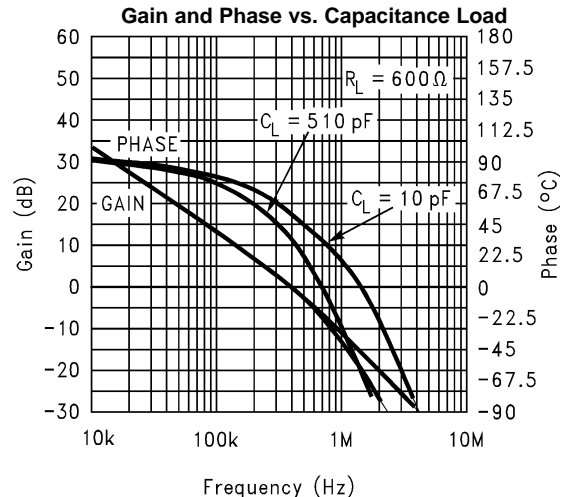


Figure 5.

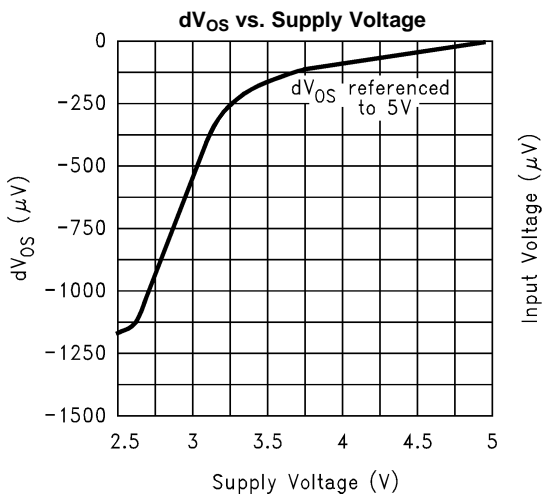


Figure 6.

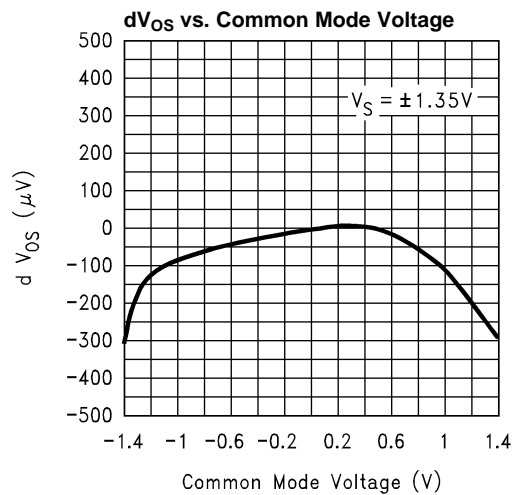
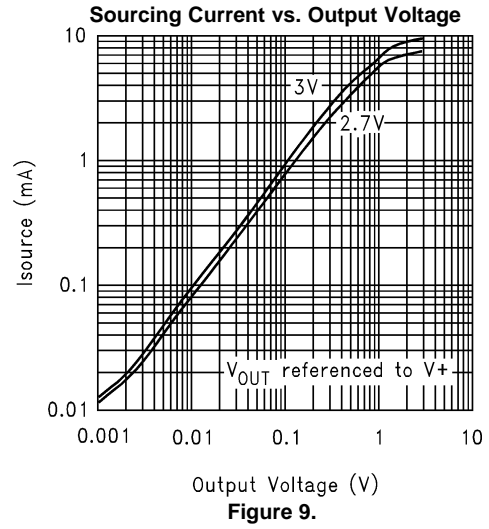
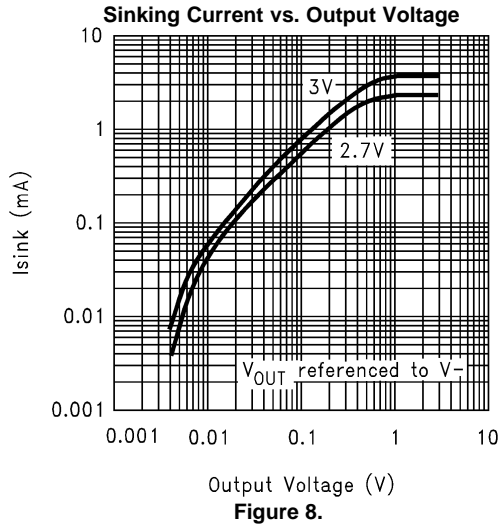


Figure 7.

**2.7V Typical Performance Characteristics (continued)**

$V^+ = 2.7V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.





### 3V Typical Performance Characteristics

$V^+ = 3V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

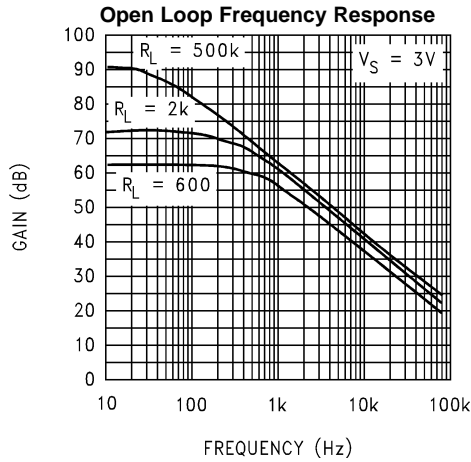


Figure 10.

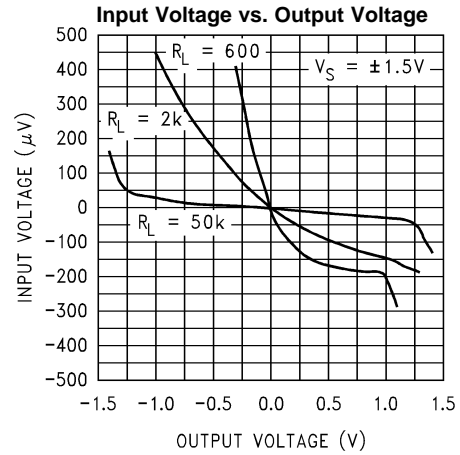


Figure 11.

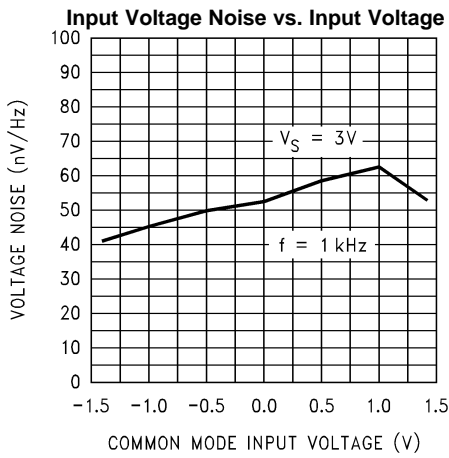


Figure 12.

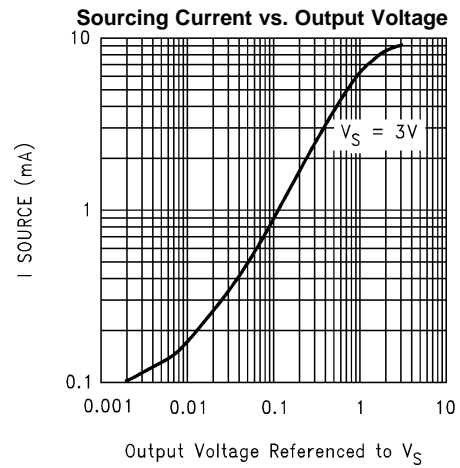


Figure 13.

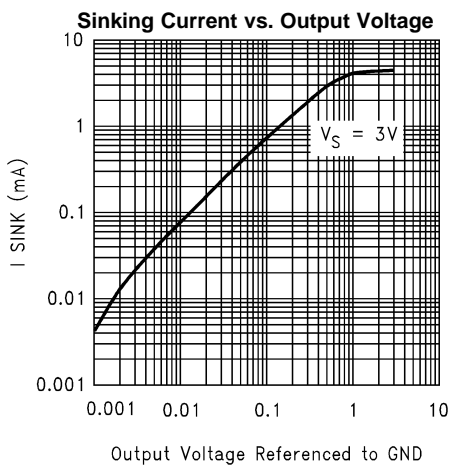


Figure 14.

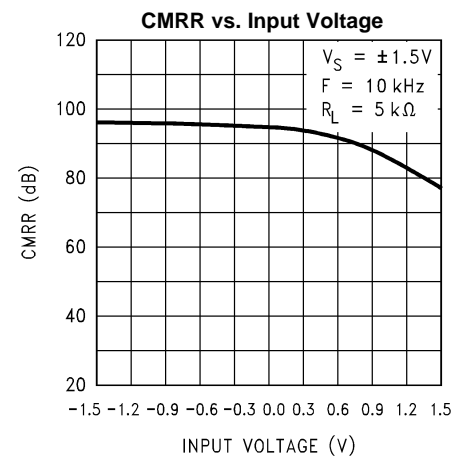


Figure 15.

### 5V Typical Performance Characteristics

$V^+ = 5V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

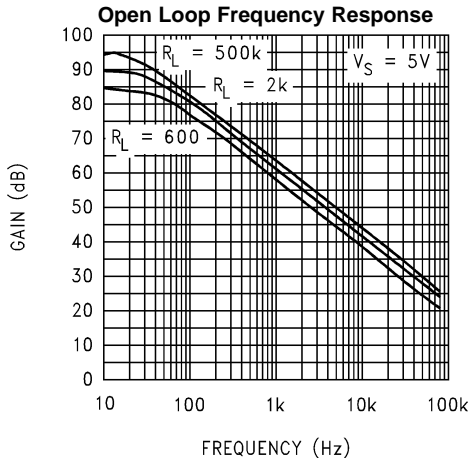


Figure 16.

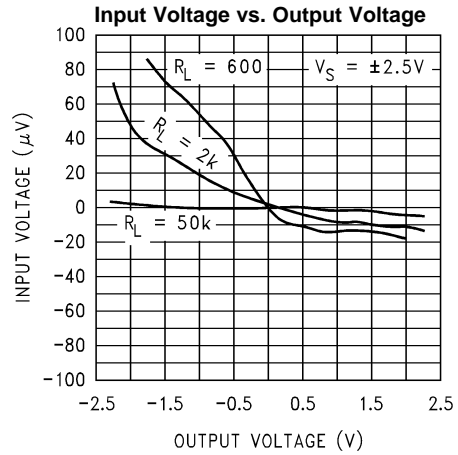


Figure 17.

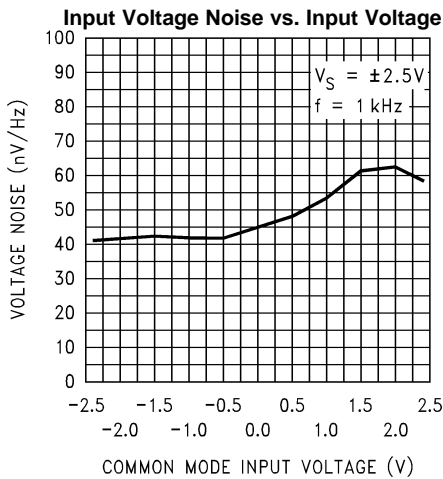


Figure 18.

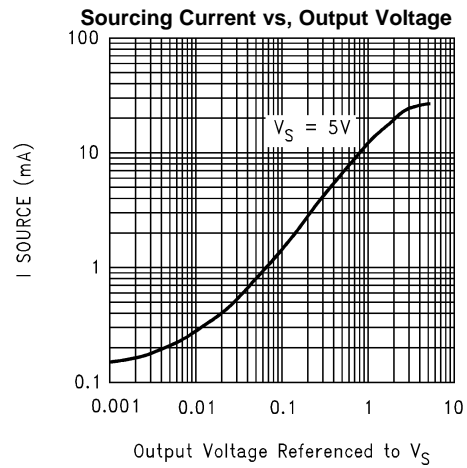


Figure 19.

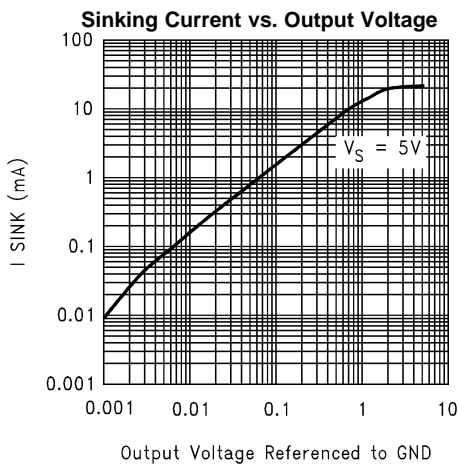


Figure 20.

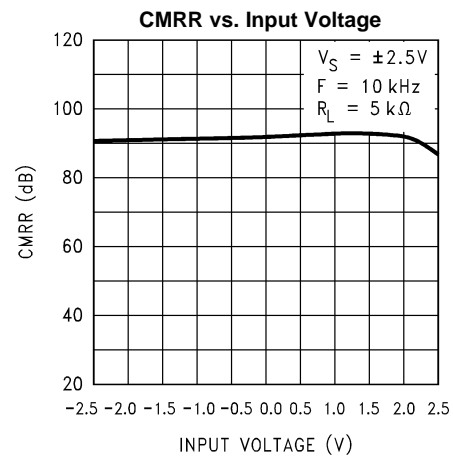


Figure 21.

### 15V Typical Performance Characteristics

$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

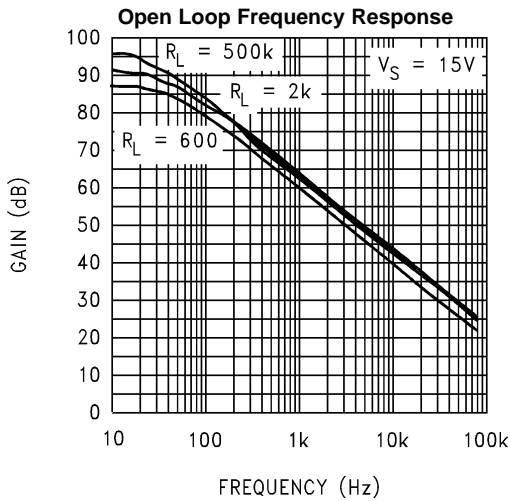


Figure 22.

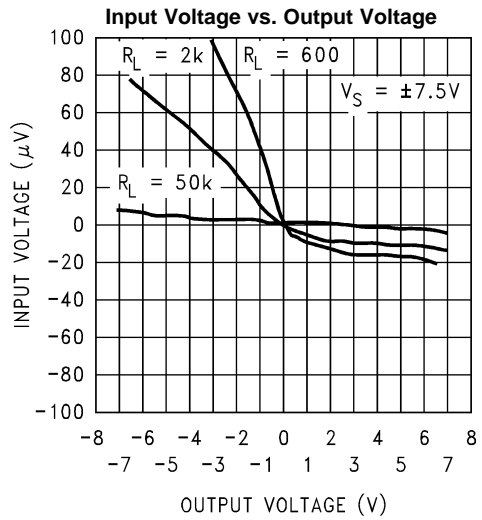


Figure 23.

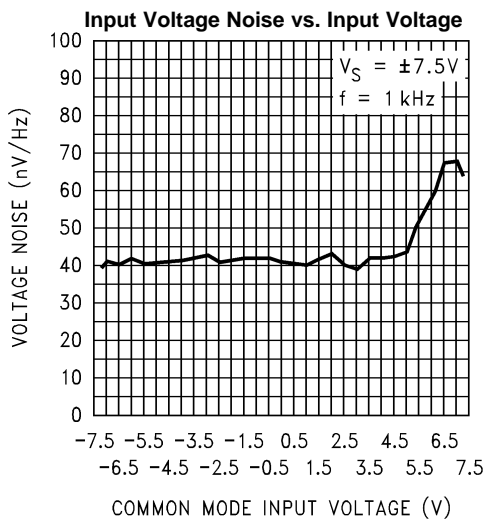


Figure 24.

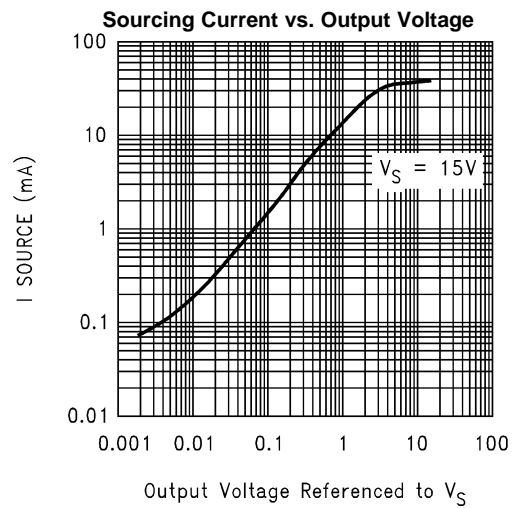
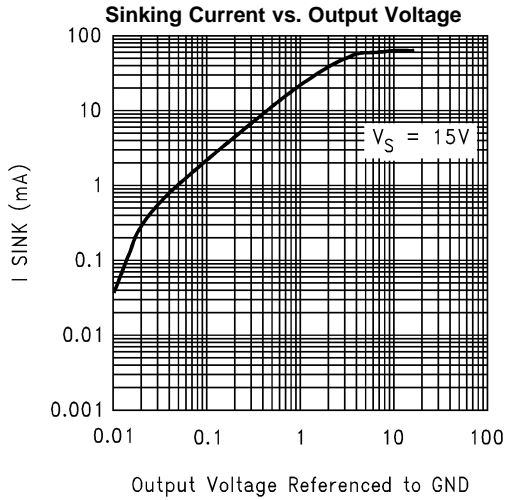


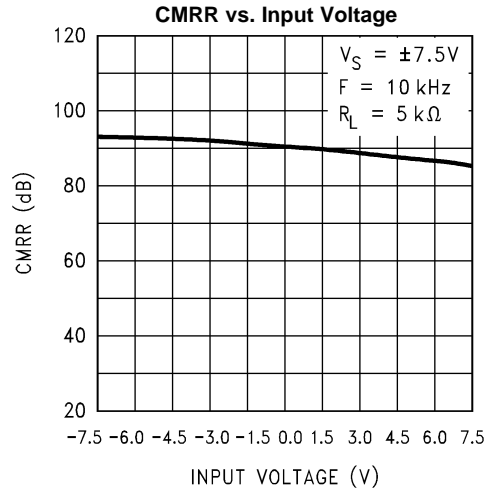
Figure 25.

**15V Typical Performance Characteristics (continued)**

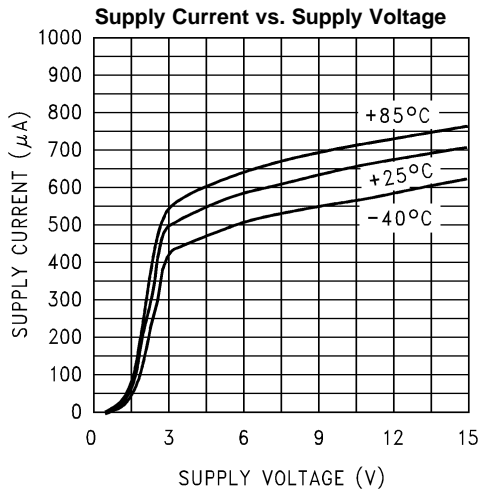
$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.



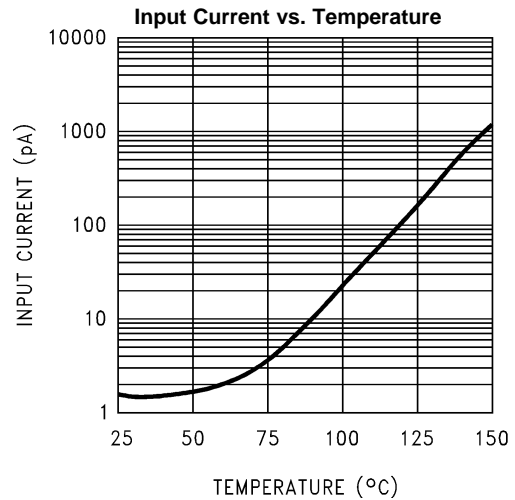
**Figure 26.**



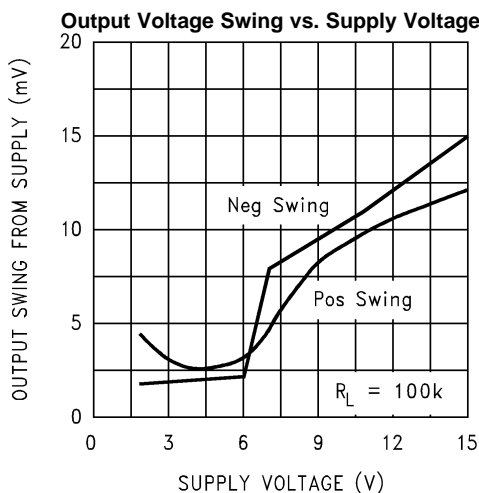
**Figure 27.**



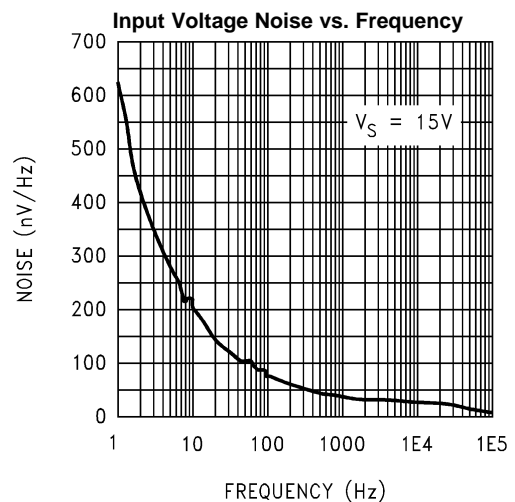
**Figure 28.**



**Figure 29.**



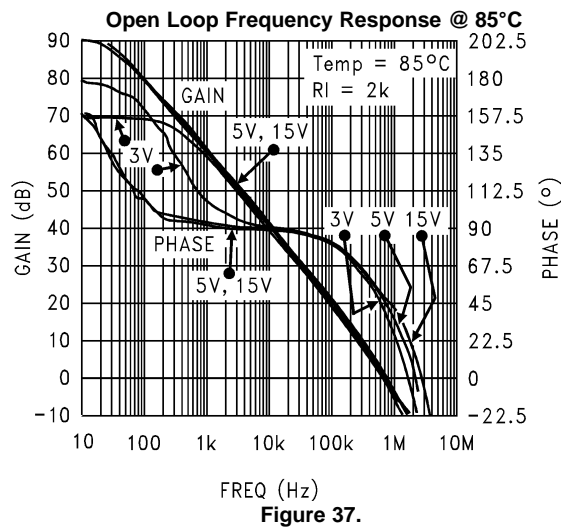
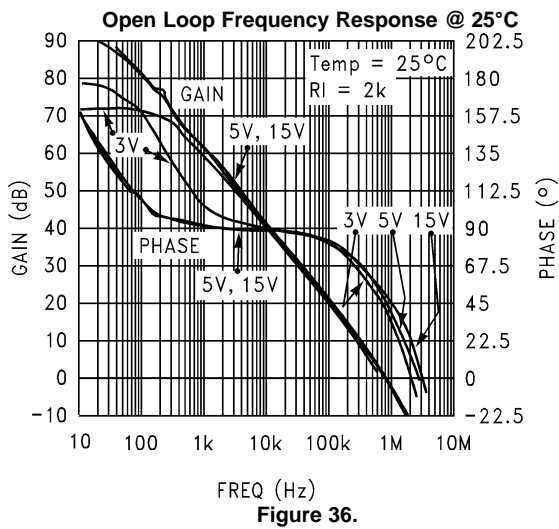
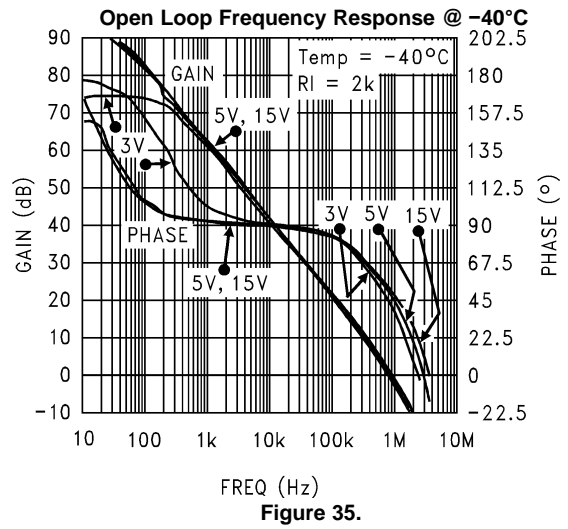
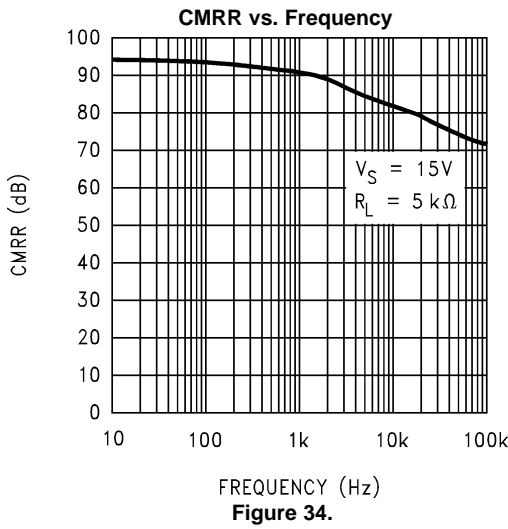
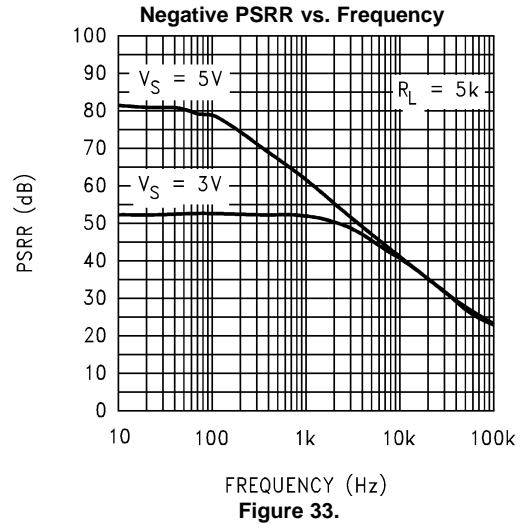
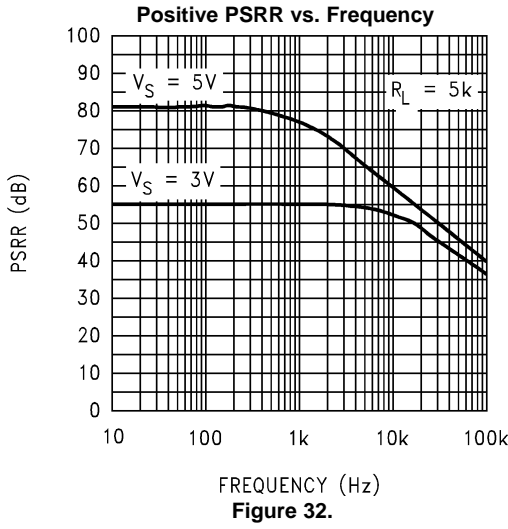
**Figure 30.**



**Figure 31.**

15V Typical Performance Characteristics (continued)

$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.



15V Typical Performance Characteristics (continued)

$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

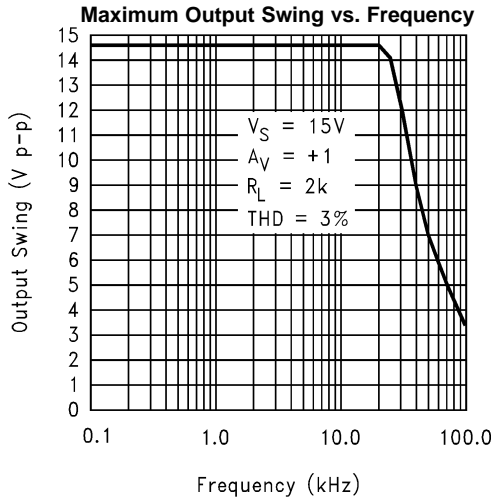


Figure 38.

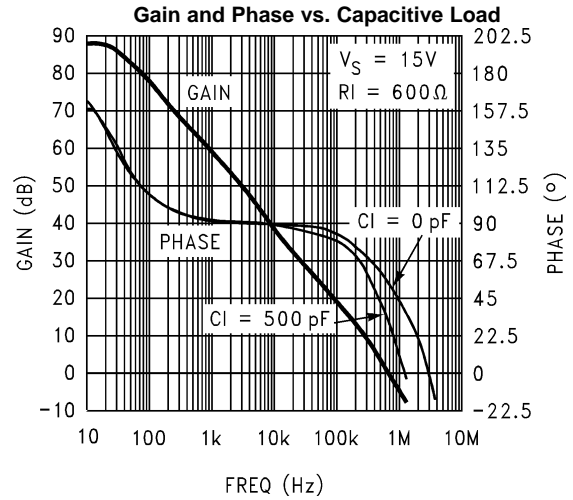


Figure 39.

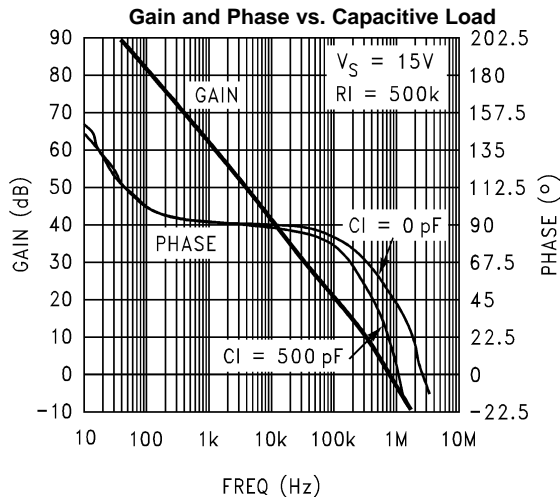


Figure 40.

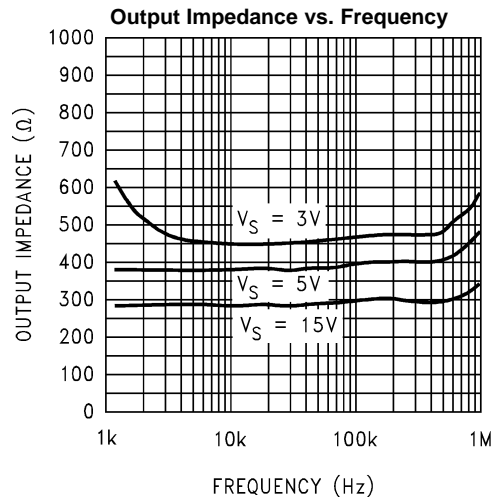


Figure 41.

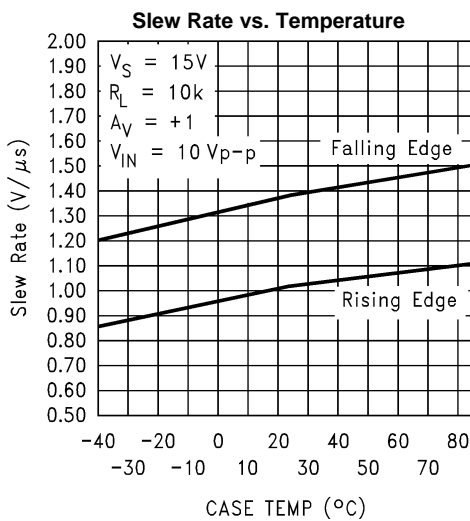


Figure 42.

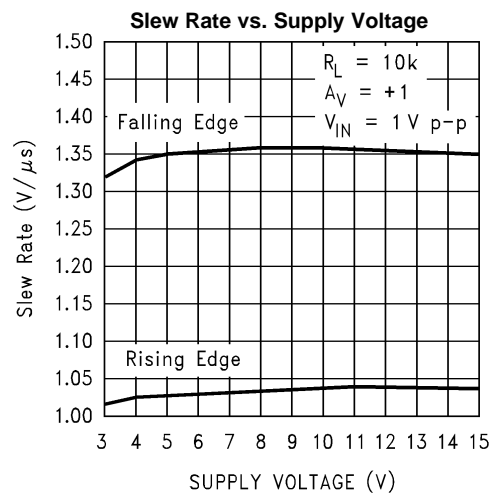
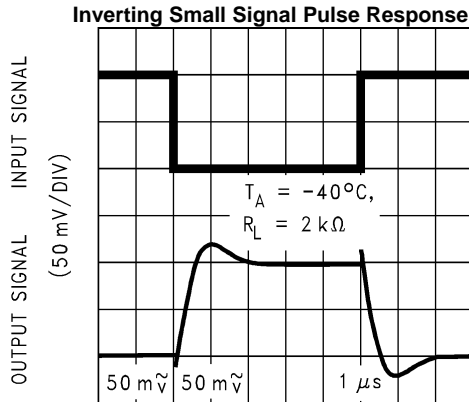


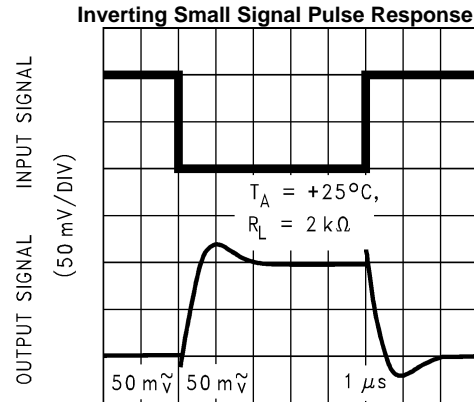
Figure 43.

15V Typical Performance Characteristics (continued)

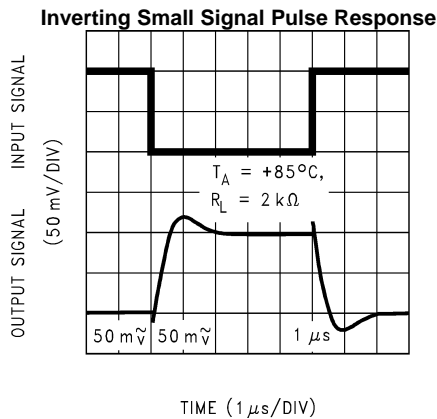
$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.



TIME (1 μs/DIV)  
Figure 44.

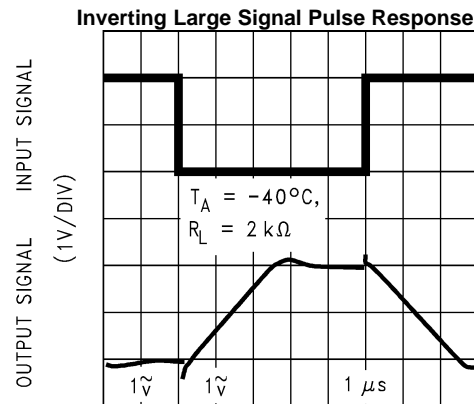


TIME (1 μs/DIV)  
Figure 45.

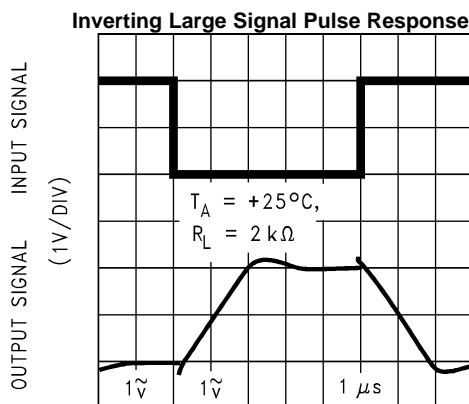


TIME (1 μs/DIV)

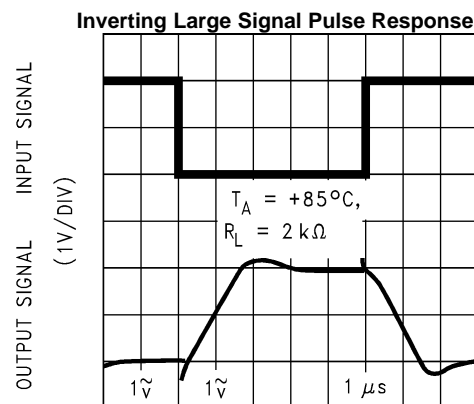
Figure 46.



TIME (1 μs/DIV)  
Figure 47.



TIME (1 μs/DIV)  
Figure 48.



TIME (1 μs/DIV)  
Figure 49.

**15V Typical Performance Characteristics (continued)**

$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

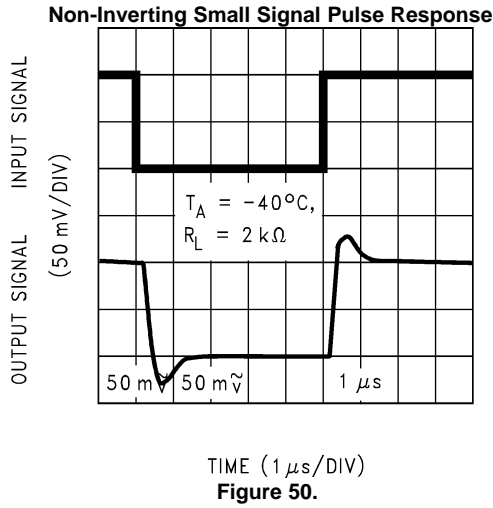


Figure 50.

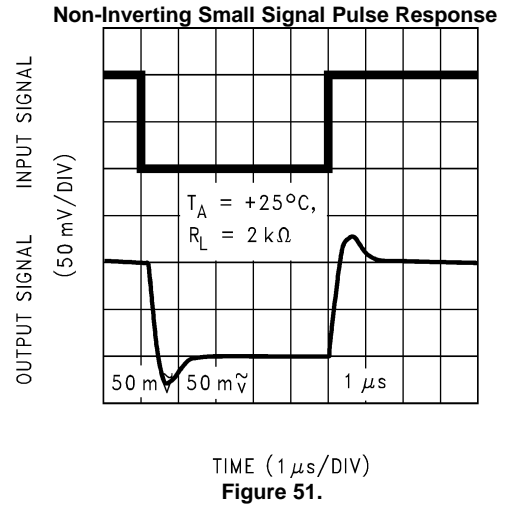


Figure 51.

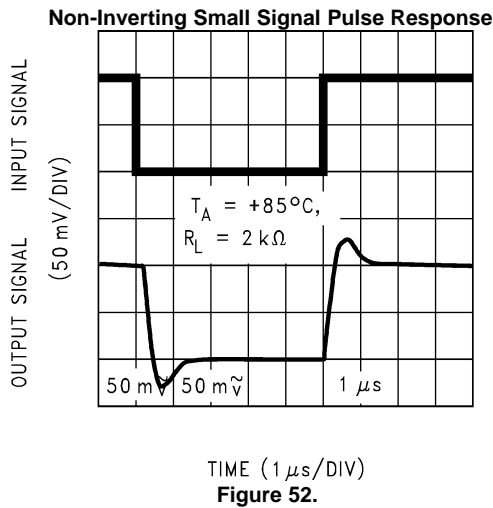


Figure 52.

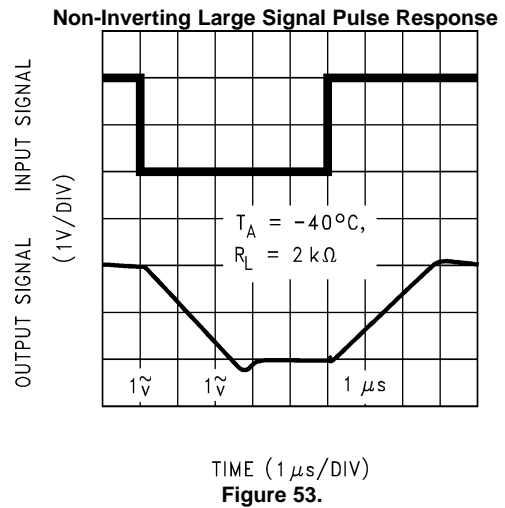


Figure 53.

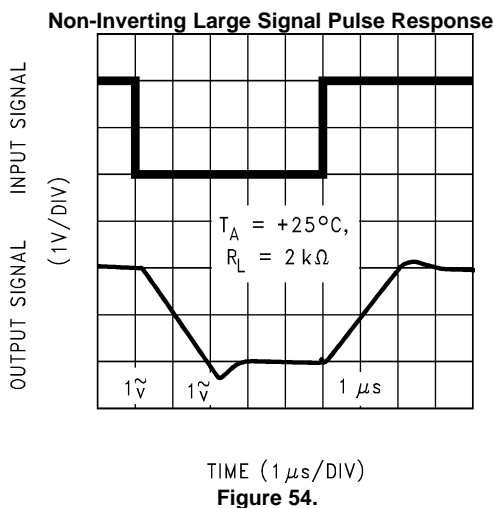


Figure 54.

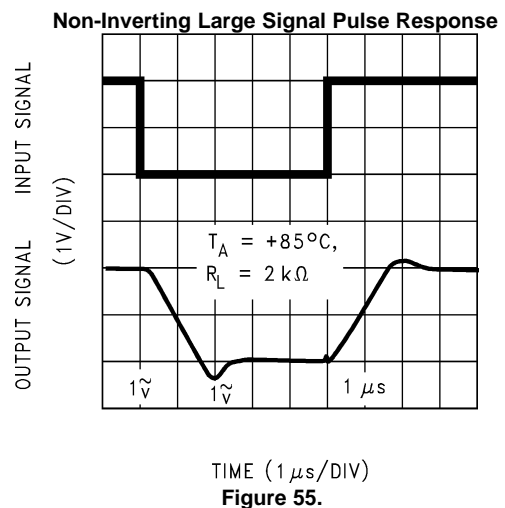


Figure 55.



15V Typical Performance Characteristics (continued)

$V^+ = +15V$ ,  $V^- = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.

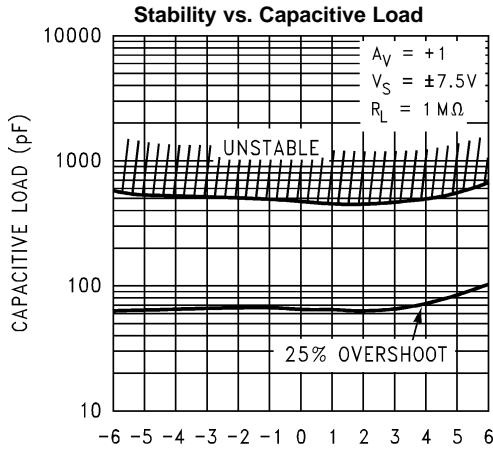


Figure 56.

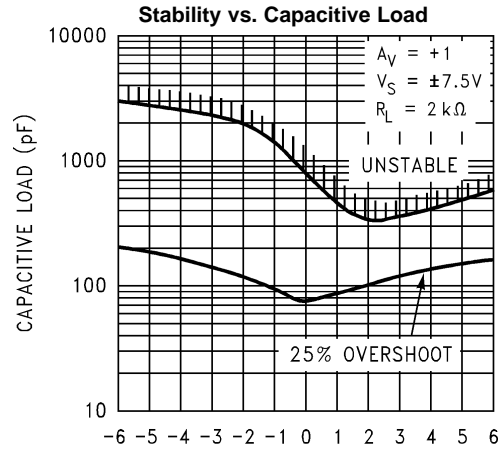


Figure 57.

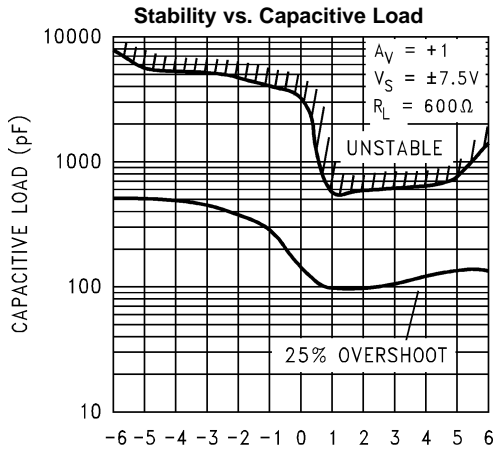


Figure 58.

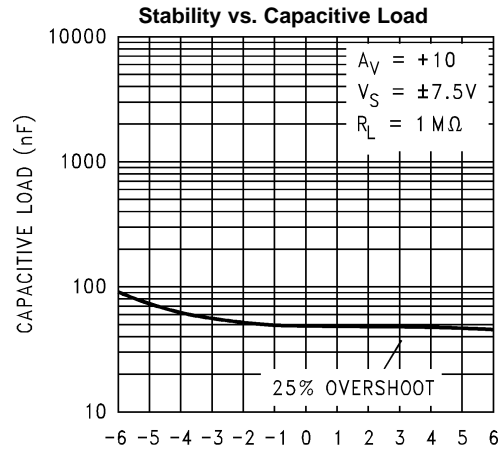


Figure 59.

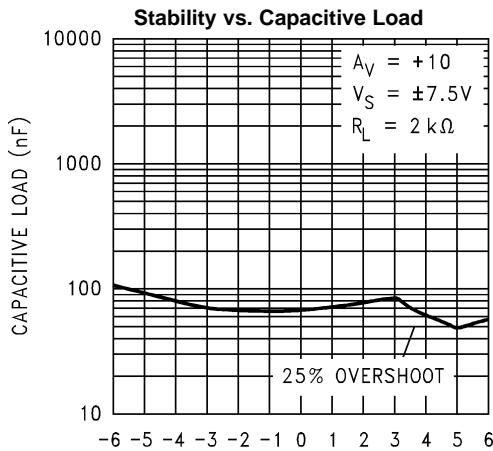


Figure 60.

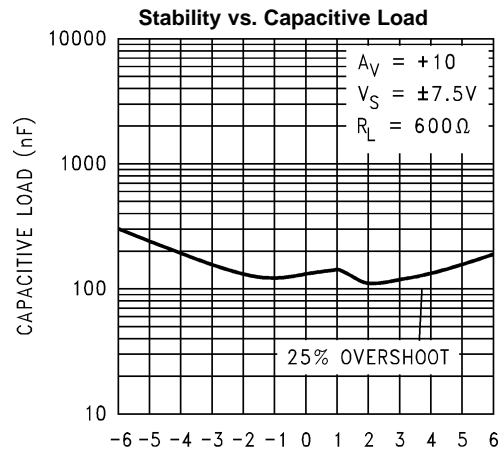


Figure 61.

## APPLICATION INFORMATION

### BENEFITS OF THE LMC7101 TINY AMP

#### Size

The small footprint of the SOT-23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

#### Height

The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

#### Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

#### Simplified Board Layout

The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

#### Low THD

The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10 kΩ load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

#### Low Supply Current

The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

#### Wide Voltage Range

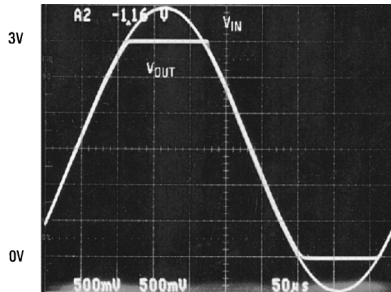
The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

### INPUT COMMON MODE

#### Voltage Range

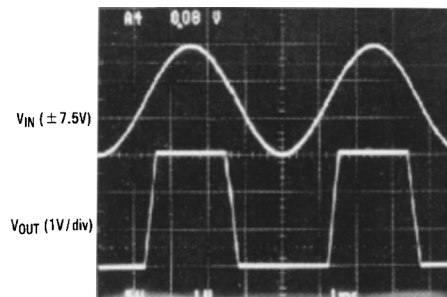
The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. [Figure 62](#) shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in [Figure 63](#), can cause excessive current to flow in or out of the input pins, adversely affecting reliability.



An input voltage signal exceeds the LMC7101 power supply voltages with no output phase inversion.

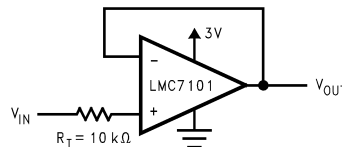
**Figure 62. Input Voltage**



A  $\pm 7.5\text{V}$  input signal greatly exceeds the 3V supply in [Figure 64](#) causing no phase inversion due to  $R_I$ .

**Figure 63. Input Signal**

Applications that exceed this rating must externally limit the maximum input current to  $\pm 5\text{ mA}$  with an input resistor as shown in [Figure 64](#).



**Figure 64.  $R_I$  Input Current Protection for Voltages Exceeding the Supply Voltage**

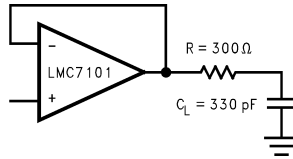
## RAIL-TO-RAIL OUTPUT

The approximate output resistance of the LMC7101 is  $180\Omega$  sourcing and  $130\Omega$  sinking at  $V_S = 3\text{V}$  and  $110\Omega$  sourcing and  $80\Omega$  sinking at  $V_S = 5\text{V}$ . Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

## CAPACITIVE LOAD TOLERANCE

The LMC7101 can typically directly drive a  $100\text{ pF}$  load with  $V_S = 15\text{V}$  at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op amps. The combination of the op amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in [Figure 65](#). This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.



**Figure 65. Resistive Isolation of a 330 pF Capacitive Load**

**COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS**

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in [Figure 66](#)),  $C_f$  is first estimated by:

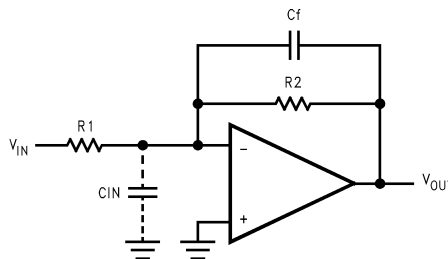
$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for  $C_f$  may be different. The values of  $C_f$  should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)



**Figure 66. Cancelling the Effect of Input Capacitance**

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## REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">20</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC7101AIM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A00A	
LMC7101AIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00A	<b>Samples</b>
LMC7101AIM5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A00A	
LMC7101AIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00A	<b>Samples</b>
LMC7101BIM5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A00B	
LMC7101BIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00B	<b>Samples</b>
LMC7101BIM5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A00B	
LMC7101BIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00B	<b>Samples</b>
LMC7101QM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT6A	<b>Samples</b>
LMC7101QM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT6A	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7101AIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7101AIM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101AIM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101BIM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101BIM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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