Quad Digitally Programmable Potentiometer (DPP™) with 256 Taps and SPI Interface

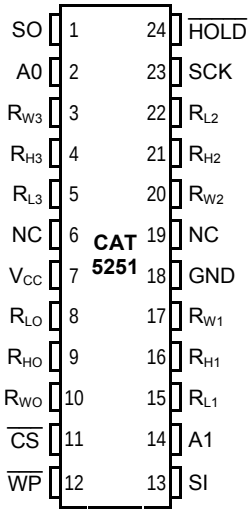
FEATURES

- Four linear-taper digitally programmable potentiometers
- 254 resistor taps per potentiometer
- End to end resistance 50 kΩ or 100 kΩ
- Potentiometer control and memory access via SPI interface
- Low wiper resistance, typically 100 Ω
- Nonvolatile memory storage for up to four wiper settings for each potentiometer
- Automatic recall of saved wiper settings at power up
- 2.5 to 6.0 volt operation
- Standby current less than 1 μA
- 1,000,000 nonvolatile WRITE cycles
- 100 year nonvolatile memory data retention
- SOIC 24-lead and TSSOP 24-lead
- Industrial temperature range

For Ordering Information details, see page 14.

PIN CONFIGURATION

SOIC 24-Lead (W)
TSSOP 24-Lead (Y)

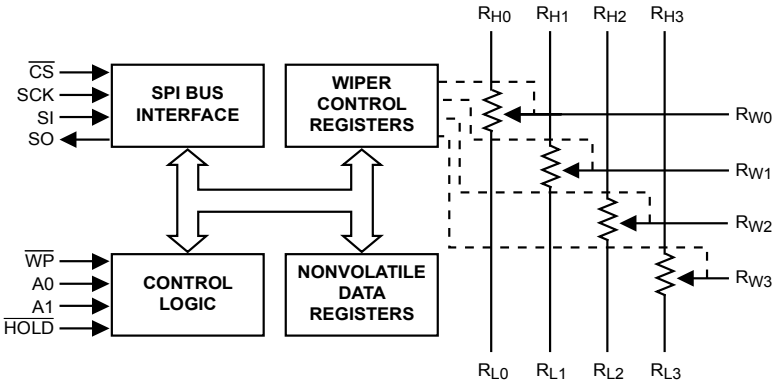


DESCRIPTION

The CAT5251 is four Digitally Programmable Potentiometers (DPPs™) integrated with control logic and 16 bytes of NVRAM memory. Each DPP consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. A separate 8-bit control register (WCR) independently controls the wiper tap switches for each DPP. Associated with each wiper control register are four 8-bit non-volatile memory data registers (DR) used for storing up to four wiper settings. Writing to the wiper control register or any of the non-volatile data registers is via a SPI serial bus. On power-up, the contents of the first data register (DR0) for each of the four potentiometers is automatically loaded into its respective wiper control register.

The CAT5251 can be used as a potentiometer or as a two terminal, variable resistor. It is intended for circuit level or system level adjustments in a wide variety of applications. It is available in the -40°C to 85°C industrial operating temperature range and offered in a 24-lead SOIC and TSSOP package.

FUNCTIONAL DIAGRAM



PIN DESCRIPTION

SI: Serial Input
SI is the serial data input pin. This pin is used to input all opcodes, byte addresses and data to be written to the CAT5251. Input data is latched on the rising edge of the serial clock.

SO: Serial Output
SO is the serial data output pin. This pin is used to transfer data out of the CAT5251. During a read cycle, data is shifted out on the falling edge of the serial clock.

SCK: Serial Clock
SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the CAT5251. Opcodes, byte addresses or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

A0, A1: Device Address Inputs
These inputs set the device address when addressing multiple devices. A total of four devices can be addressed on a single bus. A match in the slave address must be made with the address input in order to initiate communication with the CAT5251.

R_H, R_L: Resistor End Points
The four sets of R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper
The four R_W pins are equivalent to the wiper terminal of a mechanical potentiometer.

$\overline{CS}$: Chip Select

$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the CAT5251 and $\overline{CS}$ high disables the CAT5251. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby mode (unless an internal write operation is underway). The CAT5251 draws ZERO current in the Standby mode. A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect

$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low, all non-volatile write operations to the Data registers are inhibited (change of wiper control register is allowed). $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the registers. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

$\overline{HOLD}$: Hold
The $\overline{HOLD}$ pin is used to pause transmission to the CAT5251 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{CC} or tied to V_{CC} through a resistor.

PIN DESCRIPTION

Pin #	Name	Function
1	SO	Serial Data Output
2	A0	Device Address, LSB
3	R_{W3}	Wiper Terminal for Potentiometer 3
4	R_{H3}	High Reference Terminal for Potentiometer 3
5	R_{L3}	Low Reference Terminal for Potentiometer 3
6	NC	No Connect
7	V_{CC}	Supply Voltage
8	R_{L0}	Low Reference Terminal for Potentiometer 0
9	R_{H0}	High Reference Terminal for Potentiometer 0
10	R_{W0}	Wiper Terminal for Potentiometer 0
11	$\overline{CS}$	Chip Select
12	$\overline{WP}$	Write Protection
13	SI	Serial Input
14	A1	Device Address
15	R_{L1}	Low Reference Terminal for Potentiometer 1
16	R_{H1}	High Reference Terminal for Potentiometer 1
17	R_{W1}	Wiper Terminal for Potentiometer 1
18	GND	Ground
19	NC	No Connect
20	R_{W2}	Wiper Terminal for Potentiometer 2
21	R_{H2}	High Reference Terminal for Potentiometer 2
22	R_{L2}	Low Reference Terminal for Potentiometer 2
23	SCK	Bus Serial Clock
24	$\overline{HOLD}$	Hold

SERIAL BUS PROTOCOL

The CAT5251 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT5251 to interface directly with many of today's popular microcontrollers. The CAT5251 contains an 8-bit instruction register. The instruction set and the operation codes are detailed in Table 3, Instruction Set on page 8.

After the device is selected with $\overline{CS}$ going low the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

DEVICE OPERATION

The CAT5251 is four resistor arrays integrated with an SPI serial interface logic, four 8-bit wiper control registers and sixteen 8-bit, non-volatile memory data registers. Each resistor array contains 255 separate resistive elements connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). R_H and R_L are symmetrical and may be interchanged. The tap positions between and at the ends of the series resistors are connected to the output wiper terminals (R_W) by a CMOS transistor switch. Only one tap point for each potentiometer is connected to its wiper terminal at a time and is determined by the value of the wiper control register. Data can be read or written to the wiper control registers or the non-volatile memory data registers via the SPI bus. Additional instructions allow data to be transferred between the wiper control registers and each respective potentiometer's non-volatile data registers. Also, the device can be instructed to operate in an "increment/decrement" mode.

ABSOLUTE MAXIMUM RATINGS (1)

Parameter	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to V_{SS} (2)(3)	-2.0 to +V_{CC} +2.0	V
V_{CC} with Respect to Ground	-2.0 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 s)	300	°C
Wiper Current	±6	mA

Recommended Operating Conditions

V_{CC} = +2.5 V to +6 V

Parameter	Ratings	Units
Operating Ambient Temperature (Industrial)	-40 to +85	°C

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20ns.

(3) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POTENTIOMETER CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance (-00)			100		kΩ
R_{POT}	Potentiometer Resistance (-50)			50		kΩ
	Potentiometer Resistance Tolerance				±20	%
	R_{POT} Matching				1	%
	Power Rating	25°C, each pot			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	I_W = ±3 mA @ V_{CC} = 3 V		200	300	Ω
		I_W = ±3 mA @ V_{CC} = 5 V		100	150	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0 V	GND		V_{CC}	V
V_N	Noise	(1)				nV/√Hz
	Resolution			0.4		%
	Absolute Linearity (2)	$R_{W(n)(actual)}$ - $R_{(n)(expected)}$ (5)			±1	LSB(4)
	Relative Linearity (3)	$R_{W(n+1)}$ - [$R_{W(n)+LSB}$](5)			±0.5	LSB(4)
TC_{RPOT}	Temperature Coefficient of R_{POT}	(1)		±300		ppm/°C
TC_{RATIO}	Ratiometric Temp. Coefficient	(1)			20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	(1)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50 kΩ (1)		0.4		MHz

D.C. OPERATING CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC1}	Power Supply Current	f_{SCK} = 2.5 MHz, SO Open V_{CC} = 6 V Inputs = GND			1	mA
I_{CC2}	Power Supply Current Non-volatile Write	f_{SCK} = 2.5 MHz, SO = Open V_{CC} = 6 V Inputs = GND			5	mA
I_{SB}	Standby Current (V_{CC} = 5.0 V)	V_{IN} = GND or V_{CC}; SO Open			1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			10	µA
V_{IL}	Input Low Voltage		-1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3 V)	I_{OL} = 3 mA			0.4	V
V_{OH1}	Output High Voltage (V_{CC} = 6 V)	I_{OH} = -1.6 mA	V_{CC} - 0.8			V

Notes:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

(2) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

(3) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.

(4) LSB = R_{TOT} / 255 or (R_H - R_L) / 255, single pot

(5) n = 0, 1, 2, ..., 255.

PIN CAPACITANCE [1]

Applicable over recommended operating range from T_A = 25ºC, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{OUT}	Output Capacitance (SO)	V_{OUT} = 0 V			8	pF
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$, A0, A1)	V_{IN} = 0 V			6	pF

A.C. CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{SU}	Data Setup Time	C_L = 50 pF	50			ns
t_H	Data Hold Time		50			ns
t_{WH}	SCK High Time		125			ns
t_{WL}	SCK Low Time		125			ns
f_{SCK}	Clock Frequency		DC		3	MHz
t_{LZ}	$\overline{HOLD}$ to Output Low Z				50	ns
t_{RI} [1]	Input Rise Time				2	µs
t_{FI} [1]	Input Fall Time				2	µs
t_{HD}	$\overline{HOLD}$ Setup Time		100			ns
t_{CD}	$\overline{HOLD}$ Hold Time		100			ns
t_V	Output Valid from Clock Low				200	ns
t_{HO}	Output Hold Time		0			ns
t_{DIS}	Output Disable Time				250	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z				100	ns
t_{CS}	$\overline{CS}$ High Time		250			ns
t_{CSS}	$\overline{CS}$ Setup Time		250			ns
t_{CSH}	$\overline{CS}$ Hold Time		250			ns

POWER UP TIMING [1][2]

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

WIPER TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	µs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	µs

Notes:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

WRITE CYCLE LIMITS

Over recommended operating conditions unless otherwise stated.

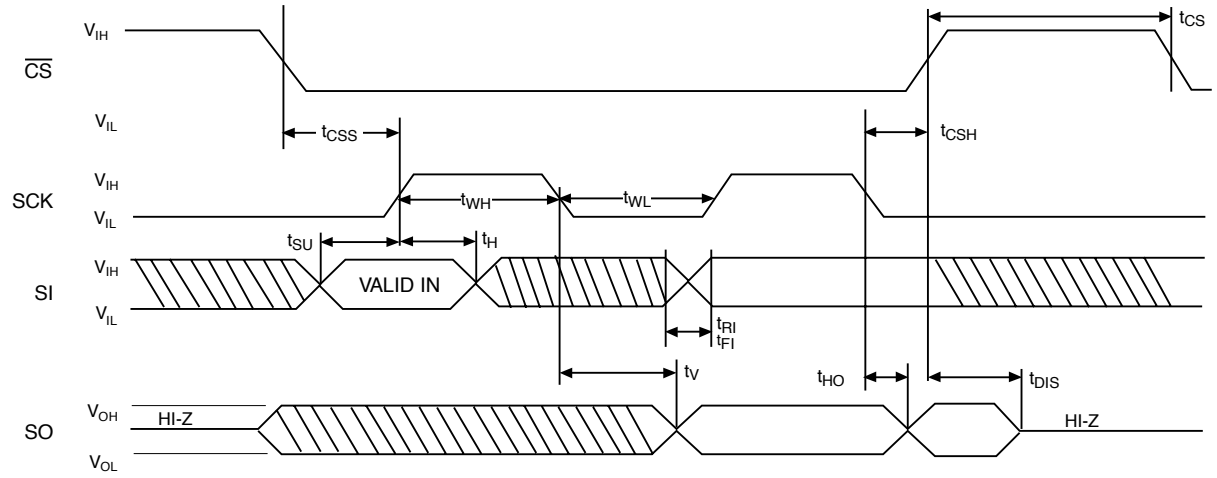
Symbol	Parameter		Min	Typ	Max	Units
t_{WR}	Write Cycle Time				5	ms

RELIABILITY CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

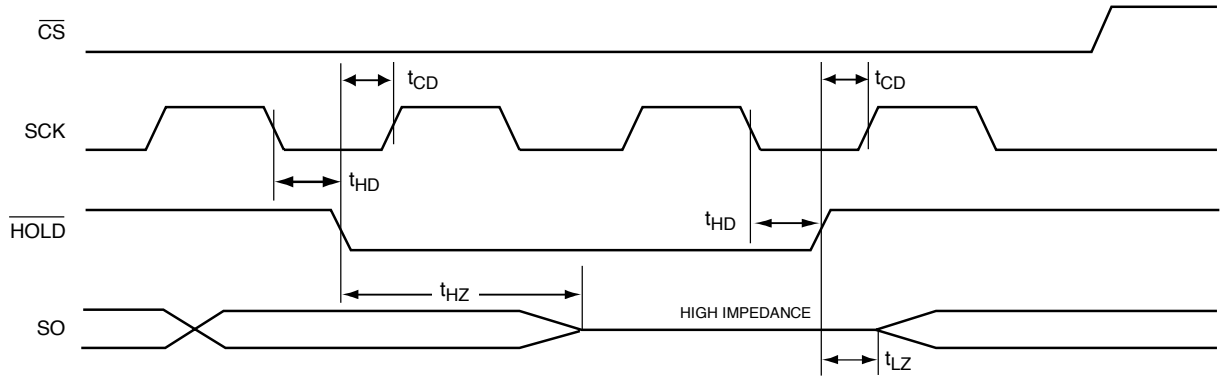
Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N_{END} (1)	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T_{DR} (1)	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V_{ZAP} (1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
I_{LTH} (1)	Latch-Up	JEDEC Standard 17	100			mA

Figure 1. Sychronous Data Timing



Note: Dashed Line = mode (1, 1)

Figure 2. $\overline{HOLD}$ Timing



Notes:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

INSTRUCTION AND REGISTER DESCRIPTION

DEVICE TYPE / ADDRESS BYTE

The first byte sent to the CAT5251 from the master/processor is called the Device Address Byte. The most significant four bits of the Device Type address are a device type identifier. These bits for the CAT5251 are fixed at 0101[B] (refer to Table 1).

The two least significant bits in the slave address byte, A1 - A0, are the internal slave address and must match the physical device address which is defined by the state of the A1 - A0 input pins for the CAT5251 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A1 - A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The remaining two bits in the device address byte must be set to 0.

INSTRUCTION BYTE

The next byte sent to the CAT5251 contains the instruction and register pointer information. The four most significant bits used provide the instruction opcode I3-I0. The R1 and R0 bits point to one of the four data registers of each associated potentiometer. The least two significant bits point to one of four Wiper Control Registers. The format is shown in Table 2.

Data Register Selection

Data Register Selected	R1	R0
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

Table 1. Identification Byte Format

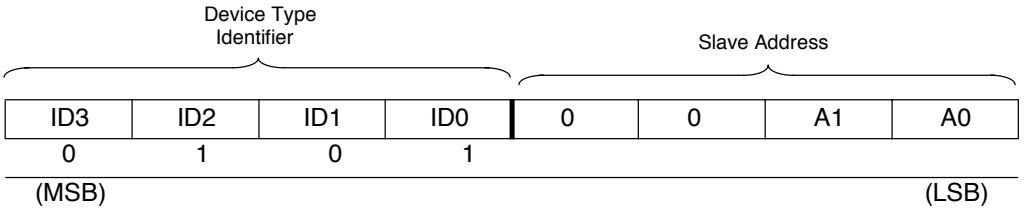
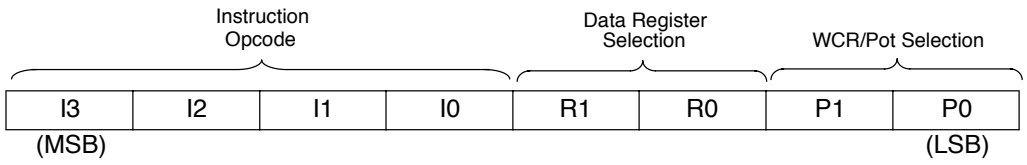


Table 2. Instruction Byte Format



WIPER CONTROL AND DATA REGISTERS

Wiper Control Register (WCR)

The CAT5251 contains four 8-bit Wiper Control Registers, one for each potentiometer. The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written by the host via Write Wiper Control Register instruction; it may be written by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction; it can be modified one step at a time by the Increment/decrement instruction (see Instruction section for more details). Finally, it is loaded with the content of its data register zero (DR0) upon power-up.

The Wiper Control Register is a volatile register that loses its contents when the CAT5251 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down.

Data Registers (DR)

Each potentiometer has four 8-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Control Register. Any data changes in one of the Data Registers is a non-volatile operation and will take a maximum of 5ms.

If the application does not require storage of multiple settings for the potentiometer; the Data Registers can be used as standard memory locations for system parameters or user preference data.

Write in Process

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ input goes HIGH after a write sequence is received. The status of the internal write cycle can be monitored by issuing a Read Status command to read the Write in Process (WIP) bit.

INSTRUCTIONS

Four of the ten instructions are three bytes in length. These instructions are:

- **Read Wiper Control Register** – read the current wiper position of the selected potentiometer in the WCR
- **Write Wiper Control Register** – change current wiper position in the WCR of the selected potentiometer
- **Read Data Register** – read the contents of the selected Data Register
- **Write Data Register** – write a new value to the selected Data Register
- **Read Status** – Read the status of the WIP bit which when set to "1" signifies a write cycle is in progress.

Table 3. Instruction Set

Note: 1/0 = data is one or zero

Instruction	Instruction Set								Operations
	I3	I2	I1	I0	R1	R0	WCR1/ P1	WCR0/ P0	
Read Wiper Control Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Control Register pointed to by P1-P0
Write Wiper Control Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Control Register pointed to by P1-P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1-P0 and R1-R0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1-P0 and R1-R0
XFR Data Register to Wiper Control Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1-P0 and R1-R0 to its associated Wiper Control Register
XFR Wiper Control Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Control Register pointed to by P1-P0 to the Data Register pointed to by R1-R0
Global XFR Data Registers to Wiper Control Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by R1-R0 of all four pots to their respective Wiper Control Registers
Global XFR Wiper Control Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Control Registers to their respective data Registers pointed to by R1-R0 of all four pots
Increment/Decrement Wiper Control Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1-P0
Read Status (WIP bit)	0	1	0	1	0	0	0	1	Read WIP bit to check internal write cycle status

The basic sequence of the three byte instructions is illustrated in Figure 8. These three-byte instructions exchange data between the WCR and one of the Data Registers. The WCR controls the position of the wiper. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or the transfer can occur between all potentiometers and one associated register.

Four instructions require a two-byte sequence to complete, as illustrated in Figure 7. These instructions transfer data between the host/processor and the CAT5251; either between the host and one of the data registers or directly between the host and the Wiper Control Register. These instructions are:

— **XFR Data Register to Wiper Control Register**
This transfers the contents of one specified Data Register to the associated Wiper Control Register.

— **XFR Wiper Control Register to Data Register**
This transfers the contents of the specified Wiper Control Register to the specified associated Data Register.

— **Global XFR Data Register to Wiper Control Register**
This transfers the contents of all specified Data Registers to the associated Wiper Control Registers.

— **Global XFR Wiper Counter Register to Data Register**
This transfers the contents of all Wiper Control Registers to the specified associated Data Registers.

INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (Figure 9 and 10). The Increment/Decrement command is different from the other commands. Once the command is issued the master can clock the selected wiper up and/or down in one segment steps; thereby providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the R_L terminal.

See Instructions format for more detail.

Figure 7. Two-Byte Instruction Sequence

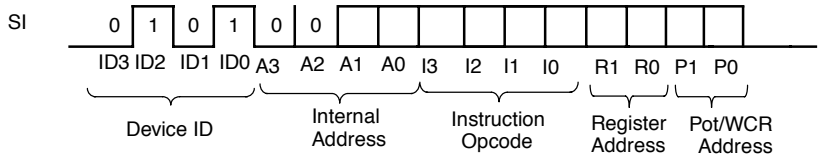


Figure 8. Three-Byte Instruction Sequence

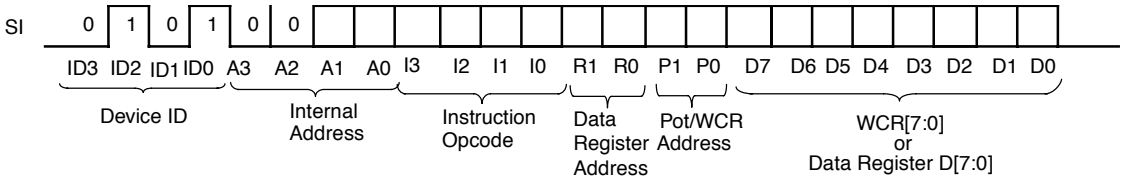


Figure 9. Increment/Decrement Instruction Sequence

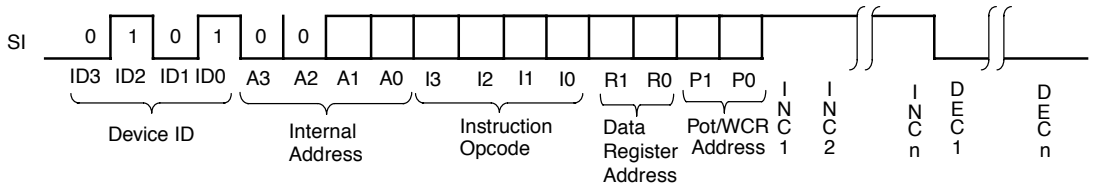
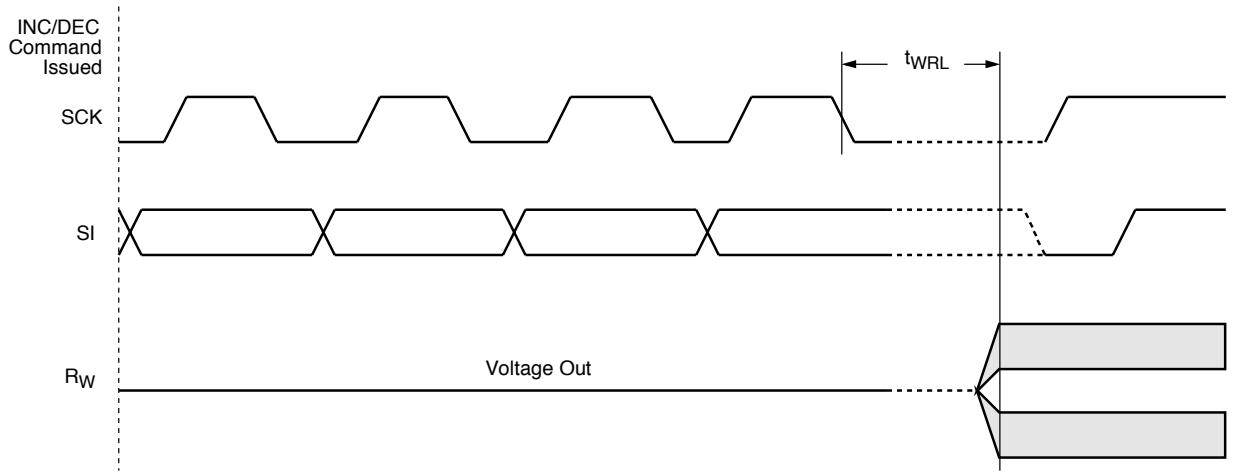


Figure 10. Increment/Decrement Timing Limits



INSTRUCTION FORMAT

Read Wiper Control Register (WCR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA								$\overline{CS}$
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	P1	P0	7	6	5	4	3	2	1	0	

Write Wiper Control Register (WCR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA								$\overline{CS}$
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	P1	P0	7	6	5	4	3	2	1	0	

Read Data Register (DR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA								$\overline{CS}$
	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	P1	P0	7	6	5	4	3	2	1	0	

Write Data Register (DR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA								$\overline{CS}$	
	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	P1	P0	7	6	5	4	3	2	1	0		High Voltage Write Cycle

Read Status (WIP)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA								$\overline{CS}$
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	70	60	50	40	30	20	10	WIP	

Global Transfer Data Register (DR) to Wiper Control Register (WCR)

	DEVICE ADDRESSES								INSTRUCTION								
	0	1	0	1	0	0	A1	A0	0	0	0	1	R1	R0	0	0	$\overline{CS}$

Global Transfer Wiper Control Register (WCR) to Data Register (DR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								$\overline{CS}$	High Voltage Write Cycle
	0	1	0	1	0	0	A1	A0	1	0	0	0	R1	R0	0	0		

Transfer Wiper Control Register (WCR) to Data Register (DR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								$\overline{CS}$	High Voltage Write Cycle
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	P1	P0		

Transfer Data Register (DR) to Wiper Control Register (WCR)

$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								$\overline{CS}$
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	P1	P0	

Increment (I)/Decrement (D) Wiper Control Register (WCR)

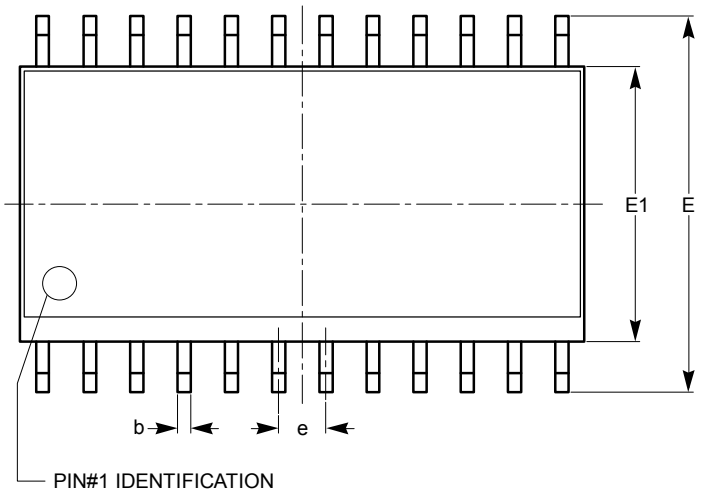
$\overline{CS}$	DEVICE ADDRESSES								INSTRUCTION								DATA					$\overline{CS}$
	0	1	0	1	0	0	A1	A0	0	0	1	0	0	0	P1	P0	I/D	I/D	. . .	I/D	I/D	

Notes:

(1) Any write or transfer to the Non-volatile Data Registers is followed by a high voltage cycle after a STOP has been issued.

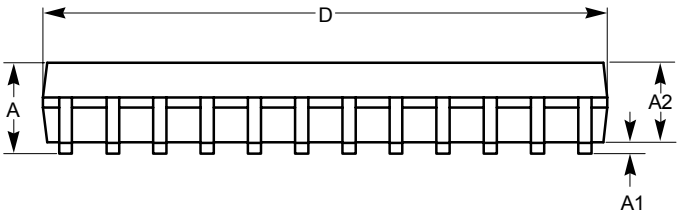
PACKAGING OUTLINE DRAWINGS

SOIC 24-Lead 300 mils (W) (1)(2)

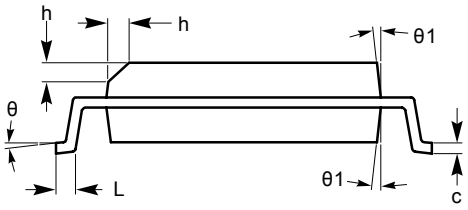


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW



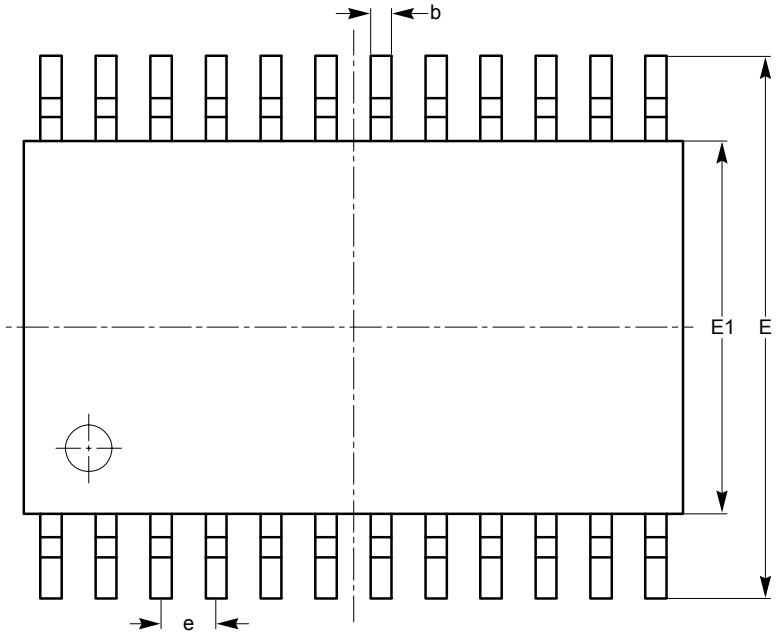
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.

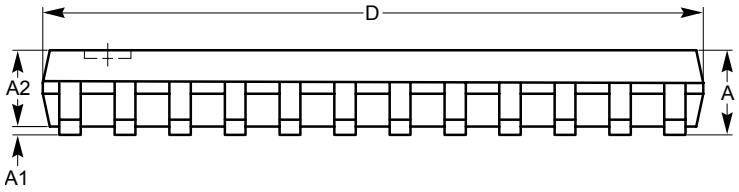
(2) Complies with JEDEC standard MS-013.

TSSOP 24-Lead 4.4 mm (Y) [1][2]

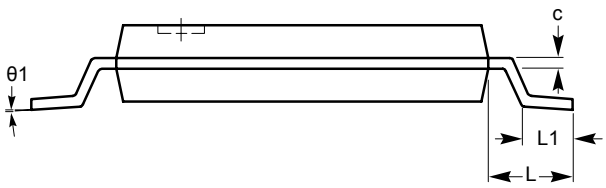


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.70
θ1	0°		8°



SIDE VIEW



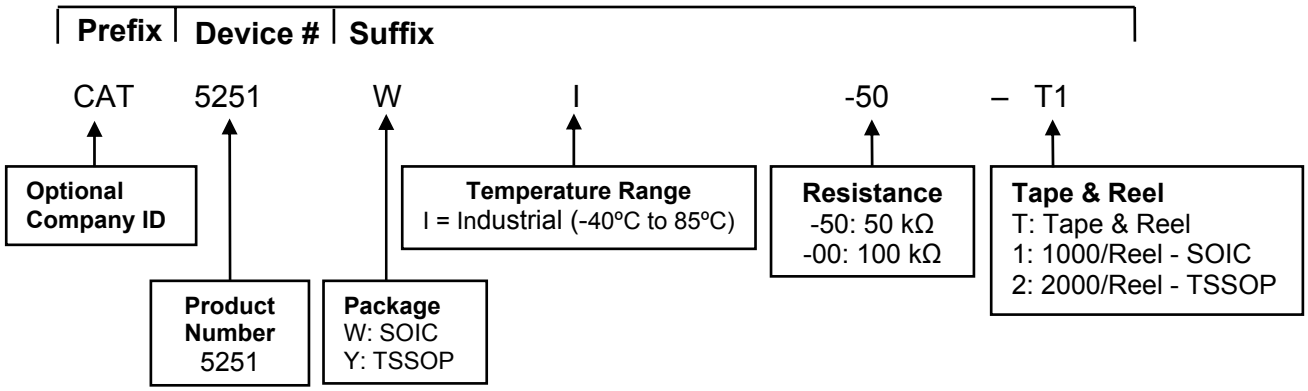
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.

(2) Complies with JEDEC standard MO-153.

EXAMPLE OF ORDERING INFORMATION



ORDERING INFORMATION

Orderable Part Number	Resistance (kΩ)	Package	Lead Finish
CAT5251WI-50-T1	50	SOIC	Matte-Tin
CAT5251WI-00-T1	100		
CAT5251YI-50-T2	50	TSSOP	
CAT5251YI-00-T2	100		
CAT5251WI50	50	SOIC	
CAT5251WI00	100		
CAT5251YI50	50	TSSOP	
CAT5251YI00	100		

Notes:

(1) All packages are RoHS compliant (Lead-free, Halogen-free).

(2) This device used in the above example is a CAT5251WI-50-T1 (SOIC, Industrial Temperature, 50 kΩ, Tape & Reel).

REVISION HISTORY

Date	Rev.	Description
11-Nov-03	C	Eliminated BGA package in all areas Eliminated Commercial temperature range
06-May-04	D	Updated Functional Diagram Updated wiper resistance from 50Ω to 100Ω Updated notes in Absolute Max Ratings Eliminated Commercial temperature range in all areas Updated Potentiometer Characteristics table Updated DC Characteristics table Updated AC Characteristics table Added Wiper Timing Table on page 6 Corrected Synchronous Data Timing (Figure 1) drawing
13-Dec-07	E	Updated Package Outline Drawings Updated Example of Ordering Information Added MD- to document number Reformatted data sheet layout
07-Feb-08	F	Update Instruction Format – Read Data Register (DR) and Write Data Register (DR)
26-Nov-08	G	Change logo and fine print to ON Semiconductor
31-Jul-09	H	Update Ordering Information table

PUBLICATION ORDERING INFORMATION
LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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