LP3470

LP3470 Tiny Power On Reset Circuit

Literature Number: SNVS003E

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National Semiconductor

LP3470

Tiny Power On Reset Circuit

General Description

The LP3470 is a micropower CMOS voltage supervisory circuit designed to monitor power supplies in microprocessor (µP) and other digital systems. It provides maximum adjustability for power-on-reset (POR) and supervisory functions. It is available in the following six standard reset threshold voltage (V_{RTH}) options: 2.63V, 2.93V, 3.08V, 3.65V, 4.00V, 4.38V, and 4.63V. If other voltage options between 2.4V and 5.0V are desired please contact your National Semiconductor representative.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage falls below a reset threshold. The reset time-out period is adjustable using an external capacitor. Reset remains asserted for an interval (programmed by an external capacitor) after V_{CC} has risen above the threshold voltage.

The device is available in the tiny SOT23-5 package.

Key Specifications

- ±1% Reset Threshold Accuracy Over Temperature
- Standard Reset Threshold Voltages: 2.63V, 2.93V, 3.08V, 3.65V, 4.00V, 4.38V, and 4.63V
- Custom Reset Threshold Voltages: For other voltages between 2.4V and 5.0V contact your National Semiconductor representative
- Very Low Quiescent Current (16 µA typical)
- Guaranteed $\overline{\text{Reset}}$ valid down to V_{CC}=0.5V

Features

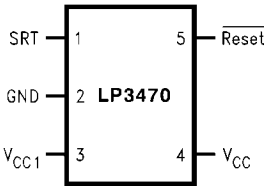
- Tiny SOT23-5 Package
- Open Drain $\overline{\text{Reset}}$ Output
- Programmable Reset Timeout Period Using an External Capacitor
- Immune to Short V_{CC} Transients

Applications

- Critical µP and µC Power Monitoring
- Intelligent Instruments
- Computers
- Portable/Battery-Powered Equipments

Pin Configuration and Basic Operating Circuit

Pin Configuration



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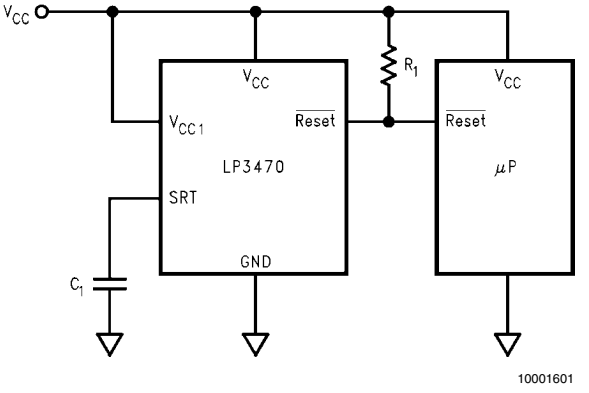
Top View
See NS Package Number MF05A

Basic Operating Circuit



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Ordering Information

Operating Temperature Range	Nominal V_{RTH} (V)	Order Number	Package Marking	Package Type	Supplied As
−20°C to +85°C	2.63	LP3470M5-2.63	D25B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-2.63	D25B	SOT23-5	3000 Units on Tape and Reel
	2.93	LP3470M5-2.93	D26B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-2.93	D26B	SOT23-5	3000 Units on Tape and Reel
	3.08	LP3470M5-3.08	D28B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-3.08	D28B	SOT23-5	3000 Units on Tape and Reel
	4.00	LP3470M5-4.00	D29B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-4.00	D29B	SOT23-5	3000 Units on Tape and Reel
	4.38	LP3470M5-4.38	D30B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-4.38	D30B	SOT23-5	3000 Units on Tape and Reel
	4.63	LP3470M5-4.63	D31B	SOT23-5	1000 Units on Tape and Reel
		LP3470M5X-4.63	D31B	SOT23-5	3000 Units on Tape and Reel
−40°C to +85°C	2.63	LP3470IM5-2.63	D25C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-2.63	D25C	SOT23-5	3000 Units on Tape and Reel
	2.75	LP3470IM5-2.75	D38C	SOT23-5	1000 Units on Tape and Reel
	2.83	LP3470IM5-2.83	D39C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-2.83	D39C	SOT23-5	3000 Units on Tape and Reel
	2.93	LP3470IM5-2.93	D26C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-2.93	D26C	SOT23-5	3000 Units on Tape and Reel
	3.08	LP3470IM5-3.08	D28C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-3.08	D28C	SOT23-5	3000 Units on Tape and Reel
	3.65	LP3470IM5-3.65	D37C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-3.65	D37C	SOT23-5	3000 Units on Tape and Reel
	4.00	LP3470IM5-4.00	D29C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-4.00	D29C	SOT23-5	3000 Units on Tape and Reel
	4.38	LP3470IM5-4.38	D30C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-4.38	D30C	SOT23-5	3000 Units on Tape and Reel
	4.63	LP3470IM5-4.63	D31C	SOT23-5	1000 Units on Tape and Reel
		LP3470IM5X-4.63	D31C	SOT23-5	3000 Units on Tape and Reel
	4.80	LP3470IM5X-4.8	D15C	SOT23-5	1000 Units on Tape and Reel

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Voltage	−0.3V to +6V
$\overline{\text{Reset}}$ Voltage	−0.3V to +6V
Output Current ($\overline{\text{Reset}}$)	10 mA
Operating Temperature Range	
LP3470	−20°C to +85°C
LP3470I	−40°C to +85°C
Junction Temperature (T_{Jmax})	125°C
Power Dissipation (T_A = 25°C) (*Note 2*)	300 mW
θ_{JA} (*Note 2*)	280°C/W
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 5 sec)	260°C
ESD Rating (*Note 3*)	2 kV

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface** type apply over the full operating temperature range, unless otherwise specified. V_{CC} = +2.4V to +5.0V unless otherwise noted.

Symbol	Parameter	Conditions	Typ (*Note 4*)	Min (*Note 5*)	Max (*Note 5*)	Units
V_{CC}	Operating Voltage Range			**0.5**	**5.5**	V
I_{CC}	V_{CC} Supply Current	V_{CC} = 4.5V	16		**30**	µA
V_{RTH}	Reset Threshold Voltage (*Note 6*)	LP3470	V_{RTH}	0.99 V_{RTH} **0.99 V_{RTH}**	1.01 V_{RTH} **1.01 V_{RTH}**	V
		LP3470I	V_{RTH}	0.99 V_{RTH} **0.985 V_{RTH}**	1.01 V_{RTH} **1.015 V_{RTH}**	
V_{HYST}	Hysteresis Voltage (*Note 7*)		35	**15**	**65**	mV
t_{PD}	V_{CC} to Reset Delay	V_{CC} falling at 1 mV/µs	100		**300**	µs
t_{RP}	Reset Timeout Period (*Note 8*)	C_1 = 1 nF	2	**1.0**	**3.5**	ms
V_{OL}	Reset Output Voltage Low	V_{CC} = 0.5V; I_{OL} = 30 µA			**0.1**	V
		V_{CC} = 1.0V; I_{OL} = 100 µA			**0.1**	
		V_{CC} = V_{RTH} −100 mV; I_{OL} = 4 mA			**0.4**	
R_1	External Pull-up Resistor		20	0.68	68	kΩ
I_{LEAK}	Reset Output Leakage Current		0.15		1 **6**	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its operating conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (Maximum Junction Temperature), θ_{JA} (Junction to Ambient Thermal Resistance), and T_A (Ambient Temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 4: Typical numbers are at 25°C and represent the most likely parametric norm.

Note 5: Min. and Max. limits in standard typeface are 100% production tested at 25°C. Min. and Max. limits in boldface are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 6: Factory-trimmed reset thresholds are available in 50 mV increments from 2.4V to 5.0V. Contact your National Semiconductor representative.

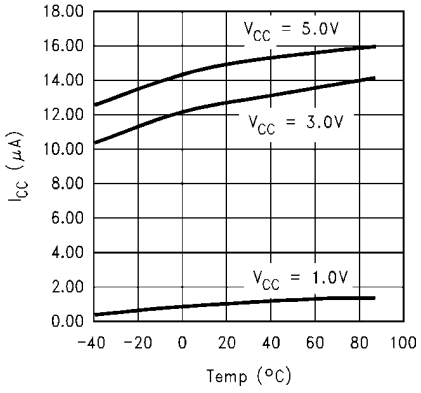
Note 7: V_{HYST} affects the relation between V_{CC} and $\overline{\text{Reset}}$ as shown in the timing diagram.

Note 8: t_{RP} is programmable by varying the value of the external capacitor (C_1) connected to pin SRT. The equation is: $t_{RP} = 2000 \times C_1$ (C_1 in µF and t_{RP} in ms).

Typical Operating Characteristics

T_A = +25°C, unless otherwise specified.

I_{CC} vs Temperature



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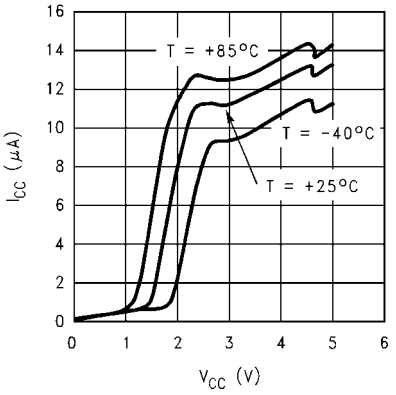
I_{CC} vs V_{CC}



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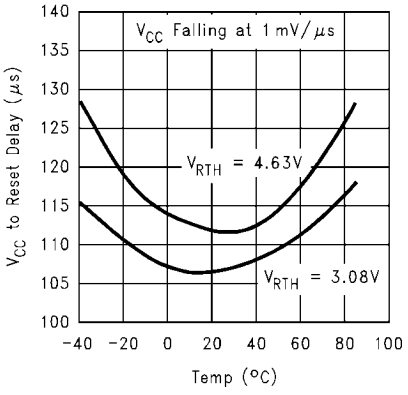
V_{CC} to Reset Delay vs Temp



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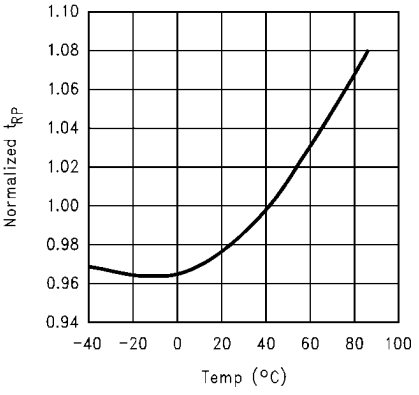
Normalized t_{RP} vs Temp.



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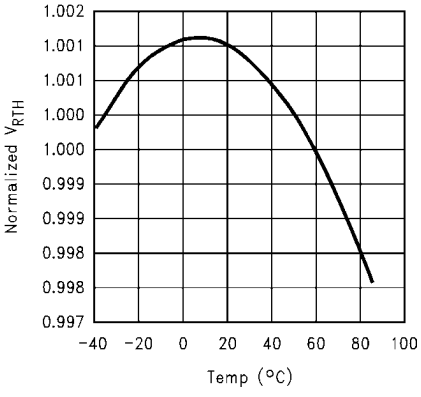
Normalized V_{RTH} vs Temp.



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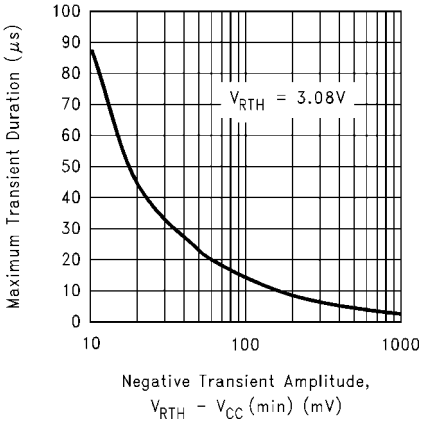
Transient Rejection



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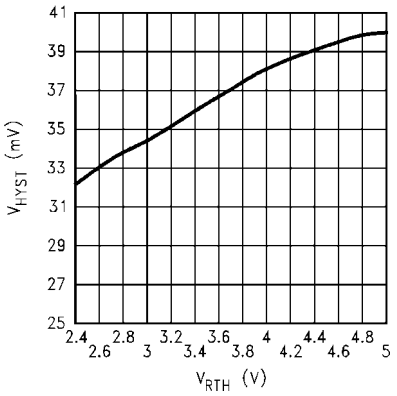
V_{HYST} vs V_{RTH}



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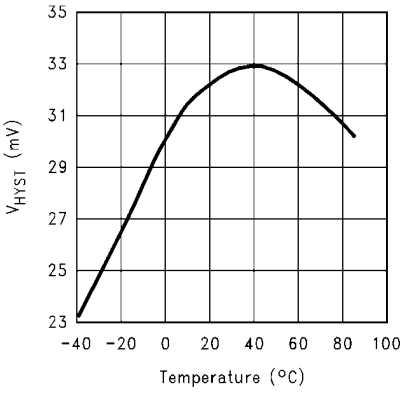
V_{HYST} vs Temperature



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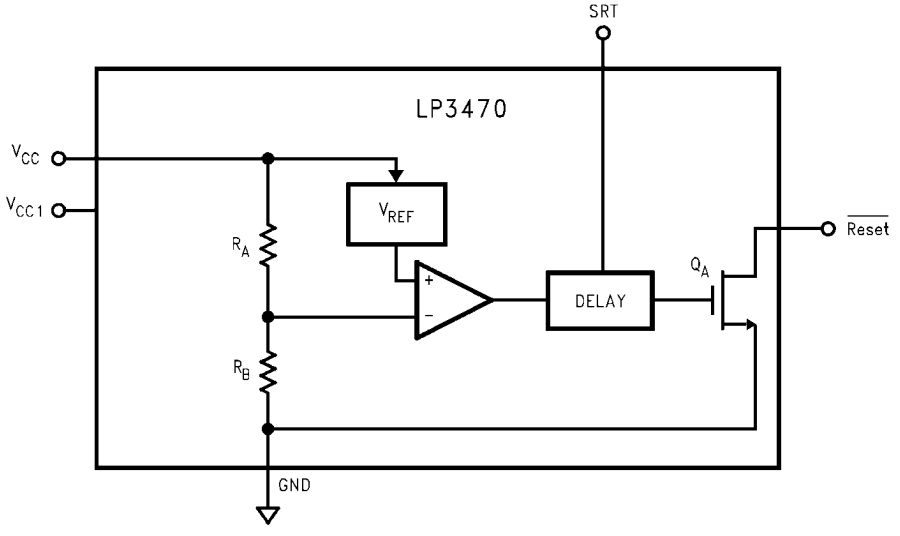
Pin Descriptions

Pin	Name	Function
1	SRT	Set Reset Time-out Input. Connect a capacitor between this input and ground to select the Reset Time-out period (t_{RP}). t_{RP} = 2000 x C_1 (C_1 in µF and t_{RP} in ms). If no capacitor is connected, leave this pin floating.
2	GND	Ground pin.
3	V_{CC1}	Always connect to pin V_{CC} (Pin 4).
4	V_{CC}	Supply voltage, and reset threshold monitor input.
5	$\overline{\text{Reset}}$	Open-Drain, Active-Low reset output. Connect to an external pull-up resistor. $\overline{\text{Reset}}$ changes from high to low whenever the monitored voltage (V_{CC}) drops below the reset threshold voltage (V_{RTH}). Once V_{CC} exceeds V_{RTH}, $\overline{\text{Reset}}$ remains low for the reset timeout period (t_{RP}) and then goes high.

Functional Block Diagram



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Application Information

RESET TIMEOUT PERIOD

The Reset Timeout Period (t_{RP}) is programmable using an external capacitor (C_1) connected to pin SRT of LP3470. A Ceramic chip capacitor rated at or above 10V is sufficient. The Reset Timeout Period (t_{RP}) can be calculated using the following formula:

$$t_{RP}\ (ms) = 2000 \times C_1\ (\mu F).$$

For example a C_1 of 100 nF will achieve a t_{RP} of 200 ms. If no delay due to t_{RP} is needed in a certain application, the pin SRT should be left floating.

RESET OUTPUT

In applications like microprocessor (µP) systems, errors might occur in system operation during power-up, power-down, or brownout conditions. It is imperative to monitor the power supply voltage in order to prevent these errors from occurring.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage is below a threshold (V_{RTH}) voltage. $\overline{\text{Reset}}$ is guaranteed to be a logic low for $V_{CC} > 0.5V$. Once V_{CC} exceeds the reset threshold, the reset is kept asserted for a time period (t_{RP}) programmed by an external capacitor (C_1); after this interval $\overline{\text{Reset}}$ goes to logic high. If a brownout condition occurs (monitored voltage falls below the reset threshold minus a small hysteresis), $\overline{\text{Reset}}$ goes low. When V_{CC} returns above the reset threshold, $\overline{\text{Reset}}$ remains low for a time period t_{RP} before going to logic high.

PULL-UP RESISTOR SELECTION

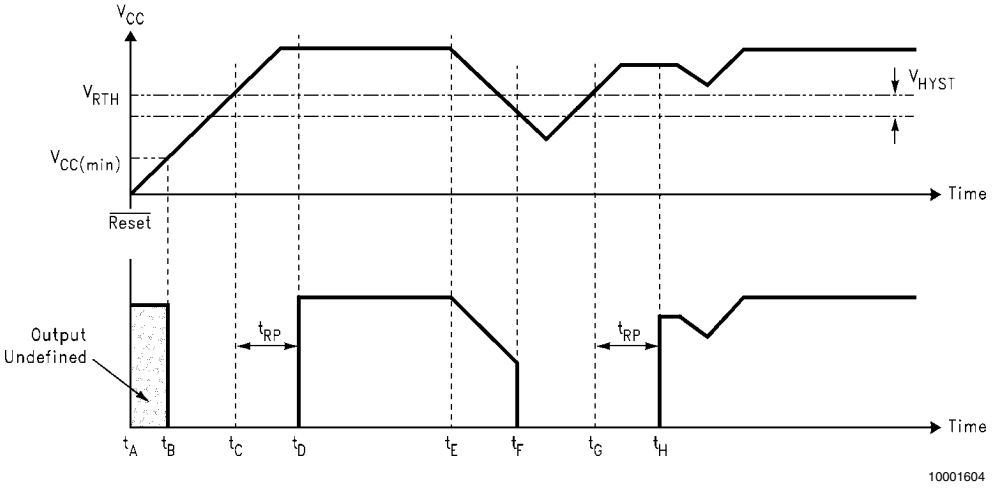
The LP3470's $\overline{\text{Reset}}$ output structure is a simple open-drain N-channel MOSFET switch. A pull-up resistor (R_1) should be connected to V_{CC}.

R_1 should be large enough to limit the current through the output MOSFET (Q_1) below 10 mA. A resistor value of more than 680Ω guarantees this. R_1 should also be small enough to ensure a logic high while supplying all the leakage current through the $\overline{\text{Reset}}$ pin. A resistor value of less than 68kΩ satisfies this condition. A typical pull-up resistor value of 20 kΩ is sufficient in most applications.

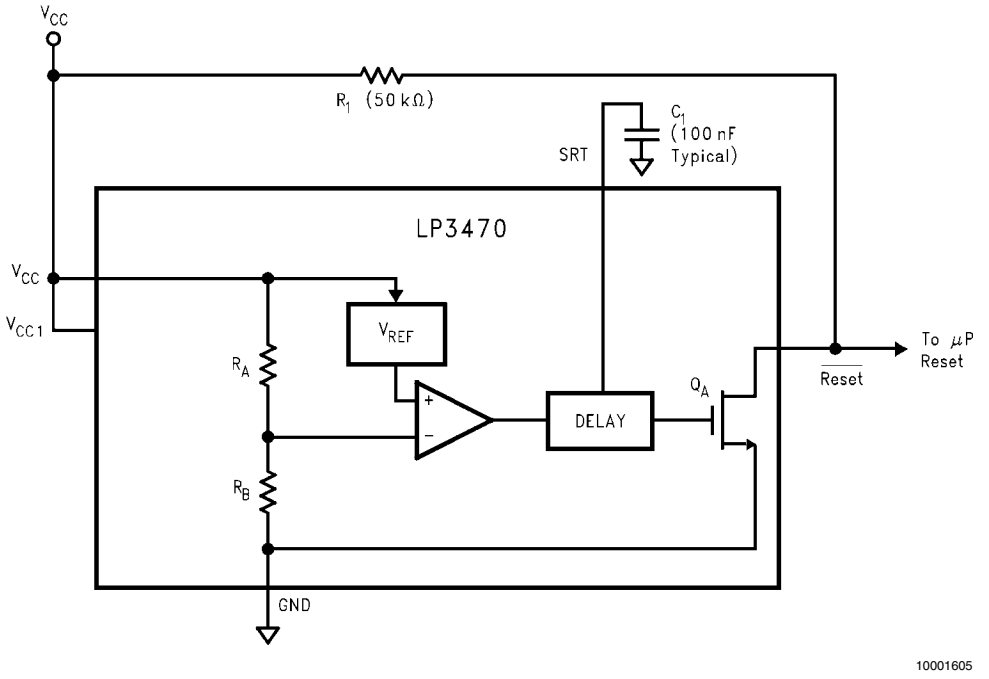
NEGATIVE-GOING V_{CC} TRANSIENTS

The LP3470 is relatively immune to short duration negative-going V_{CC} transients (glitches). The Typical Operating Characteristics show the Maximum Transient Duration vs. Negative Transient Amplitude (graph titled Transient Rejection), for which reset pulses are not generated. This graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the transient amplitude increases (i.e. goes farther below the reset threshold), the maximum allowable pulse width decreases. A 0.1 µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

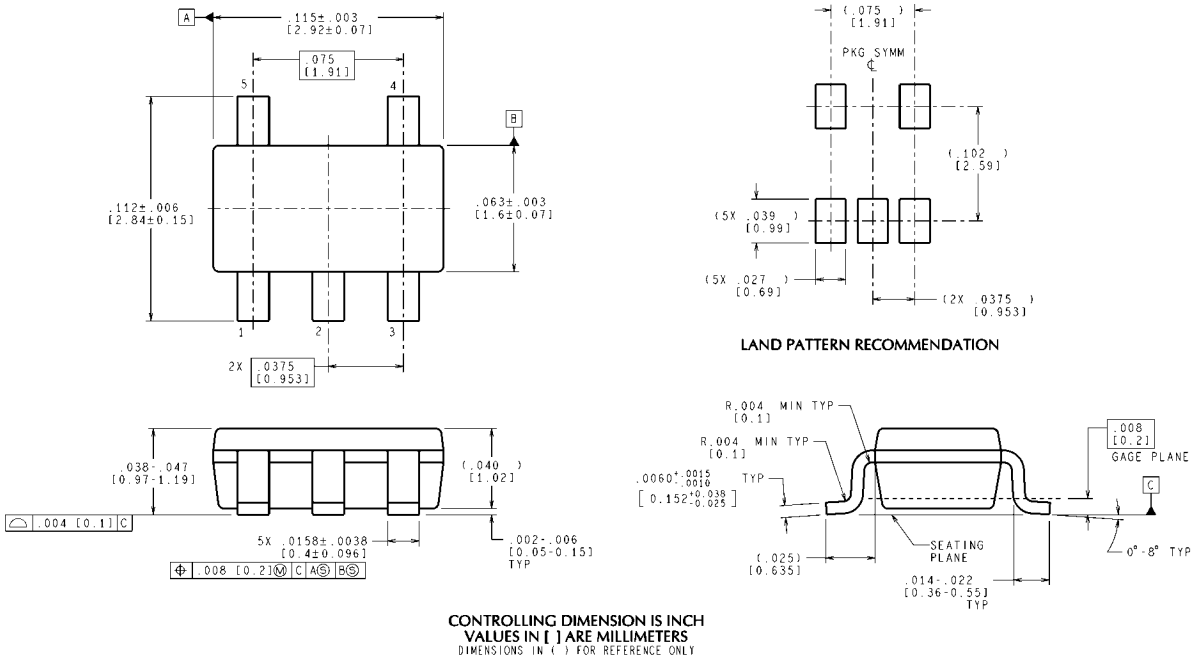
Timing Diagram



Typical Application Circuit



Physical Dimensions inches (millimeters) unless otherwise noted



MF05A (Rev D)

5-Lead Small Outline Package (M5)
For Ordering Information See *Ordering Information* Table In This Data Sheet
NSPackage Number MF05A

Notes

Notes

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