- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})

- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
    – 2000-V Human-Body Model (A114-A)
    – 200-V Machine Model (A115-A)
   – 1000-V Charged-Device Model (C101)

SN54LVCH244A . . . J OR W PACKAGE
SN74LVCH244A . . . DB, DBQ, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)

1OE	1	20	V_{CC}
1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
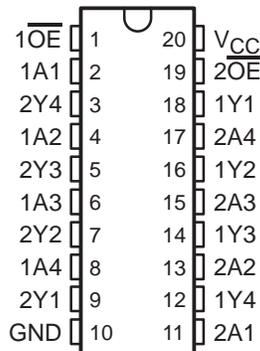
SN74LVCH244A . . . RGY PACKAGE
(TOP VIEW)

1OE, V_{CC}

1A1	2	19	2OE
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4

GND, 2A1
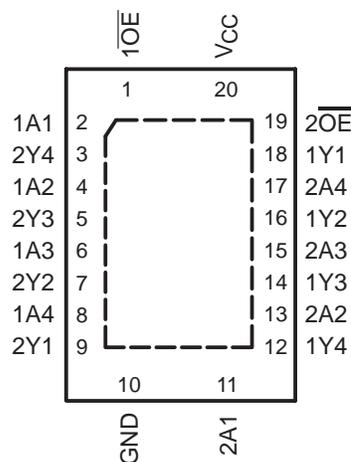
SN54LVCH244A . . . FK PACKAGE
(TOP VIEW)

2Y4, 1A1, 1OE, V_{CC}, 2OE

1A2	4	18 1Y1
2Y3	5	17 2A4
1A3	6	16 1Y2
2Y2	7	15 2A3
1A4	8	14 1Y3

2Y1, GND, 2A1, 1Y4, 2A2
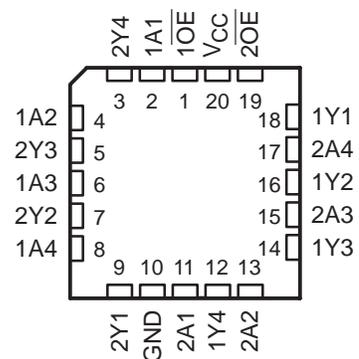
description/ordering information

The SN54LVCH244A octal buffer/line driver is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH244A octal buffer/line driver is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices are organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, these devices pass data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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description/ordering information (continued)

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVCH244ARGYR	LCH244A
	SOIC – DW	Tube of 25	SN74LVCH244ADW	LVCH244A
		Reel of 2000	SN74LVCH244ADWR	
	SOP – NS	Reel of 2000	SN74LVCH244ANSR	LVCH244A
	SSOP – DB	Reel of 2000	SN74LVCH244ADBR	LCH244A
	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCH244ADBQR	LCH244A
	TSSOP – PW	Tube of 70	SN74LVCH244APW	LCH244A
		Reel of 2000	SN74LVCH244APWR	
		Reel of 250	SN74LVCH244APWT	
	TVSOP – DGV	Reel of 2000	SN74LVCH244ADGVR	LCH244A
−55°C to 125°C	CDIP – J	Tube of 20	SNJ54LVCH244AJ	SNJ54LVCH244AJ
	CFP – W	Tube of 85	SNJ54LVCH244AW	SNJ54LVCH244AW
	LCCC – FK	Tube of 55	SNJ54LVCH244AFK	SNJ54LVCH244AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)
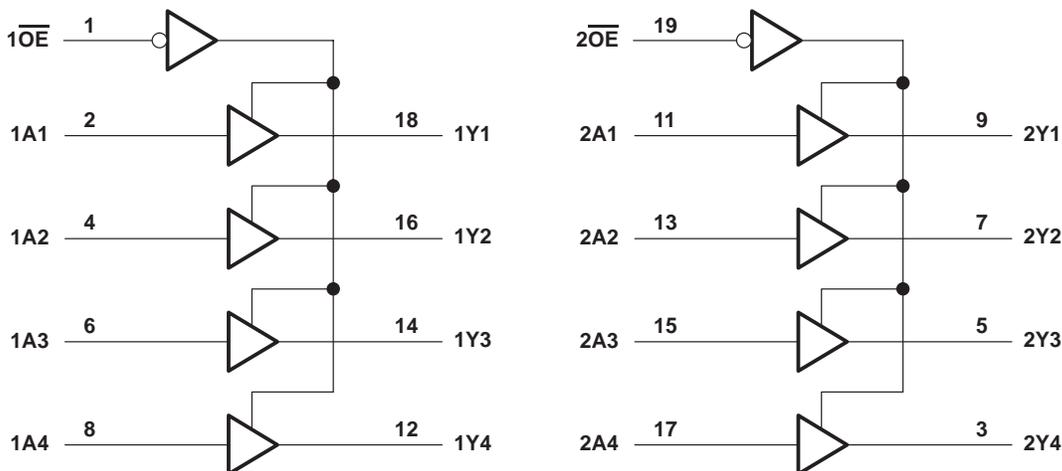
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 6.5 V
Input voltage range, V_I (see Note 1) .... –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O
   (see Note 1) .... –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O
   (see Notes 1 and 2) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$) .... –50 mA
Output clamp current, I_{OK} ($V_O < 0$) .... –50 mA
Continuous output current, I_O .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package .... 70°C/W
                    (see Note 3): DBQ package .... 68°C/W
                    (see Note 3): DGV package .... 92°C/W
                    (see Note 3): DW package .... 58°C/W
                    (see Note 3): NS package .... 60°C/W
                    (see Note 3): PW package .... 83°C/W
                    (see Note 4): RGY package .... 37°C/W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
      2. The value of V_{CC} is provided in the recommended operating conditions table.
      3. The package thermal impedance is calculated in accordance with JESD 51-7.
      4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVCH244A		SN74LVCH244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVCH244A			SN74LVCH244A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	$I_{OH} = -100\ \mu A$		1.65 V to 3.6 V				$V_{CC}{-}0.2$			V
			2.7 V to 3.6 V	$V_{CC}{-}0.2$						
	$I_{OH} = -4\ mA$		1.65 V				1.2			
	$I_{OH} = -8\ mA$		2.3 V				1.7			
	$I_{OH} = -12\ mA$		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	$I_{OH} = -24\ mA$		3 V	2.2			2.2			
V_{OL}	$I_{OL} = 100\ \mu A$		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	$I_{OL} = 4\ mA$		1.65 V						0.45	
	$I_{OL} = 8\ mA$		2.3 V						0.7	
	$I_{OL} = 12\ mA$		2.7 V			0.4			0.4	
	$I_{OL} = 24\ mA$		3 V			0.55			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5			±5	µA
I_{off}	V_I or $V_O = 5.5$ V		0						±10	µA
$I_{I(hold)}$	$V_I = 0.58$ V		1.65 V					‡		µA
	$V_I = 1.07$ V							‡		
	$V_I = 0.7$ V		2.3 V					45		
	$V_I = 1.7$ V							−45		
	$V_I = 0.8$ V		3 V		75			75		
	$V_I = 2$ V				−75			−75		
	$V_I = 0$ to 3.6 V§		3..6 V			±500			±500	
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±15			±10	µA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			10			10	µA
	$3.6\ V \leq V_I \leq 5.5\ V$¶					10			10	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4	12		4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		5.5	12		5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This information was not available at the time of publication.
§ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
¶ This applies in the disabled state only.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH244A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t_{pd}	A	Y		7.5	1	6.5	ns
t_{en}	$\overline{OE}$	Y		9	1	8	ns
t_{dis}	$\overline{OE}$	Y		8	1	7	ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH244A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	†	†	†	†		6.9	1.5	5.9	ns
t_{en}	$\overline{OE}$	Y	†	†	†	†		8.6	1	7.6	ns
t_{dis}	$\overline{OE}$	Y	†	†	†	†		6.8	1.5	5.8	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V TYP	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	†	†	47	pF
	Outputs disabled		†	†	2	

† This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION
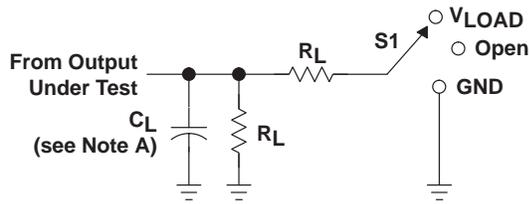
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
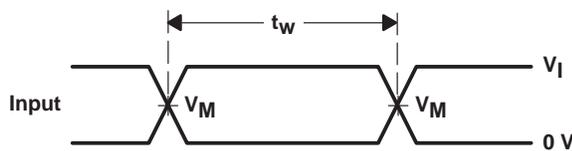
**VOLTAGE WAVEFORMS
PULSE DURATION**
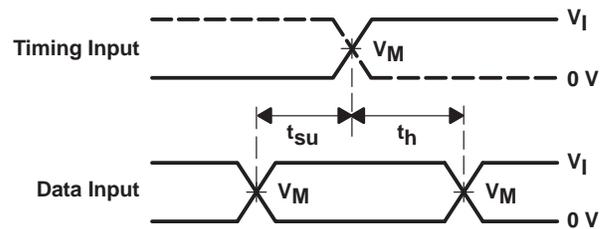
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
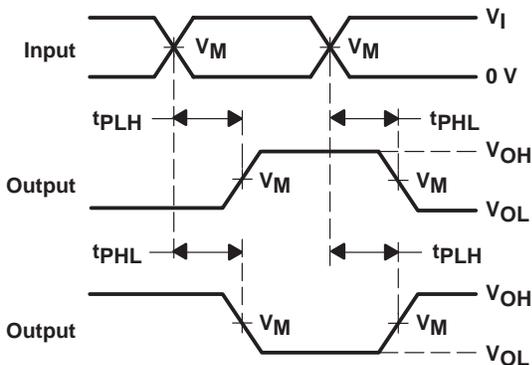
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**
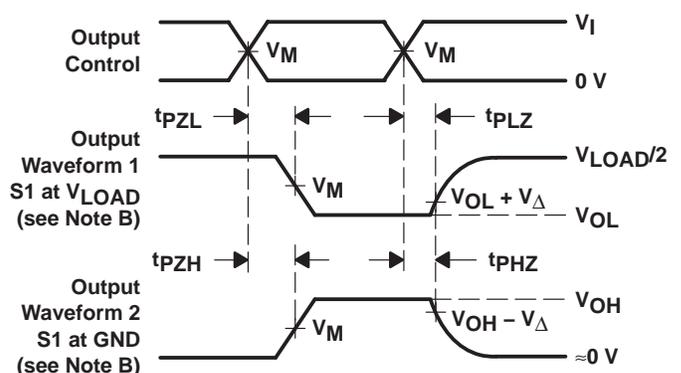
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 Ω$.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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7
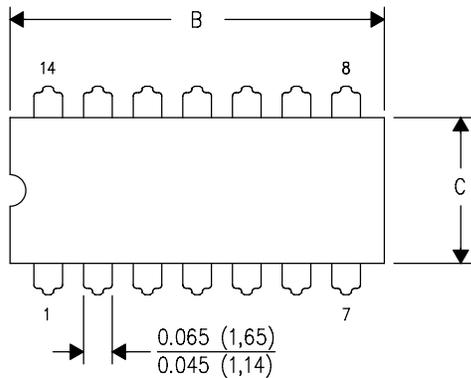
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

0.065 (1,65) / 0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52) / 0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66) / 0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36) / 0.008 (0,20)
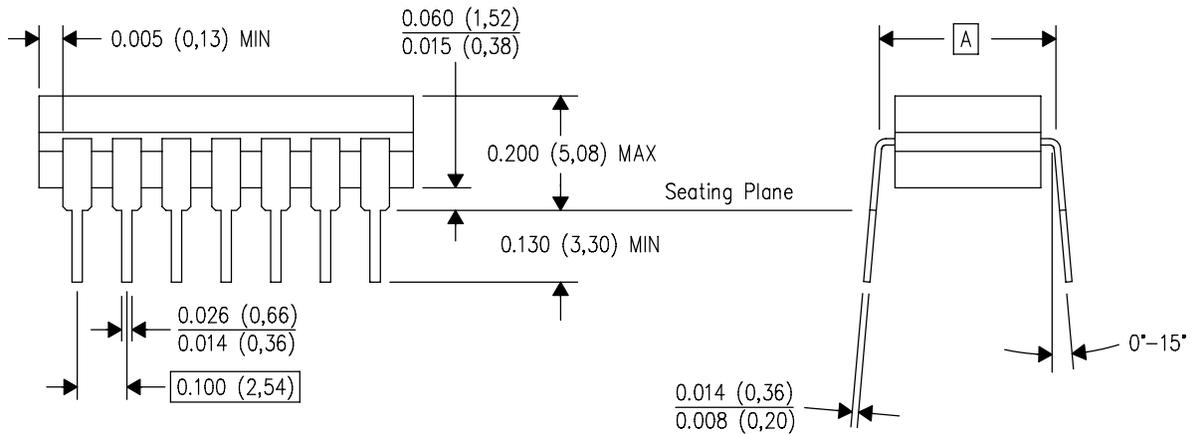
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
    B. This drawing is subject to change without notice.
    C. This package is hermetically sealed with a ceramic lid using glass frit.
    D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
    E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

W (R-GDFP-F20)   **CERAMIC DUAL FLATPACK**
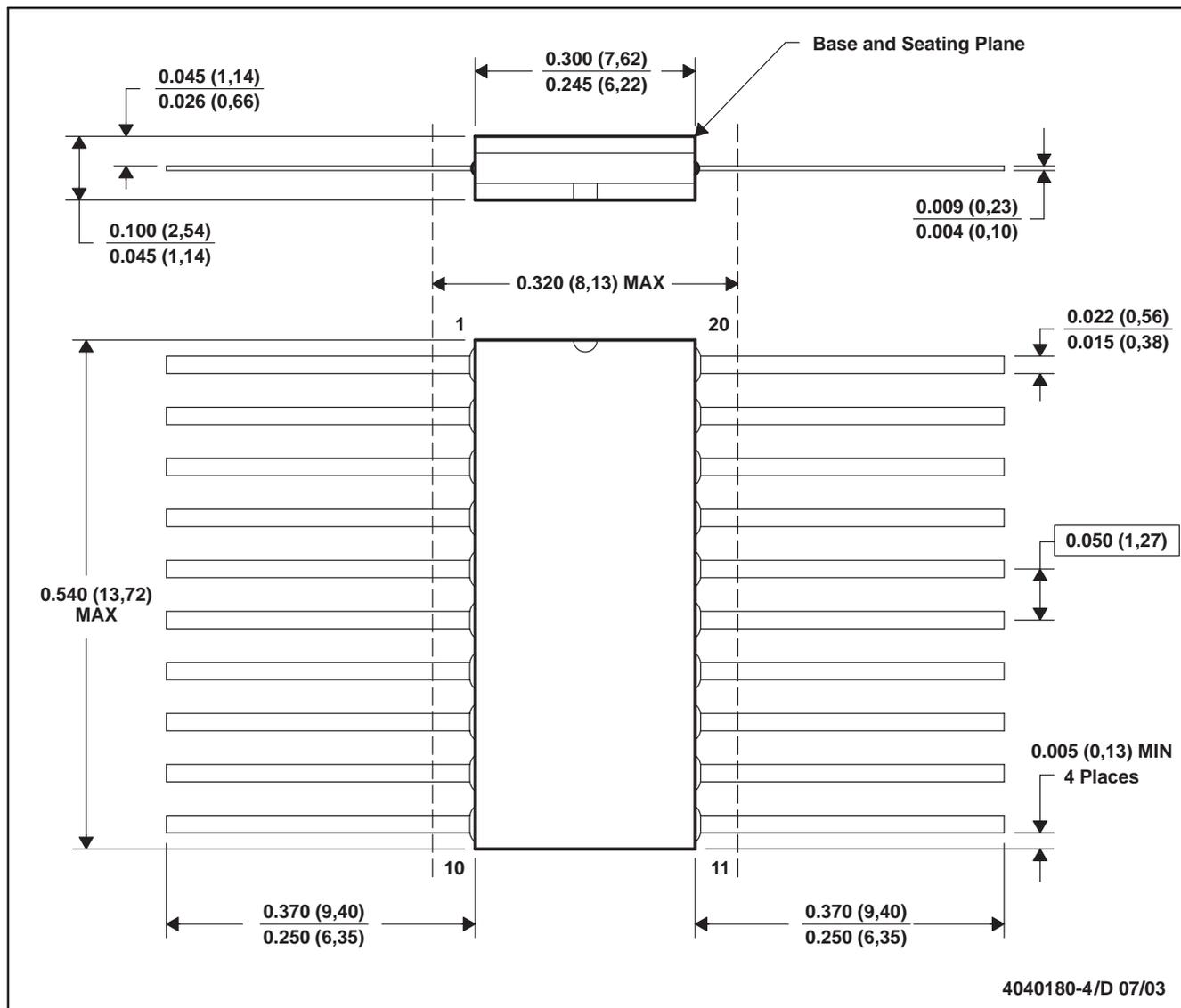
4040180-4/D 07/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within Mil-Std 1835 GDFP2-F20

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1

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER
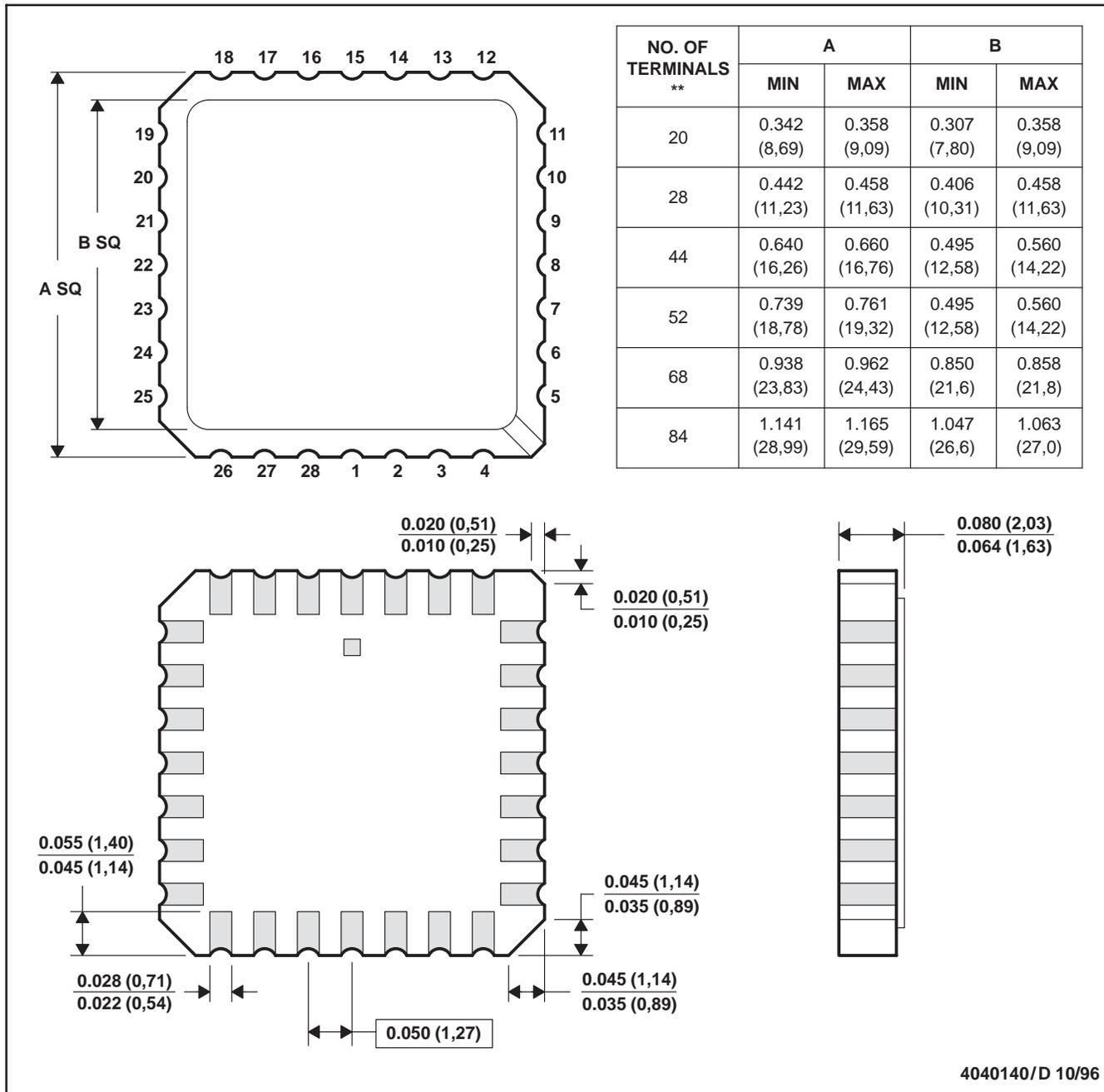
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. The terminals are gold plated.
        E. Falls within JEDEC MS-004

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DGV (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
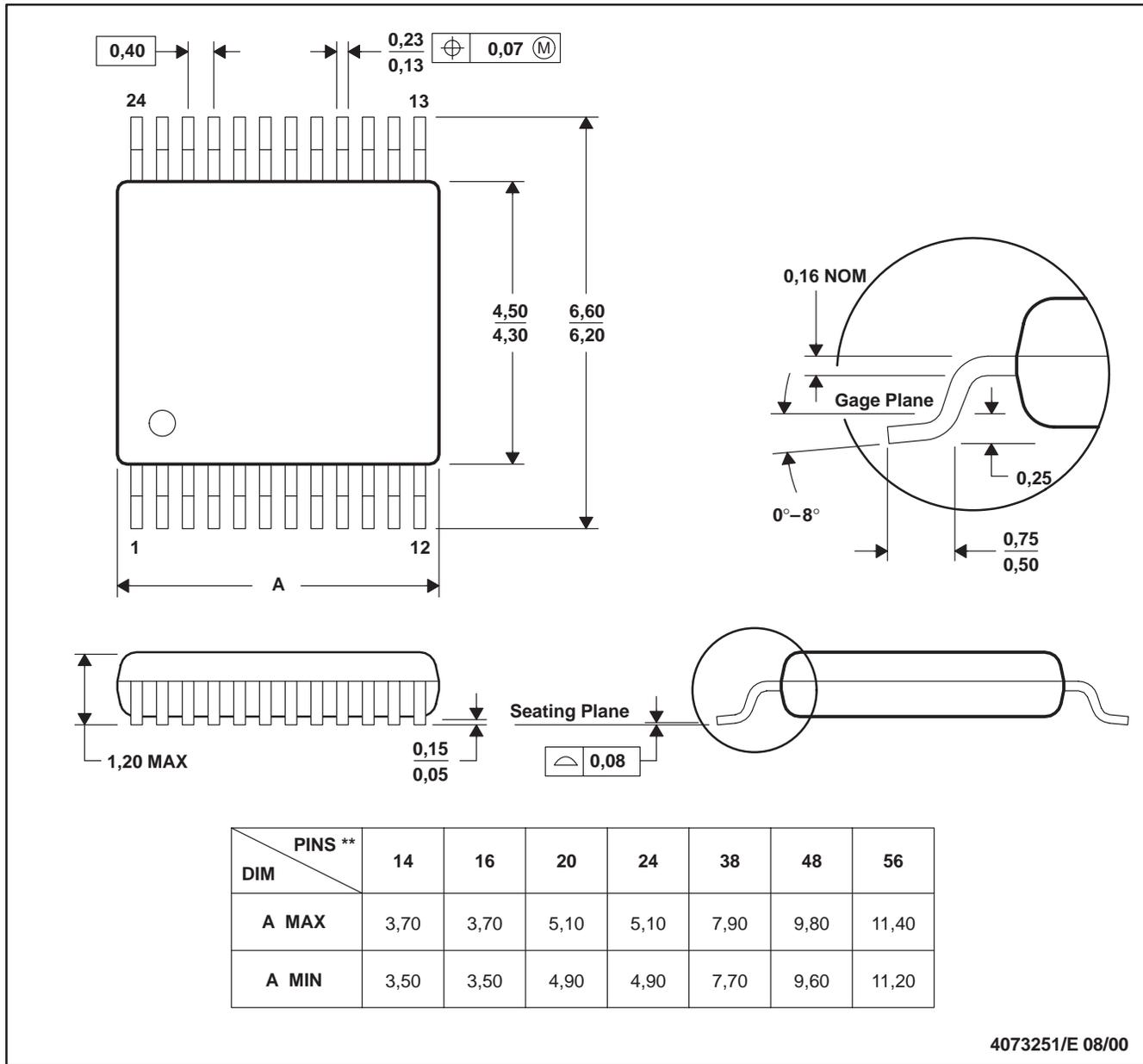
| PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
                                        14/16/20/56 Pins – MO-194

RGY (R–PQFP–N20)   **PLASTIC QUAD FLATPACK**
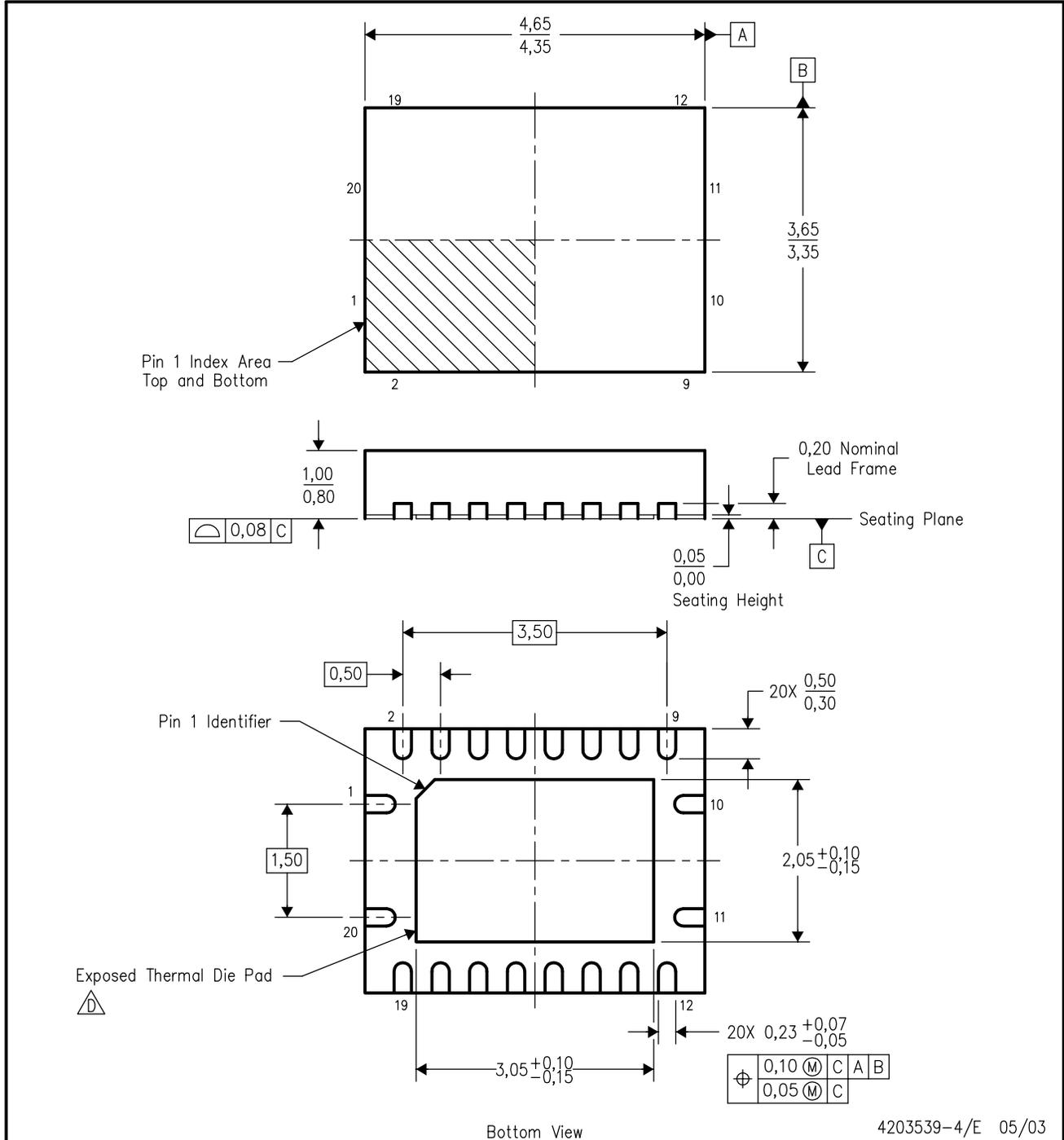
Pin 1 Index Area
Top and Bottom

0,20 Nominal
Lead Frame

Seating Plane

Seating Height

Pin 1 Identifier

Exposed Thermal Die Pad

Bottom View

4203539–4/E 05/03

NOTES: A. All linear dimensions are in millimeters.
  B. This drawing is subject to change without notice.
  C. QFN (Quad Flatpack No–Lead) package configuration.

  D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
      This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.

  E. Package complies to JEDEC MO–241 variation BC.

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DW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN

PINS ** / DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)
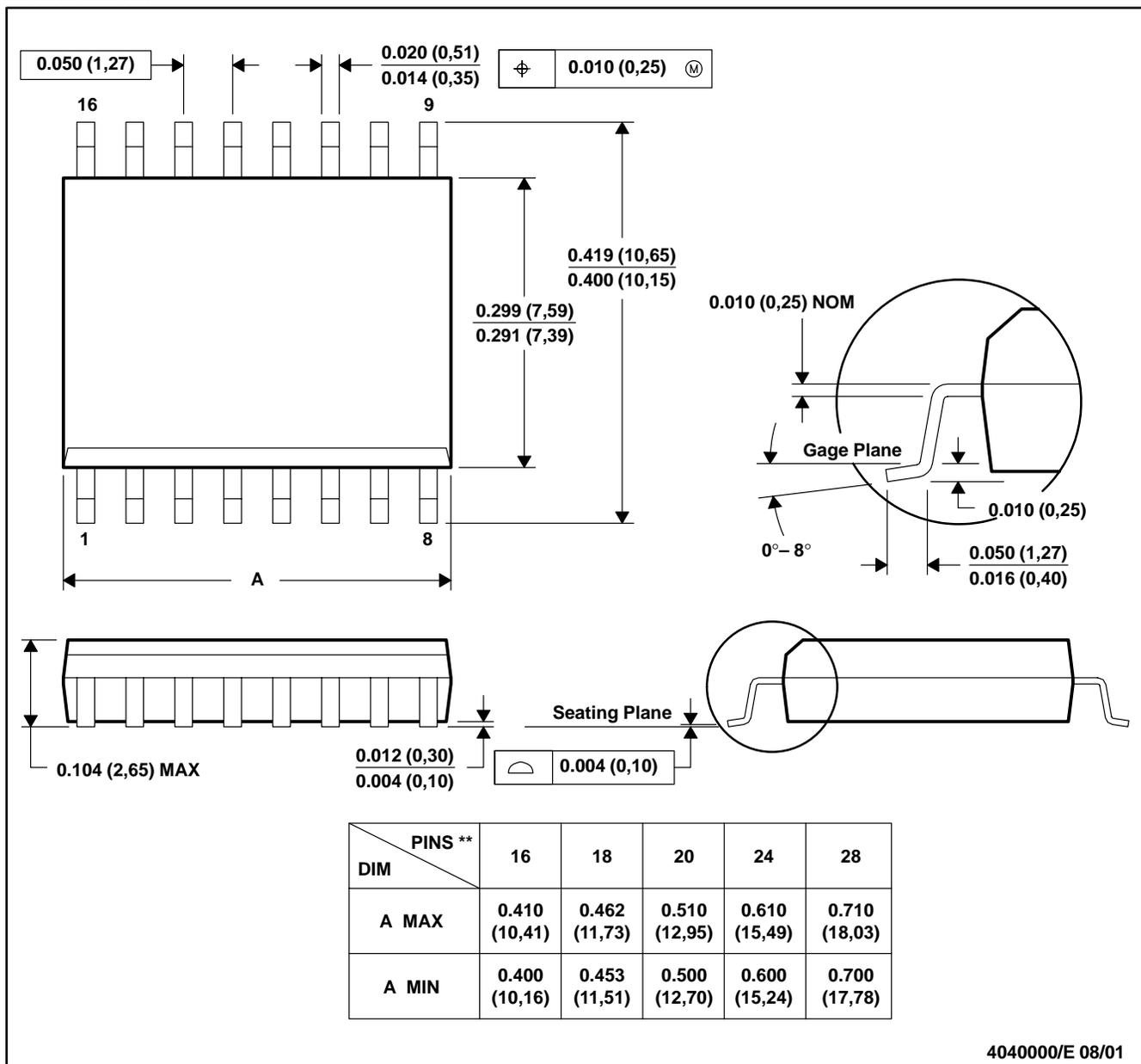
4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
   D. Falls within JEDEC MS-013

TEXAS INSTRUMENTS

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DBQ (R–PDSO–G**)   **PLASTIC SMALL–OUTLINE PACKAGE**

PINS ** DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0–137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

NOTES: A.   All linear dimensions are in millimeters.
        B.   This drawing is subject to change without notice.
        C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D.   Falls within JEDEC MO–137.

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MECHANICAL DATA

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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MECHANICAL DATA

DB (R-PDSO-G**)　　　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
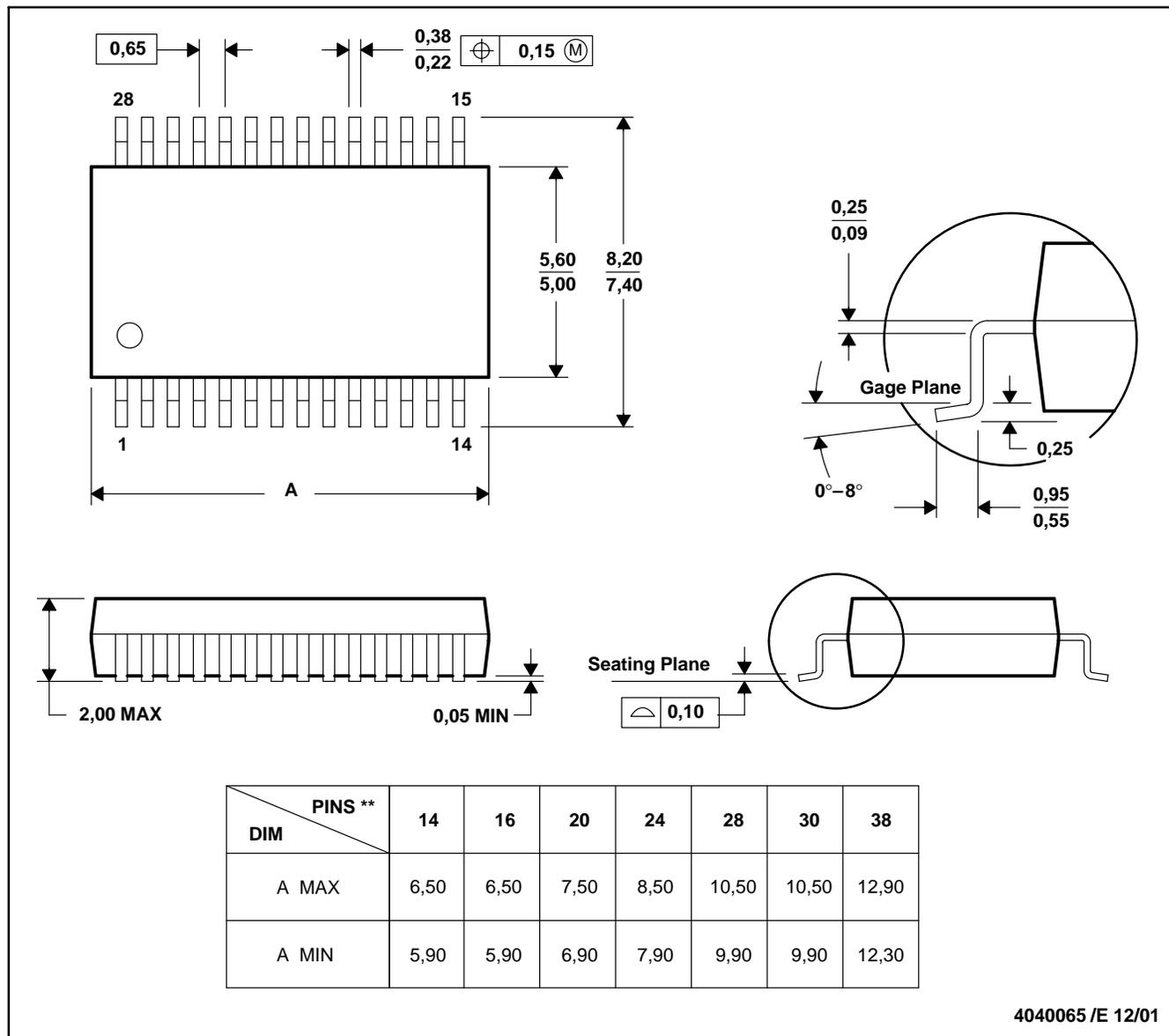
0,38 / 0,22　⊕　**0,15** Ⓜ

0,25 / 0,09

Gage Plane

0,25

0°–8°

0,95 / 0,55

5,60 / 5,00　**8,20 / 7,40**

A

2,00 MAX　　**0,05 MIN**

Seating Plane

△ **0,10**

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:　A.　All linear dimensions are in millimeters.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　D.　Falls within JEDEC MO-150

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

MECHANICAL DATA

PW (R-PDSO-G**) **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
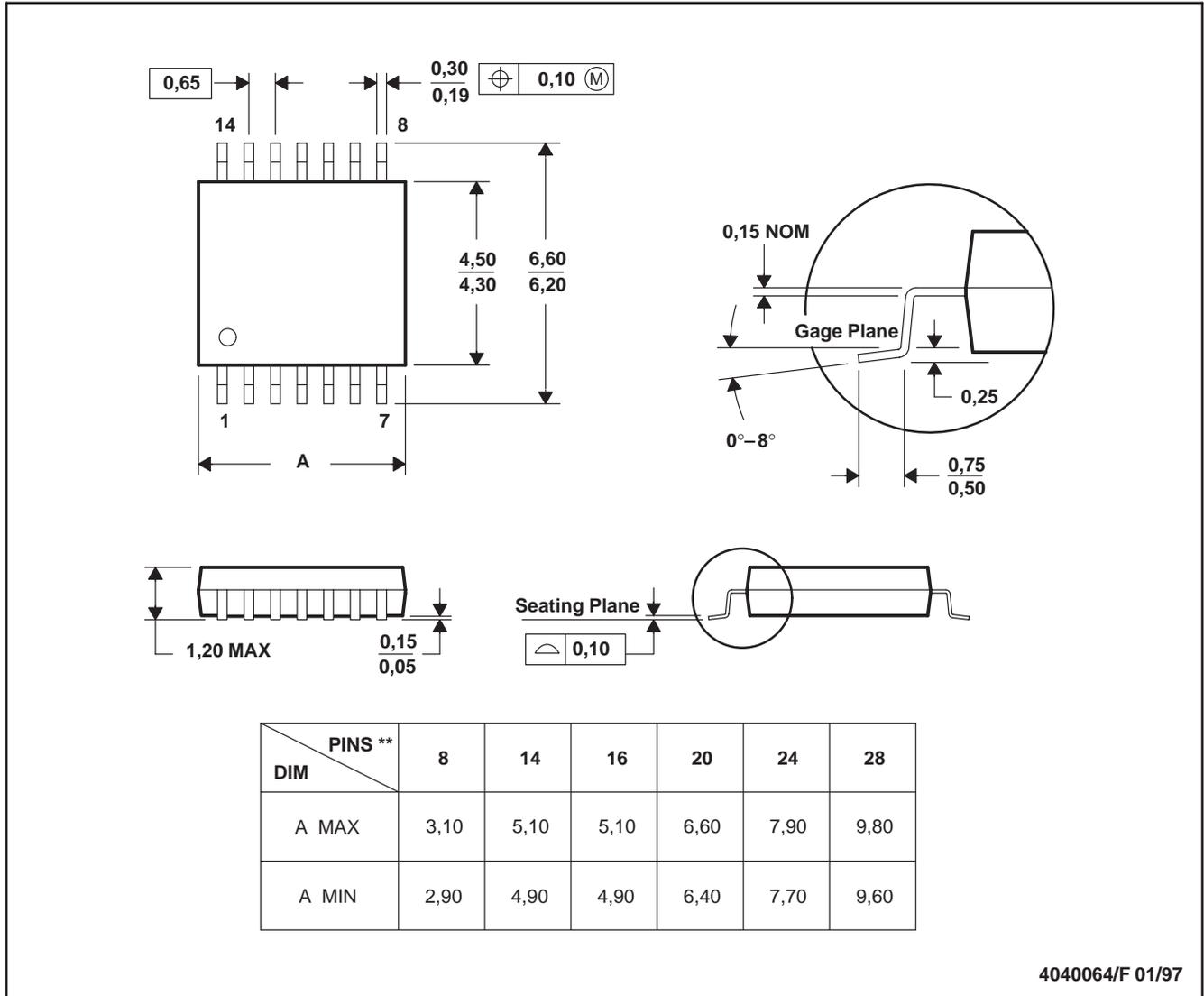
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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