

## CLC111

# Ultra High Slew Rate, Closed Loop Buffer

### General Description

The CLC111 is a high performance, closed loop, monolithic buffer designed for applications requiring very high frequency signals. The CLC111's high performance includes an extremely fast 800MHz small signal bandwidth (0.5<sub>pp</sub>) and an ultra high (3500V/μs) slew rate while requiring only 10.5mA quiescent current. Signal fidelity is maintained with low harmonic distortion (-62dBc 2nd and 3rd harmonics at 20MHz). These performance characteristics are for a demanding 100Ω load.

Featuring a patented closed loop design, the CLC111 offers nearly ideal unity gain (0.996) with a very low (1.4Ω) output impedance. The CLC111 is ideally suited for buffering video signals with its 0.15%/0.04° differential gain and phase performance at 4.43MHz. Power sensitive applications will benefit from the CLC111's excellent performance on reduced or single supply voltages.

Constructed using an advanced, complementary bipolar process and National's proven high performance architectures, the CLC111 is available in several versions to meet a variety of requirements.

#### Enhanced Solutions (Military/Aerospace)

SMD Number: contact factory

Space level versions also available.

For more information, visit <http://www.national.com/mil>

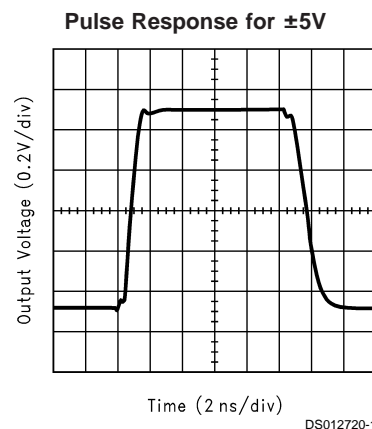
### Features

- Very wideband (800MHz)
- Ultra high (3500V/μs) slew rate

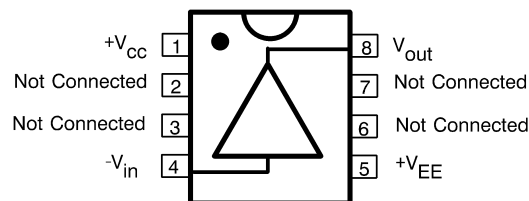
- Very low output impedance (1.4Ω)
- Low (-62dBc) 2nd/3rd harmonics @ 20MHz
- 60mA output current (±5 supplies)
- Single supply operation (0 to 3V supply min.)
- Evaluation boards and Spice models

### Applications

- Video switch buffers
- Test point drivers
- High frequency active filters
- Wideband DC clamping buffer
- High-speed peak detector circuits



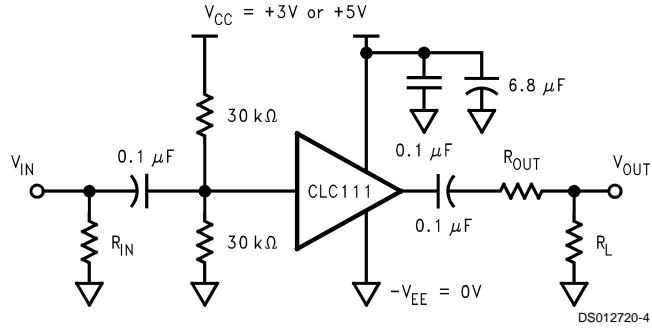
### Connection Diagram



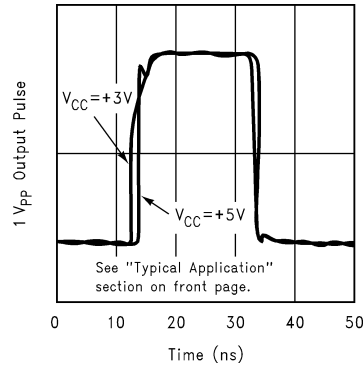
**Pinout  
DIP & SOIC**

DS012720-2

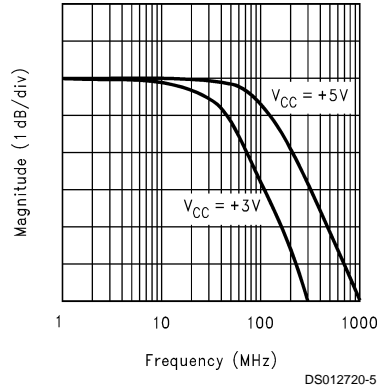
## Typical Application



Single-Supply Circuit



Pulse Response



Small Signal Bandwidth

## Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	-40°C to +85°C	CLC111AJP	CLC111AJP	N08E
8-pin plastic SOIC	-40°C to +85°C	CLC111AJE	CLC111AJE	M08A

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	$\pm 7.0V$
$I_{OUT}$	80mA
Output is short circuit protected to ground, but maximum reliability will be maintained if $I_{OUT}$ does not exceed...	
Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature Range	+150°C

Operating Temperature Range	40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec
ESD rating	1000V

**Operating Ratings**

Thermal Resistance			
Package	( $\theta_{JC}$ )	( $\theta_{JA}$ )	
MDIP	70°C/W	125°C/W	
SOIC	65°C/W	145°C/W	

**Electrical Characteristics**

$\pm V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC111AJ	+25°C	-40°C	+25°C	+85°C	
<b>Frequency Domain Response</b>							
SSBW	Small Signal Bandwidth	$V_{OUT} < 0.5V_{PP}$	800	400	400	300	MHz
LSBW	Small Signal Bandwidth	$V_{OUT} < 4.0V_{PP}$	450	250	250	200	MHz
	Gain Flatness	$V_{OUT} < 0.5V_{PP}$					
GFL	Flatness	DC-50MHz	0.02	$\pm 0.1$	$\pm 0.1$	$\pm 0.2$	dB
GFPH	Peaking	DC-200MHz	0.1	1.0	0.5	0.5	dB
GFRH	Rolloff	DC-200MHz	0.1	0.8	0.8	1.2	dB
DG	Differential Gain	$R_L = 150\Omega$ , 4.43MHz,	0.15	0.4	0.25	0.25	%
DP	Differential Phase	$R_L = 150\Omega$ , 4.43MHz	0.04	0.08	0.08	0.08	deg
<b>Time Domain Response</b>							
TRS	Rise and Fall Time	0.5V step	0.6	0.8	0.8	1.1	ns
TRL		4.0V step	1.0	1.4	1.4	1.7	ns
TS	Settling Time to $\pm 0.1\%$	2.0V Step	16	20	20	20	ns
OS1	Overshoot	4V Step	0	8	5	5	%
SR	Slew Rate	4V Step	3500	2700	2700	2300	V/ $\mu$ sec
<b>Distortion And Noise Performance</b>							
HD2	2nd Harmonic Distortion	$2V_{PP}$ , 20MHz	-62	-47	-50	-50	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$ , 20MHz	-62	-55	-55	-52	dBc
	Equivalent Output Noise						
VN	Voltage	>1MHz	4.0	4.8	4.8	5.3	nV/ $\sqrt{Hz}$
ICN	Current	>1MHz	1.6	4.0	3.0	3.0	pA/ $\sqrt{Hz}$
<b>Static, DC Performance</b>							
GA1	Small Signal Gain	No Load	0.996	0.994	0.994	0.992	V/V
GA2	Small Signal Gain	100 $\Omega$ Load	.98	.96	.97	.97	V/V
RO	Output Resistance	DC	1.4	3.0	2.0	2.0	$\Omega$
VIO	Output Offset Voltage (Note 3)		2	17	9	9	mV
DVIO	Average Temperature Coefficient		$\pm 30$	$\pm 100$	-	$\pm 50$	$\mu V/^\circ C$
IBN	Input Bias Current (Note 3)		5	30	15	15	$\mu A$
DIBN	Average Temperature Coefficient		50	$\pm 187$	-	$\pm 100$	nA/ $^\circ C$
PSRR	Power Supply Rejection Ratio		-52	-48	-48	-46	dB

**Electrical Characteristics** (Continued) $\pm V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
<b>Static, DC Performance</b>							
ICC	Supply Current (Note 3)	No Load	10.5	12	12	12	mA
<b>Miscellaneous Performance</b>							
ILIN	Integral Endpoint Linearity	$\pm 2V$ , Full Scale	0.2	1.0	0.5	0.5	%
RIN	Input Resistance		1	0.3	0.7	1	M $\Omega$
CIN	Input Capacitance	CERDIP	2.5	3.5	3.5	3.5	pF
CIN	Input Capacitance	Plastic DIP	1.25	2.0	2.0	2.0	pF
VO	Output Voltage Range	No Load	3.9	3.5	3.6	3.6	V
VOL	Output Voltage Range	$R_L = 100\Omega$	3.5	+3.1,-2.5	3.2	3.2	V
VOL	Output Voltage Range	$R_L = 100\Omega$ , 0°C		$\pm 3.1$			V
IO	Output Current		60	50,25	50	40	mA
IO	Output Current	0°-70°C		50,35	50	50	mA

**Electrical Characteristics** $V_{CC} = +3V$  or  $V_{CC} = +5V$ ,  $-V_{EE} = 0V$ ,  $T_A = +25^\circ C$ ,  $R_L = 100\Omega$ ; unless specified

Symbol	Parameter	Conditions	$V_{CC} = 3V$	$V_{CC} = 5V$	Units
<b>Frequency Domain Response</b>					
SSBW	-3dB Bandwidth	$V_{OUT} < 0.5V_{PP}$	120	300	MHz
LSBW	-3dB Bandwidth	$V_{OUT} < 2.0V_{PP}$		210	MHz
	Gain Flatness	$V_{OUT} < 0.5V_{PP}$			
GFL	Flatness	DC-30MHz	0.5	0.1	dB
GFPH	Peaking	DC-200MHz	0	0	dB
GFRH	Rolloff	DC-60MHz	1.5	0.25	dB
<b>Time Domain Response</b>					
TRS	Rise and Fall Time	0.5V step	3.9	1.2	ns
TRL	Rise and Fall Time	2.0V step		1.5	ns
OS1	Overshoot	1.0V step	3	3	%
SR	Slew Rate	0.5V step	260	425	V/ $\mu$ sec
<b>Distortion And Noise Performance</b>					
HD2	2nd Harmonic Distortion	0.5V <sub>PP</sub> , 20MHz	-46		dBc
		1.0V <sub>PP</sub> , 20MHz		-55	
HD3	3rd Harmonic Distortion	0.5V <sub>PP</sub> , 20MHz	-44		dBc
		1.0V <sub>PP</sub> , 20MHz		-64	
<b>Static, DC Performance</b>					
GA1	Small Signal Gain	AC coupled	0.96	0.97	V/V
		$R_L = \infty$	2.0	4.5	mA
<b>Miscellaneous Performance</b>					
VO	Output Voltage Range	$R_L = \infty$	1.5	3.4	V <sub>PP</sub>
VOL	Output Voltage Range	$R_L = 100\Omega$	1.1	2.6	V <sub>PP</sub>

## Electrical Characteristics (Continued)

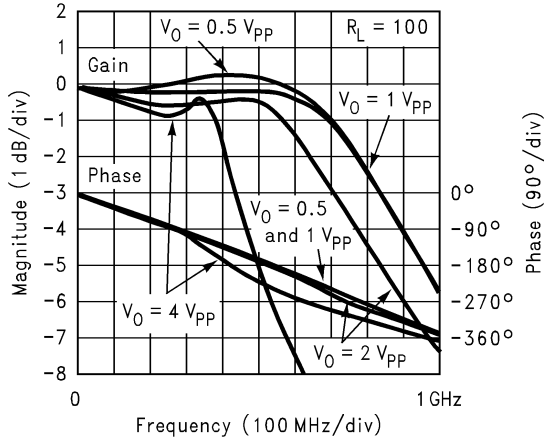
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

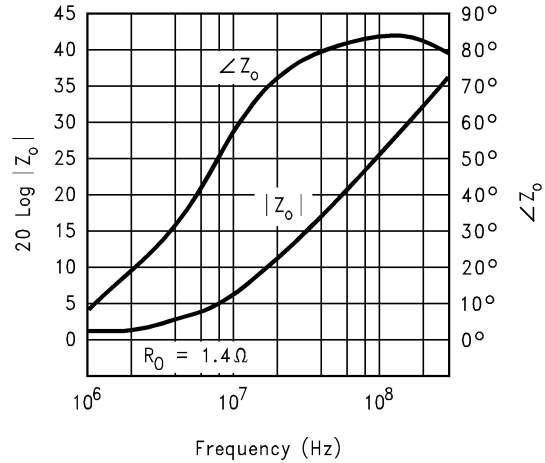
**Note 3:** AJ-level: spec. is 100% tested at +25°C.

## Typical Performance Characteristics

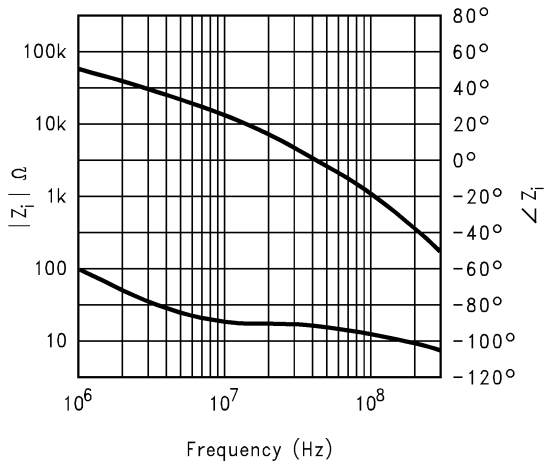
### Frequency Response vs. Output Swing



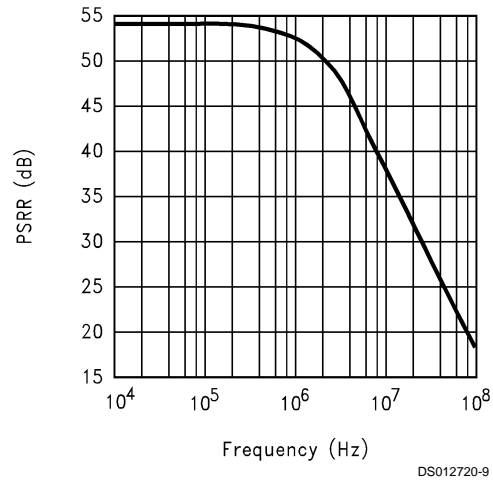
### Output Impedance



### Input Impedance

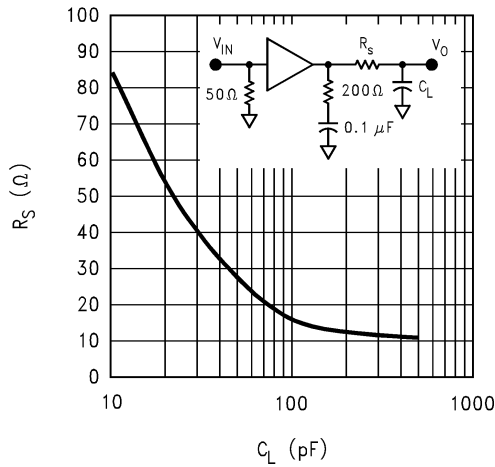


### PSRR

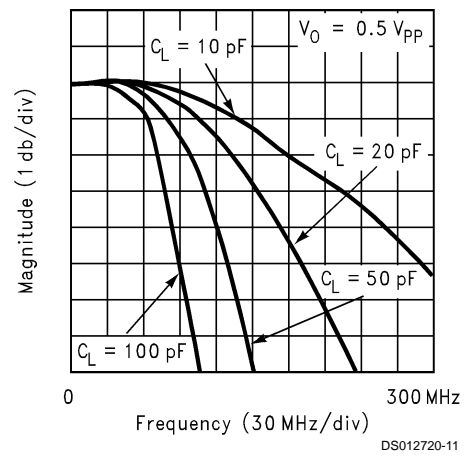


# Typical Performance Characteristics (Continued)

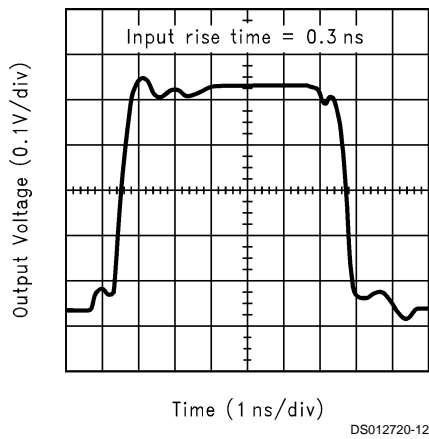
Recommended  $R_S$  vs. Load Capacitance



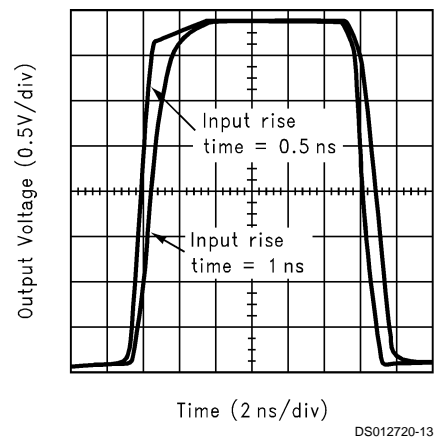
Gain vs.  $C_L$  with Recommended  $R_S$



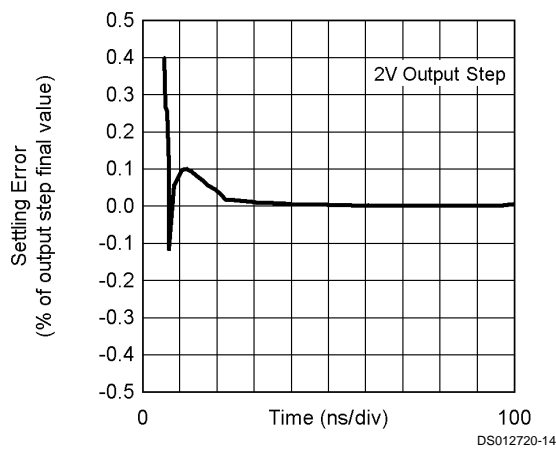
Small Signal Pulse Response



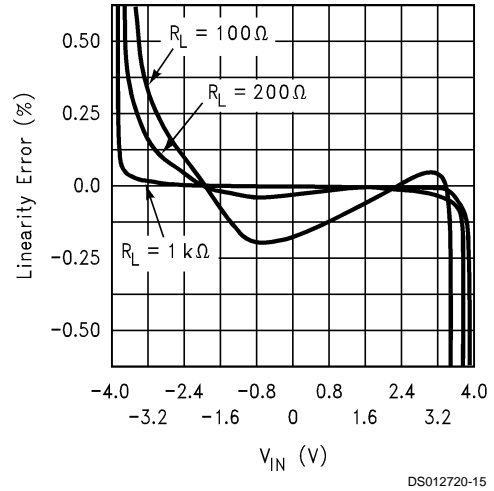
Large Signal Pulse Response



Short-Term Settling Time

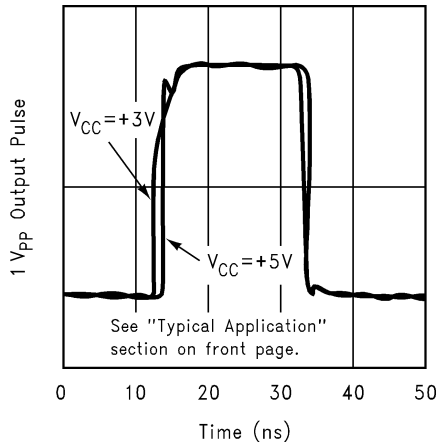


Integral Linearity Error

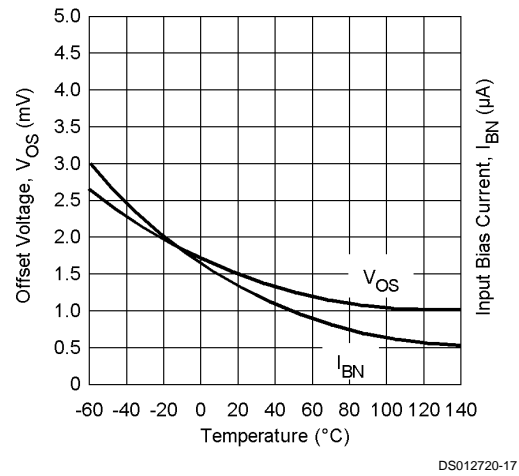


# Typical Performance Characteristics (Continued)

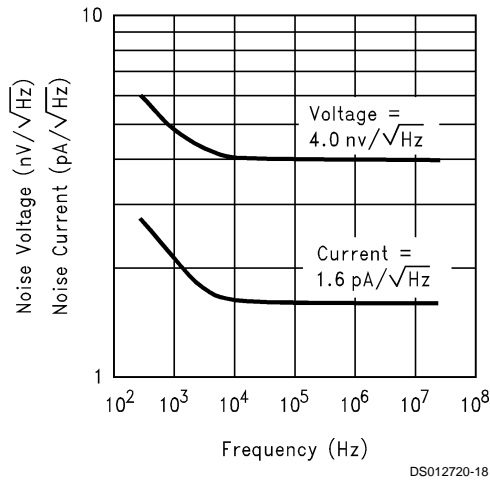
## Pulse Response



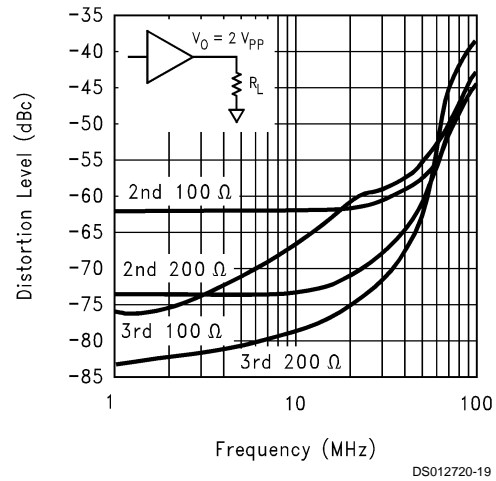
## Typical D.C. Errors vs. Temperature



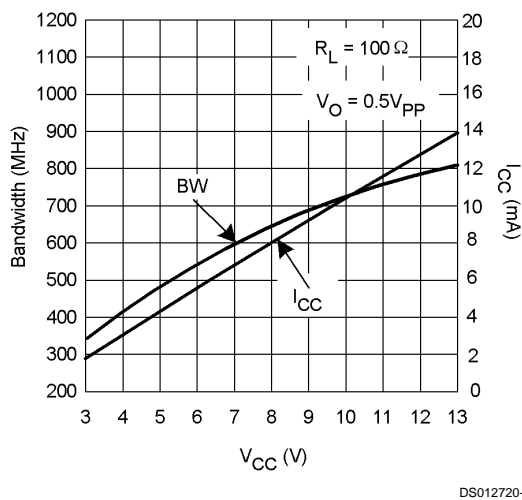
## Equivalent Input Noise



## 2nd and 3rd Harmonic Distortion



## Bandwidth and I<sub>CC</sub> vs. V<sub>CC</sub> (Single Supply)



## Application Division

### Operation

the CLC111 is a low-power, very high speed unity gain buffer. It uses a closed loop topology which allows for accuracy not usually found in high speed open loop buffers. A slew enhanced front end allows for low quiescent power while not sacrificing AC performance.

### Single Supply Operation

Although the CLC111 is specified to operate from split  $\pm 5V$  power supplies, there is no internal ground reference that prevents operation from a single voltage power supply. For single supply operation, the input signal should be biased at a DC value of  $1/2V_{CC}$ . This can be accomplished by AC coupling and rebiasing, as shown in *Figure 1*.

The above electrical specifications provide typical performance specifications for the CLC111 at 25° C while operating from a single +3V or a single +5V power supply.

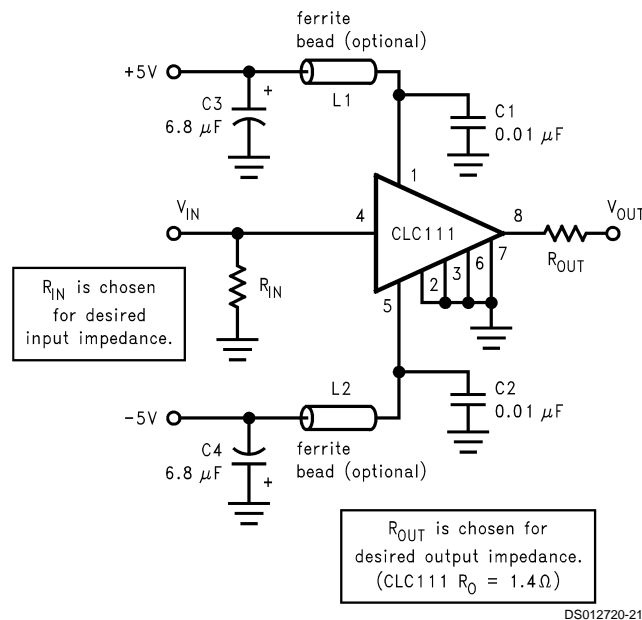
### Printed Circuit Layout and Supply Bypassing

As with any high frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC111.

To minimize capacitive feedthrough, pins 2, 3, 6, and 7 should be connected to the ground plane, as shown in *Figure 1*. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC111. On a 0.065 inch epoxy PCB material, a 50 transmission line (commonly called stripline) can be constructed by using a trace width of 0.01" over a complete ground plane.

*Figure 1* shows recommended power supply bypassing.

The ferrite beads are optional and are recommended only where additional isolation is needed from high frequency (>400MHz) resonances in the power supply.



**FIGURE 1. Recommended Circuit & Evaluation Board Schematic**

Parasitic or load capacitance directly on the output of the CLC111 will introduce additional phase shift in the device. This phase shift can decrease phase margin and increase frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs in this data sheet illustrate the required resistor value and the resulting performance vs. capacitance.

Precision buffered resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard

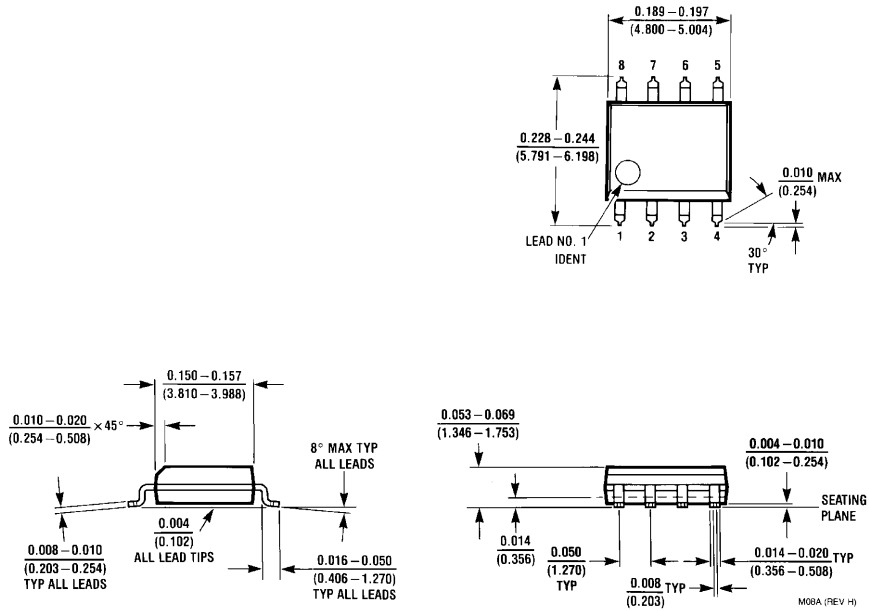
spirally-trimmed RN55D metal film resistors will work, though they will cause a slight degradation of AC performance due to their reactive nature at high frequencies.

### Evaluation Boards

Evaluation boards are available from National as part numbers CLC730012 (DIP) and CLC730045 (SOIC). This board was used in the characterization of the device and provides optimal performance. Designers are encouraged to copy these printed circuit board layouts for their applications.

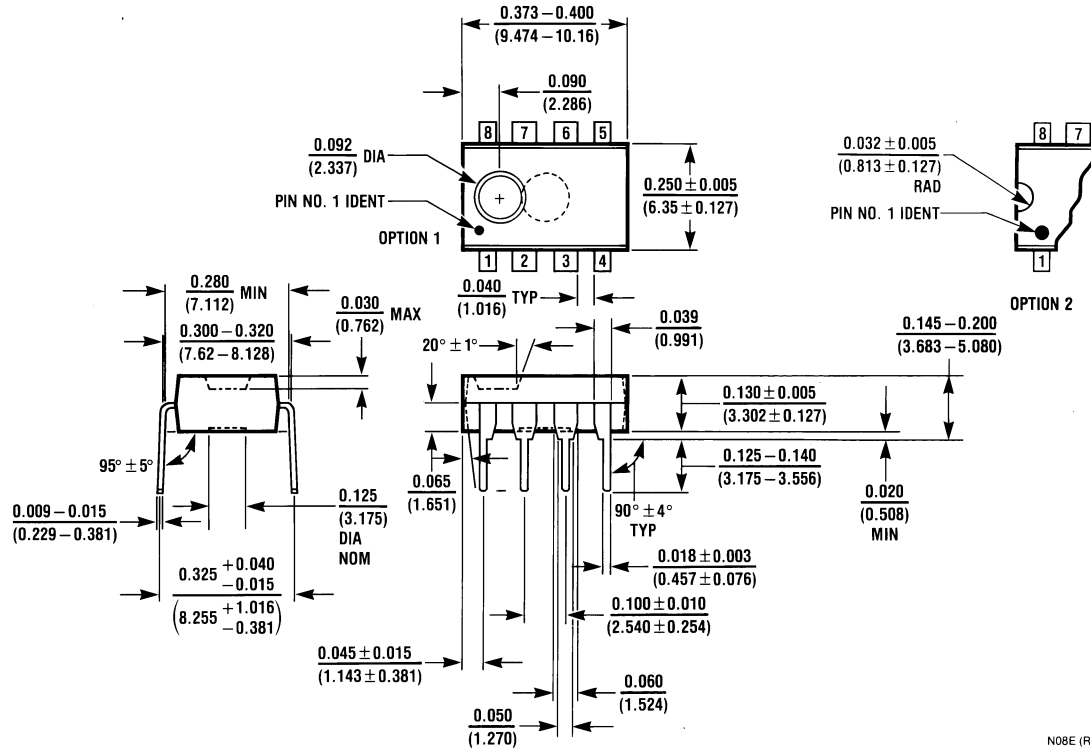


**Physical Dimensions** inches (millimeters) unless otherwise noted



**8-Pin SOIC  
NS Package Number M08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**8-Pin MDIP  
NS Package Number N08E**

N08E (REV F)

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