SBAS017C – NOVEMBER 1996 – REVISED OCTOBER 2006

16-Bit 10μs Serial CMOS Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

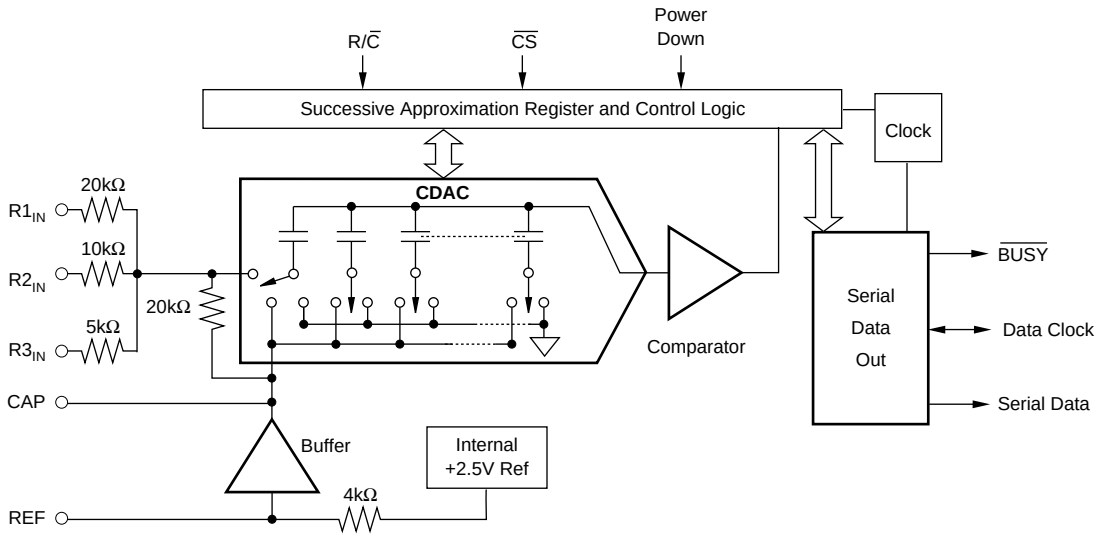
- **100kHz SAMPLING RATE**
- **86dB SINAD WITH 20kHz INPUT**
- **±2LSB INL**
- **DNL: 16 Bits No Missing Codes**
- **SIX SPECIFIED INPUT RANGES**
- **SERIAL OUTPUT**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 12-BIT ADS7808**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **100mW MAX POWER DISSIPATION**
- **0.3" SO-20**
- **SIMPLE DSP INTERFACE**

DESCRIPTION

The ADS7809 is a complete 16-bit sampling Analog-to-Digital (A/D) converter using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based Successive Approximation Register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be outputted using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and specified over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ±10V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The ADS7809 is available in a 0.3" SO-20, and is fully specified for operation over the industrial –40°C to +85°C range.



ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
$R3_{IN}$	±25V
REF	V_{ANA} + 0.3V to AGND2 – 0.3V
CAP	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} + 0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7809U	±3	15	83	SO-20	DW	–40°C to +85°C	ADS7809U	ADS7809U	Rail, 38
"	"	"	"	"	"	"	"	ADS7809U/1K	Tape and Reel, 1000
ADS7809UB	±2	16	86	"	"	"	ADS7809UB	ADS7809UB	Rail, 38
"	"	"	"	"	"	"	"	ADS7809UB/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors (see Figure 4), unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U MIN	ADS7809U TYP	ADS7809U MAX	ADS7809UB MIN	ADS7809UB TYP	ADS7809UB MAX	UNITS
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			±10, 0V to 5V, etc. (See Table I)					
Impedance			See Table I					
Capacitance			35			*		pF
THROUGHPUT SPEED								
Complete Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±3			±2	LSB[1]
Differential Linearity Error				+3, –2			±1	LSB
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full-Scale Error[3,4]				±0.5			*	%
Full-Scale Error Drift			±7			*		ppm/°C
Full-Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			*	%
Full-Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]	Bipolar Ranges			±10			*	mV
Bipolar Zero Error Drift	Bipolar Ranges		±2			*		ppm/°C
Unipolar Zero Error[3]	0V to 10V Ranges			±5			*	mV
Unipolar Zero Error[3]	0V to 4V, 0V to 5V Ranges			±3			*	mV
Unipolar Zero Error Drift	Unipolar Ranges		±2			*		ppm/°C
Recovery to Rated Accuracy after Power-Down	1µF Capacitor to CAP		1			*		ms
Power-Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90	100		96	*		dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz		–100	–90		*	–94	dB
Signal-to-(Noise + Distortion)	f_{IN} = 20kHz	83	88		86	*		dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 20kHz	83	88		86	*		dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage	No Load	2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer)			1			*		µA
External Reference Voltage Range For Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}[8]		+2.0		V_D + 0.3V	*		*	V
I_{IL}	V_{IL} = 0V			±10			*	µA
I_{IH}	V_{IH} = 5V			±10			*	µA

ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = –40°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U			ADS7809UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL OUTPUTS								
Data Format				Serial 16 bits				
Data Co				Binary Two's Complement or Straight Binary				
Pipeline Delay				Conversion results only available after completed conversion.				
Data Clock				Selectable for internal or external data clock				
Internal	EXT/$\overline{INT}$ LOW		2.3			*		MHz
(Output Only When Transmitting Data)								
External	EXT/$\overline{INT}$ HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			*	pF
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation: PWRD LOW	V_{ANA} = V_{DIG} = 5V, f_S = 100kHz			100			*	mW
PWRD HIGH			50			*		µW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
SO			75			*		°C/W

* Same as specification for ADS7809U.

NOTES: (1) LSB means Least Significant Bit. For the ±10V input range, one LSB is 305µV.

(2) Typical rms noise at worst case transitions and temperatures.

(3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

(4) For bipolar input ranges, full-scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

(5) All specifications in dB are referred to a full-scale ±10V input.

(6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB.

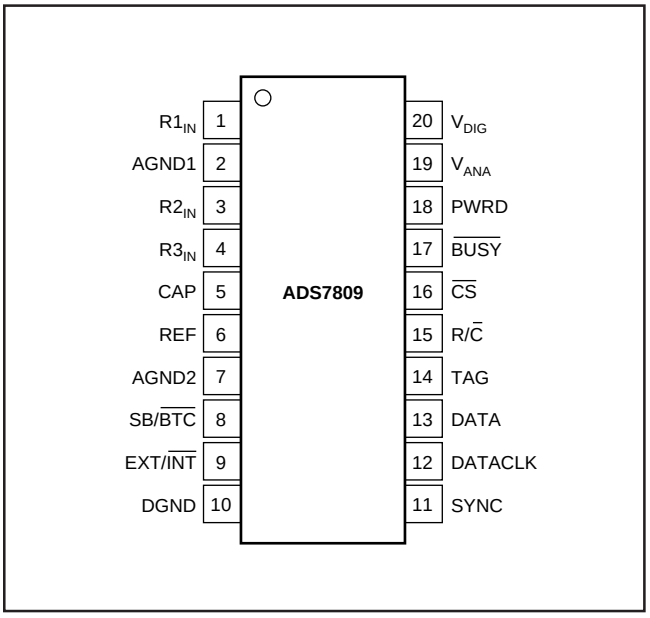
(7) Recovers to specified performance after 2 • FS input overvoltage.

(8) The minimum V_{IH} level for the DATACLK signal is 3V.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	$R1_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	$R2_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
4	$R3_{IN}$	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2µF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2µF Tantalum capacitor.
7	AGND2	Analog Ground
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground
11	SYNC	Synch Output. If EXT/$\overline{INT}$ is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/$\overline{BTC}$. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH (see Figure 3). If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. See Figure 3.
15	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{CS}$	Chip Select. Internally OR'ed with R/$\overline{C}$.
17	$\overline{BUSY}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V_{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
20	V_{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V_{ANA}.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	CONNECT $R3_{IN}$ TO	IMPEDANCE
±10V	V_{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V_{IN}	CAP	13.3kΩ
±3.33V	V_{IN}	V_{IN}	CAP	10.7kΩ
0V to 10V	AGND	V_{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V_{IN}	10.0kΩ
0V to 4V	V_{IN}	AGND	V_{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

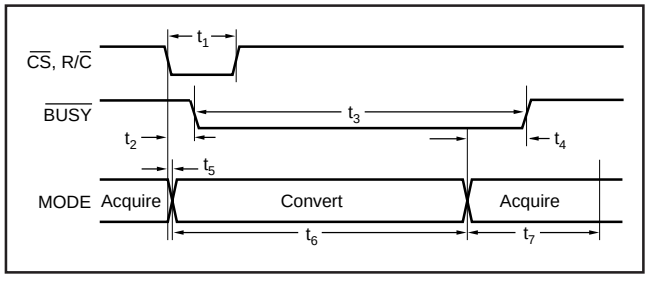


FIGURE 1. Basic Conversion Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	$\overline{BUSY}$ Delay			65	ns
t_3	$\overline{BUSY}$ LOW			8	µs
t_4	$\overline{BUSY}$ Delay After End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		7.6	8	µs
t_7	Acquisition Time			2	µs
$t_6 + t_7$	Throughput Time		9	10	µs
t_8	R/$\overline{C}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid After DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		t_{12} + 5	ns
t_{16}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{CS}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{CS}$ LOW	6			µs

TABLE II. Conversion and Data Timing. T_A = –40°C to +85°C.

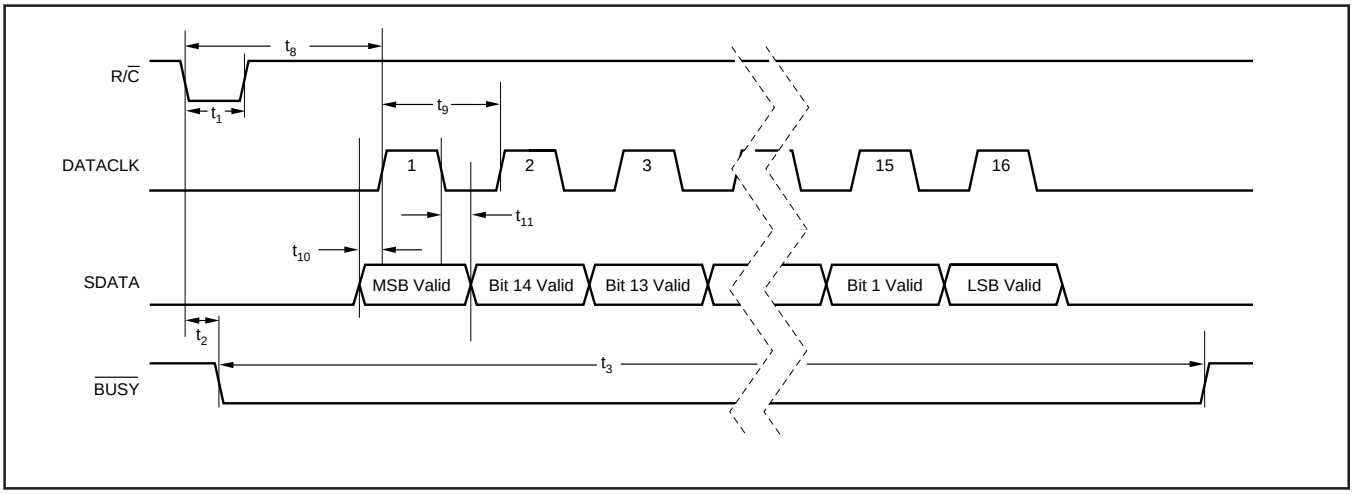


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{CS}$, EXT/$\overline{INT}$ and TAG Tied LOW.)

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1 > 0	0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n – 1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	Initiates conversion “n”. Data from conversion “n – 1” clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1 > 0	0	1	1	Input	0	x	Initiates conversion “n”.
	0	1 > 0	1	1	Input	0	x	Initiates conversion “n”.
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion “n” clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion “n – 1” clocked out synchronized to external DATACLK.(1) Conversion “n” in process.
	0	0 > 1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion “n – 1” clocked out synchronized to external DATACLK .(1) Conversion “n” in process.
Incorrect Conversions	0	0	0 > 1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power-Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two’s Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO’S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE IV. Output Codes and Ideal Input Voltages.

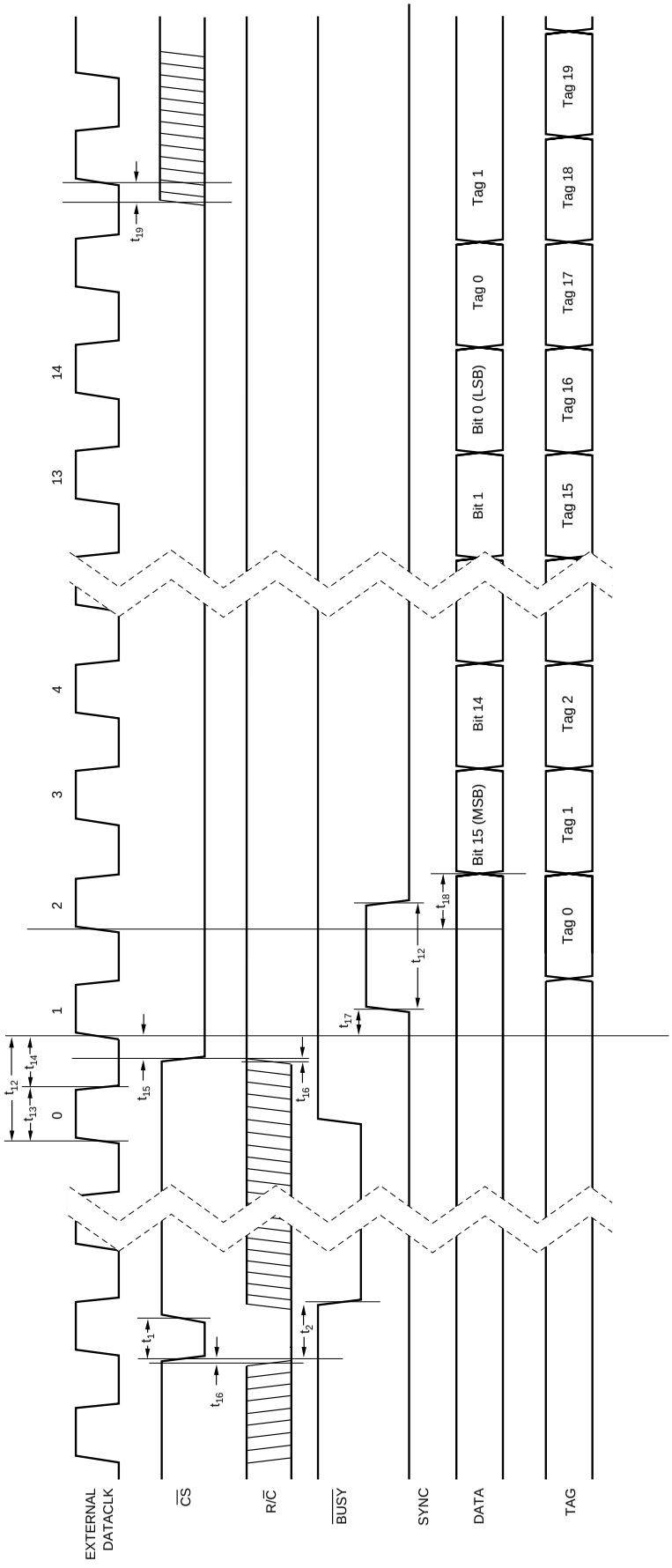


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied High.) Read After Conversion.

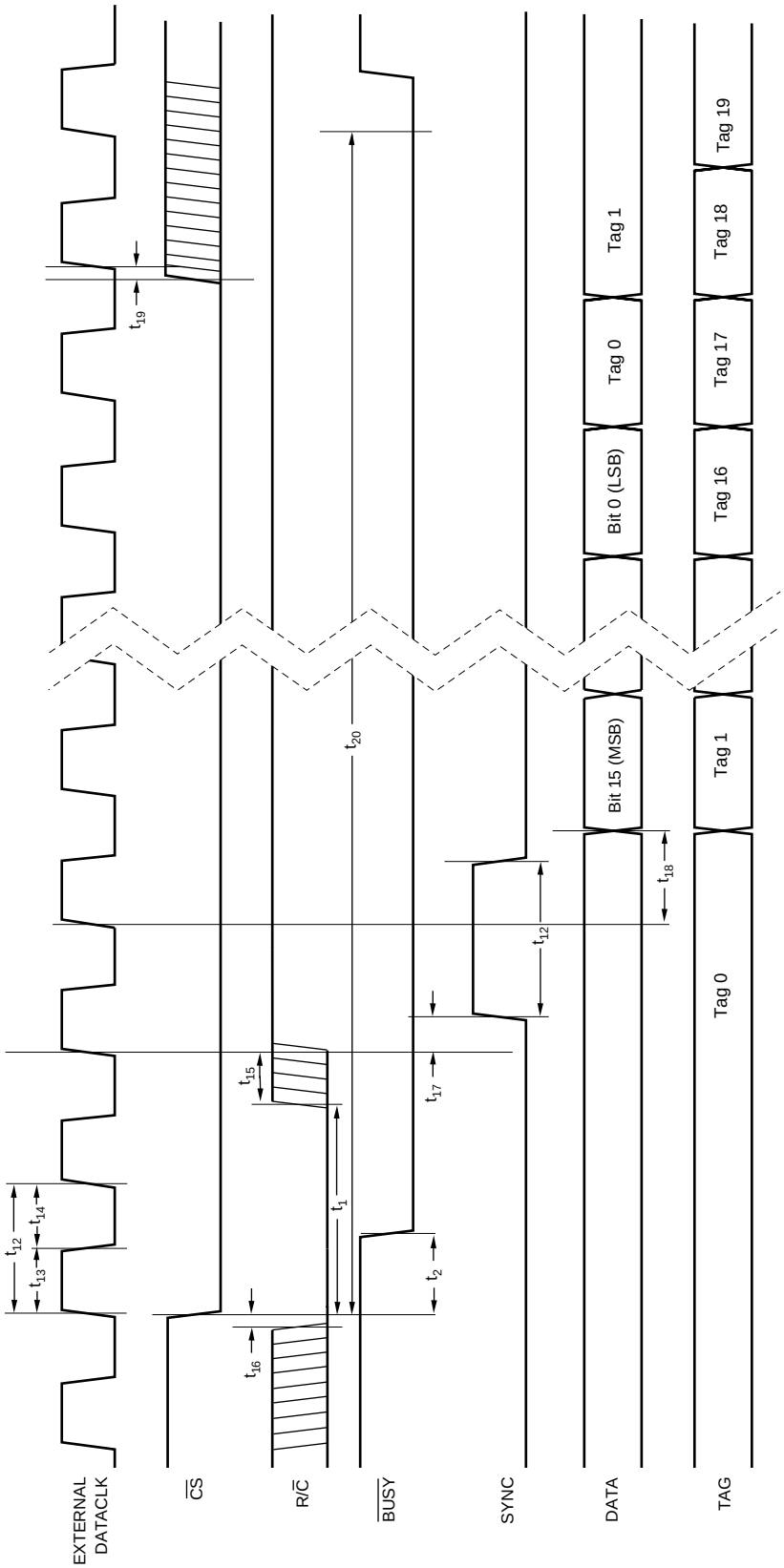


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/$\overline{INT}$ Tied High.) Read During Conversion (Previous Conversion Results).

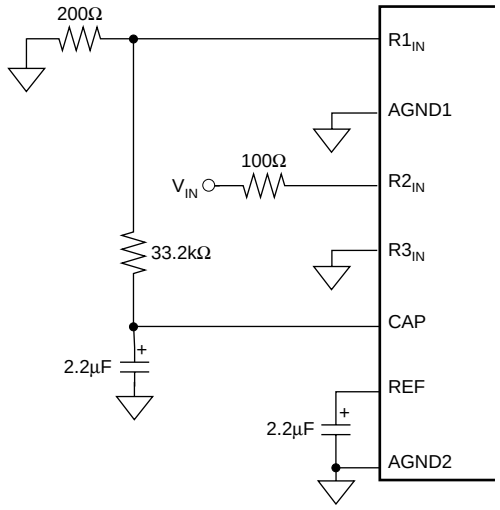
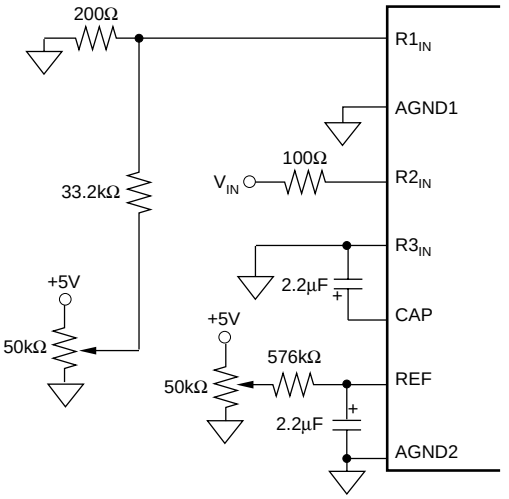
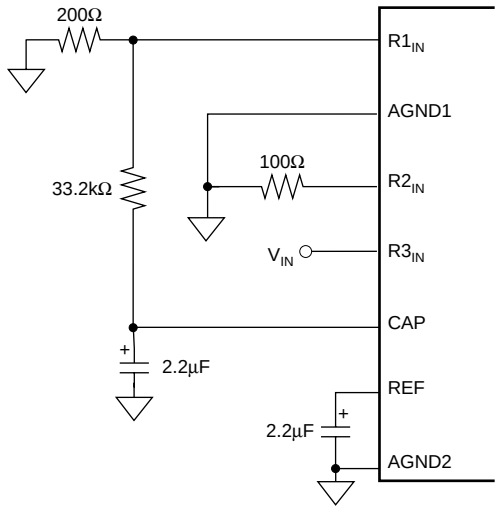
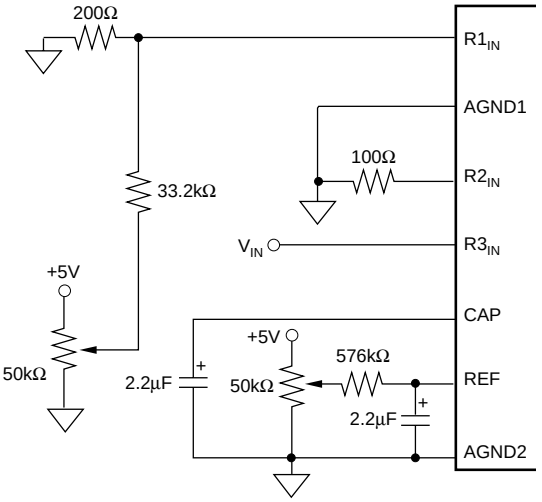
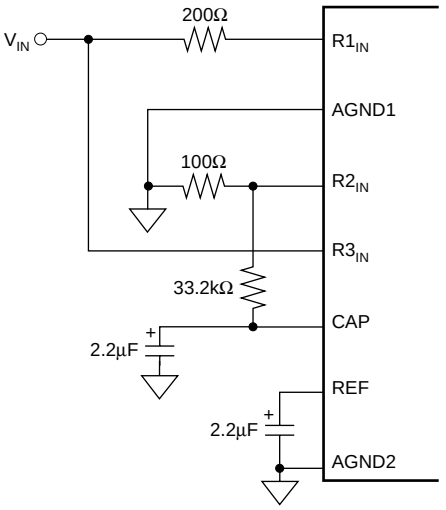
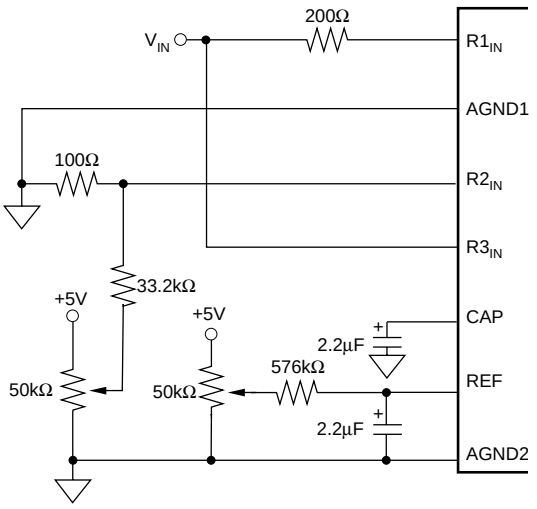
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V-10V		
0V-5V		
0V-4V		

FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

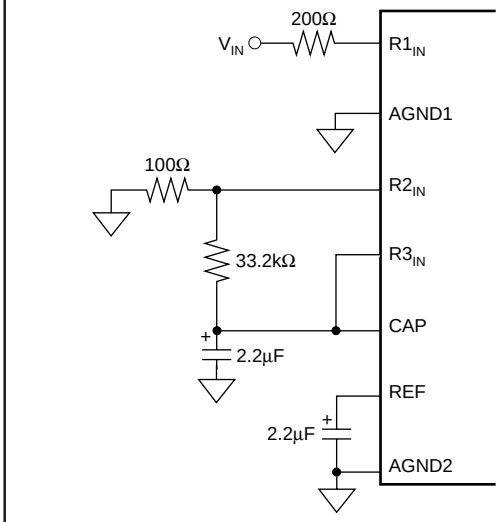
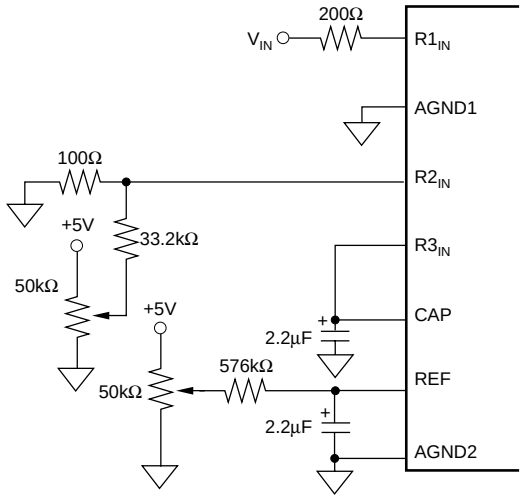
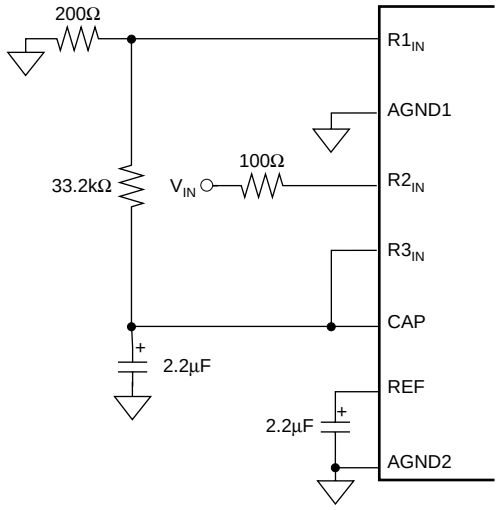
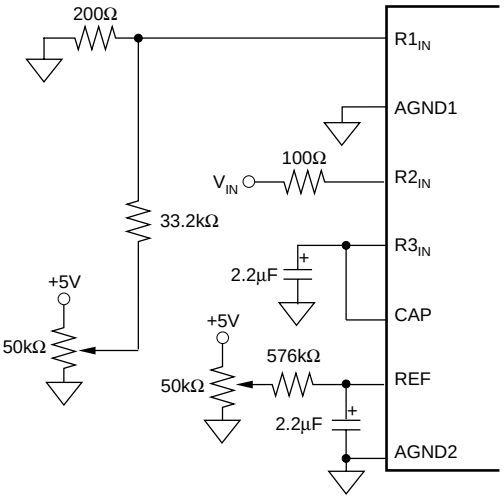
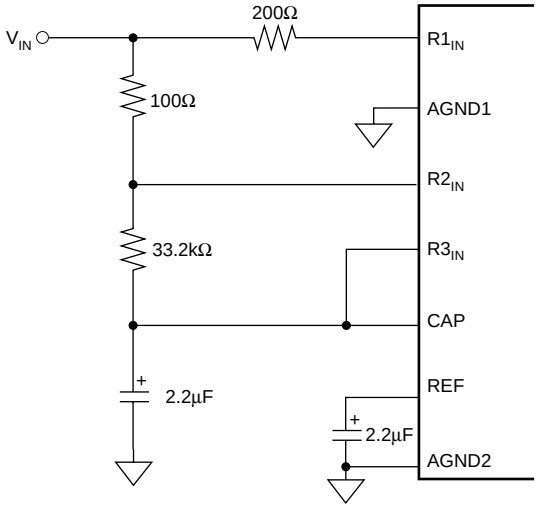
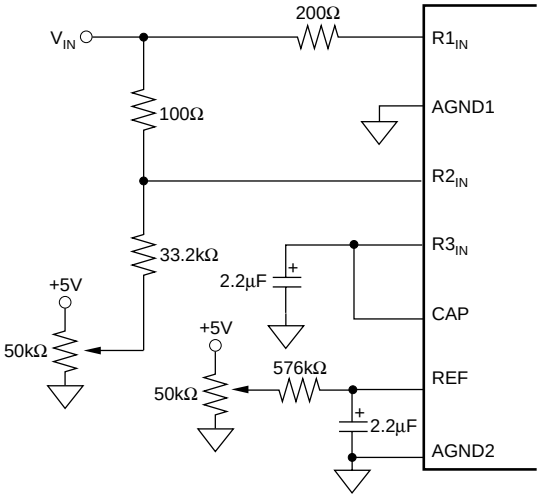
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
± 5V		
±3.3V		

FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/06	C	3	Absolute Maximum Ratings	CAP and REF were switched.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7809U	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809U/1K	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809U/1KE4	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809UB	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U B	Samples
ADS7809UB/1K	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U B	Samples
ADS7809UE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

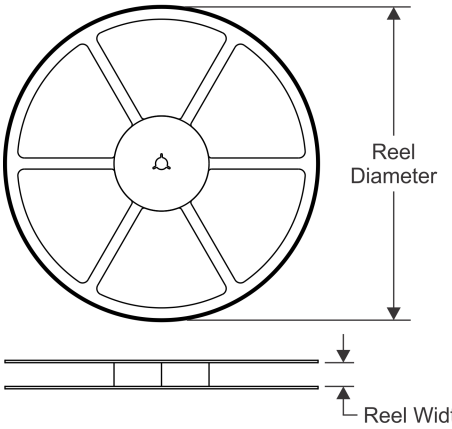
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

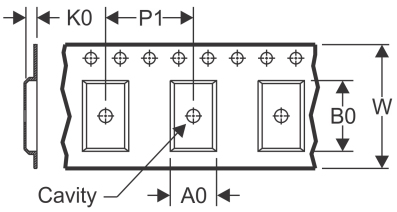
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

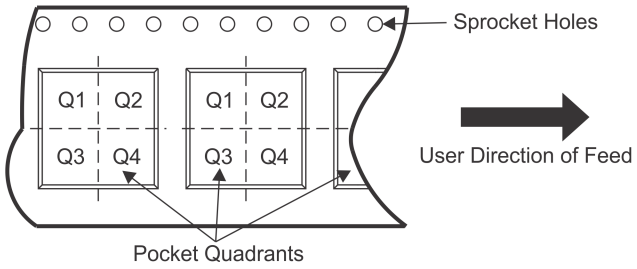


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

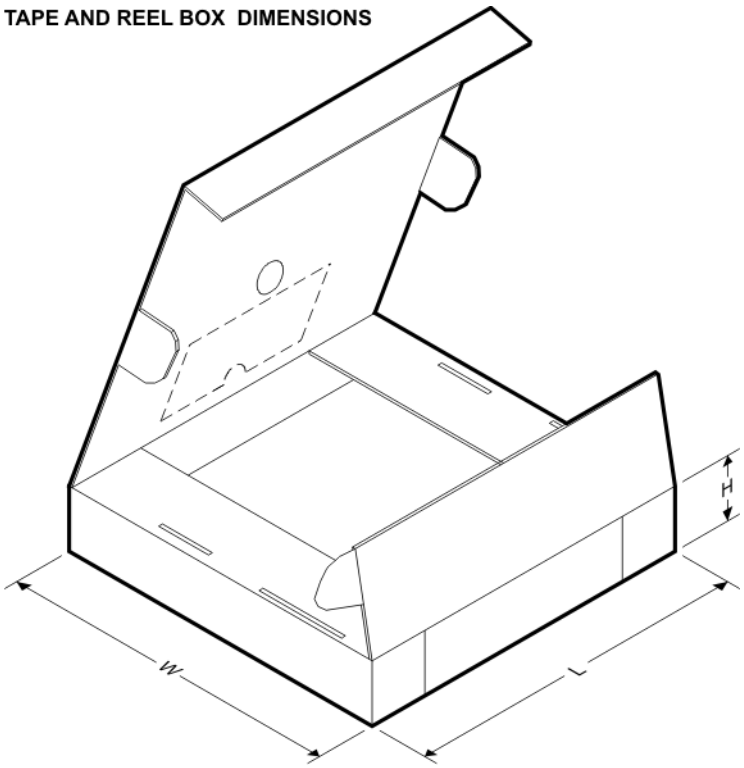
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

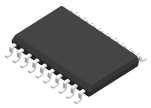
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7809U/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
ADS7809UB/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7809U/1K	SOIC	DW	20	1000	367.0	367.0	45.0
ADS7809UB/1K	SOIC	DW	20	1000	367.0	367.0	45.0

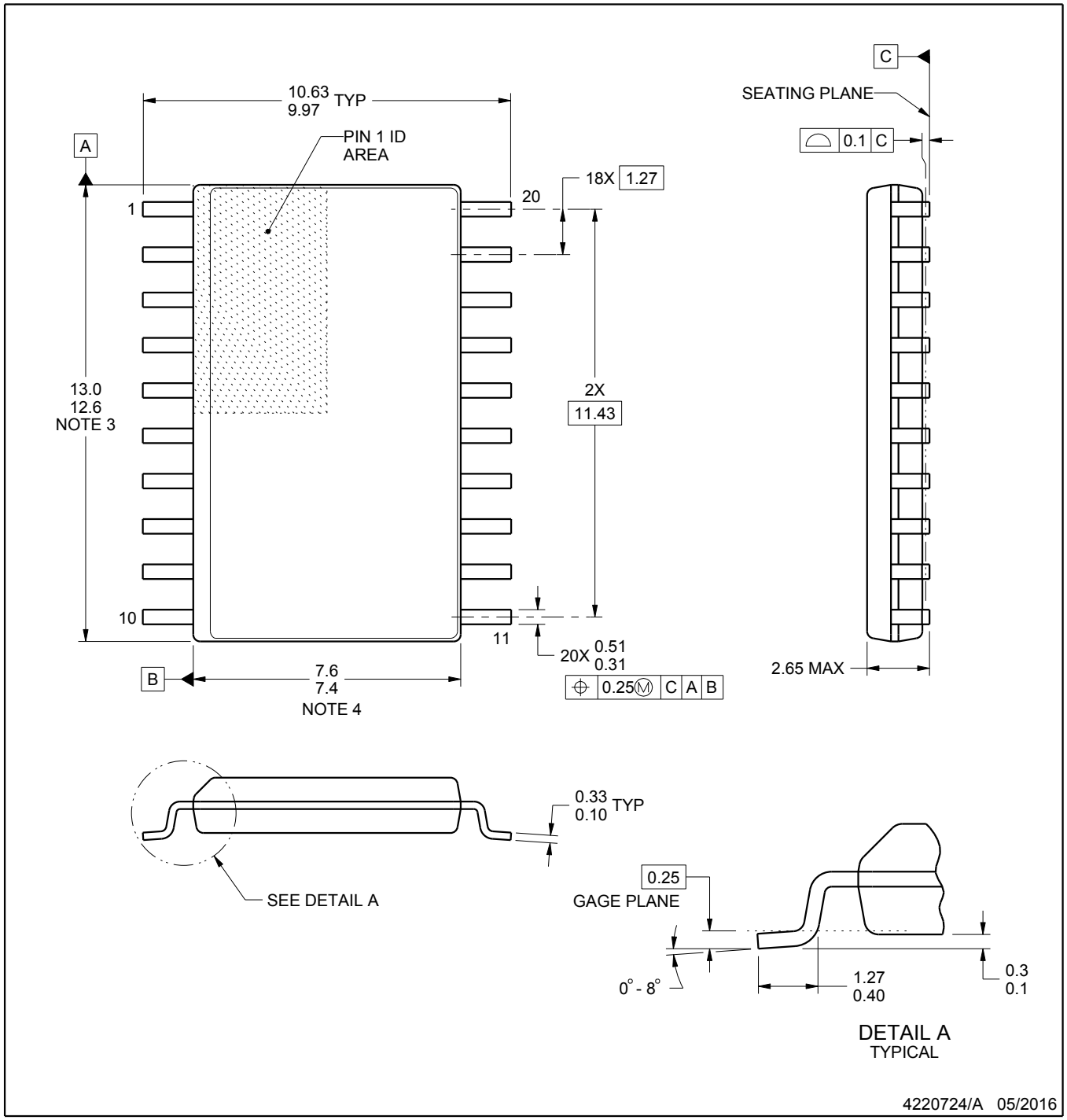


PACKAGE OUTLINE

DW0020A

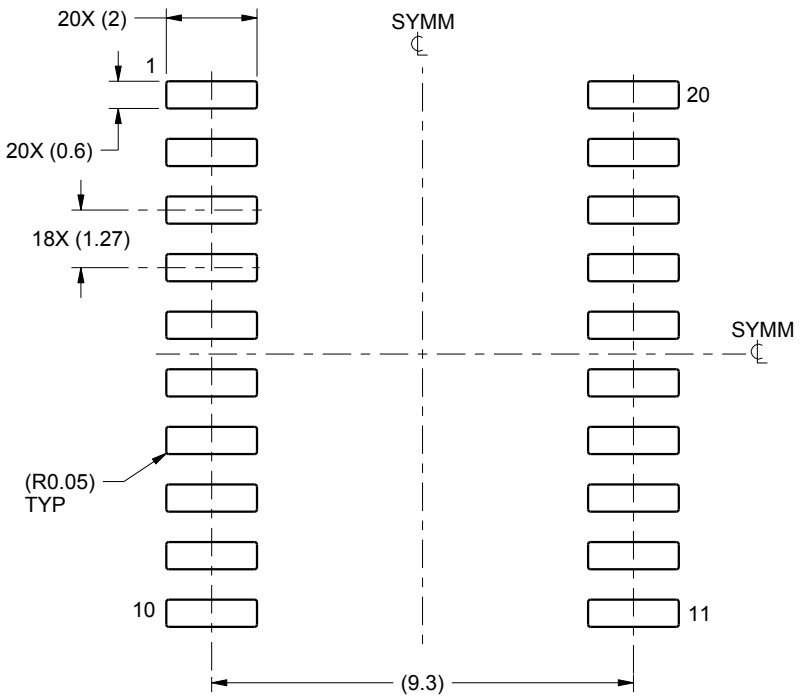
SOIC - 2.65 mm max height

SOIC

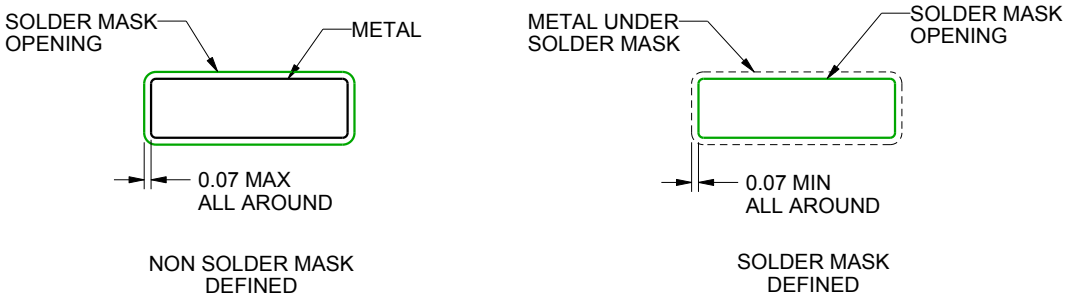


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

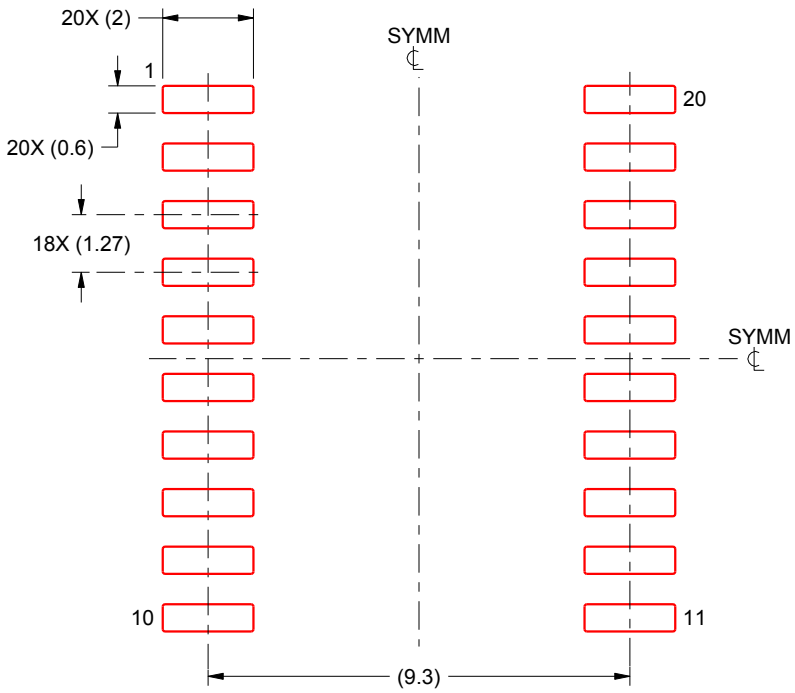


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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