

## FEATURES

- Triaxial digital gyroscope with digital range scaling**  
 $\pm 62^\circ/\text{sec}$ ,  $\pm 125^\circ/\text{sec}$ ,  $\pm 250^\circ/\text{sec}$  settings  
 Axis-to-axis alignment,  $<0.05^\circ$
- Triaxial digital accelerometer,  $\pm 5 g$  minimum**
- Autonomous operation and data collection**  
 No external configuration commands required  
 175 ms start-up time
- Factory calibrated sensitivity, bias, and axial alignment**  
 Calibration temperature range:  $-40^\circ\text{C}$  to  $+70^\circ\text{C}$
- SPI-compatible serial interface**
- Embedded temperature sensor**
- Programmable operation and control**  
 Automatic and manual bias correction controls  
 Bartlett window FIR length, number of taps  
 Digital I/O: data ready, alarm indicator, general-purpose  
 Alarms for condition monitoring  
 Enable external sample clock input up to 1.1 kHz  
 Single command self-test
- Single-supply operation: 3.15 V to 3.45 V**
- 2000 g shock survivability**
- Operating temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$**

## APPLICATIONS

- Platform stabilization and control
- Navigation
- Robotics

## GENERAL DESCRIPTION

The [ADIS16445](#) *iSensor*® device is a complete inertial system that includes a triaxial gyroscope and a triaxial accelerometer. Each sensor in the [ADIS16445](#) combines industry-leading *iMEMS*® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, and alignment. As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The [ADIS16445](#) provides a simple, cost-effective method for integrating accurate, multi-axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structures provide a simple interface for data collection and configuration control.

The [ADIS16445](#) has a compatible pinout for systems that currently use other Analog Devices, Inc., IMU products ([ADIS163xx/ADIS164xx](#)). The [ADIS16445](#) is packaged in a module that is approximately 24.1 mm  $\times$  37.7 mm  $\times$  10.8 mm and has a standard connector interface.

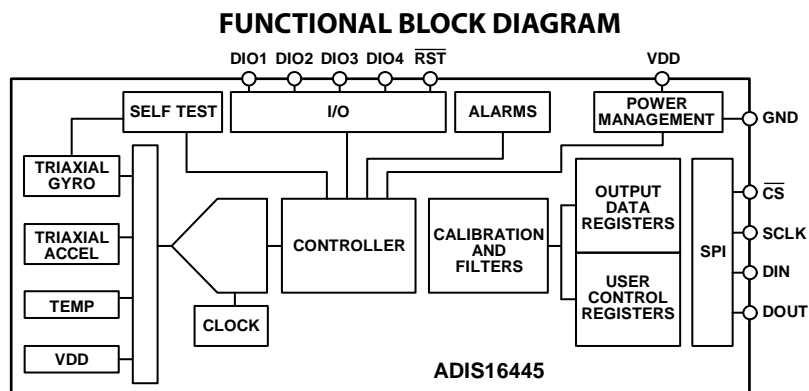


Figure 1.

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## REVISION HISTORY

### 10/14—Rev. C to Rev. D

Changes to Gyroscopes, Bias Temperature Coefficient Parameter, and Accelerometers, Bias Temperature Coefficient Parameter, Table 1.....	3
Changes to Table 41.....	20

### 5/14—Rev. B to Rev. C

Change to General Description Section .....	1
Change to Status/Error Flags Section .....	15
Added Mounting Tips Section.....	21

### 7/13—Rev. A to Rev. B

Change to Linear Acceleration Effect on Bias Parameter, Table 1....	3
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### 3/13—Rev. 0 to Rev. A

Changes to Table 1.....	3
Deleted Mounting Approaches Section.....	21
Updated Outline Dimensions.....	22

### 10/12—Revision 0: Initial Version

## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , angular rate =  $0^\circ/\text{sec}$ , dynamic range =  $\pm 250^\circ/\text{sec} \pm 1\text{ g}$ , unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>GYROSCOPES</b>					
Dynamic Range		$\pm 250$			$^\circ/\text{sec}$
Initial Sensitivity	$\pm 250^\circ/\text{sec}$ , see Table 12		0.01		$^\circ/\text{sec}/\text{LSB}$
	$\pm 125^\circ/\text{sec}$		0.005		$^\circ/\text{sec}/\text{LSB}$
	$\pm 62^\circ/\text{sec}$		0.0025		$^\circ/\text{sec}/\text{LSB}$
Repeatability <sup>1</sup>	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$			1	%
Sensitivity Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		$\pm 40$		ppm/ $^\circ\text{C}$
Misalignment	Axis to axis		$\pm 0.05$		Degrees
	Axis to frame (package)		$\pm 0.5$		Degrees
Nonlinearity	Best fit straight line		$\pm 0.1$		% of FS
Bias Repeatability <sup>1, 2</sup>	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ , $1\sigma$		0.5		$^\circ/\text{sec}$
In-Run Bias Stability	$1\sigma$ , SMPL_PRD = 0x0001		12		$^\circ/\text{hr}$
Angular Random Walk	$1\sigma$ , SMPL_PRD = 0x0001		0.56		$^\circ/\sqrt{\text{hr}}$
Bias Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		$\pm 0.005$		$^\circ/\text{sec}/^\circ\text{C}$
Linear Acceleration Effect on Bias	Any axis, $1\sigma$		$\pm 0.015$		$^\circ/\text{sec}/\text{g}$
Bias Supply Sensitivity	$+3.15\text{ V} \leq V_{DD} \leq +3.45\text{ V}$		$\pm 0.2$		$^\circ/\text{sec}/\text{V}$
Output Noise	$\pm 250^\circ/\text{sec}$ range, no filtering		0.22		$^\circ/\text{sec rms}$
Rate Noise Density	$f = 25\text{ Hz}$ , $\pm 250^\circ/\text{sec}$ range, no filtering		0.011		$^\circ/\text{sec}/\sqrt{\text{Hz rms}}$
-3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			17.5		kHz
<b>ACCELEROMETERS</b>					
Dynamic Range	Each axis	$\pm 5$			<i>g</i>
Initial Sensitivity	See Table 16 for data format	0.2475	0.25	0.2525	mg/LSB
Repeatability <sup>1</sup>	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$			1	%
Sensitivity Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		$\pm 40$		ppm/ $^\circ\text{C}$
Misalignment	Axis to axis		$\pm 0.2$		Degrees
	Axis to frame (package)		$\pm 0.5$		Degrees
Nonlinearity	Best fit straight line		$\pm 0.2$		% of FS
Bias Repeatability <sup>1, 2</sup>	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ , $1\sigma$		$\pm 8$		mg
In-Run Bias Stability	$1\sigma$ , SMPL_PRD = 0x0001		0.075		mg
Velocity Random Walk	$1\sigma$ , SMPL_PRD = 0x0001		0.073		m/sec/ $\sqrt{\text{hr}}$
Bias Temperature Coefficient	$-40^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		$\pm 0.04$		mg/ $^\circ\text{C}$
Bias Supply Sensitivity	$+3.15\text{ V} \leq V_{DD} \leq +3.45\text{ V}$		1.5		mg/V
Output Noise	No filtering		2.25		mg rms
Noise Density	No filtering		0.105		mg/ $\sqrt{\text{Hz rms}}$
-3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
<b>TEMPERATURE</b>					
Sensitivity	See Table 17		0.07386		$^\circ\text{C}/\text{LSB}$
<b>LOGIC INPUTS<sup>3</sup></b>					
Input High Voltage, $V_{IH}$		2.0			V
Input Low Voltage, $V_{IL}$				0.8	V
Logic 1 Input Current, $I_{IH}$	$V_{IH} = 3.3\text{ V}$		$\pm 0.2$	$\pm 10$	$\mu\text{A}$
Logic 0 Input Current, $I_{IL}$	$V_{IL} = 0\text{ V}$				$\mu\text{A}$
All Pins Except $\overline{\text{RST}}$			40	60	$\mu\text{A}$
$\overline{\text{RST}}$ Pin			1		mA
Input Capacitance, $C_{IN}$			10		pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL OUTPUTS <sup>3</sup>					
Output High Voltage, V <sub>OH</sub>	I <sub>SOURCE</sub> = 1.6 mA	2.4			V
Output Low Voltage, V <sub>OL</sub>	I <sub>SINK</sub> = 1.6 mA			0.4	V
FLASH MEMORY	Endurance <sup>4</sup>	10,000			Cycles
Data Retention <sup>5</sup>	T <sub>J</sub> = 85°C	20			Years
FUNCTIONAL TIMES <sup>6</sup>	Time until new data is available				
Power-On Start-Up Time			175		ms
Reset Recovery Time <sup>7</sup>			55		ms
Flash Memory Back-Up Time			55		ms
Flash Memory Test Time			20		ms
Automatic Self-Test Time	SMPL_PRD = 0x0001		16		ms
CONVERSION RATE					
xGYRO_OUT, xACCL_OUT	SMPL_PRD = 0x0001		819.2		SPS
Clock Accuracy				±3	%
Sync Input Clock <sup>8</sup>		0.8		1.1	kHz
POWER SUPPLY	Operating voltage range, VDD	3.15	3.3	3.45	V
Power Supply Current	VDD = 3.15 V		74		mA

<sup>1</sup> The repeatability specifications represent analytical projections, which are based off of the following drift contributions and conditions: temperature hysteresis (–40°C to +70°C), electronics drift (high-temperature operating life test: 85°C, 500 hours), drift from temperature cycling (JESD22, Method A104-C, Method N, 500 cycles, –40°C to +85°C), rate random walk (10 year projection), and broadband noise.

<sup>2</sup> Bias repeatability describes a long-term behavior, over a variety of conditions. Short-term repeatability is related to the in-run bias stability and noise density specifications.

<sup>3</sup> The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.

<sup>4</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at –40°C, +25°C, +85°C, and +125°C.

<sup>5</sup> The data retention lifetime equivalent is at a junction temperature (T<sub>J</sub>) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.

<sup>6</sup> These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.

<sup>7</sup> The RST line must be held low for at least 10 μs to assure a proper reset and recovery sequence.

<sup>8</sup> The sync input clock functions below the specified minimum value but at reduced performance levels.

**TIMING SPECIFICATIONS**

T<sub>A</sub> = 25°C, VDD = +3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Normal Mode			Burst Read			Unit
		Min <sup>1</sup>	Typ	Max	Min <sup>1</sup>	Typ	Max	
f <sub>SCLK</sub>	Serial clock	0.01		2.0	0.01		1.0	MHz
t <sub>STALL</sub>	Stall period between data	9			N/A <sup>2</sup>			μs
t <sub>READRATE</sub>	Read rate	40						μs
t <sub>CS</sub>	Chip select to SCLK edge	48.8			48.8			ns
t <sub>DAV</sub>	DOUT valid after SCLK edge			100			100	ns
t <sub>DSU</sub>	DIN setup time before SCLK rising edge	24.4			24.4			ns
t <sub>DHD</sub>	DIN hold time after SCLK rising edge	48.8			48.8			ns
t <sub>SCLKR</sub> , t <sub>SCLKF</sub>	SCLK rise/fall times, not shown in timing diagrams		5	12.5		5	12.5	ns
t <sub>DR</sub> , t <sub>DF</sub>	DOUT rise/fall times, not shown in timing diagrams		5	12.5		5	12.5	ns
t <sub>SFS</sub>	$\overline{CS}$ high after SCLK edge	5			5			ns
t <sub>1</sub>	Input sync positive pulse width	25			25			μs
t <sub>STDR</sub>	Input sync to data ready valid transition		670			670		μs
t <sub>NV</sub>	Data invalid time		210			210		μs
t <sub>3</sub>	Input sync period	910			910			μs

<sup>1</sup> Guaranteed by design and characterization, but not tested in production.

<sup>2</sup> When using the burst read mode, the stall period is not applicable.

**Timing Diagrams**

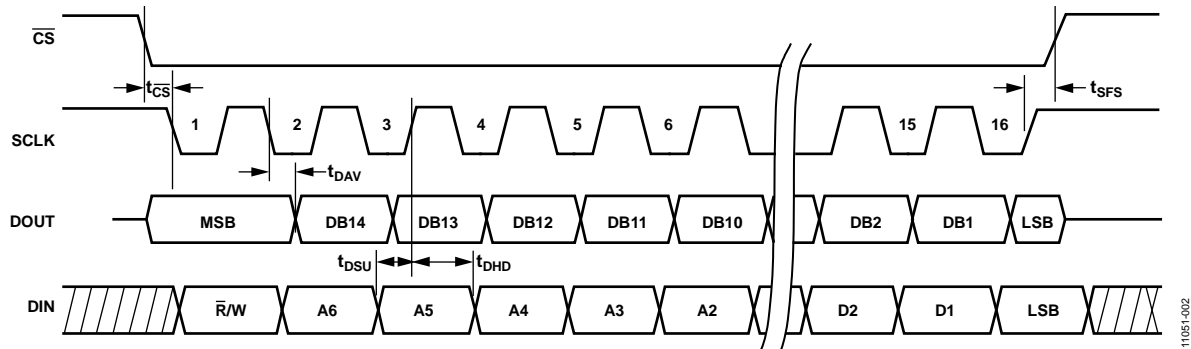


Figure 2. SPI Timing and Sequence

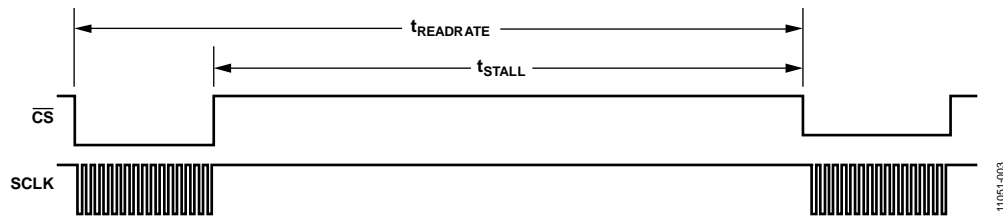


Figure 3. Stall Time and Data Rate

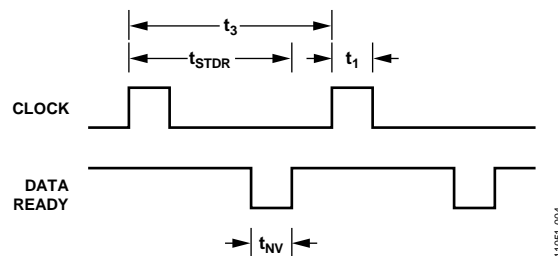


Figure 4. Input Clock Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 <i>g</i>
Any Axis, Powered	2000 <i>g</i>
VDD to GND	−0.3 V to +3.45 V
Digital Input Voltage to GND	−0.3 V to +VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to +VDD + 0.3 V
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +125°C <sup>1,2</sup>

<sup>1</sup> Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +105°C.

<sup>2</sup> Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

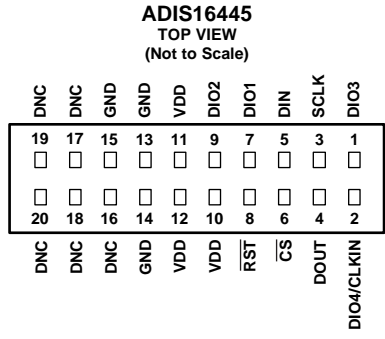
Package Type	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)	Mass (grams)
20-Lead Module (ML-20-3)	36.5	16.9	15

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. THIS REPRESENTATION DISPLAYS THE TOP VIEW WHEN THE CONNECTOR IS VISIBLE AND FACING UP.
  2. MATING CONNECTOR: SAMTEC CLM-110-02 OR EQUIVALENT.
  3. DNC = DO NOT CONNECT.

Figure 5. Pin Configuration

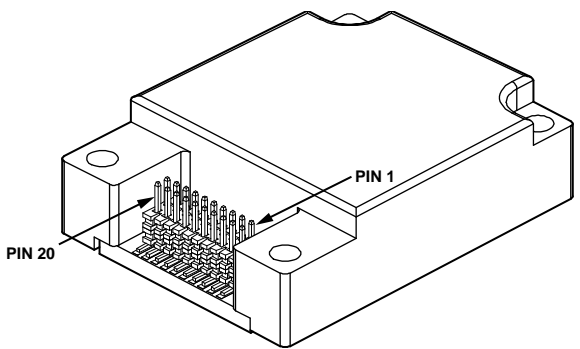


Figure 6. Pin Locations

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type <sup>1</sup>	Description
1	DIO3	I/O	Configurable Digital Input/Output.
2	DIO4/CLKIN	I/O	Configurable Digital Input/Output or Sync Clock Input.
3	SCLK	I	SPI Serial Clock.
4	DO UT	O	SPI Data Output. Clocks the output on the SCLK falling edge.
5	DIN	I	SPI Data Input. Clocks the input on the SCLK rising edge.
6	CS	I	SPI Chip Select.
7	DIO1	I/O	Configurable Digital Input/Output.
8	RST	I	Reset.
9	DIO2	I/O	Configurable Digital Input/Output.
10, 11, 12	VDD	S	Power Supply.
13, 14, 15	GND	S	Power Ground.
16, 17, 18, 19, 20	DNC	N/A	Do Not Connect. Do not connect to these pins.

<sup>1</sup>S is supply, O is output, I is input, N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

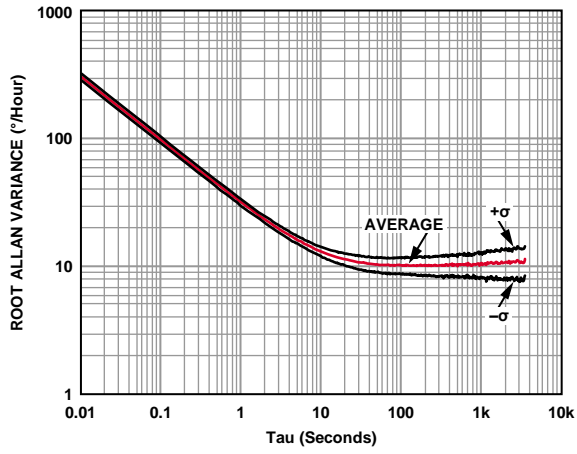


Figure 7. Gyroscope Root Allan Variance

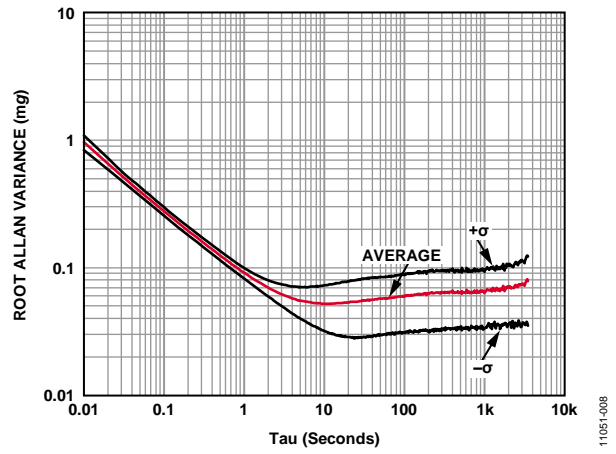


Figure 8. Accelerometer Root Allan Variance



## USER REGISTERS

Table 6. User Register Memory Map

Name	R/W	Flash Backup	Address <sup>1</sup>	Default	Function	Bit Assignments
FLASH_CNT	R	Yes	0x00	N/A	Flash memory write count	See Table 26
Reserved	N/A	N/A	0x02	N/A	N/A	N/A
XGYRO_OUT	R	No	0x04	N/A	X-axis gyroscope output	See Table 9
YGYRO_OUT	R	No	0x06	N/A	Y-axis gyroscope output	See Table 10
ZGYRO_OUT	R	No	0x08	N/A	Z-axis gyroscope output	See Table 11
XACCL_OUT	R	No	0x0A	N/A	X-axis accelerometer output	See Table 13
YACCL_OUT	R	No	0x0C	N/A	Y-axis accelerometer output	See Table 14
ZACCL_OUT	R	No	0x0E	N/A	Z-axis accelerometer output	See Table 15
Reserved	N/A	N/A	0x10 to 0x16	N/A	Reserved	N/A
TEMP_OUT	R	No	0x18	N/A	Temperature output	See Table 17
XGYRO_OFF	R/W	Yes	0x1A	0x0000	X-axis gyroscope bias offset factor	See Table 30
YGYRO_OFF	R/W	Yes	0x1C	0x0000	Y-axis gyroscope bias offset factor	See Table 31
ZGYRO_OFF	R/W	Yes	0x1E	0x0000	Z-axis gyroscope bias offset factor	See Table 32
XACCL_OFF	R/W	Yes	0x20	0x0000	X-axis acceleration bias offset factor	See Table 33
YACCL_OFF	R/W	Yes	0x22	0x0000	Y-axis acceleration bias offset factor	See Table 34
ZACCL_OFF	R/W	Yes	0x24	0x0000	Z-axis acceleration bias offset factor	See Table 35
Reserved	N/A	N/A	0x26 to 0x30	N/A	Reserved	N/A
GPIO_CTRL	R/W	No	0x32	0x0000	Auxiliary digital input/output control	See Table 27
MSC_CTRL	R/W	Yes	0x34	0x0006	Miscellaneous control	See Table 24
SMPL_PRD	R/W	Yes	0x36	0x0001	Internal sample period (rate) control	See Table 28
SENS_AVG	R/W	Yes	0x38	0x0402	Dynamic range and digital filter control	See Table 29
Reserved	N/A	N/A	0x3A	N/A	Reserved	N/A
DIAG_STAT	R	No	0x3C	0x0000	System status	See Table 25
Reserved	N/A	N/A	0x3A	N/A	Reserved	N/A
GLOB_CMD	W	N/A	0x3E	0x0000	System command	See Table 19
ALM_MAG1	R/W	Yes	0x40	0x0000	Alarm 1 amplitude threshold	See Table 36
ALM_MAG2	R/W	Yes	0x42	0x0000	Alarm 2 amplitude threshold	See Table 37
ALM_SMPL1	R/W	Yes	0x44	0x0000	Alarm 1 sample size	See Table 38
ALM_SMPL2	R/W	Yes	0x46	0x0000	Alarm 2 sample size	See Table 39
ALM_CTRL	R/W	Yes	0x48	0x0000	Alarm control	See Table 40
Reserved	N/A	N/A	0x4A to 0x51	N/A	Reserved	N/A
LOT_ID1	R	Yes	0x52	N/A	Lot identification number	See Table 20
LOT_ID2	R	Yes	0x54	N/A	Lot identification number	See Table 21
PROD_ID	R	Yes	0x56	0x403D	Product identifier	See Table 22
SERIAL_NUM	R	Yes	0x58	N/A	Lot-specific serial number	See Table 23

<sup>1</sup> Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

## USER INTERFACE

The ADIS16445 is an autonomous system that requires no user initialization. When it has a valid power supply, it initializes itself and starts sampling, processing, and loading sensor data into the output registers at a sample rate of 819.2 SPS. DIO1 pulses high after each sample cycle concludes. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 9 (electrical connection) and Table 7 (pin functions).

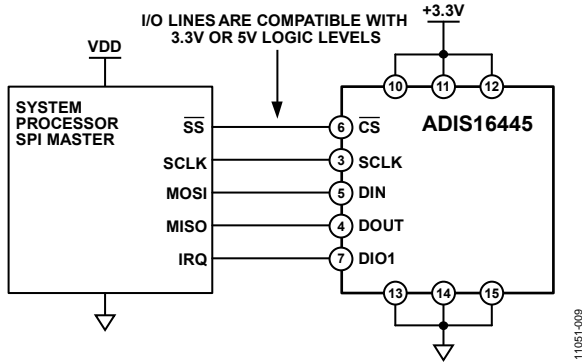


Figure 9. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Pin Name	Function
SS	Slave select
SCLK	Serial clock
MOSI	Master output, slave input
MISO	Master input, slave output
IRQ	Interrupt request

The ADIS16445 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 12. Table 8 provides a list of the most common settings that require attention to initialize the serial port of a processor for the ADIS16445 SPI interface.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	The ADIS16445 operates as a slave
SCLK Rate $\leq 2$ MHz <sup>1</sup>	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB-First Mode	Bit sequence
16-Bit Mode	Shift register/data length

<sup>1</sup> For burst read, SCLK rate  $\leq 1$  MHz.

## READING SENSOR DATA

The ADIS16445 provides two different options for acquiring sensor data: a single register and a burst register. A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 12. Bit DC7 to Bit DC0 are don't cares for a read, and then the output register contents follow on DOUT during the second sequence. Figure 10 includes three single register reads in succession.

In this example, the process starts with DIN = 0x0400 to request the contents of XGYRO\_OUT, then follows with 0x0600 to request YGYRO\_OUT, and 0x0800 to request ZGYRO\_OUT. Full duplex operation enables processors to use the same 16-bit SPI cycle to read data from DOUT while requesting the next set of data on DIN. Figure 11 provides an example of the four SPI signals when reading XGYRO\_OUT in a repeating pattern.

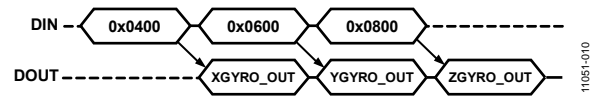


Figure 10. SPI Read Example

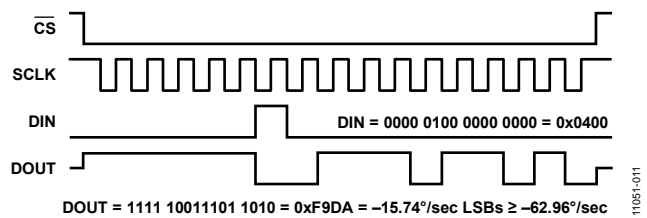
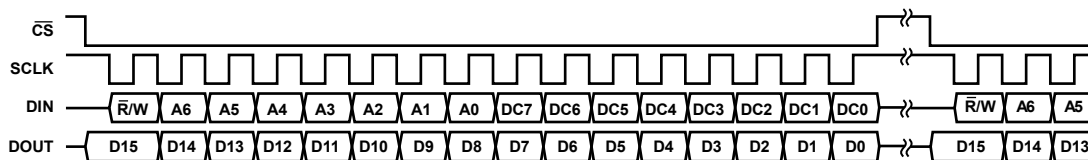


Figure 11. Example SPI Read, Second Sequence, SENS\_AVG[15:8] = 0x04



NOTES

- THE DOUT BIT PATTERN REFLECTS THE ENTIRE CONTENTS OF THE REGISTER IDENTIFIED BY [A6:A0] IN THE PREVIOUS 16-BIT DIN SEQUENCE WHEN R/W = 0.
- IF R/W = 1 DURING THE PREVIOUS SEQUENCE, DOUT IS NOT DEFINED.

Figure 12. SPI Communication Bit Sequence

**Burst Read Function**

The burst read function provides a way to read all of the data in one continuous stream of bits, with no stall time. As shown in Figure 13, start this mode by setting DIN = 0x3E00 while keeping CS low for eight additional 16-bit read cycles. These eight cycles produce the following sequence of output registers on DOUT: DIAG\_STAT, XGYRO\_OUT, YGYRO\_OUT, ZGYRO\_OUT, XACCL\_OUT, YACCL\_OUT, ZACCL\_OUT, and TEMP\_OUT.

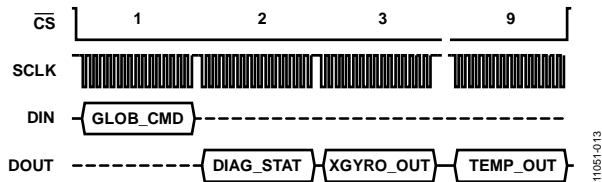


Figure 13. Burst Read Sequence

**SPI Read Test Sequence**

Figure 14 provides a test pattern for testing the SPI communication. In this pattern, write 0x5600 to the DIN line in a repeating pattern and raise chip select for at least 9 μs between each 16-bit sequence. Starting with the second 16-bit sequence, DOUT produces the contents of the PROD\_ID register, 0x403D (see Table 22).

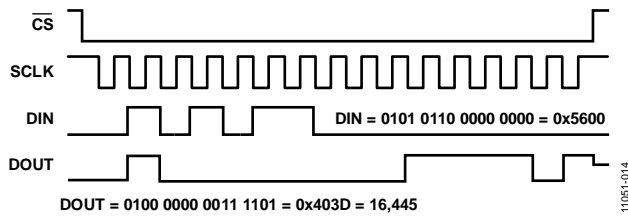


Figure 14. SPI Test Read Pattern DIN = 0x5600, DOUT = 0x403D

**DEVICE CONFIGURATION**

The control registers in Table 6 provide users with a variety of configuration options. The SPI provides access to these registers, one byte at a time, using the bit assignments in Figure 12. Each register has 16 bits, where Bits[7:0] represent the lower address, and Bits[15:8] represent the upper address. Figure 15 provides an example of writing 0x04 to Address 0x37 (SMPL\_PRD[15:8], using DIN = 0xB704). This example reduces the sample rate by a factor of eight (see Table 28).

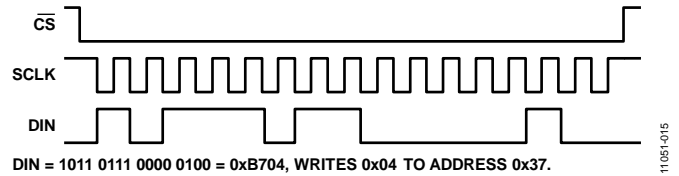


Figure 15. Example SPI Write Sequence

**Dual Memory Structure**

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, set GLOB\_CMD[3] = 1 (DIN = 0xBE08) to back up these settings in nonvolatile flash memory. The flash backup process requires a valid power supply level for the entire process time, 75 ms. Table 6 provides a user register memory map that includes a flash backup column. A Yes in this column indicates that a register has a mirror location in flash and, when backed up properly, it automatically restores itself during startup or after a reset. Figure 16 provides a diagram of the dual memory structure used to manage operation and store critical user settings.

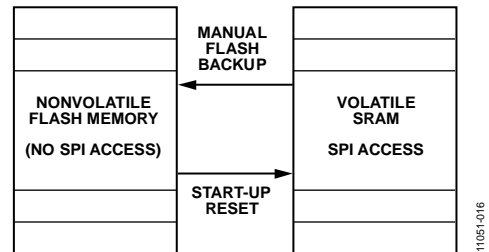


Figure 16. SRAM and Flash Memory Diagram

## OUTPUT DATA REGISTERS

Each sensor in the ADIS16445 has a dedicated output register in the user register map (see Table 6). Figure 17 provides arrows, which describe the direction or rotation ( $g_x$ ,  $g_y$ ,  $g_z$ ) and acceleration ( $a_x$ ,  $a_y$ ,  $a_z$ ) that produces a positive response in the output data.

### GYROSCOPES

XGYRO\_OUT (see Table 9) contains x-axis gyroscope data ( $g_x$  in Figure 17), YGYRO\_OUT (see Table 10) contains y-axis gyroscope data ( $g_y$  in Figure 17), and ZGYRO\_OUT (see Table 11) contains z-axis gyroscope data ( $g_z$  in Figure 17). Table 12 illustrates the gyroscope data format with numerical examples.

Table 9. XGYRO\_OUT (Base Address = 0x04), Read Only

Bits	Description
[15:0]	X-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 10. YGYRO\_OUT (Base Address = 0x06), Read Only

Bits	Description
[15:0]	Y-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 11. ZGYRO\_OUT (Base Address = 0x08), Read Only

Bits	Description
[15:0]	Z-axis gyroscope data, twos complement format, 100 LSB/°/sec (SENS_AVG[15:8] = 0x04), 0°/sec = 0x0000

Table 12. Rotation Rate, Twos Complement Format<sup>1</sup>

Rotation Rate (°/sec)	Decimal	Hex	Binary
+250	25,000	0x61A8	0110 0001 1010 1000
+2 ÷ 100	+2	0x0002	0000 0000 0000 0010
+1 ÷ 100	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
-1 ÷ 100	-1	0xFFFF	1111 1111 1111 1111
-2 ÷ 100	-2	0xFFFE	1111 1111 1111 1110
-250	-25,000	0x9E58	1001 1110 0101 1000

<sup>1</sup> SENS\_AVG[15:8] = 0x04, see Table 29.

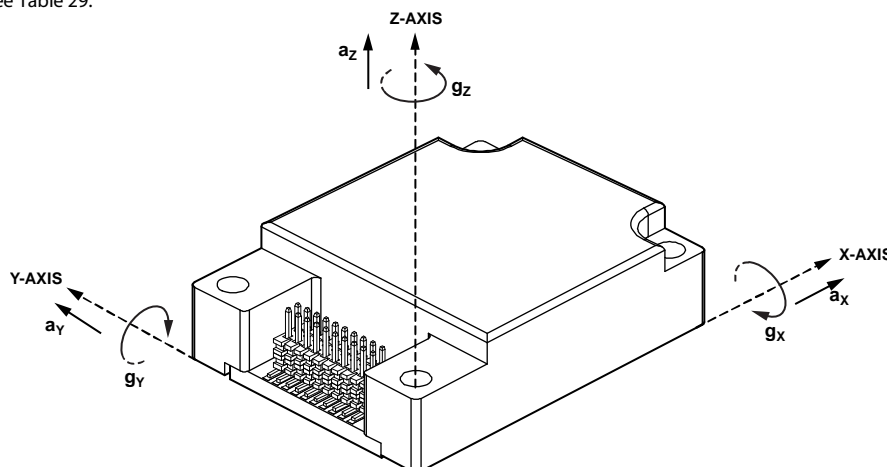


Figure 17. Inertial Sensor Direction Reference

### ACCELEROMETERS

XACCL\_OUT (see Table 13) contains x-axis accelerometer data ( $a_x$  in Figure 17), YACCL\_OUT (see Table 14) contains y-axis accelerometer data ( $a_y$  in Figure 17), and ZACCL\_OUT (see Table 15) contains z-axis accelerometer data ( $a_z$  in Figure 17). Table 16 illustrates the accelerometer data format with numerical examples.

Table 13. XACCL\_OUT (Base Address = 0x0A), Read Only

Bits	Description
[15:0]	X-axis acceleration data, twos complement format, 4000 LSB/g, 0 g = 0x0000

Table 14. YACCL\_OUT (Base Address = 0x0C), Read Only

Bits	Description
[15:0]	Y-axis acceleration data, twos complement format, 4000 LSB/g, 0 g = 0x0000

Table 15. ZACCL\_OUT (Base Address = 0x0E), Read Only

Bits	Description
[15:0]	Z-axis acceleration data, twos complement format, 4000 LSB/g, 0 g = 0x0000

Table 16. Acceleration, Twos Complement Format

Acceleration (g)	Decimal	Hex	Binary
+5	20,000	0x4E20	0100 1110 0010 0000
+2 ÷ 4000	+2	0x0002	0000 0000 0000 0010
+1 ÷ 4000	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
-1 ÷ 4000	-1	0xFFFF	1111 1111 1111 1111
-2 ÷ 4000	-2	0xFFFE	1111 1111 1111 1110
-5	-20,000	0xB1E0	1011 0001 1110 0000

11051-007

**INTERNAL TEMPERATURE**

The internal temperature measurement data loads into the TEMP\_OUT (see Table 17) register. Table 18 illustrates the temperature data format. Note that this temperature represents an internal temperature reading, which does not precisely represent external conditions. The intended use of TEMP\_OUT is to monitor relative changes in temperature.

**Table 17. TEMP\_OUT (Base Address = 0x18), Read Only**

Bits	Description
[15:12]	Not used
[11:0]	Twos complement, 0.07386°C/LSB, 31°C = 0x000

**Table 18. Temperature, Twos Complement Format**

Temperature (°C)	Decimal	Hex	Binary
+105	+1002	0x3EA	0011 1110 1010
+85	+731	0x2DB	0010 1101 1011
+31.14771	+2	0x002	0000 0000 0010
+31.07386	+1	0x001	0000 0000 0001
+31	0	0x000	0000 0000 0000
+30.92614	-1	0xFFF	1111 1111 1111
+30.85229	-2	0xFFE	1111 1111 1110
-40	-962	0xC3E	1100 0011 1110

## SYSTEM FUNCTIONS

### GLOBAL COMMANDS

The GLOB\_CMD register in Table 19 provides trigger bits for software reset, flash memory management, and calibration control. Start each of these functions by writing a 1 to the assigned bit in GLOB\_CMD. After completing the task, the bit automatically returns to 0.

For example, set GLOB\_CMD[7] = 1 (DIN = 0xBE80) to initiate a software reset. Set GLOB\_CMD[3] = 1 (DIN = 0xBE08) to back up the user register contents in nonvolatile flash. This sequence includes loading the control registers with the data in their respective flash memory locations prior to producing new data.

**Table 19. GLOB\_CMD (Base Address = 0x3E), Write Only**

Bits	Description (Default = 0x0000)
[15:8]	Not used
7	Software reset
[6:4]	Not used
3	Flash update
2	Not used
1	Factory calibration restore
0	Gyroscope bias correction

### PRODUCT IDENTIFICATION

The PROD\_ID register in Table 22 contains the binary equivalent of 16,445. It provides a product-specific variable for systems that need to track this in their system software. The LOT\_ID1 and LOT\_ID2 registers in Table 20 and Table 21, respectively, combine to provide a unique, 32-bit lot identification code.

The SERIAL\_NUM register in Table 23 contains a binary number that represents the serial number on the device label. The assigned serial numbers in SERIAL\_NUM are lot specific.

**Table 20. LOT\_ID1 (Base Address = 0x52), Read Only**

Bits	Description
[15:0]	Lot identification, binary code

**Table 21. LOT\_ID2 (Base Address = 0x54), Read Only**

Bits	Description
[15:0]	Lot identification, binary code

**Table 22. PROD\_ID (Base Address = 0x56), Read Only**

Bits	Description (Default = 0x403D)
[15:0]	Product identification = 0x403D (16,445)

**Table 23. SERIAL\_NUM (Base Address = 0x58), Read Only**

Bits	Description
[15:12]	Reserved
[11:0]	Serial number, 1 to 4094 (0xFFE)

### SELF-TEST FUNCTION

The MSC\_CTRL register in Table 24 provides a self-test function for the gyroscopes and accelerometers. This function allows the user to verify the mechanical integrity of each MEMS sensor. When enabled, the self-test applies an electrostatic force to each internal sensor element, which causes them to move. The movement in each element simulates its response to actual rotation/acceleration and generates a predictable electrical response in the sensor outputs. Set MSC\_CTRL[10] = 1 (DIN = 0xB504) to activate the internal self-test routine, which compares the response to an expected range of responses and reports a pass/fail response to DIAG\_STAT[5]. If this bit is high, review DIAG\_STAT[15:10] to identify the failing sensor.

**Table 24. MSC\_CTRL (Base Address = 0x34), Read/Write**

Bits	Description (Default = 0x0006)
[15:12]	Not used
11	Checksum memory test (cleared upon completion) <sup>1</sup> 1 = enabled, 0 = disabled
10	Internal self-test (cleared upon completion) <sup>1</sup> 1 = enabled, 0 = disabled
[9:8]	Do not use, always set to 00
7	Not used
6	Point of percussion, see Figure 21 1 = enabled, 0 = disabled
[5:3]	Not used
2	Data ready enable 1 = enabled, 0 = disabled
1	Data ready polarity 1 = active high when data is valid 0 = active low when data is valid
0	Data ready line select 1 = DIO2, 0 = DIO1

<sup>1</sup> The bit is automatically reset to 0 after finishing the test.

## STATUS/ERROR FLAGS

The DIAG\_STAT register in Table 25 provides error flags for a number of functions. Each flag uses 1 to indicate an error condition and 0 to indicate a normal condition. Reading this register provides access to the status of each flag and resets all of the bits to 0 for monitoring future operation. If the error condition remains, the error flag returns to 1 at the conclusion of the next sample cycle. The SPI communication error flag in DIAG\_STAT[3] indicates that the number of SCLKs in a SPI sequence did not equal a multiple of 16 SCLKs.

**Table 25. DIAG\_STAT (Base Address = 0x3C), Read Only**

Bits	Description (Default = 0x0000)
15	Z-axis accelerometer self-test failure 1 = fail, 0 = pass
14	Y-axis accelerometer self-test failure 1 = fail, 0 = pass
13	X-axis accelerometer self-test failure 1 = fail, 0 = pass
12	Z-axis gyroscope self-test failure 0 = pass
11	Y-axis gyroscope self-test failure 1 = fail, 0 = pass
10	X-axis gyroscope self-test failure 1 = fail, 0 = pass
9	Alarm 2 status 1 = active, 0 = inactive
8	Alarm 1 status 1 = active, 0 = inactive
7	Not used
6	Flash test, checksum flag 1 = fail, 0 = pass
5	Self-test diagnostic error flag 1 = fail, 0 = pass
4	Sensor overrange 1 = overrange, 0 = normal
3	SPI communication failure 1 = fail, 0 = pass
2	Flash update failure 1 = fail, 0 = pass
[1:0]	Not used

## MEMORY MANAGEMENT

The FLASH\_CNT register in Table 26 provides a 16-bit counter that helps track the number of write cycles to the nonvolatile flash memory. The flash updates every time a manual flash update occurs. A manual flash update is initiated by the GLOB\_CMD[3] bit and is performed at the completion of the GLOB\_CMD[1:0] functions (see Table 19).

**Table 26. FLASH\_CNT (Base Address = 0x00), Read Only**

Bits	Description
[15:0]	Binary counter

### Checksum Test

Set MSC\_CTRL[11] = 1 (DIN = 0xB508) to perform a checksum test of the internal program memory. This function takes a summation of the internal program memory and compares it with the original summation value for the same locations (from factory configuration). If the sum matches the correct value, DIAG\_STAT[6] is equal to 0. If it does not match, DIAG\_STAT[6] is equal to 1. Make sure that the power supply is within specification for the entire 20 ms that this function takes to complete.

## INPUT/OUTPUT CONFIGURATION

### DATA READY INDICATOR

The data ready indicator provides a signal that indicates when the registers are updating, so that system processors can avoid data collision, a condition when internal register updates happen at the same time that an external processor requests it. The data ready signal has valid and invalid states. Using the transition from invalid to valid to trigger an interrupt service routine provides the most time for data acquisition (before the next register update). See Figure 4 and Table 2 for specific timing information.

MSC\_CTRL[2:0] (see Table 24) provide control bits for enabling this function, selecting the polarity of the valid state and I/O line assignment (DIO1, DIO2). The factory default setting of MSC\_CTRL[2:0] = 110 establishes DIO1 as a data ready output line and assigns the valid state with a logic high (1). Set MSC\_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal on DIO1 for interrupt inputs that require negative logic inputs for activation.

### GENERAL-PURPOSE INPUT/OUTPUT

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose input/output lines that serve multiple purposes. The data ready controls in MSC\_CTRL[2:0] have the highest priority for configuring DIO1 and DIO2. The alarm indicator controls in ALM\_CTRL[2:0] have the second highest priority for configuring DIO1 and DIO2. The external clock control associated with SMPL\_PRD[0] has the highest priority for DIO4 configuration (see Table 28). GPIO\_CTRL in Table 27 has the lowest priority for configuring DIO1, DIO2, and DIO4, and has absolute control over DIO3.

**Table 27. GPIO\_CTRL (Base Address = 0x32), Read/Write**

Bits	Description (Default = 0x0000)
[15:12]	Not used
11	General-Purpose I/O Line 4 (DIO4) data level
10	General-Purpose I/O Line 3 (DIO3) data level
9	General-Purpose I/O Line 2 (DIO2) data level
8	General-Purpose I/O Line 1 (DIO1) data level
[7:4]	Not used
3	General-Purpose I/O Line 4 (DIO4) direction control 1 = output, 0 = input
2	General-Purpose I/O Line 3 (DIO3) direction control 1 = output, 0 = input
1	General-Purpose I/O Line 2 (DIO2) direction control 1 = output, 0 = input
0	General-Purpose I/O Line 1 (DIO1) direction control 1 = output, 0 = input

### Example Input/Output Configuration

For example, set GPIO\_CTRL[3:0] = 0100 (DIN = 0xB204) to set DIO3 as an output signal pin and DIO1, DIO2, and DIO4 as input signal pins. Set the output on DIO3 to 1 by setting GPIO\_CTRL[10] = 1 (DIN = 0xB304). Then, read GPIO\_CTRL[7:0] (DIN = 0x3200) and mask off GPIO\_CTRL[9:8] and GPIO\_CTRL[11] to monitor the digital signal levels on DIO4, DIO2, and DIO1.



## DIGITAL PROCESSING CONFIGURATION GYROSCOPES/ACCELEROMETERS

Figure 19 provides a diagram that describes all signal processing components for the gyroscopes and accelerometers. The internal sampling system produces new data in the xGYRO\_OUT and xACCL\_OUT output data registers at a rate of 819.2 SPS. The SMPL\_PRD register in Table 28 provides two functional controls that affect sampling and register update rates. SMPL\_PRD[12:8] provides a control for reducing the update rate, using an averaging filter with a decimated output. These bits provide a binomial control that divides the data rate by a factor of 2 every time this number increases by 1. For example, set SMPL\_PRD[15:8] = 0x04 (DIN = 0xB704) to set the decimation factor to 16. This reduces the update rate to 51.2 SPS and the bandwidth to ~25 Hz. The SMPL\_PRD[12:8] setting affects the update rate for the TEMP\_OUT register (see Table 17) as well.

**Table 28. SMPL\_PRD (Base Address = 0x36), Read/Write**

Bits	Description (Default = 0x0001)
[15:13]	Not used
[12:8]	D, decimation rate setting, binomial, see Figure 19
[7:1]	Not used
0	Clock 1 = internal sampling clock, 819.2 SPS 0 = external sampling clock

### INPUT CLOCK CONFIGURATION

SMPL\_PRD[0] (see Table 28) provides a control for synchronizing the internal sampling to an external clock source. Set SMPL\_PRD[0] = 0 (DIN = 0xB600) and GPIO\_CTRL[3] = 0 (DIN = 0xB200) to enable the external clock. See Table 2 and Figure 4 for timing information.

### Digital Filtering

The SENS\_AVG register in Table 29 provides user controls for the low-pass filter. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 19). For example, set SENS\_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 819.2 SPS and zero decimation (SMPL\_PRD[15:8] = 0x00), this value reduces the sensor bandwidth to approximately 16 Hz.

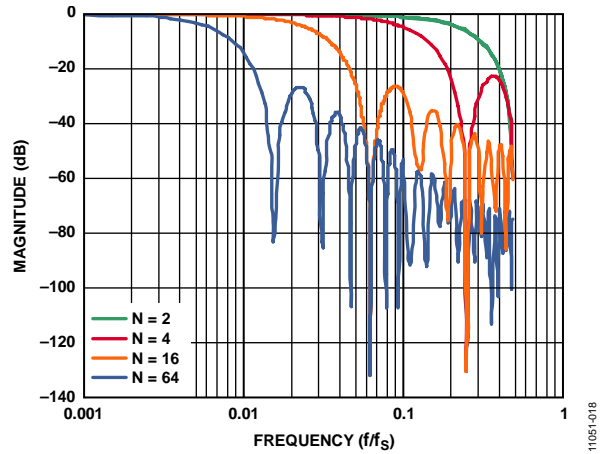


Figure 18. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

### Dynamic Range

The SENS\_AVG[10:8] bits provide three dynamic range settings for the gyroscopes. The lower dynamic range settings ( $\pm 62.5^\circ/\text{sec}$  and  $\pm 125^\circ/\text{sec}$ ) limit the minimum filter tap sizes to maintain resolution. For example, set SENS\_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of  $\pm 125^\circ/\text{sec}$ . Because this setting can influence the filter settings, program SENS\_AVG[10:8] before programming SENS\_AVG[2:0] if more filtering is required.

**Table 29. SENS\_AVG (Base Address = 0x38), Read/Write**

Bits	Description (Default = 0x0402)
[15:11]	Not used
[10:8]	Measurement range (sensitivity) selection 100 = $\pm 250^\circ/\text{sec}$ (default condition) 010 = $\pm 125^\circ/\text{sec}$ , filter taps $\geq 4$ (Bits[2:0] $\geq 0x02$ ) 001 = $\pm 62.5^\circ/\text{sec}$ , filter taps $\geq 16$ (Bits[2:0] $\geq 0x04$ )
[7:3]	Not used
[2:0]	Filter Size Variable B Number of taps in each stage; $N_B = 2^B$ See Figure 18 for filter response

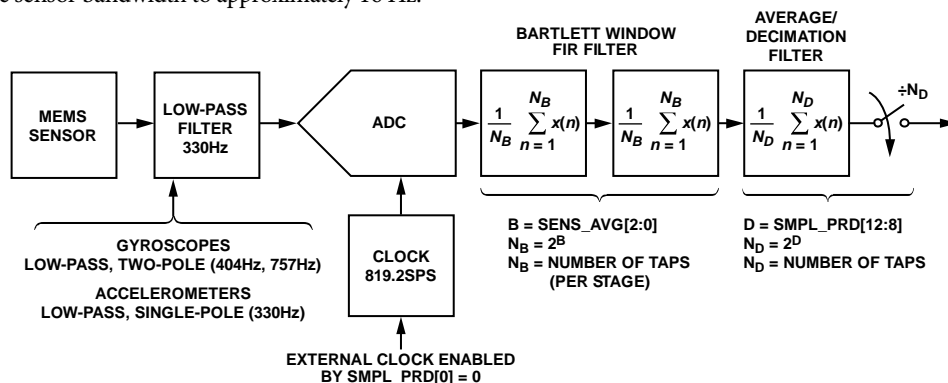


Figure 19. Sampling and Frequency Response Block Diagram

## CALIBRATION

The mechanical structure and assembly process of the ADIS16445 provide excellent position and alignment stability for each sensor, even after subjected to temperature cycles, shock, vibration, and other environmental conditions. The factory calibration includes a dynamic characterization of each gyroscope and accelerometer over temperature and generates sensor specific correction formulas.

### GYROSCOPES

The XGYRO\_OFF (see Table 30), YGYRO\_OFF (see Table 31), and ZGYRO\_OFF (see Table 32) registers provide user-programmable bias adjustment function for the x-, y-, and z-axis gyroscopes, respectively. Figure 20 illustrates that they contain bias correction factors that adjust to the sensor data immediately before it loads into the output register.

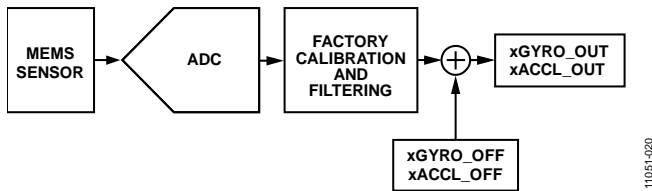


Figure 20. User Calibration, Gyroscopes, and Accelerometers

### Gyroscope Bias Error Estimation

Any system level calibration function must start with an estimate of the bias errors, which typically comes from a sample of gyroscope output data, when the device is not in motion. The sample size of data depends on the accuracy goals. Figure 7 provides a trade-off relationship between averaging time and the expected accuracy of a bias measurement. Vibration, thermal gradients, and power supply instability can influence the accuracy of this process.

Table 30. XGYRO\_OFF (Base Address = 0x1A), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

Table 31. YGYRO\_OFF (Base Address = 0x1C), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Y-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

Table 32. ZGYRO\_OFF (Base Address = 0x1E), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	Z-axis, gyroscope offset correction factor, twos complement, 0.0025°/sec/LSB, 0°/sec = 0x0000

### Gyroscope Bias Correction Factors

When the bias estimate is complete, multiply the estimate by  $-1$  to change its polarity, convert it into digital format for the offset correction registers (see Table 30, Table 31, and Table 32), and write the correction factors to the correction registers. For example, lower the x-axis bias by 10 LSB (0.025°/sec) by setting XGYRO\_OFF = 0x1FF6 (DIN = 0x9B1F, 0x9AF6).

### Single Command Bias Correction

GLOB\_CMD[0] (see Table 19) loads the xGYRO\_OFF registers with the values that are the opposite of the values that are in xGYRO\_OUT, at the time of initiation. Use this command, together with the decimation filter (SMPL\_PRD[12:8], see Table 28), to automatically average the gyroscope data and improve the accuracy of this function, as follows:

1. Set SENS\_AVG[10:8] = 001 (DIN = 0xB901) to optimize the xGYRO\_OUT sensitivity to 0.0025°/sec/LSB.
2. Set SMPL\_PRD[12:8] = 0x10 (DIN = 0xB710) to set the decimation rate to 65,536 ( $2^{16}$ ), which provides an averaging time of 80 seconds ( $65,536 \div 819.2$  SPS).
3. Wait for 80 seconds while keeping the device motionless.
4. Set GLOB\_CMD[0] = 1 (DIN = 0xBE01) and wait for the time it takes to perform the flash memory backup.

### ACCELEROMETERS

The XACCL\_OFF (see Table 33), YACCL\_OFF (see Table 34), and ZACCL\_OFF (see Table 35) registers provide user-programmable bias adjustment function for the x-, y-, and z-axis accelerometers, respectively. These registers adjust the accelerometer data in the same manner as XGYRO\_OFF in Figure 20.

Table 33. XACCL\_OFF (Base Address = 0x20), Read/Write

Bits	Description (Default = 0x0000)
[15:0]	X-axis, accelerometer offset correction factor, twos complement, 0.25 mg/LSB, 0 g = 0x0000

Table 34. YACCL\_OFF (Base Address = 0x22), Read/Write

Bits	Description (Default = 0x0000)
[15:14]	Not used
[13:0]	Y-axis, accelerometer offset correction factor, twos complement, 0.25 mg/LSB, 0 g = 0x0000

Table 35. ZACCL\_OFF (Base Address = 0x24), Read/Write

Bits	Description (Default = 0x0000)
[15:14]	Not used
[13:0]	Z-axis, accelerometer offset correction factor, twos complement, 0.25 mg/LSB, 0 g = 0x0000

### Accelerometer Bias Error Estimation

Under static conditions, orient each accelerometer in positions where the response to gravity is predictable. A common approach is to measure the response of each accelerometer when they are oriented in peak response positions, that is, where  $\pm 1 g$  is the ideal measurement position. Next, average the  $+1 g$  and  $-1 g$  accelerometer measurements together to estimate the residual bias error. Using more points in the rotation can improve the accuracy of the response.

### Accelerometer Bias Correction Factors

When the bias estimate is complete, multiply the estimate by  $-1$  to change its polarity, convert it to the digital format for the offset correction registers (see Table 33, Table 34 or Table 35), and write the correction factors to the correction registers. For example, lower the x-axis bias by 12 LSB (3 mg) by setting  $XACCL\_OFF = 0xFFF4$  (DIN =  $0xA1FF$ ,  $0xA0F4$ ).

### Point of Percussion Alignment

Set  $MSC\_CTRL[6] = 1$  (DIN =  $0xB446$ ) to enable this feature and maintain the factory default settings for DIO1. This feature performs a point of percussion translation to the point identified in Figure 21. See Table 24 for more information on  $MSC\_CTRL$ .

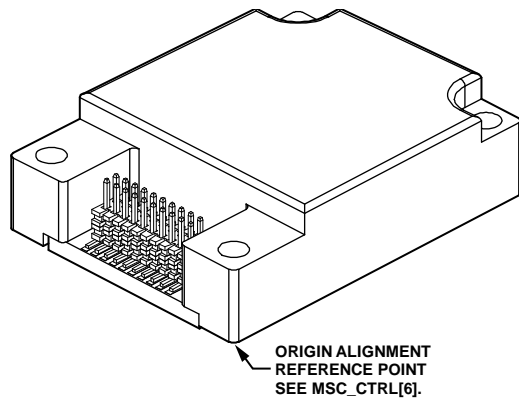


Figure 21. Point of Percussion Physical Reference

### FLASH UPDATES

When using the user calibration registers to optimize system level accuracy, set  $GLOB\_CMD[3] = 1$  (DIN =  $0xBE04$ ) to save these settings in nonvolatile flash memory. Be sure to consider the endurance rating of the flash memory when determining how often to update the user correction factors in the flash memory.

### RESTORING FACTORY CALIBRATION

Set  $GLOB\_CMD[1] = 1$  (DIN =  $0xBE02$ ) to execute the factory calibration restore function, which resets the gyroscope and accelerometer offset registers to  $0x0000$  and all sensor data to 0. Then, it automatically updates the flash memory and restarts sampling and processing data. See Table 19 for information on  $GLOB\_CMD$ .

## ALARMS

Alarm 1 and Alarm 2 provide two independent alarms with programmable levels, polarity, and data sources.

### STATIC ALARM USE

The static alarms setting compares the data source selection (ALM\_CTRL[15:8]) with the values in the ALM\_MAGx registers listed in Table 36 and Table 37, using ALM\_MAGx[15] to determine the trigger polarity. The data format in these registers matches the format of the data selection in ALM\_CTRL[15:8]. See Table 41, Alarm 1, for a static alarm configuration example.

**Table 36. ALM\_MAG1 (Base Address = 0x40), Read/Write**

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[11:8] output register selection

**Table 37. ALM\_MAG2 (Base Address = 0x42), Read/Write**

Bits	Description (Default = 0x0000)
[15:0]	Threshold setting; matches for format of ALM_CTRL[15:12] output register selection

### DYNAMIC ALARM USE

The dynamic alarm setting monitors the data selection for a rate-of-change comparison. The rate-of-change comparison is represented by the magnitude in the ALM\_MAGx registers over the time represented by the number-of-samples setting in the ALM\_SMPLx registers, located in Table 38 and Table 39. See Table 41, Alarm 2, for a dynamic alarm configuration example.

**Table 38. ALM\_SMPL1 (Base Address = 0x44), Read/Write**

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

**Table 39. ALM\_SMPL2 (Base Address = 0x46), Read/Write**

Bits	Description (Default = 0x0000)
[15:8]	Not used
[7:0]	Binary, number of samples (both 0x00 and 0x01 = 1)

### ALARM REPORTING

The DIAG\_STAT[9:8] bits provide error flags that indicate an alarm condition. The ALM\_CTRL[2:0] bits provide controls for a hardware indicator using DIO1 or DIO2.

**Table 40. ALM\_CTRL (Base Address = 0x48), Read/Write**

Bits	Description (Default = 0x0000)
[15:12]	Alarm 2 data source selection 0000 = disable 0001 = XGYRO_OUT 0010 = YGYRO_OUT 0011 = ZGYRO_OUT 0100 = XACCL_OUT 0101 = YACCL_OUT 0110 = ZACCL_OUT
[11:8]	Alarm 1 data source selection (same as Alarm 2)
7	Alarm 2, dynamic/static (1 = dynamic, 0 = static)
6	Alarm 1, dynamic/static (1 = dynamic, 0 = static)
5	Alarm 2, polarity (1 = greater than ALM_MAG2)
4	Alarm 1, polarity (1 = greater than ALM_MAG1)
3	Data source filtering (1 = filtered, 0 = unfiltered)
2	Alarm indicator (1 = enabled, 0 = disabled)
1	Alarm indicator active polarity (1 = high, 0 = low)
0	Alarm output line select (1 = DIO2, 0 = DIO1)

### Alarm Example

Table 41 offers an example that configures Alarm 1 to trigger when filtered ZACCL\_OUT data drops below 0.7 g, and Alarm 2 to trigger when filtered ZGYRO\_OUT data changes by more than 50°/sec over a 100 ms period, or 500°/sec<sup>2</sup>. The filter setting helps reduce false triggers from noise and refines the accuracy of the trigger points. The ALM\_SMPL2 setting of 82 samples provides a comparison period that is approximately equal to 100 ms for an internal sample rate of 819.2 SPS.

**Table 41. Alarm Configuration Example**

DIN	Description
0xC936, 0xC8AF	ALM_CTRL = 0x36AF Alarm 2: dynamic, $\Delta$ -ZGYRO_OUT ( $\Delta$ -time, ALM_SMPL2) > ALM_MAG2 Alarm 1: static, ZACCL_OUT < ALM_MAG1, filtered data DIO2 output indicator, positive polarity
0xC313, 0xC288	ALM_MAG2 = 0x1388 = 5000 LSB = 50°/sec
0xC10A, 0xC0F0	ALM_MAG1 = 0x0AF0 = 2800 LSB = 0.7 g
0xC652	ALM_SMPL2[7:0] = 0x52 = 82 samples 82 samples ÷ 819.2 SPS = ~100 ms

# APPLICATIONS INFORMATION

## MOUNTING TIPS

The mounting and installation process can influence gyroscope bias repeatability and other key parametric behaviors. To preserve the best performance, use the following guidelines when developing an attachment approach for the [ADIS16445](#):

- Focus mounting force at the machine screw locations.
- Avoid direct force application on the substrate.
- Avoid placing mounting pressure on the package lid, except for the edges that border the exposed side of the substrate.
- Use a consistent mounting torque of 28 inch-ounces on mounting hardware.
- Avoid placing translational forces on the electrical connector.

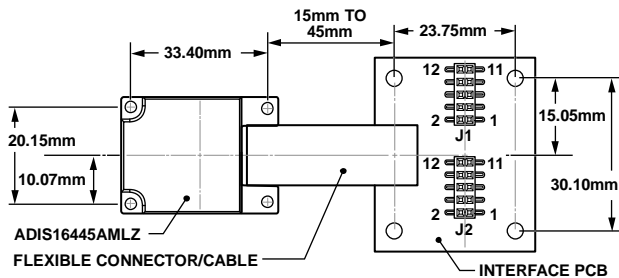
For more ideas on mounting ideas and tips, please refer to [Application Note AN-1305](#).

## POWER SUPPLY CONSIDERATIONS

The power supply must be within 3.15 V and 3.45 V for normal operation and optimal performance. During start up, the internal power conversion system starts drawing current when VDD reaches 1.6 V. The internal processor begins initializing when VDD is equal to 2.35 V. After the processor starts, VDD must reach 2.7 V within 128 ms. Also, make sure that the power supply drops below 1.6 V to shut the device down. Figure 9 shows a 10  $\mu$ F capacitor on the power supply. Using this capacitor supports optimal noise performance in the sensors.

## ADIS16445/PCBZ

The [ADIS16445/PCBZ](#) includes one [ADIS16445AMLZ](#), one interface PCB, and one flexible connector/cable. This particular flexible cable mates the [ADIS16445AMLZ](#) to any system that is currently using the [ADIS1636x](#), [ADIS16375](#), [ADIS1640x](#), or [ADIS1648x](#) IMU products, which use a 24-pin interface, rather than the 20-pin interface that the [ADIS16445](#) uses. This combination of components enables quicker installation for prototype evaluation and algorithm development. Figure 22 provides a mechanical design example for using these three components in a system.



- NOTES
1. USE FOUR M2 MACHINE SCREWS TO ATTACH THE ADIS16445.
  2. USE FOUR M3 MACHINE SCREWS TO ATTACH THE INTERFACE PCB.

Figure 22. Physical Diagram for Mounting the [ADIS16445/PCBZ](#)

Figure 23 provides the pin assignments for the interface board.

J1				J2			
RST	1	2	SCLK	DNC	1	2	GND
CS	3	4	DOUT	DNC	3	4	DIO3
DNC	5	6	DIN	GND	5	6	DIO4
GND	7	8	GND	DNC	7	8	DNC
GND	9	10	VDD	DNC	9	10	DNC
VDD	11	12	VDD	DIO2	11	12	DIO1

Figure 23. J1/J2 Pin Assignments for Interface PCB

## Installation

The following steps provide an example installation process for using these three components:

- Drill and tap M2 and M3 holes in the system frame, according to the locations in Figure 22.
- Install the [ADIS16445](#) using M2 machine screws. Use a mounting torque of 25 inch-ounces.
- Install the interface PCB using M3 machine screws.
- Connect J1 on the interface flex to the [ADIS16445AMLZ](#) connector.
- Connect J2 on the interface flex to J3 on the interface PCB. Note that J2 (interface flex) has 20 pins and J3 (interface PCB) has 24 pins. Make sure that Pin 1 on J2 (interface flex) connects to Pin 20 on J3 (interface PCB). J3 has a Pin 1 indicator to help guide this connection.
- Use J1 and J2 on the interface PCB to make the electrical connection with the system supply and embedded processor, using 12-pin, 1 mm ribbon cables. The following parts may be useful in building this type of cable: 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable).

The C1/C2 pads on the interface PCB do not have capacitors on them, but these pads can support the suggested power supply capacitor of 10  $\mu$ F (see Figure 9).

## PC-BASED EVALUATION TOOLS

The [EVAL-ADIS](#) supports PC-based evaluation of the [ADIS16445](#). Go to [www.analog.com/EVAL-ADIS](http://www.analog.com/EVAL-ADIS), to download the user guide ([UG-287](#)) and software (IMU evaluation).

OUTLINE DIMENSIONS

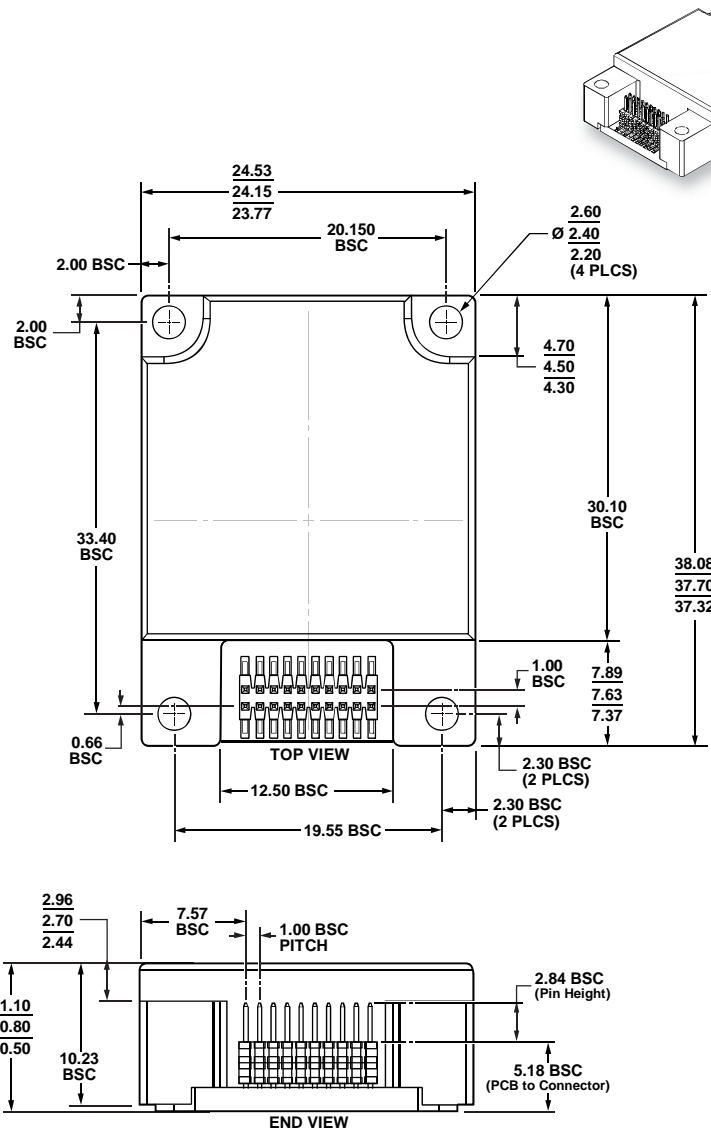


Figure 24. 20-Lead Module with Connector Interface [MODULE] (ML-20-3)  
Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADIS16445AMLZ	-40°C to +85°C	20-Lead Module with Connector Interface [MODULE]	ML-20-3
ADIS16445/PCBZ		Interface PCB	

<sup>1</sup> Z = RoHS Compliant Part.