I²C Guide

TEXAS INSTRUMENTS

Expanders, Multiplexers and Switches

Hubs, Translators, Buffers and Repeaters

2013

Table of Contents

Texas Instruments (TI) has supported the highly efficient I²C bus interface for many years. This overview provides an updated look at I²C applications and how TI's I/O expanders, multiplexers, buffers and repeaters can help system designers achieve effective subsystem communications using proven I²C devices.

History
During the 1980s, Philips (Koninklijke Philips Electronics N.V.) developed the two-wire inter-integrated circuit (I²C) bus to provide an easy way to connect multiple peripheral circuits to a central processing unit (CPU/MCU) in TV applications.

As circuits became more complex with many peripheral connections, a method was needed to simplify designs and reduce costs. By limiting the number of printed circuit board (PCB) traces and lowering general-purpose input and output (GPIO) usage on the microprocessor, the I²C bus met this requirement.

Operation
The I²C bus is used in a wide range of applications because it is simple and quick to use. It consists of a two-wire communication bus that supports bidirectional data transfer between a master and several slaves. The master or processor controls the bus – in particular, the serial clock (SCL) line. Data is transferred between the master and slave through a serial data (SDA) line. This data can be transferred in four speeds: standard mode (0 to 100 Kbps), fast mode (0 to 400 Kbps), fast-mode plus (0 to 1 Mbps) and high-speed mode (0 to 3.4 Mbps). The most common speeds are the standard and fast modes. See block diagram below for a generic system.

There can be more than one master on a system; the software protocol uses arbitration and synchronization to manage data collisions and loss.

Since successive specification enhancements are backward-compatible, mixed-speed communication is possible with the bus speed controlled by the processor or I²C master.

Typical I²C Features
- Requires one master (processor) and one or more slave devices
- Each device on the bus has a unique address
- Bus capacitive load: 550 pF max
- Rise time 1000 ns (standard mode), 300 ns (fast mode) and 120 ns (fast mode plus)

I²C Applications
The I²C bus is useful for many of today's microcontroller- and microprocessor-based systems or other systems linking many I/O devices. These systems may include applications in the following fields:

- Automotive
- Consumer
- Industrial
- Mobile
- PC/server
- Radio/TV
- Telephony
- Notebooks
- Battery-powered portable applications
- Telecom/networking

Many of the I²C bus products are designed to operate in the SMBus environment.
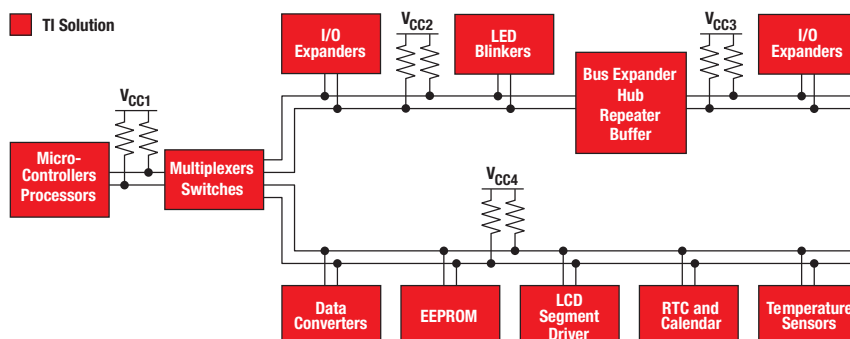
Block diagram of generic system using I²C devices

I²C Guide
I/O Expanders

The I²C I/O expanders (as shown in the block diagram) allow system layout to be greatly simplified. The two-wire bus reduces PCB complexity through trace reduction and routing simplification.

Key Features
- Easy board routing
- Board-space savings
- Processor-pin savings
- Low cost
- Industry standard

Applications
- Complements processors with limited I/Os
- Feature enhancements
- Keypad control
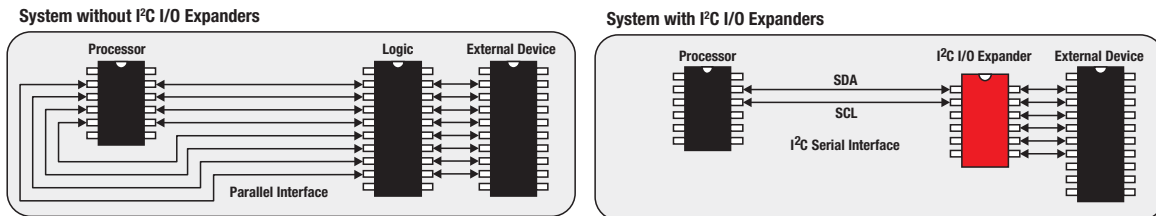
I/O expanders can simplify board layout

Low-Voltage I/O Expanders Selection Guide

Device	Max Frequency (kHz)	I²C Address	V_CC Range (V)	No. of I/Os	Additional Features					I/O Type		Pull-Up Integrated
					Low Power	Interrupt	Reset	Configuration Registers	5-V-Tolerant I/O	Push-Pull	Open-Drain	
LM8335	26 MHz	MIPI RFFE 0001 or 1001	1.8 to 3.3	8-bit	✔		✔	✔			✔	
TCA6408A	400	0100 00x	1.65 to 5.5	8-bit	✔	✔	✔	✔	✔	✔		
TCA6416A	400	0100 00x	1.65 to 5.5	16-bit	✔	✔		✔	✔	✔		
TCA6418E	1000	0110 100	1.65 to 3.6	18-bit	✔	✔	✔	✔		✔		
TCA6424A	400	0100 01x	1.65 to 5.5	24-bit	✔	✔	✔	✔	✔	✔		
TCA7408	1000	0100 00x	1.65 to 5.5	8-bit	✔	✔	✔	✔	✔	✔	✔	
TCA9535	400	0100 xxx	1.65 to 5.5	16-bit	✔	✔		✔	✔	✔		
TCA9538	400	1110 0xx	1.65 to 5.5	8-bit	✔	✔	✔	✔	✔	✔		
TCA9539	400	1110 1xx	1.65 to 5.5	16-bit	✔	✔	✔	✔	✔	✔		
TCA9554/A	400	0100 xxx/0111 xxx	1.65 to 5.5	8-bit	✔	✔		✔	✔	✔		✔
TCA9555	400	0100 xxx	1.65 to 5.5	16-bit	✔	✔		✔	✔	✔		✔

5-V tolerant on the GPIO sides.

*Preview products are listed in **bold teal**.*

I/O Expanders Selection Guide

| Device	Max I²C Frequency (kHz)	I²C Address	V_CC Range (V)	No. of I/Os	Additional Features					I/O Type		Pull-Up Integrated
					Low Power	Interrupt	Reset	Configuration Registers	5-V-Tolerant I/O	Push-Pull	Open-Drain	
PCA9536	400	1000 001	2.3 to 5.5	4-bit				✔	✔	✔		✔
PCA6107	400	0011 xxx	2.3 to 5.5	8-bit	✔	✔	✔	✔	✔	✔	✔	
PCA9534	400	0100 xxx	2.3 to 5.5	8-bit	✔	✔		✔	✔	✔		
PCA9534A	400	0111 xxx	2.3 to 5.5	8-bit	✔	✔		✔	✔	✔		
PCA9538	400	1110 0xx	2.3 to 5.5	8-bit	✔	✔	✔	✔	✔	✔		
PCA9557	400	0011 xxx	2.3 to 5.5	8-bit	✔		✔	✔	✔	✔	✔	
PCF8574	100	0100 xxx	2.5 to 6.0	8-bit		✔				✔		
PCF8574A	100	0111 xxx	2.5 to 6.0	8-bit		✔				✔		
PCF8575	400	0100 xxx	2.5 to 5.5	16-bit		✔				✔		
PCF8575C	400	0100 xxx	4.5 to 5.5	16-bit		✔					✔	

I²C Guide
Multiplexers and Switches

Low Voltage 8-Channel I²C Switch with Reset
TCA9548A

The I²C multiplexer/switch shown in this diagram allows further expansion of I²C systems while maintaining the simple two-wire bus. It can also perform voltage translation and segment isolation.
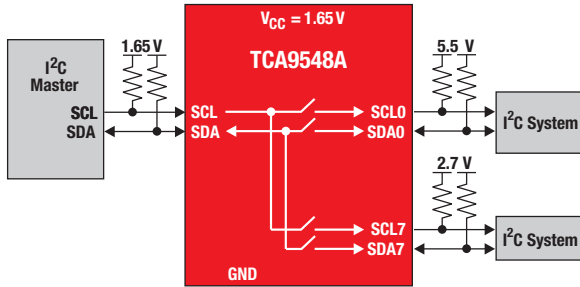
Dual bidirectional translating switch controlled via I²C bus

Key Features
- Pin savings on the I²C master, as each switch is activated or isolated through the I²C software
- Supports voltage-level translation for any bus voltages in the range of 1.65 V-5.5 V which is essential in mixed voltage I²C systems

Applications
- Resolves I²C address conflicts
- I²C bus isolation
- I²C bus expansion

Multiplexers and Switches Selection Guide

| Device	Max I²C Frequency (kHz)	I²C Address	V_CC Range (V)	Channel Width	Additional Features			
					Interrupt	Reset	Simultaneously Active Channel	5-V-Tolerant I/O
PCA9543A	400	1110 0xx	2.3 to 5.5	2-Channel	✔	✔	1 to 2	✔
PCA9544A	400	1110 xxx	2.3 to 5.5	4-Channel	✔		1	✔
PCA9545A	400	1110 0xx	2.3 to 5.5	4-Channel	✔	✔	1 to 4	✔
PCA9546A	400	1110 xxx	2.3 to 5.5	4-Channel		✔	1 to 4	✔
TCA9546A	400	1110 xxx	1.65 to 5.5	4-Channel		✔	1 to 4	✔
TCA9548A	400	1110 xxx	1.65 to 5.5	8-Channel		✔	1 to 8	✔

*Preview products are listed in **bold teal**.*

Hubs, Translators, Buffers and Repeaters

Level-Translating FM+ I²C Bus Repeater
TCA9617A

I²C hubs, buffers and repeaters permit bus expansion, sectional bus isolation, address conflict resolution and voltage-level translation, as shown in this diagram.
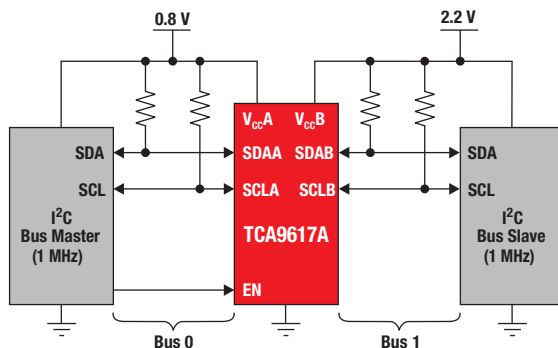
Two-channel bidirectional repeater

Key Features
- Can isolate a section on the I²C bus through enable (EN) pin
- Supports voltage-level translation from 0.8-V_{CCB} to 2.2 V-5.5 V buses, which is essential in mixed-voltage I²C systems
- Supports fast-mode plus (1 MHz)

Applications
- I²C-bus expansion through buffering of I²C signals
- Resolving address conflicts

I²C Guide

Hubs, Translators, Buffers and Repeaters (continued)

Hubs, Translators, Buffers and Repeaters Selection Guide

| Device | Max I²C Frequency (kHz) | I²C Address | V_CC Range (V) | Channel Width | Enable Pin | I²C Bus Capacitance Supported | | 5-V-Tolerant I/O | I/O Type | |
						Master Side (pF)	Each Slave Side (pF)		Push-Pull	Open-Drain
PCA9306	400	None	0 to 5.5		✔	Bypass	Bypass	✔		
PCA9515A/B	400	None	2.3 to 5.5	2-Channel	✔	400	400	✔		✔
P82B715	1,000	None	3.0 to 12.0	2-Channel		400	3000			
P82B96	400	None	2.0 to 15.0	2-Channel		400	4000	✔		✔
TCA4311A	400	None	2.7 to 5.5	2-Channel	✔	400	400	✔		✔
TCA9406	1 MHz	None	1.65 to 5.5		✔	Bypass	Bypass	✔	✔	✔
TCA9509	400	None	0.9 to 5.5	2-Channel	✔	50	400	✔		✔
TCA9517	400	None	0.9 to 5.5	2-Channel	✔	400	400	✔		✔
TCA9617A	1,000	None	0.9 to 5.5	2-Channel	✔	550	550	✔		✔

*Preview products are listed in **bold teal**.*

Types of I²C translators

	No Offset	Static Offset
TI Products	TCA9406, PCA9306	TCA9517/A, TCA9617A, TCA9509, PCA9515A/B, P82B96

Note: PCA9306 does not include integrated pull up resistors and one shot circuitry

	Incremental Offset	Amplifier
TI Products	TCA4311A	P82B715

$$V_{LOW2} = V_{LOW1} + 75\ mV + (V_{CC/R}) \times 100$$

Special Functions
LED Driver

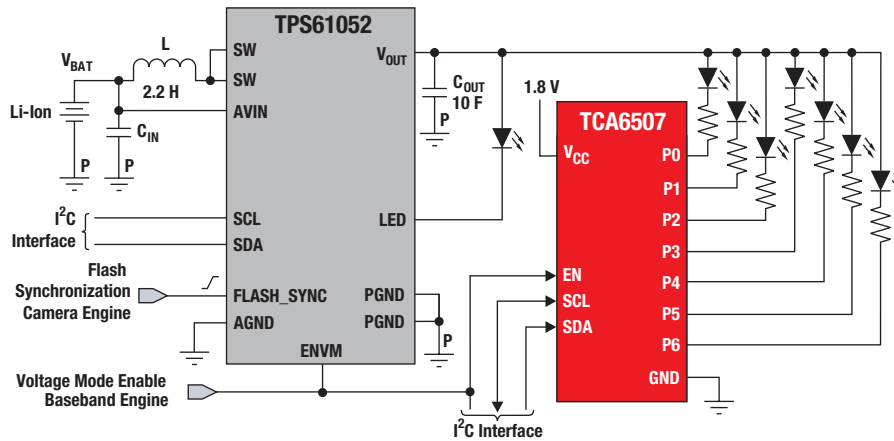### Low-Voltage 7-Bit I²C and SMBus LED Driver
TCA6507

The LED driver frees the processed from having to manage the LEDs. It will manage turning the LEDs on and off (per the required dimming rate). This will free up valuable processor time, thus creating a more efficient system.

White-LED flashlight driver and high-brightness LED indicator/backlight power supply

Key Features
- Supports brightness control and blink modes at the same time
- 1.8-V compatible for use with next-generation processors
- Multiple PWMs for multiple blink modes

Applications
- Fun light (decoration)
- Enhanced feature set
- Driving RGB LEDs
- Control function (indicator lights)

LED Drivers Selection Guide

| Device	Max I²C Frequency (kHz)	I²C Address	Max Unique Addresses	LED Output Channels	V_CC Range (V)	LED Voltage (Max) (V)	LED Output Current (mA)	Brightness Control (Bits)	Ch-Ch Accuracy (Max) (%)	Constant-Current LED Output	Open-drain LED Output
TLC59108	1000	100x xxx	14	8	3 - 5.5	17	120	8	±3	✔	
TLC59108F	1000	100x xxx	14	8	3 - 5.5	17	120	8	N/A		✔
TLC59208F	1000	Various	64	8	3 - 5.5	17	50	8	N/A		✔
TLC59116	1000	110x xxx	14	16	3 - 5.5	17	120	8	±6	✔	
TLC59116F	1000	110x xxx	14	16	3 - 5.5	17	120	8	N/A		✔
TCA6507	400	1000 101	1	7	1.65 - 3.6	5.5	40	4	N/A		✔
LM3435	1000	0101 000	1	3	2.7 - 5.5	5.5	2000	10	±3	✔	
LP5521	400	0110 xxx	4	3	2.7 - 5.5	6	25.5	8	±2	✔	
LP5523	400	0110 xxx	4	9	2.7 - 5.5	6	25.5	8	±2.5	✔	
LP8501	400	0110 010	1	9	2.7 - 5.5	6	25.5	8	±2.5	✔	
LP3943	400	0110 xxx	8	16	2.3 - 5.5	6	25	8	—		✔

5-V tolerant on the GPIO sides.

I²C Guide
LCD Bias

Fully I²C programmable 6 Channel LCD Bias IC
TPS65177

The TPS65177 is a fully I²C programmable six-channel LCD Bias IC for all television sizes and includes Gate Pulse Modulation. The device provides all supply rails needed by a GIP (Gate-in-Panel) or non-GIP TFT-LCD panel.
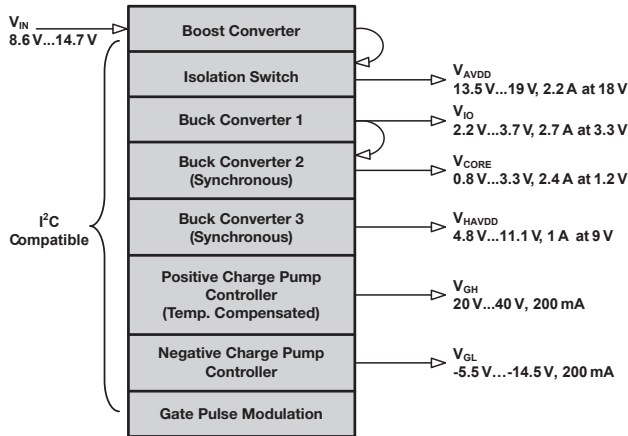
TPS65177 block diagram

Key Features
- Temperature compensation for V_{GH}
- 40-pin 6x6 mm QFN package
- Input voltage: 8.6 V to 14.7 V
- Integrated V_{AVDD} isolation switch
- Three-bit programmable switch current limit up to 4.25 A
- Four-bit programmable high voltage stress mode
- One-bit programmable soft-start
- 1.7 A switch current limit
- Four-bit programmable high voltage stress mode

Applications
- GIP (Gate-in-Panel) LCD TVs
- Non-GIP LCD TVs

LCD Bias Selection Guide

Device	V_{IN} (V)	Boost ILimit (min) (A)	Buck ILimit (min) (A)	Isolation Switch	V_{GH}	V_{GL}	GVS	Other	Price*
TPS65168	12	3.5	2.8	Integrated	Controller	Controller	—	I²C programmable, 2 buck, temp. compensation, reset	2.10
TPS65177	12	4.25	3	Integrated	Controller	Controller	Yes	Temp compensation, I²C, 1 boost, 3 bucks	1.90
TPS65178	12	3.5	2.6	Integrated	Controller	Controller	—	Integrated 6-ch gamma buffer, I²C, V_{com}, bucks for V_{HVDD}, V_{CC}, V_{CORE}, V_{EPI}, boost for V_{DD}	1.90

Suggested resale price in U.S. dollars in quantities of 1,000.

Single-Wire Interface

Low Voltage 5-Bit Self-Timed, Single-Wire Output Expander
TCA5405

The TCA5405 is a 5-bit output expander controlled using a single wire input. This device is ideal for portable applications as it has a wide V_{CC} range of 1.65 V to 3.6 V. The TCA5405 uses a self-timed serial data protocol with a single data input driven by a master device synchronized to an internal clock of that device. During a Setup phase, the bit period is sampled, then the TCA5405 generates its own internal clock synchronized to that of the Master device to sample the input over a five-bit-period Data Transfer phase and writes the bit states on the parallel outputs after the last bit is sampled. The TCA5405 is available in an 8-pin 1.5mm x 1.5mm RUG µQFN package.
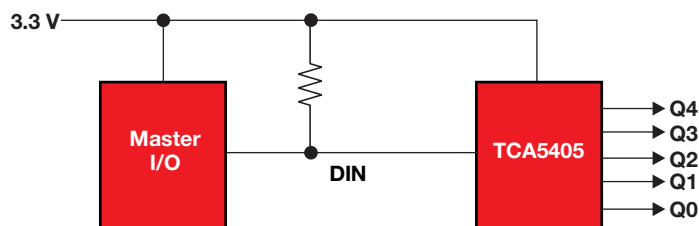
TCA5405 block diagram

Key Features
- Operating power-supply voltage range of 1.65 V to 3.6 V
- Five independent push-pull outputs
- Single input (DIN) controls state of all outputs
- High-current drive outputs maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model
  - 1000-V charged-device model

Applications
- Cell phones
- PDAs
- Portable media players
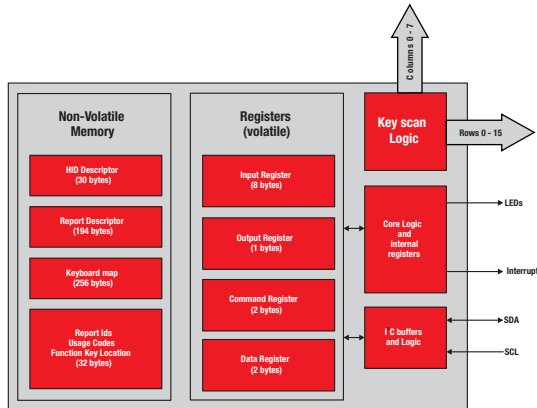- MP3 players
- Portable instrumentation

I²C Guide
Keypad Controller

Low-Voltage 8x16 Keyboard Scanner with HID over I²C Compliant Interface
TCA8424

The TCA8424 keypad controller frees the processor from having to scan the keypad for presses and releases. It is a keypad scan device with 18 GPIOs that can be configured into 8 inputs and 16 outputs to support up to an 8 x 16 keypad array (128 buttons).

TCA8424 simplified block diagram

Key Features
- Smaller package options
- Lower power consumption
- No firmware development
- Support of 128 keys

Applications
- Smart phones
- Notebooks
- GPSs
- MP3 players
- Tablets

I²C-Compatible Keypad Controller with GPIO, PWM, and IEC61000 ESD Protection
LM8330

The LM8330 I/O Expander and Keypad Controller is a dedicated device designed to unburden a host processor from scanning a matrix-addressed keypad and to provide flexible and general purpose, host programmable input/output functions. Three independent Pulse Width Modulation (PWM) timer outputs are provided for dynamic LED brightness modulation.
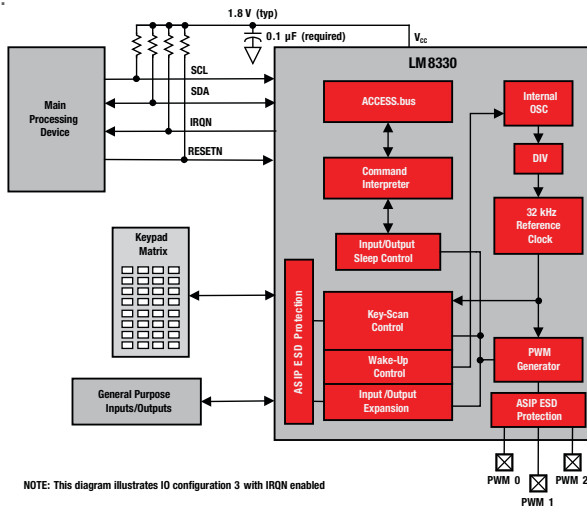
NOTE: This diagram illustrates IO configuration 3 with IRQN enabled

LM8330 block diagram

Key Features
- Unburden a host processor from scanning a matrix-addressed keypad
- Ultra-low-power operation
- No need for external RC passives for ESD

Applications
- Mobile phones
- Qwerty keyboard
- Universal remote

I/O Expander and Keypad Controller Selection Guide

Device	No. of I/O's	Max I²C Frequency (kHz)	V_CC (Min) (V)	V_CC (Max) (V)	I²C Address	Pin/Package
LM8330	20	400	1.65	3.6	Yes; ACCESS.bus	DSBGA-25
TCA8418	18	1000	1.65	3.6	0110 100	WQFN-24
TCA8418E	18	1000	1.65	3.6	0110 100	DSBGA-25
TCA8424	24	1000	1.65	3.6	0111 011	VQFN-40

*New products are listed in **bold red**.*

Texas Instruments

Q. Why doesn't the slave device respond to the master after an I2C call is made from the master?

A. • If the device is not responding properly, there may be an I2C protocol violation.
  ◦ To begin, a proper I2C start condition must be issued.
  ◦ After stop condition, the master must reissue the start condition.
  ◦ After every start condition, the master must send the full slave address.
  ◦ During communication, if the master issues a restart condition, the full slave address must be sent.
  ◦ If the device does not respond with an ACK, it did not recognize the address.
 • Partial data cannot be written to the I/O.
  ◦ To write to the I/O, complete 8-bit data must be sent to the slave.
  ◦ If fewer than 8 bits are sent, the slave will not respond with an ACK and will not update the I/O port.

Q. When using I2C I/O expanders, what is the functionality difference between power-on reset and /RESET? (See figure on this page.)

A. Power-on reset:
 • When power (from 0 V) is applied to the V_{CC}, the internal power-on reset holds the device in a reset condition until V_{CC} reaches Vpor (~1.4 V).
 • Once V_{CC} reaches Vpor, the internal registers and I2C/SMBus state machine are initialized to their default states.
 • After this, the device can be returned to its default reset state if V_{CC} is lowered to 0 V.

 /RESET:
 • Simply asserting a low on the /RESET input returns the device to its default state.

• Creates the same effect as a power-on reset without power cycling the device.
• The /RESET input is 5.5-V tolerant (regardless of voltage level on V_{CCP}).
• Partial data cannot be written to the I/O.
  ◦ To write to the I/O, complete 8-bit data must be sent to the slave.
  ◦ If fewer than 8 bits are sent, the slave will not respond with an ACK and will not update the I/O port.

Q. How should an unused /RESET pin be terminated?

A. /RESET is an input to the master. It requires a pull-up resistor to V_{CC} if no active connection is used.

Q. What is the functionality of the interrupt (/INT) control?

A. • The /INT is an open-drain output in the I2C slave. It is used to inform the I2C master if any of the inputs in the slave device have changed state.
 • If any of the I/Os configured as inputs change state before the I/O is read (i.e., if a mismatch between the I/O and the contents of the internal input register occurs), /INT will become low.
 • /INT is not affected by I/Os configured as outputs.
 • /INT can be tied to any voltage (or V_{CC} pin) up to 5.5 V through a pull-up resistor.

Q. How should an unused /INT pin be terminated?

A. /INT is an open-drain output that requires a pull-up resistor for proper operation. If /INT is not used, it can be left open or connected directly to GND.

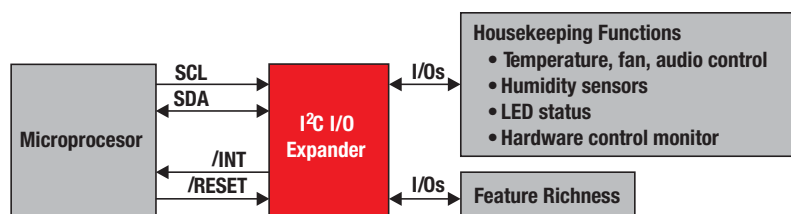Q. What is the power-on default for the interrupt (/INT) pin?

A. High.

Q. How can an /INT be cleared (returned back to high state)?

A. • Read (clock) the data on the I/O port that generated the /INT.
 • Change the data on the I/O to the original setting.
 • A stop event will clear the /INT.

Q. How can a low /INT be avoided at power up in I2C I/O expanders?

A. • At power up, the P ports are configured as inputs by default.
 • When power up ends and the device has a valid V_{CC} value, the input port (P port) is compared to the internal input register (no clock needed), and /INT goes active (low) unless there is a match.
 • The internal input registers are designed to power up with all ones or high.
 • The /INT should start high at power up if the P port is initially high (all ones) to match the internal input register.

Housekeeping Functions
 • Temperature, fan, audio control
 • Humidity sensors
 • LED status
 • Hardware control monitor

Microprocesor — SCL / SDA — I²C I/O Expander — I/Os

/INT / /RESET

I/Os — Feature Richness

Typical I²C I/O expander applications

Resources
Frequently Asked Questions

Q. What is the power-on default for the P port (I/O port) in an I2C I/O expander?

A. For the PCF8574/A, PCF8575 and devices with internal pull-up resistors like the PCA9536, PCA9554, PCA9554A and PCA9555, the input default is high.

For the PCF8575C and devices without internal pull-up resistors, the input is 3-state.

Q. What is a fun light and what is its purpose?

A. • Fun lights are any set of lights used for less critical tasks such as:
  ○ Decoration.
  ○ Enhancing the feature set of an application.
  ○ Control functions (such as indicator lights).
  • Fun lights are mostly found on battery-powered portable applications:
  ○ Notebooks
  ○ Handsets
  ○ Consumer portables
  ○ Portable media players
  • Some example fun-light applications are:
  ○ Predictive key entry for text messages.
  ○ Making a smartphone flash to remind the user of an appointment.
  ○ Providing battery-charging status.
  ○ Enhancing audio experience through supporting a "base."

Solution No. 1: Using Legacy I2C Devices
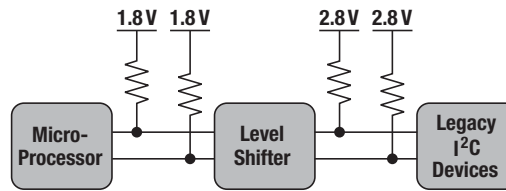
Solution No. 2: Using TCA Devices
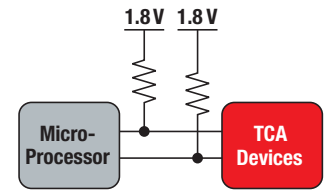
Q. How should an unused I/O pin in an I2C I/O expander be terminated?

A. For devices with internal resistors between V_{CC} and the I/O, such as PCA9555, PCA9536 and PCA9554/A, the I/O can be connected directly to V_{CC} or GND.

For devices without internal resistors, a resistor can be used to terminate unused I/Os to V_{CC} or GND.

Q. What are the benefits of using TCA-series devices? (See figure above.)

A. • Low-voltage operation. TCA-series devices provide a one-chip interface with processors operating at 1.8 V to:
  ○ Save board costs.
  ○ Save board space.
  ○ Provide better inventory management.
  • Wide-voltage operation:
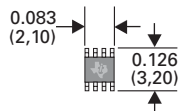 ○ Can interface with legacy and next-generation processors.
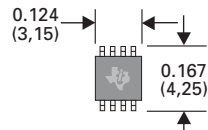 • Low power consumption.

Resources

Packages
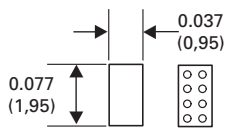
8-ball WCSP NanoFree™ package (YZP)
0.037 (0,95)
0.077 (1,95)
Ball pitch = 0.020 (0,50)
Height = 0.020 (0,50)
Area = 0.003 (1,85)

8-pin US8/VSSOP (DCU)
0.083 (2,10)
0.126 (3,20)
Lead pitch = 0.020 (0,50)
Height = 0.035 (0,90)
Area = 0.010 (6,72)

8-pin SM8/SSOP (DCT)
0.124 (3,15)
0.167 (4,25)
Lead pitch = 0.026 (0,65)
Height = 0.051 (1,30)
Area = 0.010 (6,72)

8-pin QFN (RUG)
1.55 (1,45)
Lead pitch = 0.020 (0,5)
Height = 0.015 (0,37)
Area = 2.4025 mm²
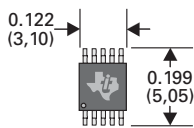
10-pin MSOP (DGS)
0.122 (3,10)
0.199 (5,05)
Lead pitch = 0.020 (0,50)
Height = 0.043 (1,10)
Area = 0.024 (15,7)
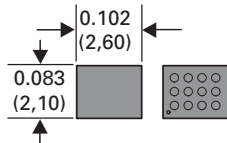
12-ball UFBGA (ZXU)
0.102 (2,60)
0.083 (2,10)
Ball pitch = 0.020 (0,50)
Height = 0.016 (0,41)
Area = 0.008 (5,46)
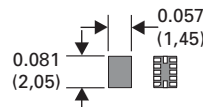
12-pin QFN (RUE)
0.057 (1,45)
0.081 (2,05)
Lead pitch = 0.016 (0,40)
Height = 0.016 (0,40)
Area = 0.005 (2,97)
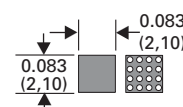
16-pin µCSP (ZSZ)
0.083 (2,10)
0.083 (2,10)
Lead pitch = 0.50 (0.019685 in)
Height = 0.55 (0.02165 in)
Area = 4.0 mm²
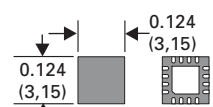
16-pin QFN (RGT)
0.124 (3,15)
0.124 (3,15)
Lead pitch = 0.020 (0,50)
Height = 0.039 (1,00)
Area = 0.015 (9,9)
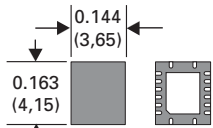
16-pin QFN (RGY)
0.144 (3,65)
0.163 (4,15)
Lead pitch = 0.020 (0,50)
Height = 0.039 (1,00)
Area = 0.023 (15,1)
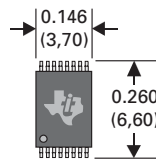
16-pin TVSOP (DGV)
0.146 (3,70)
0.260 (6,60)
Lead pitch = 0.016 (0,40)
Height = 0.047 (1,20)
Area = 0.038 (24,4)
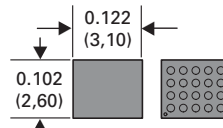
20-ball VFBGA (ZXY)
0.122 (3,10)
0.102 (2,60)
Ball pitch = 0.020 (0,50)
Height = 0.016 (0,41)
Area = 0.012 (8,1)
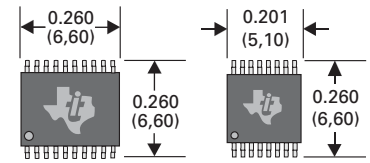
16-/20-pin TSSOP (PW)
0.260 (6,60)
0.201 (5,10)
0.260 (6,60)
0.260 (6,60)
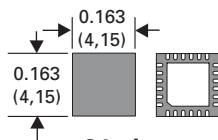Lead pitch = 0.026 (0,65)
Height = 0.047 (1,20)
Area (20-pin) = 0.068 (44)
Area (16-pin) = 0.052 (33,7)
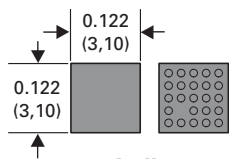
24-ball VFBGA (ZQS)
0.122 (3,10)
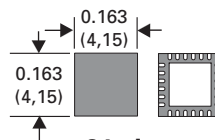0.122 (3,10)
Ball pitch = 0.020 (0,50)
Height = 0.030 (0,77)
Area = 0.015 (9,61)

24-pin QFN (RGE)
0.163 (4,15)
0.163 (4,15)
Lead pitch = 0.020 (0,50)
Height = 0.039 (1,00)
Area = 0.027 (17,2)

24-pin QFN (RTW)
0.163 (4,15)
0.163 (4,15)
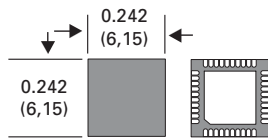Lead pitch = 0.020 (0,50)
Height = 0.032 (0,80)
Area = 0.027 (17,2)
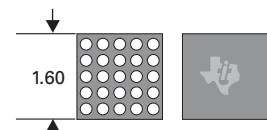
25-ball WCSP (YFP)
1.60
Lead pitch = 0.016 (0,40)
Height = 0.020 (0,50)
Area = 4 mm²

40-pin QFN (RHA)
0.242 (6,15)
0.242 (6,15)
Lead pitch = 0.020 (0,50)
Height = 0.039 (1,00)
Area = 0.059 (37,8)

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