# 2:1 High Speed Video Multiplexer

## General Description

The LMH®6570 is a high performance analog multiplexer optimized for professional grade video and other high fidelity high bandwidth analog applications. The output amplifier selects one of two buffered input signals based on the state of the SEL pin. The LMH6570 provides a 400 MHz bandwidth at 2 $V_{PP}$ output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the LMH6570's 0.1 dB bandwidth of 150 MHz and its 2200 V/µs slew rate.

The LMH6570 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. An 80 mA linear output current is available for driving multiple video load applications.

The LMH6570 gain is set by external feedback and gain set resistors for maximum flexibility.

The LMH6570 is available in the 8-pin SOIC package.

## Features

- 500 MHz, 500 $mV_{PP}$, −3 dB bandwidth, $A_V=2$
- 400 MHz, 2$V_{PP}$, −3 dB bandwidth, $A_V=2$
- 8 ns channel switching time
- 70 dB channel to channel isolation @ 10 MHz
- 0.02%, 0.05° diff. gain, diff. phase
- 0.1 dB gain flatness to 150 MHz
- 2200 V/µs slew rate
- Wide supply voltage range: 6V (±3V) to 12V (±6V)
- −68 dB HD2 @ 5 MHz
- −84 dB HD3 @ 5 MHz

## Applications

- Video router
- Multi input video monitor
- Instrumentation / Test equipment
- Receiver IF diversity switch
- Multi channel A/D driver
- Picture in Picture video switch

## Connection Diagram



**8-Pin SOIC**

**Top View**

20129905
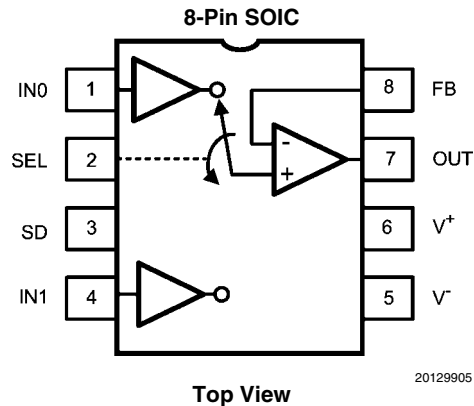
## Truth Table

| SEL | SD | OUTPUT |
|---|---|---|
| 1 | 0 | IN1 * (1+RF/RG) |
| 0 | 0 | IN0 * (1+RF/RG) |
| X | 1 | Shutdown |

## Absolute Maximum Ratings (*Note 1*)

**If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance | (*Note 4*) |
| Human Body Model | 2000V |
| Machine Model | 200V |
| Supply Voltage (V+ − V−) | 13.2V |
| $I_{OUT}$ (*Note 3*) | 130 mA |
| Signal & Logic Input Pin Voltage | ±(V$_S$+0.6V) |
| Signal & Logic Input Pin Current | ±20 mA |
| Maximum Junction Temperature | +150°C |
| Storage Temperature Range | −65°C to +150°C |
| Soldering Information | |
| See product folder at www.ti.com and www.ti.com/ lit/an/snoa549c /snoa549c.pdf. | |

## Operating Ratings

(*Note 1*)

| | | |
|---|---|---|
| Operating Temperature | −40 °C to 85 °C | |
| Supply Voltage Range | 6V to 12V | |
| **Thermal Resistance** | | |
| Package | (θ$_{JA}$) | (θ$_{JC}$) |
| 8-Pin SOIC | 150°C/W | 50°C/W |

## ±5V Electrical Characteristics

V$_S$ = ±5V, R$_L$ = 100Ω, R$_F$=576Ω, A$_V$=2 V/V, T$_J$=25 °C, Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

| Symbol | Parameter | Conditions (*Note 2*) | Min (*Note 5*) | Typ (*Note 9*) | Max (*Note 5*) | Units |
|---|---|---|---|---|---|---|
| **Frequency Domain Performance** | | | | | | |
| SSBW | −3 dB Bandwidth | V$_{OUT}$ = 0.5 V$_{PP}$ | | 500 | | MHz |
| LSBW | −3 dB Bandwidth | V$_{OUT}$ = 2 V$_{PP}$ | | 400 | | MHz |
| .1 dBBW | 0.1 dB Bandwidth | V$_{OUT}$ = 0.25 V$_{PP}$ | | 150 | | MHz |
| DG | Differential Gain | R$_L$ = 150Ω, f=4.43 MHz | | 0.02 | | % |
| DP | Differential Phase | R$_L$ = 150Ω, f=4.43 MHz | | 0.05 | | deg |
| XTLK | Channel to Channel Crosstalk | All Hostile, f = 5 MHz | | −70 | | dBc |
| **Time Domain Response** | | | | | | |
| TRS | Channel to Channel Switching Time | Logic transition to 90% output | | 8 | | ns |
| | Enable and Disable Times | Logic transition to 90% or 10% output. | | 10 | | ns |
| TRL | Rise and Fall Time | 4V Step | | 2.4 | | ns |
| TSS | Settling Time to 0.05% | 2V Step | | 17 | | ns |
| OS | Overshoot | 2V Step | | 5 | | % |
| SR | Slew Rate | 4V Step, (*Note 8*) | | 2200 | | V/µs |
| **Distortion** | | | | | | |
| HD2 | 2$^{nd}$ Harmonic Distortion | 2 V$_{PP}$ , 5 MHz | | −68 | | dBc |
| HD3 | 3$^{rd}$ Harmonic Distortion | 2 V$_{PP}$ , 5 MHz | | −84 | | dBc |
| IMD | 3$^{rd}$ Order Intermodulation Products | 10 MHz, Two tones 2 Vpp at output | | −80 | | dBc |
| **Equivalent Input Noise** | | | | | | |
| VN | Voltage | >1 MHz, Input Referred | | 5 | | nV$\sqrt{Hz}$ |
| ICN | Current | >1 MHz, Input Referred | | 5 | | pA$\sqrt{Hz}$ |
| **Static, DC Performance** | | | | | | |

| Symbol | Parameter | Conditions (*Note 2*) | Min (*Note 5*) | Typ (*Note 9*) | Max (*Note 5*) | Units |
|--------|-----------|----------------------|-----|-----|-----|-------|
| CHGM | Channel to Channel Gain Difference | DC, Difference in gain between channels | | ±0.005 | ±0.034 **±0.036** | % |
| VIO | Input Offset Voltage | $V_{IN}$ = 0V | | 1 | ±15 **±21** | mV |
| DVIO | Offset Voltage Drift (*Note 10*) | | | 30 | | µV/°C |
| IBN | Input Bias Current (*Note 7*) | $V_{IN}$ = 0V | | −3 | ±8 **±10** | µA |
| DIBN | Bias Current Drift (*Note 10*) | | | 11 | | nA/°C |
| IBI | Inverting Input Bias Current (*Note 7*) | Pin 8, Feedback point, $V_{IN}$ = 0V | | −3 | ±18 **±22** | uA |
| PSRR | Power Supply Rejection Ratio | DC, Input referred | 48 **46** | 50 | | dB |
| ICC | Supply Current | No Load, Shutdown Pin (SD) > 0.8V | | 13.8 | 15 **16** | mA |
| | Supply Current Shutdown | Shutdown Pin (SD) > 2V | | 1.1 | 1.3 **1.4** | mA |
| VIH | Logic High Threshold | Select Pin & Shutdown pin (SEL, SD) | 2.0 | | | V |
| VIL | Logic Low Threshold | Select Pin & Shutdown pin (SEL, SD) | | | 0.8 | V |
| IiL | Logic Pin Input Current Low (*Note 7*) | Logic Input = 0V Select Pin & Shutdown pin (SEL, SD) | −8 **-10** | −1 | | µA |
| IiH | Logic Pin Input Current High (*Note 7*) | Logic Input = 5.0V, Select Pin & Shutdown pin (SEL, SD) | | 57 | 68 **75** | µA |
| **Miscellaneous Performance** | | | | | | |
| RIN+ | Input Resistance | | | 5 | | kΩ |
| CIN | Input Capacitance | | | 0.8 | | pF |
| ROUT | Output Resistance | Output Active, (SD < 0.8V) | | 0.04 | | Ω |
| ROUT | Output Resistance | Output Disabled, (SD > 2V) | | 3000 | | Ω |
| COUT | Output Capacitance | Output Disabled, (SD > 2V) | | 3.1 | | pF |
| VO | Output Voltage Range | No Load | ±3.51 **±3.50** | ±3.7 | | V |
| VOL | | $R_L$ = 100Ω | ±3.16 **±3.15** | ±3.5 | | V |
| CMIR | Input Voltage Range | | ±2.5 | ±2.6 | | V |
| IO | Linear Output Current (*Note 7*) | $V_{IN}$ = 0V, | +60 -70 **±55** | ±80 | | mA |
| ISC | Short Circuit Current(*Note 3*) | $V_{IN}$ = ±2V, Output shorted to ground | | ±230 | | mA |

## ±3.3V Electrical Characteristics

$V_S$ = ±3.3V, $R_L$ = 100Ω, $R_F$=576Ω, $A_V$=2 V/V; Unless otherwise specified.

| Symbol | Parameter | Conditions (*Note 2*) | Min (*Note 5*) | Typ (*Note 9*) | Max (*Note 5*) | Units |
|--------|-----------|----------------------|-----|-----|-----|-------|
| **Frequency Domain Performance** | | | | | | |
| SSBW | −3 dB Bandwidth | $V_{OUT}$ = 0.5 $V_{PP}$ | | 475 | | MHz |
| LSBW | −3 dB Bandwidth | $V_{OUT}$ = 2.0 $V_{PP}$ | | 375 | | MHz |
| 0.1 dBBW | 0.1 dB Bandwidth | $V_{OUT}$ = 0.5 $V_{PP}$ | | 100 | | MHz |
| GFP | Peaking | DC to 200 MHz | | 0.4 | | dB |
| XTLK | Channel to Channel Crosstalk | All Hostile, f = 5 MHz | | −70 | | dBc |
| **Time Domain Response** | | | | | | |
| TRL | Rise and Fall Time | 2V Step | | 2 | | ns |

| Symbol | Parameter | Conditions (Note 2) | Min (Note 5) | Typ (Note 9) | Max (Note 5) | Units |
|--------|-----------|---------------------|--------------|--------------|--------------|-------|
| TSS | Settling Time to 0.05% | 2V Step | | 20 | | ns |
| OS | Overshoot | 2V Step | | 5 | | % |
| SR | Slew Rate | 2V Step | | 1400 | | V/µs |
| **Distortion** | | | | | | |
| HD2 | 2nd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −67 | | dBc |
| HD3 | 3rd Harmonic Distortion | 2 $V_{PP}$, 10 MHz | | −87 | | dBc |
| **Static, DC Performance** | | | | | | |
| VIO | Input Offset Voltage | $V_{IN}$ = 0V | | 1 | | mV |
| IBN | Input Bias Current (Note 7) | $V_{IN}$ = 0V | | -3 | | µA |
| PSRR | Power Supply Rejection Ratio | DC, Input Referred | | 49 | | dB |
| ICC | Supply Current | No Load | | 12.5 | | mA |
| VIH | Logic High Threshold | Select Pin & Shutdown pin (SEL, SD), VIH ≅V+ * 0.4 | | 1.3 | | V |
| VIL | Logic Low Threshold | Select Pin & Shutdown pin (SEL, SD), VIL ≅V+ * 0.12 | | 0.4 | | V |
| **Miscellaneous Performance** | | | | | | |
| RIN+ | Input Resistance | | | 5 | | kΩ |
| CIN | Input Capacitance | | | 0.8 | | pF |
| ROUT | Output Resistance | | | 0.06 | | Ω |
| VO | Output Voltage Range | No Load | | ±2 | | V |
| VOL | | $R_L$ = 100Ω | | ±1.8 | | V |
| CMIR | Input Voltage Range | | | ±1.2 | | V |
| IO | Linear Output Current (Note 3) | $V_{IN}$ = 0V | | ±60 | | mA |
| ISC | Short Circuit Current (Note 3) | $V_{IN}$ = ±1V, Output shorted to ground | | ±150 | | mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

**Note 2:** Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$. See Applications Section for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

**Note 3:** The maximum output current ($I_{OUT}$) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the Power Dissipation section of the Application Section for more details. A short circuit condition should be limited to 5 seconds or less.

**Note 4:** Human Body model, 1.5kΩ in series with 100 pF. Machine model, 0Ω In series with 200 pF

**Note 5:** Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

**Note 6:** Parameter guaranteed by design.

**Note 7:** Positive Value is current into device.

**Note 8:** Slew Rate is the average of the rising and falling edges.

**Note 9:** Typical numbers are the most likely parametric norm.

**Note 10:** Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

# Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---------|-------------|-----------------|-----------------|-------------|
| 8-Pin SOIC | LMH6570MA | LMH6570MA | 95 Units/Rail | M08A |
| | LMH6570MAX | | 2.5k Units Tape and Reel | |

# Typical Performance Characteristics

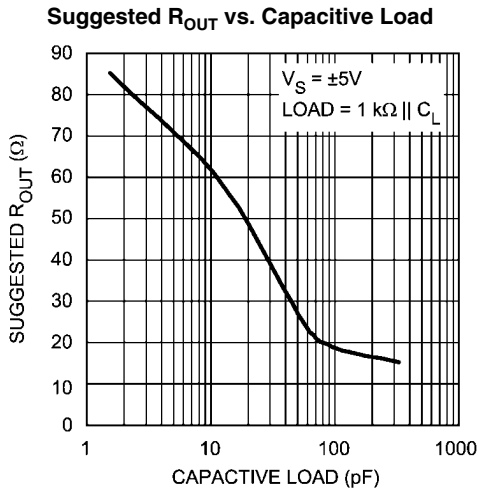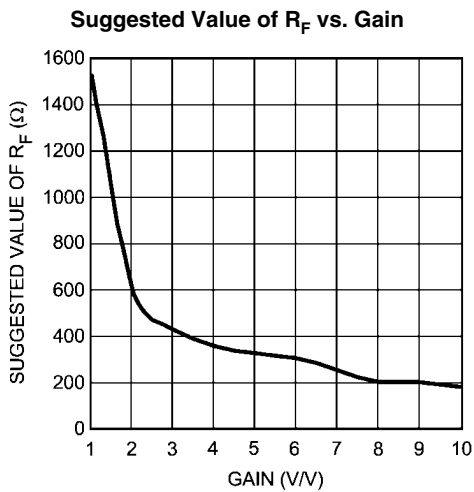$V_S = \pm 5V$, $R_L = 100\Omega$, $A_V = 2$, $R_F = R_G = 576\Omega$; unless otherwise specified.
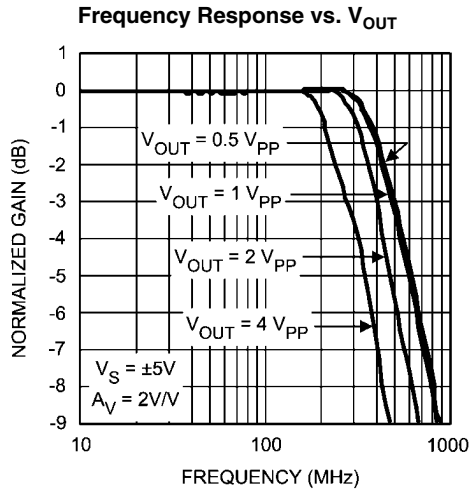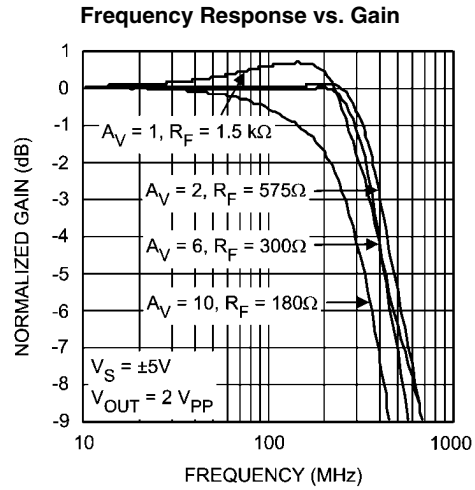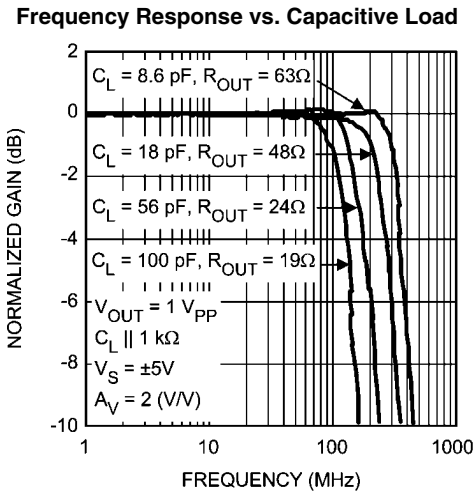
**Frequency Response vs. $V_{OUT}$**



20129902

**Frequency Response vs. Gain**



20129903

**Frequency Response vs. Capacitive Load**



20129914

**Suggested $R_{OUT}$ vs. Capacitive Load**



20129915

**Suggested Value of $R_F$ vs. Gain**



20129901

**Pulse Response 4$V_{PP}$**



20129925

**Pulse Response 2V$_{PP}$**

$V_S = \pm5V$

**Pulse Response 2V$_{PP}$**

$V_S = \pm3.3V$

20129929

20129930

**Closed Loop Output Impedance**

DISABLED

$V_S = \pm5V$
$V_{IN} = 0V$
$A_V = 2V/V$

ENABLED

20129908

**Closed Loop Output Impedance**

DISABLED

$V_S = \pm5V$
$V_{IN} = 0V$
$A_V = 1V/V$

ENABLED

20129909

**PSRR vs. Frequency**

PSRR +

PSRR -

20129904

**Channel Switching**

CH 1

CH 0

CONTROL SIGNAL
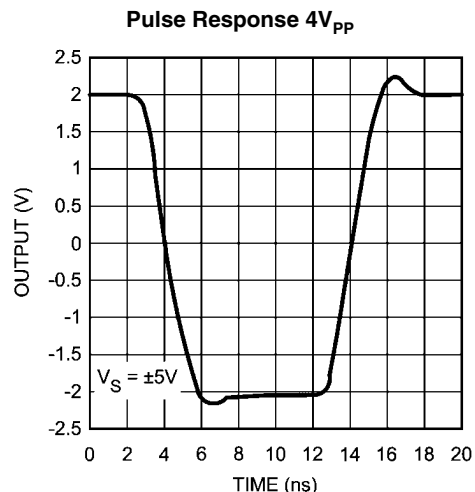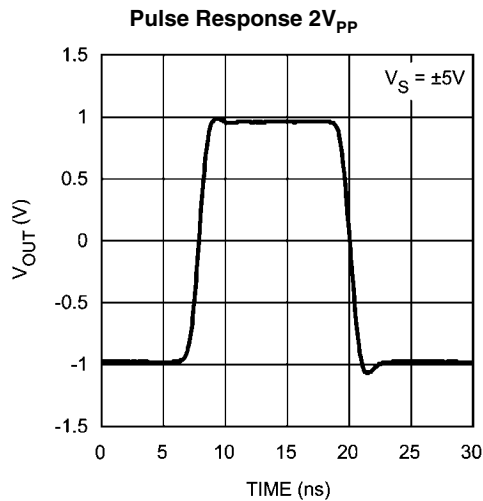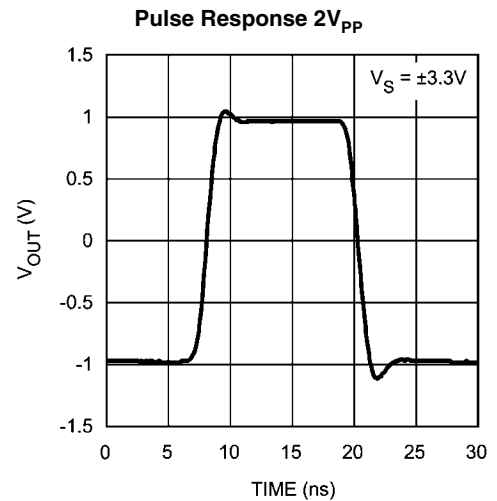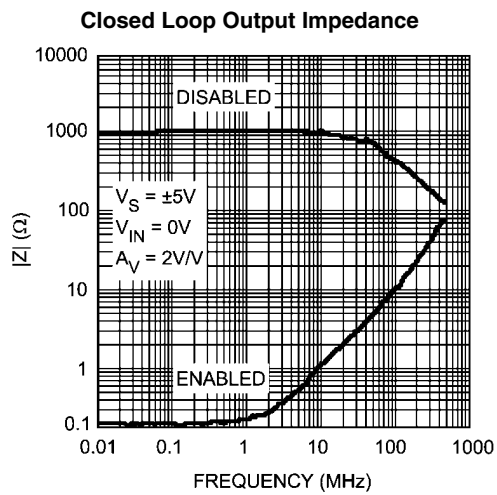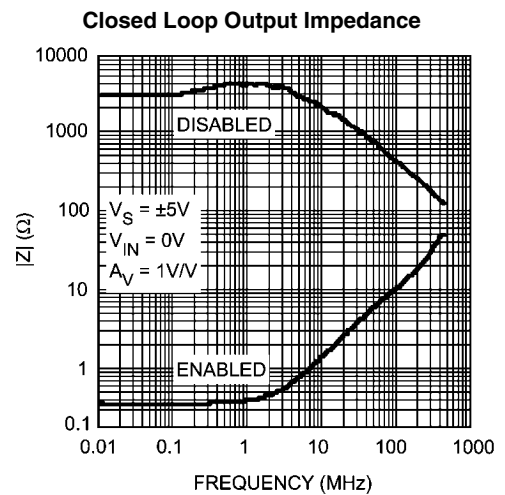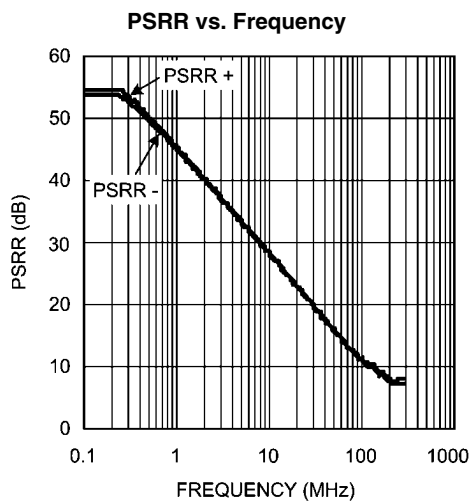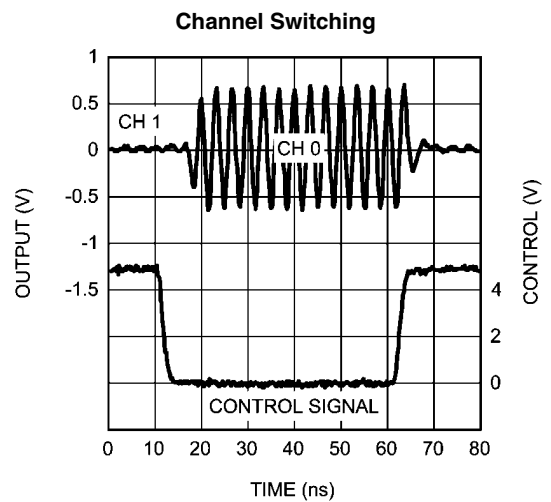
20129916

**SHUTDOWN Switching**
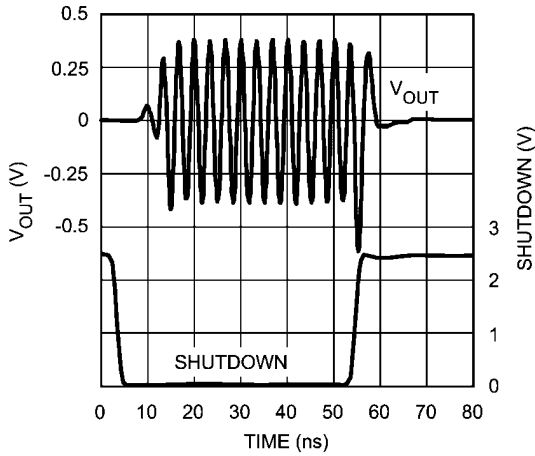


20129921

**Shutdown Glitch**
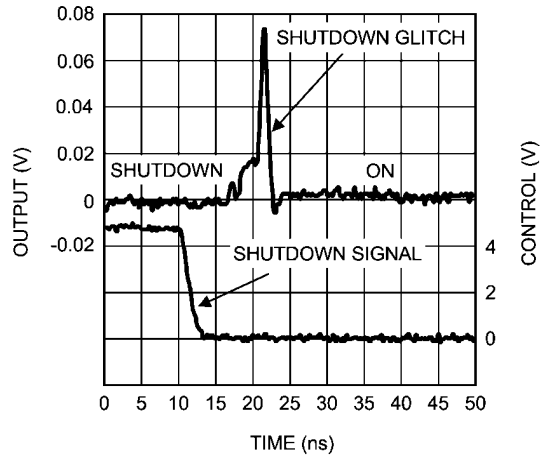


20129927

**HD2 vs. Frequency**
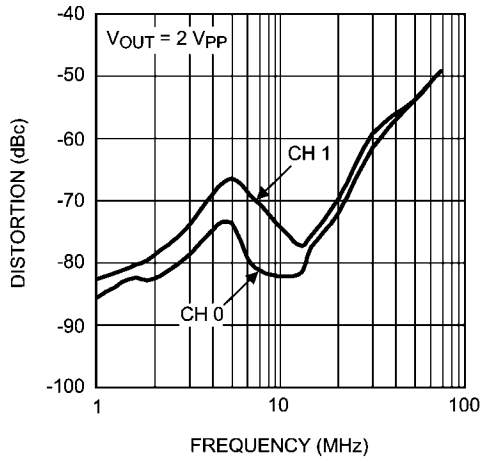


20129933

**HD3 vs. Frequency**
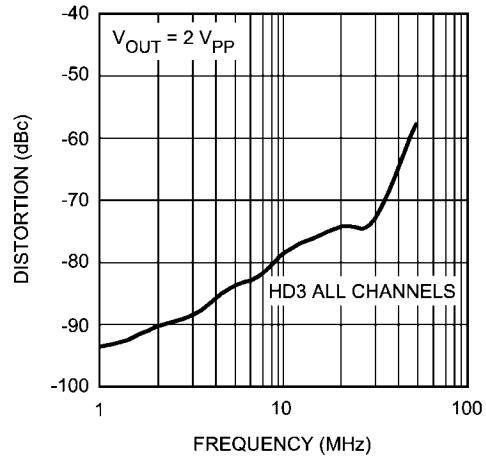


20129934

**HD2 vs. $V_S$**
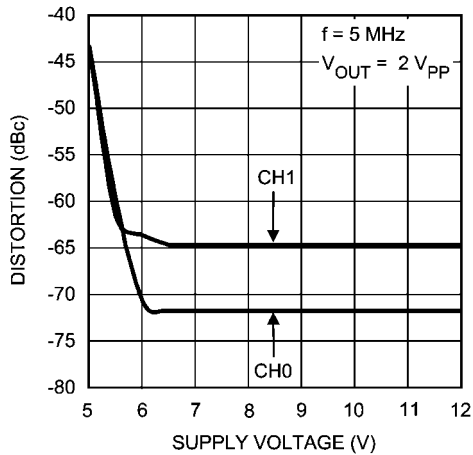


20129907

**HD3 vs. $V_S$**



20129910

**HD2 vs. V_{OUT}**



20129911

**HD3 vs. V_{OUT}**



20129906

**Minimum V_{OUT} vs. I_{OUT}** (*Note 7*)



20129912

**Maximum V_{OUT} vs. I_{OUT}** (*Note 7*)



20129913

**Crosstalk vs. Frequency**



20129935

**Off Isolation**
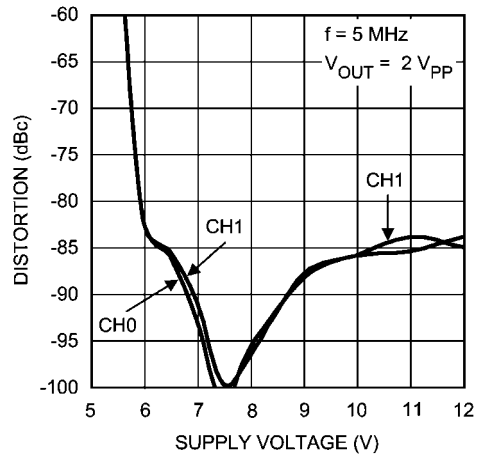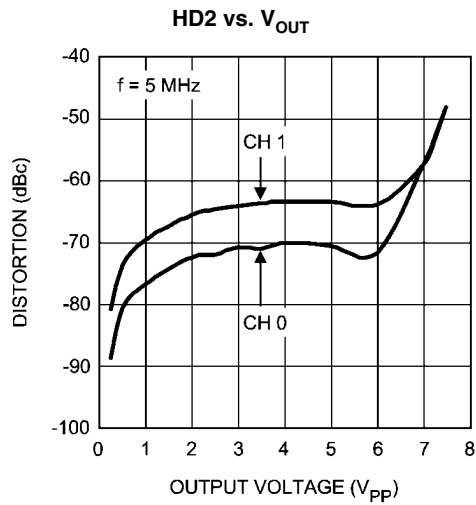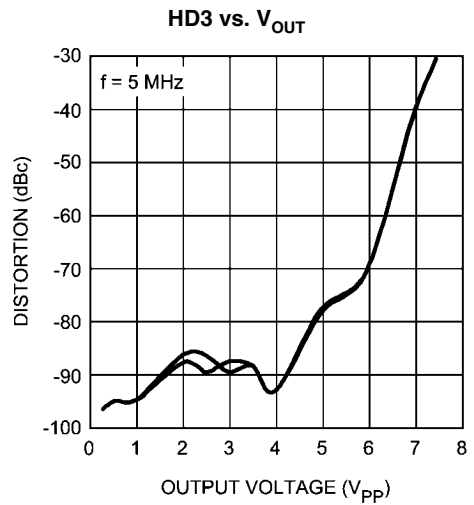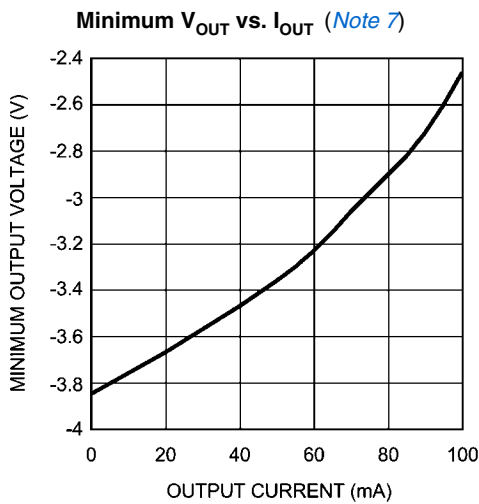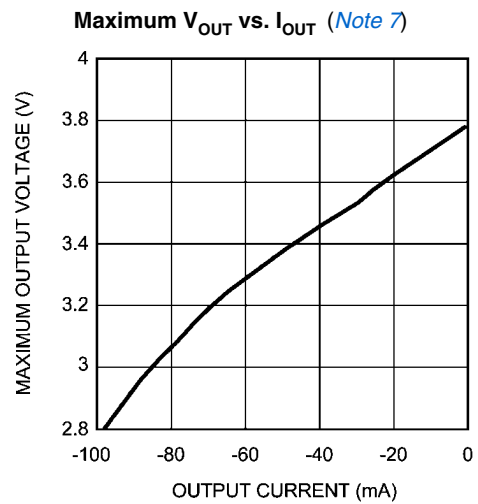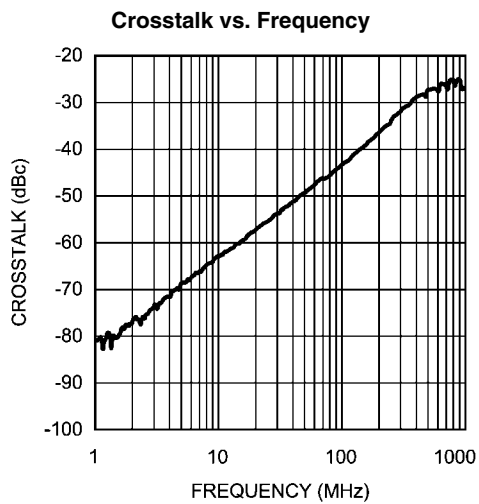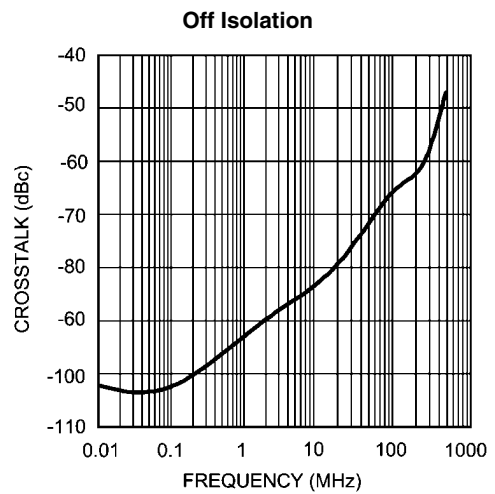


20129931

# Application Notes

**GENERAL INFORMATION**
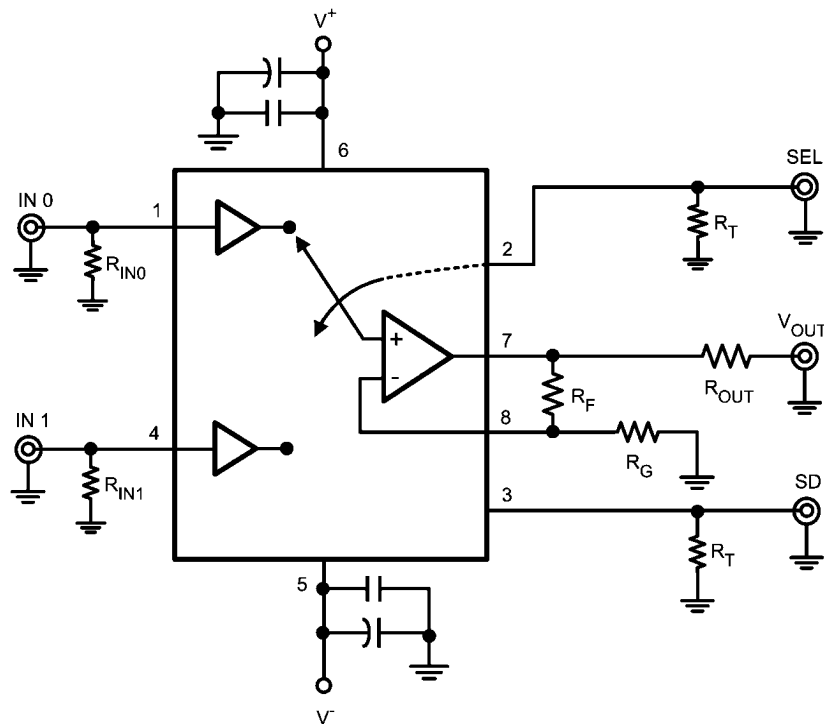
20129922

**FIGURE 1. Typical Application**

The LMH6570 is a high-speed 2:1 analog multiplexer, optimized for very high speed and low distortion. With selectable gain and excellent AC performance, the LMH6570 is ideally suited for switching high resolution, presentation grade video signals. The LMH6570 has no internal ground reference. Single or split supply configurations are both possible, however, all logic functions are referenced to the mid supply point. The LMH6570 features very high speed channel switching and disable times. When disabled the LMH6570 output is high impedance making MUX expansion possible by combining multiple devices. See "Multiplexer Expansion" section below. The LMH6570 SEL defaults to logic low (IN0 active). The default state for the SD pin is also logic low (device enabled). Both pins can be left floating if the default state is desired.

**VIDEO PERFORMANCE**

The LMH6570 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. *Figure 1* shows a typical configuration for driving a 75Ω cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

**FEEDBACK RESISTOR SELECTION**
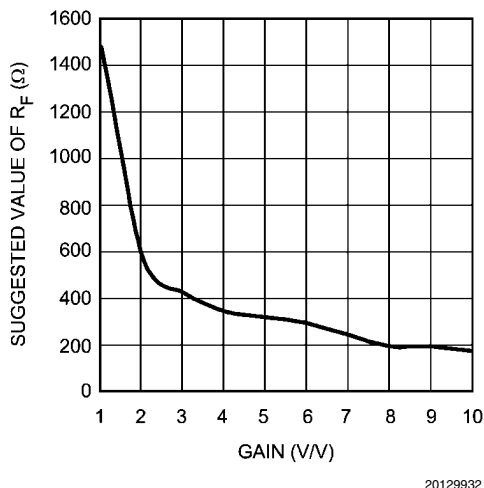


**FIGURE 2. Suggested $R_F$ vs. Gain**

The LMH6570 has a current feedback output buffer with gain determined by external feedback ($R_F$) and gain set ($R_G$) resistors. With current feedback amplifiers, the closed loop frequency response is a function of $R_F$. For a gain of 2 V/V, the recommended value of $R_F$ is 576Ω. For other gains see the chart "Suggested $R_F$ vs Gain". Generally, lowering $R_F$ from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of $R_F$ will cause the frequency response to roll off faster. Reducing the value of $R_F$ too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal $R_F$ for a given circuit. For more information see Application Note OA-13 which describes the relationship between $R_F$ and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 8 is approximately 20Ω. This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6570 will exhibit a "gain bandwidth product" similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.

**MULTIPLEXER EXPANSION**

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6570's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in *Figure 3* shows how to compensate for this effect. For the 8:1 MUX function shown in *Figure 3* below the gain error would be about 0.7% or –0.06dB. In the circuit in *Figure 3*, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).



STAGE GAIN = $1 + R_F/R_G$ = 2.18 V/V

$$\text{GAIN ERROR} = \frac{[(1138/3) \,\|\, 75] \cdot 2}{[(1138/3) \,\|\, 75] + 75} = 0.91 \text{ V/V}$$

NET GAIN = 0.5 * STAGE GAIN * GAIN ERROR = 0.993 V/V
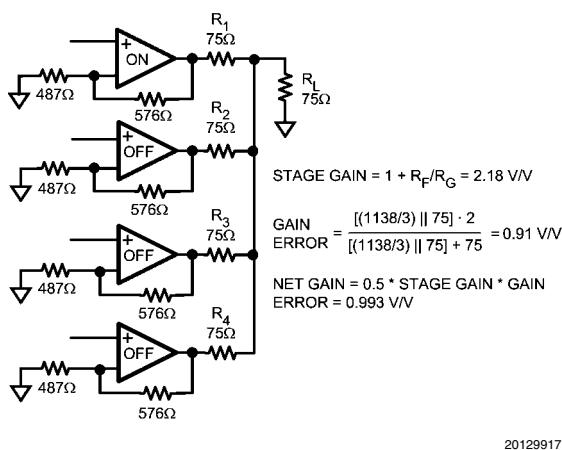
**FIGURE 3. Multiplexer Gain Compensation**

## BUILDING A 4:1 MULITPLEXER

*Figure 4* shows an 4:1 MUX using two LMH6570's.
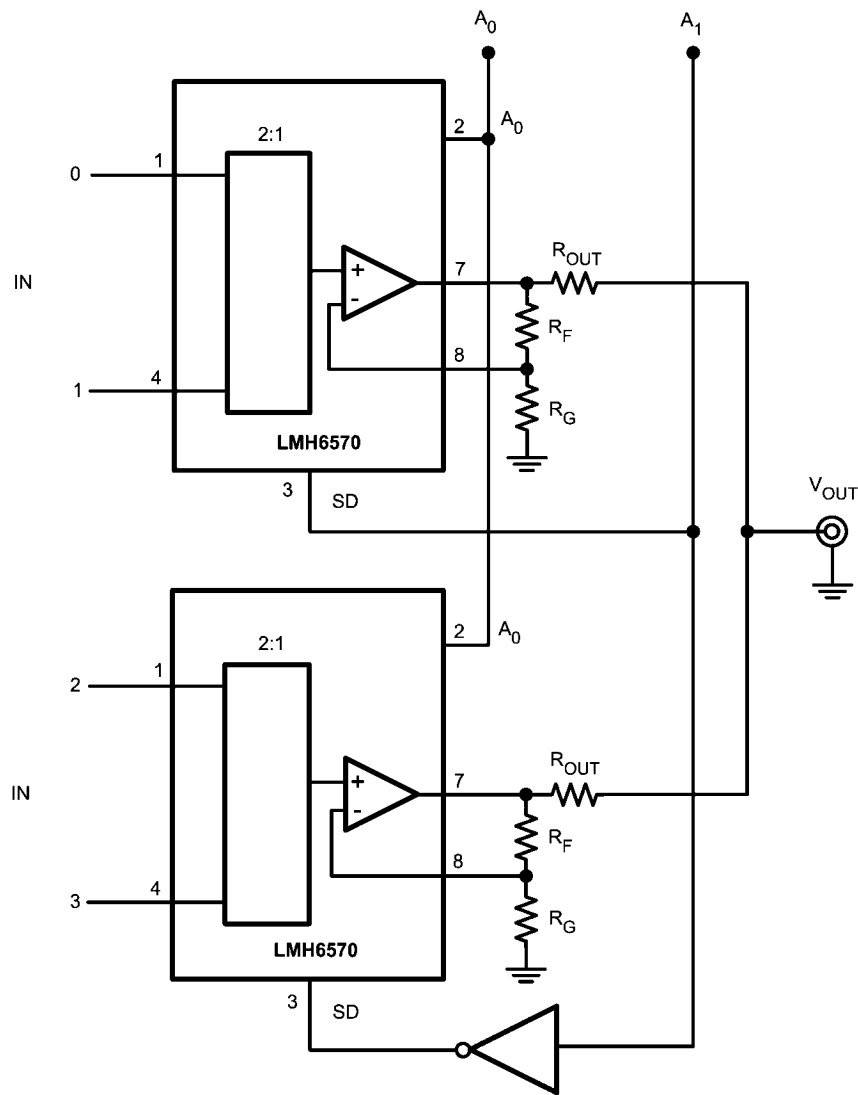


**FIGURE 4. 4:1 MUX USING TWO LMH6570's**
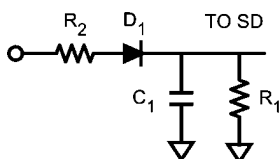


**FIGURE 5. Delay Circuit Implementation**

If it is important in the end application to make sure that no two inputs are presented to the output at the same time, an optional delay block can be added, to drive the SHUTDOWN pin of each device, as shown. *Figure 5* shows one possible approach to this delay circuit. The delay circuit shown will delay SHUTDOWN's H to L transitions ($R_1$ and $C_1$ decay) but won't delay its L to H transition. $R_2$ should be kept small compared to $R_1$ in order to not reduce the SHUTDOWN voltage and to produce little or no delay to SHUTDOWN.

## Other Applications

The LMH6570 could support a dual antenna receiver with two physically separate antennas. Monitoring the signal strength of the active antenna and switching to the other antenna when a fade is detected is a simple way to achieve spacial diversity. This method gives about a 3dB boost in average signal strength and is the least expensive method for combining signals.

### DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor $R_{OUT}$. *Figure 6* shows the use of a series output resistor, $R_{OUT}$, to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart "Suggested $R_{OUT}$ vs. Cap Load" gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of $R_{OUT}$ can be reduced slightly from the recommended values.
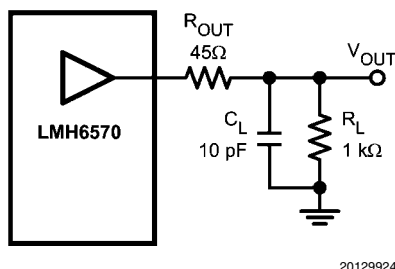


20129924

**FIGURE 6. Decoupling Capacitive Loads**
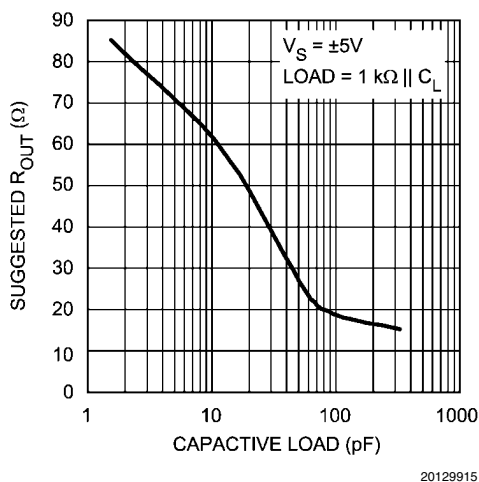


20129915

**FIGURE 7. Suggested $R_{OUT}$ vs. Capacitive Load**
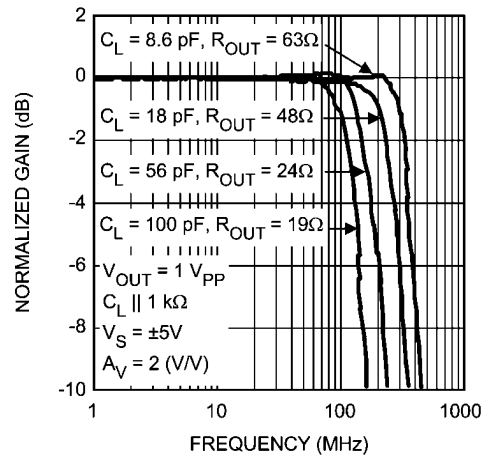
20129914

**FIGURE 8. Frequency Response vs. Capacitive Load**

## LAYOUT CONSIDERATIONS

To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In *Figure 1*, the capacitor between V+ and V− is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01µF and 0.1µF ceramic capacitors for each supply bypass.

## POWER DISSIPATION

The LMH6570 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the $T_{JMAX}$ is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6570:

1.  Calculate the quiescent (no-load) power: $P_{AMP} = I_{CC}{}^* (V_S)$, where $V_S = V^+ - V^-$.
2.  Calculate the RMS power dissipated in the output stage: $P_D$ (rms) = rms $((V_S - V_{OUT})^* I_{OUT})$, where $V_{OUT}$ and $I_{OUT}$ are the voltage across and the current through the external load and $V_S$ is the total supply voltage.
3.  Calculate the total RMS power: $P_T = P_{AMP} + P_D$.

The maximum power that t-he LMH6570 package can dissipate at a given temperature can be derived with the following equation:

$P_{MAX} = (150° − T_{AMB})/ \theta_{JA}$, where $T_{AMB}$ = Ambient temperature (°C) and $\theta_{JA}$ = Thermal resistance, from junction to ambient, for a given package (°C/W). For the SOIC package $\theta_{JA}$ is 150 °C/W.

## ESD PROTECTION

The LMH6570 is protected against electrostatic discharge (ESD) on all pins. The LMH6570 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6570 is driven by a large signal while the device is powered down the ESD diodes will conduct . The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

## Physical Dimensions inches (millimeters) unless otherwise noted
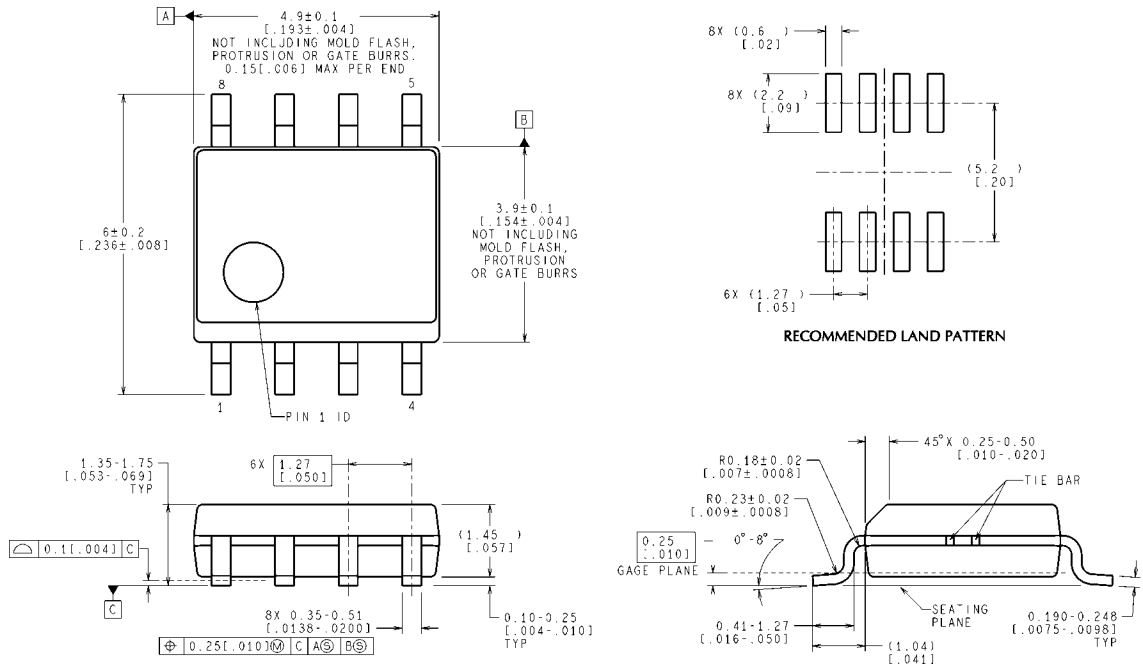


**8-Pin SOIC**
**NS Package Number M08A**

# Notes

# Notes

## IMPORTANT NOTICE

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Mobile Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |