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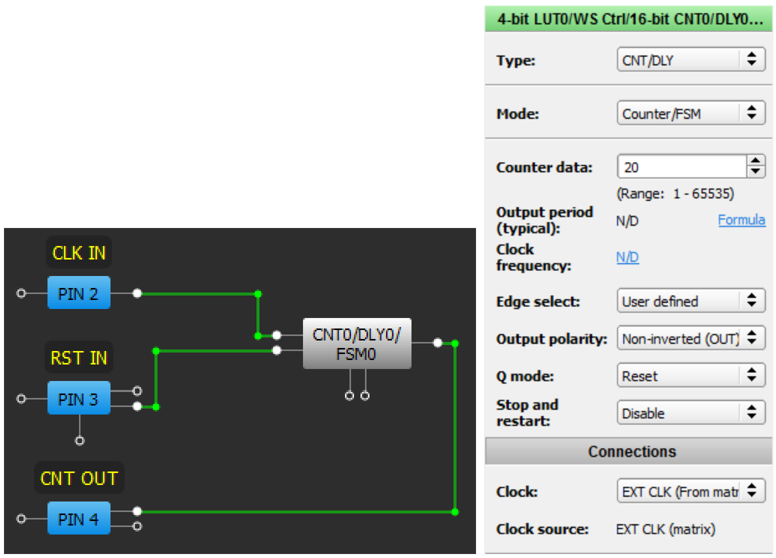
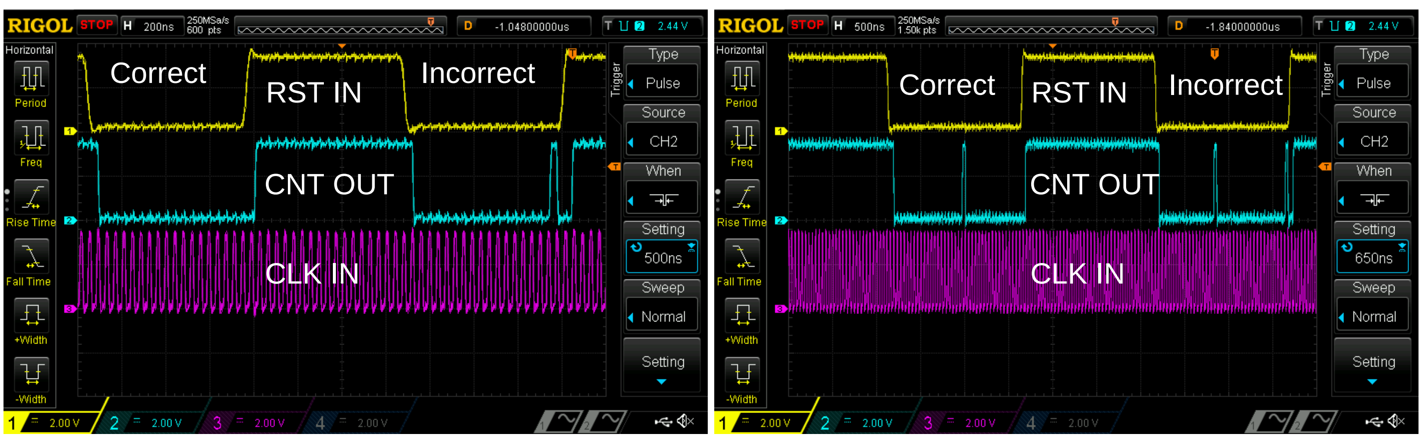
ISSUE 1: Counter Incorrect Operation after the Reset

Functional Block Affected: Counter

Description:

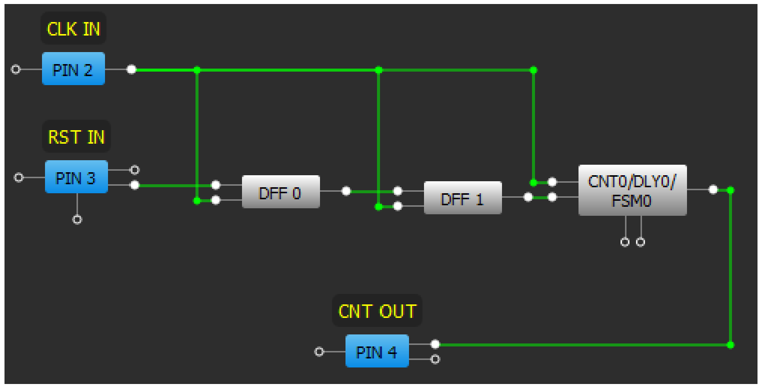
If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected. This phenomenon appears more often as the clock frequency increases.





Workaround:

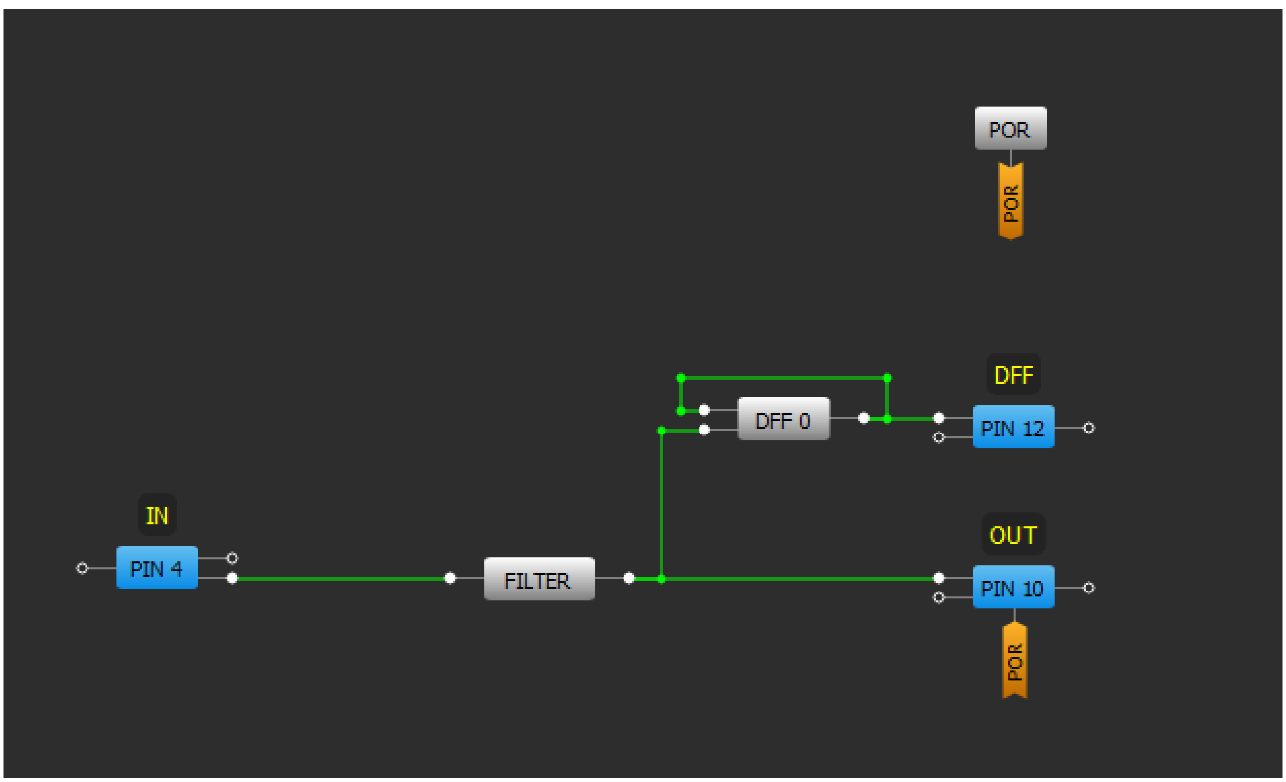
- Synchronize RESET input of the Counter with its CLK using 2 DFF cells as shown on picture below.



ISSUE 2: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

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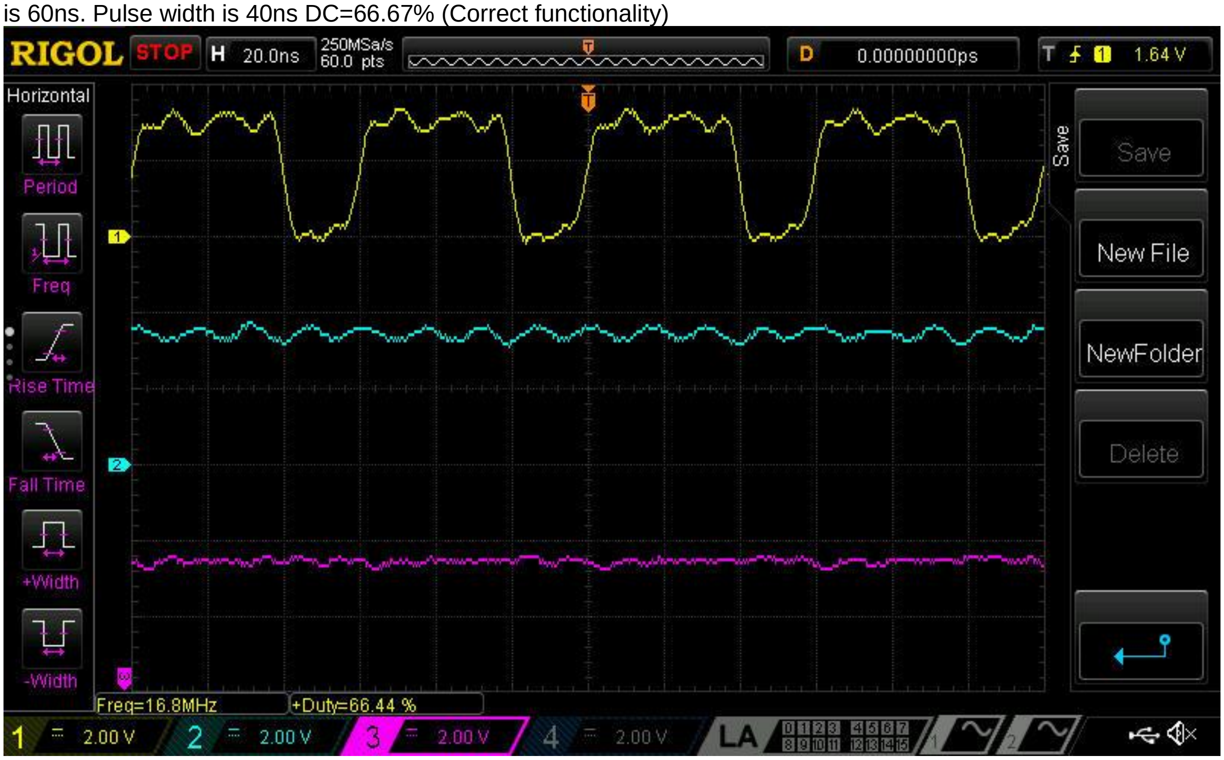
3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)



Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #2).

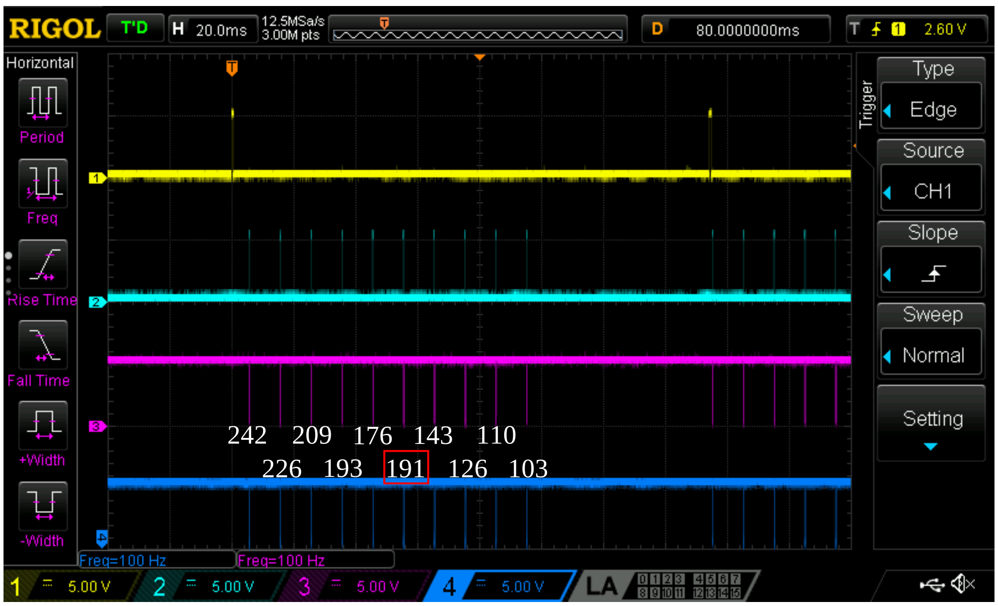
ISSUE 3: Incorrect I²C Reads of the 8-bit Counter Registers
Functional Blocks Affected: CNT2/DLY2 and CNT4/DLY4

Description:

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I²C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out)
Channel 2 (light blue/2nd line) – PIN#1 (I²C Read Triggers)
Channel 3 (magenta /3rd line) – PIN#8 (I²C SCL)
Channel 3 (dark blue /4th line) – PIN#9 (I²C SDA)



Workaround:

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select “Ext. CLK. (From Matrix).” This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I^2C read.

ISSUE 4: ACMP additional IN- leakage current
Functional Blocks Affected: ACMP, PIN

Description:

The SLG4653x has an additional leakage current through the PIN connected to the ACMP IN- input when all of the ACMPs are powered down. Typically, leakage through the PIN connected to IN- is much less than 1 µA. But when the ACMP is powered down and voltage is applied to the PIN, the leakage current may grow up to several µA (depending on the VDD and voltage applied).

Workaround:

Currently there is no workaround for this issue.

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Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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