24GHz VCO + PGA + 2 Channel PA Output

Preliminary Technical Data

ADF5901

FEATURES

24GHz VCO with 250MHz frequency range
2 Channel 24GHz PA with +8 dBm output
Single-Ended Outputs
2 Channel Muxed Outputs with Mute Function
Programmable Output Power
N Divider TX Output (Frequency Discriminator)
24GHz LO Output Buffer
250MHz Signal Bandwidth
Power Control Detector
Auxiliary 8 Bit ADC
± 5 Degree Temperature Sensor
4 wire SPI Interface
Electric static distortion (ESD) performance
Human body model (HBM): 2000 V
Charged device model (CDM): 250 V
Qualified for automotive applications

APPLICATIONS

Automotive Radar
Industrial radars
Microwave (µW) radar sensors

General Description

The ADF5901 is a 24GHz TX MMIC with on-chip 24GHz VCO with PGA and dual TX channels for Radar Systems. The on-chip 24GHz VCO generates the 24GHz signal for the 2 TX channels and the LO_{OUT}. Each TX channel contains a power control circuit. There is also an on-chip temperature sensor.

Control of all the on-chip registers is through a simple 4-wire interface.

The ADF5901 comes in a compact 32-lead, 5 mm × 5 mm LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

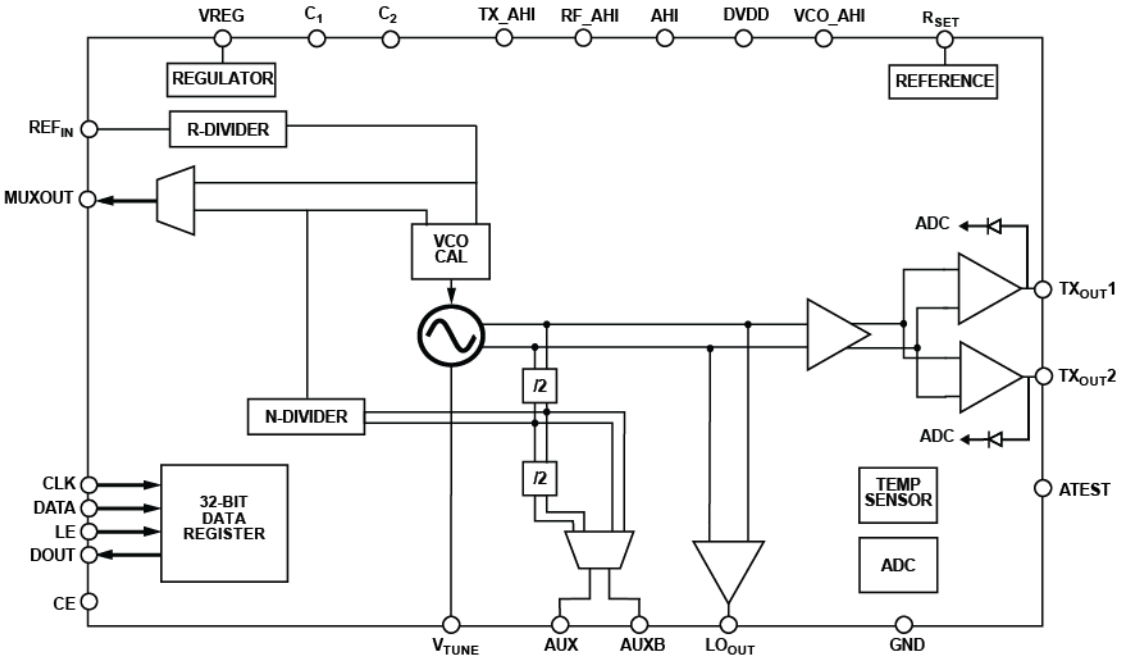

Figure 1.

PrH

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REVISION HISTORY

SPECIFICATIONS

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = 3.3 V ± 5%, AGND = 0 V, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. Operating temperature range is -40°C to 105°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Condition
OPERATING CONDITIONS					
RF Frequency Range	24		24.25	GHz	
VCO CHARACTERISITICS					
V_{TUNE}	1		2.8	V	
V_{TUNE} Impedance		100		kΩ	
VCO Phase Noise Performance					
@100kHz Offset		-88		dBc/Hz	
@1MHz Offset		-108		dBc/Hz	
@10MHz Offset		-128		dBc/Hz	
Amplitude Noise		-150		dBc/Hz	@ 1MHz Offset
Static Pulling F_{VCO} Change vs. Load		±2		MHz	Open Loop into 2:1 VSWR load
Dynamic Pulling TX ON/OFF Switch Change		±10		MHz	Open Loop
Dynamic Pulling TX to TX Switch Change		±5		MHz	Open Loop
Pushing F_{VCO} Change vs. AHI Change		±5		MHz/V	Open Loop
Spurious Level Harmonics		-30		dBc	
Spurious Level Non Harmonics		<-70		dBc	
POWER SUPPLIES					
AHI	3.135	3.3	3.465	V	
TX_AHI, RF_AHI, VCO_AHI, DVDD		AHI			
I_{TOTAL}[1]		170		mA	
Software Power Down Mode		500		µA	
Hardware Power Down Mode		200		µA	
TX OUTPUT					
Output Power	2	8	10	dBm	
Output Impedance		50		Ω	
ON/OFF Isolation		30		dB	Single TX output switched ON/OFF
TX to TX Isolation		25		dB	
Power Up/Down Time		200		ns	
LO OUTPUT					
Output Power	-7	-1	5	dBm	
Output Impedance		50		Ω	
ON/OFF Isolation		30		dB	
AUX OUTPUT					
Output Power	-9	-5	0	dBm	Single Ended
Output Frequency					
Divide by 2 Output	12		12.125	GHz	
Divide by 4 Output	6		6.0625	GHz	
Output Impedance		200		Ω	Differential
ON/OFF Isolation		30		dB	
AUX to LO Isolation		30		dB	
TEMPERATURE SENSOR					
Analog Accuracy		±5		°C	Following one-point calibration
Digital Accuracy		±5		°C	Following one-point calibration
Sensitivity		6.4		mV/°C	
ADC					
Number of Bits		8			
INL		±1		LSB	

Parameter	Min	Typ	Max	Unit	Condition
DNL		±1		LSB	
LSB		7.4		mV	
REFIN CHARACTERISITICS					
REF_{IN} Input Frequency	10		260	MHz	−5 dBm min to +9 dBm max biased at AHI/2 (ac coupling ensures 1.8/2 bias); for frequencies < 10 MHz, use a dc-coupled, CMOS-compatible square wave with a slew rate > 25 V/µs
REF_{IN} Input Capacitance			1.2	pF	
REF_{IN} Input Current			±100	µA	
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.4			V	
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage[2]	V_{DD} - 0.4			V	
V_{OL}, Output Low Voltage			0.4	V	
I_{OH}			500	µA	
I_{OL}			500	µA	

[1] T_A = 25°C; AHI = 3.3 V; f_{REFIN} = 100 MHz; RF = 24.125 GHz following initialization sequence in Table 6.

[2] V_{DD} selected from IO Level (DB9 in Register 8)

TIMING SPECIFICATIONS

AHI = TX_AHI = RF_AHI = VCO_AHI = DVDD = 3.3 V ± 5%, AGND = 0 V, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted. Operating temperature range is -40°C to 105°C.

Table 2. Write Timing

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width
t_8	10	ns max	LE setup time to DOUT
t_9	15	ns max	CLK setup time to DOUT

Write Timing Diagram

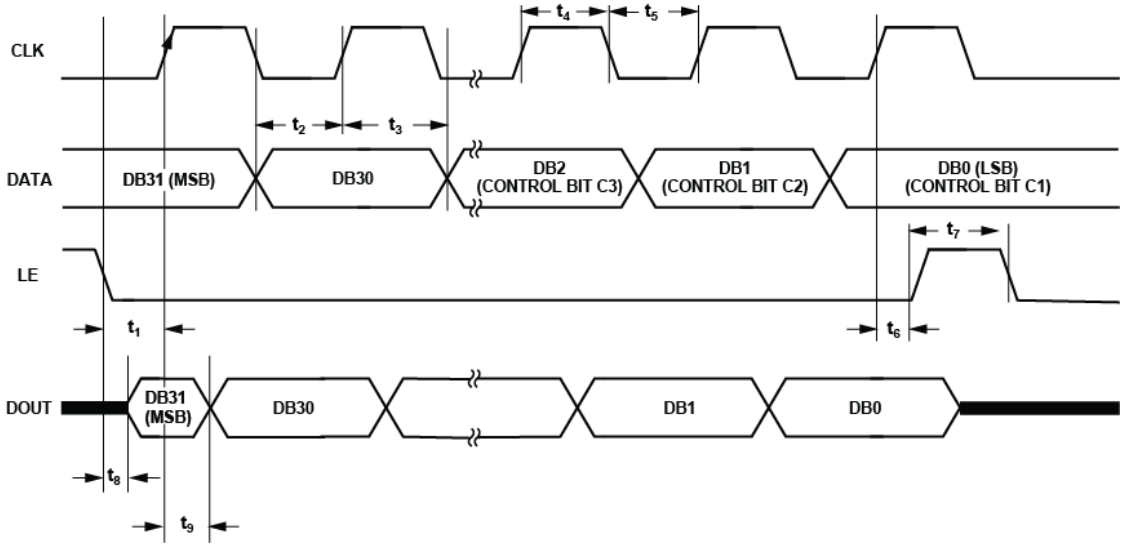


Figure 2. Write Timing Diagram

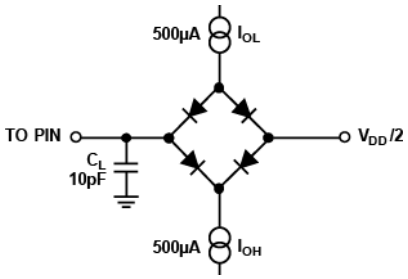


Figure 3. Load Circuit for DOUT/MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AHI to GND	−0.3 V to +3.9 V
AHI to TX_AHI	−0.3 V to +0.3 V
AHI to RF_AHI	−0.3 V to +0.3 V
AHI to VCO_AHI	−0.3 V to +0.3 V
AHI to DVDD	−0.3 V to +0.3 V
Vtune to GND	-0.3 V to +3.6V
Digital I/O Voltage to GND	−0.3 V to DVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
θ_{JA} Thermal Impedance[1] (Paddle Soldered)	40.83 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	177381
Bipolar	2315
ESD	
Charged Device Model	250V
Human Body Model	2000V

[1] 2 signal planes (i.e. on top and bottom surfaces of the board), 2 buried planes and 9 vias

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

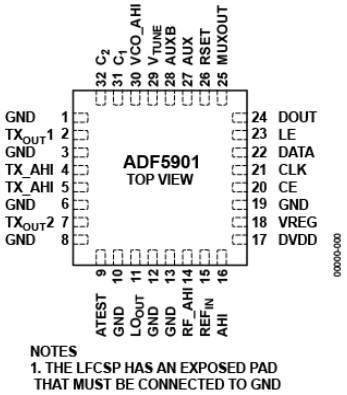


Figure 4.

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 6, 8, 10, 12, 13, 19, EP	GND	RF Ground. All ground pins should be tied together.
2	$TX_{OUT}1$	24GHz TX Output
4, 5	TX_AHI	Voltage Supply for the TX Section. Decoupling capacitors (0.1µF, 1nF and 10pF) TX_AHI must be the same value as AHI.
7	$TX_{OUT}2$	24GHz TX Output
9	ATEST	Analog Test Pin
11	LO_{OUT}	LO Output.
14	RF_AHI	Voltage Supply for the RF Section. Decoupling capacitors (0.1µF, 1nF and 10pF) RF_AHI must be the same value as AHI.
15	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $DV_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. See Figure 14. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
16	AHI	Voltage Supply for the Analog Section. Decoupling capacitors (0.1µF, 1nF and 10pF)
17	DVDD	Digital Power Supply. This may range from 3.135 V to 3.465 V. Decoupling capacitors (0.1µF, 1nF and 10pF) to the ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AHI.
18	VREG	Internal 1.8V regulator output pin. A 220 nF capacitor to ground should be placed as close as possible to this pin.
20	CE	Chip Enable. A logic low on this pin powers down the device. Taking the pin high powers up the device, depending on the status of the power-down bit, PD1.
21	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
22	DATA	Serial Data Input. The serial data is loaded MSB first with the four LSBs being the control bits. This input is a high impedance CMOS input.
23	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the 16 latches with the latch being selected using the control bits.
24	DOUT	Serial Data Output.
25	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
26	RSET	Connecting a 5.1kΩ resistor between this pin and GND sets an internal current. The nominal voltage potential at the R_{SET} pin is 0.62 V.
27	AUX	Auxiliary Output. The VCO/2 output or VCO/4 is available.
28	$\overline{AUX}$	Complementary Auxiliary Output. The VCO/2 output or VCO/4 is available.
29	V_{TUNE}	Control Input to the VCO. This voltage determines the output.
30	VCO_AHI	Voltage Supply for the VCO Section. Decoupling capacitors (0.1µF, 1nF and 10pF) VCO_AHI must be the same value as AHI.
31	C_1	Decoupling Capacitor. A 47 nF capacitor to ground should be placed as close as possible to this pin.
32	C_2	Decoupling Capacitor. A 220 nF capacitor to ground should be placed as close as possible to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

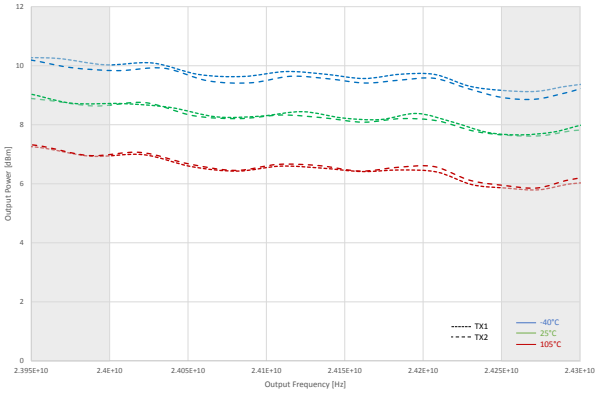


Figure 5. TX Output Power vs Frequency

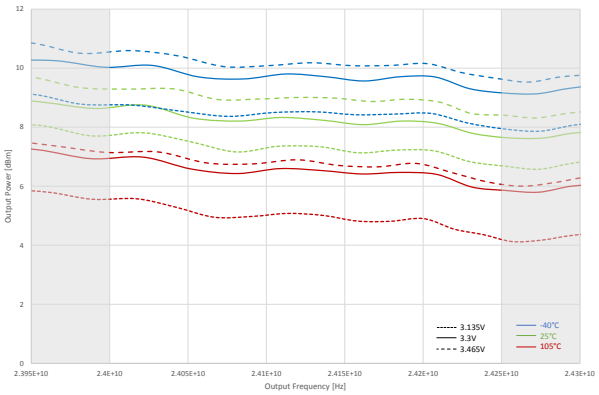


Figure 6. TX1 Output Power variation with temperature and supply vs Frequency

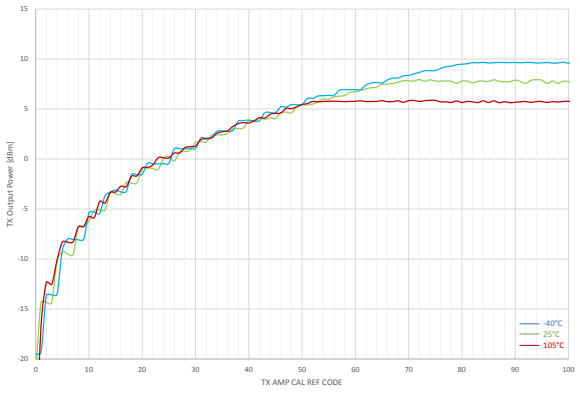


Figure 7. TX Output Power vs TX Reference Code

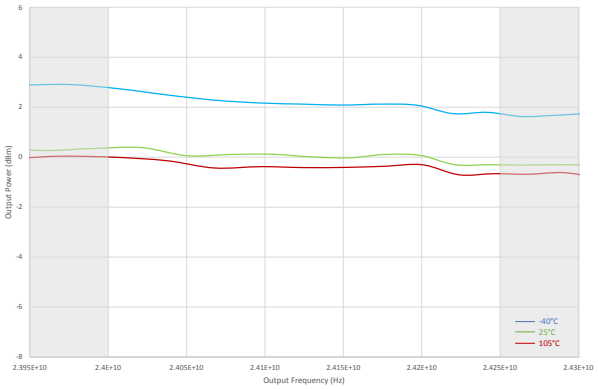


Figure 8. LO Output Power vs Frequency

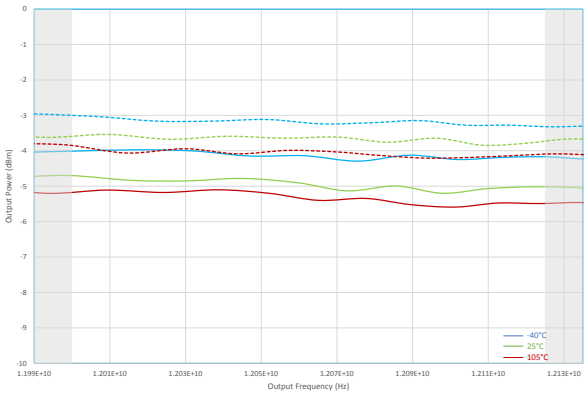


Figure 9. AUX/AUXB Output Power vs Frequency with DIV2 selected

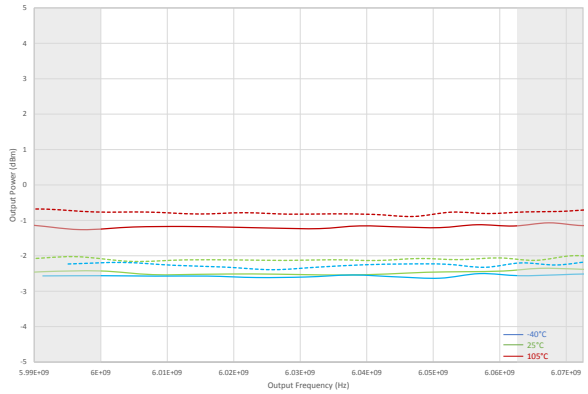


Figure 10. AUX/AUXB Output Power vs Frequency with DIV4 selected

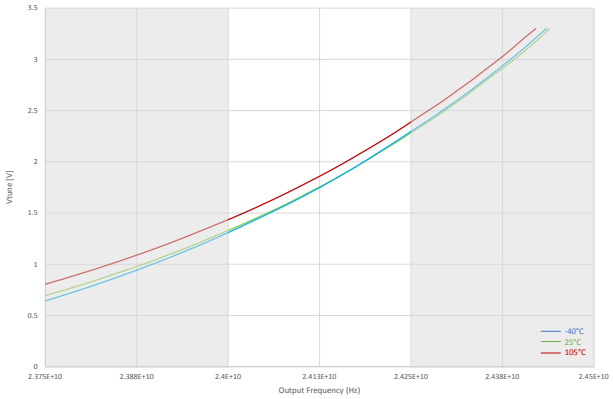


Figure 11. Vtune Frequency Range

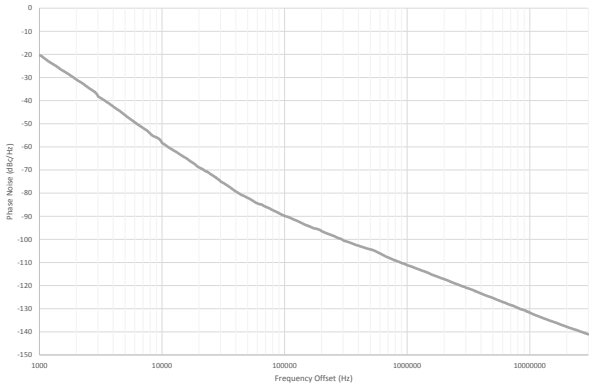


Figure 12. Open Loop Phase Noise on TX1 Output @ 24.125GHz

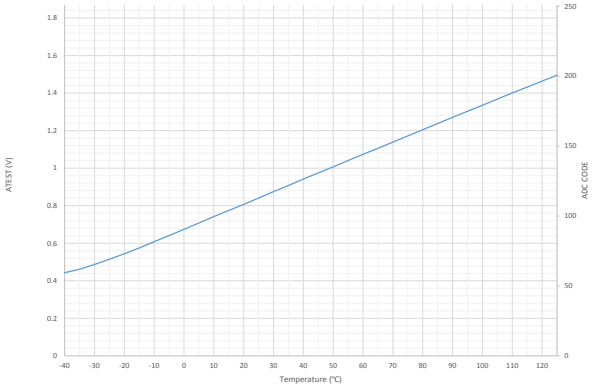


Figure 13. ATEST Voltage and ADC CODE vs Temperature

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 14. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

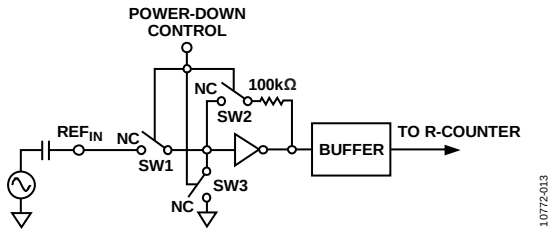


Figure 14. Reference Input Stage

RF INT DIVIDER

The RF INT counter allows a division ratio in the PLL feedback counter. Division ratios from 75 to 4095 are allowed.

INT, FRAC, AND R RELATIONSHIP

The INT and FRAC values in conjunction with the R-counter make it possible to generate the RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{REF} \times (INT + (FRAC/2^{25})) \times 2 \quad (1)$$

where:
RF_{OUT} is the output frequency of internal voltage controlled oscillator (VCO).
INT is the preset divide ratio of the binary 12-bit counter (75 to 4095).
FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$F_{REF} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit (0 or 1).
T is the REF_{IN} divide-by-2 bit (0 or 1).
R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

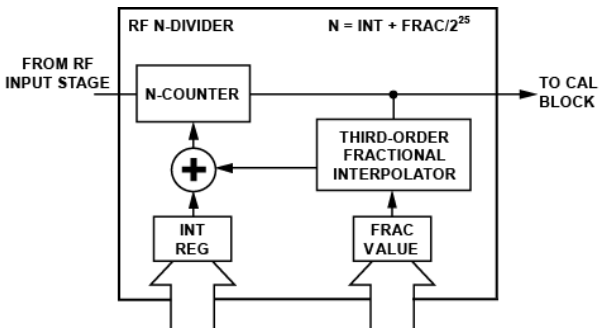


Figure 15. RF N-Divider

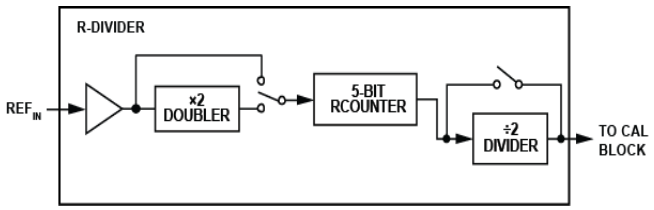


Figure 16. Reference Divider

R-COUNTER

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the VCO calibration block. Division ratios from 1 to 32 are allowed.

INPUT SHIFT REGISTER

The ADF5901 digital section includes a 5-bit RF R-counter, a 12-bit RF N-counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of 12 latches on the rising edge of LE. The destination latch is determined by the state of the five control bits (C5, C4, C3, C2, and C1) in the input shift register. These are the five LSBs (DB4, DB3, DB2, DB1, and DB0, respectively), as shown in Figure 2. The truth table for these bits is shown in Table 5. Figure 17 and Figure 18 show a summary of how the latches are programmed.

PROGRAM MODES

Table 5 and Figure 19 through Figure 29 show how to set up the program modes in the ADF5901.

Several settings in the ADF5901 are double buffered. These include the LSB fractional value, R-counter value, reference doubler, RDIV2 and MUXOUT. This means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R5.

For example, updating the fractional value can involve a write to the 13 LSB bits in R6 and the 12 MSB bits in R5. R6 should be written to first, followed by the write to R5. The frequency change begins after the write to R0. Double buffering ensures that the bits written to in R6 do not take effect until after the write to R5.

Table 5. C5, C4, C3, C2, and C1 Truth Table

Control Bits					
C5	C4	C3	C2	C1	Register
0	0	0	0	0	R0
0	0	0	0	1	R1
0	0	0	1	0	R2
0	0	0	1	1	R3
0	0	1	0	0	R4
0	0	1	0	1	R5
0	0	1	1	0	R6

0	0	1	1	1	R7
0	1	0	0	0	R8
0	1	0	0	1	R9
0	1	0	1	0	R10
0	1	0	1	1	R11

REGISTER MAPS

REGISTER 0 (R0)

RESERVED								AUX BUFFER GAIN			AUX DIV	RESERVED				PUP RCNTR	PUP NCNTR	RESERVED	TX2 AMP CAL	TX1 AMP CAL	PUP VCO	VCO CAL	PUP ADC	PUP TX2	PUP TX1	PUP LO	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	AG2	AG1	AG0	AD	1	1	1	1	PRC	PNC	1	TX2C	TX1C	PVCO	VCAL	PADC	PTX2	PTX1	PLO	C5(0)	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1 (R1)

RESERVED																			TX AMP CAL REF CODE								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	1	1	1	TAR7	TAR6	TAR5	TAR4	TAR3	TAR2	TAR1	TAR0	C5(0)	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2 (R2)

RESERVED																ADC START	ADC AVERAGE		ADC CLOCK DIVIDER								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	AS	AA0	AA0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3 (R3)

RESERVED																MUXOUT DBR[1]				IO LEVEL	READBACK CONTROL						CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	M3	M2	M1	M0	IOL	RC5	RC4	RC3	RC2	RC1	RC0	C5(0)	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4 (R4)

RESERVED															TEST BUS TO ADC	TEST BUS TO PIN	ANALOG TEST BUS										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	TBA	TBP	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	C5(0)	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5 (R5)

RESERVED			INTEGER WORD												FRAC MSB WORD												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	C5(0)	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6 (R6)

RESERVED														FRAC LSB WORD DBR[1]												CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	C5(0)	C4(0)	C3(1)	C2(1)	C1(0)

[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

Figure 17. Register Summary.

REGISTER 7 (R7)

RESERVED						MASTER RESET	RESERVED	CLOCK DIVIDER DBR[1]										RDIV2 DBR[1]	REF DOUBLER DBR[1]	R DIVIDER DBR[1]					CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	MR	1	C1D11	C1D10	C1D9	C1D8	C1D7	C1D6	C1D5	C1D4	C1D3	C1D2	C1D1	C1D0	RD2	RD	R4	R3	R2	R1	R0	C5(0)	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8 (R8)

RESERVED																	FREQENCY CAL DIVIDER										CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	C5(0)	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9 (R9)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	0	1	0	0	1	C5(0)	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10 (R10)

RESERVED																											CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C5(0)	C4(1)	C3(0)	C2(1)	C1(0)

[1] DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 5.

Figure 18. Register Summary

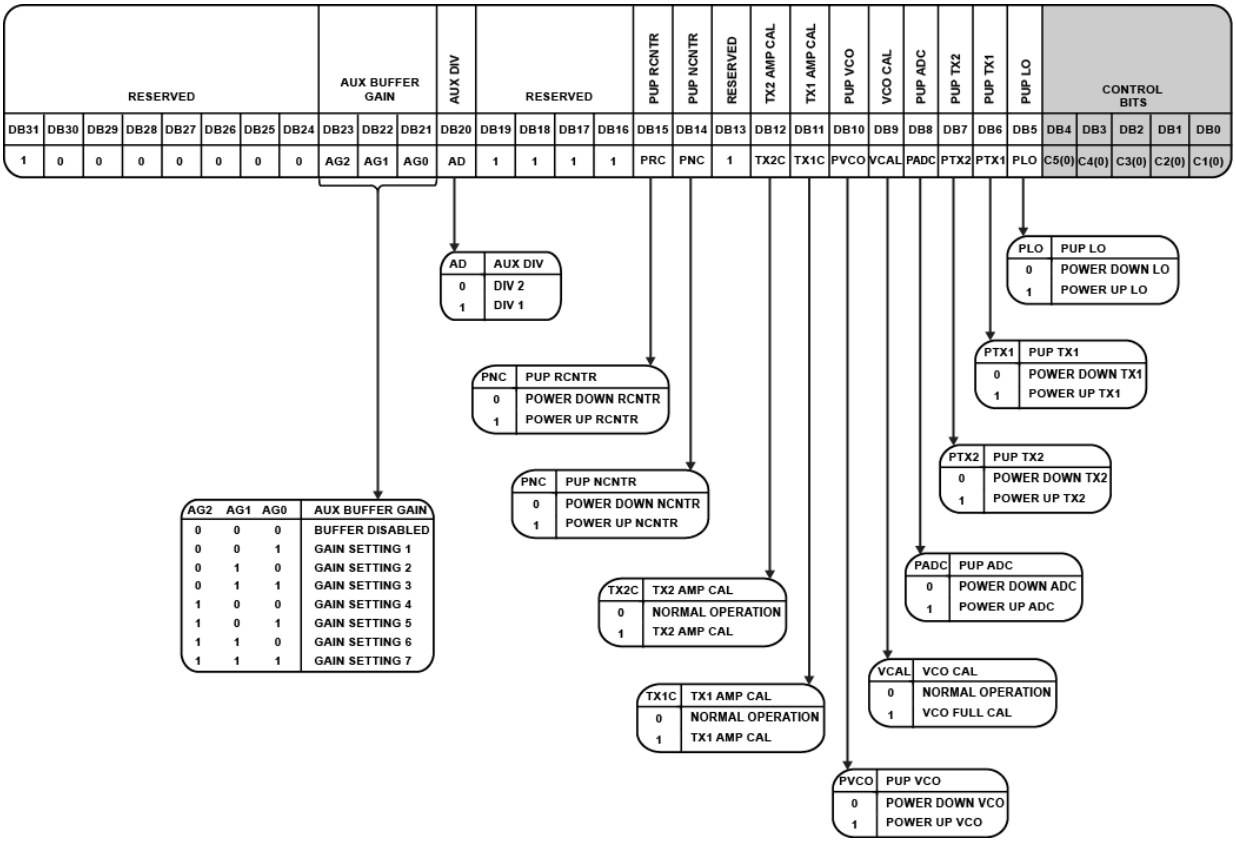


Figure 19. Register 0 (R0)

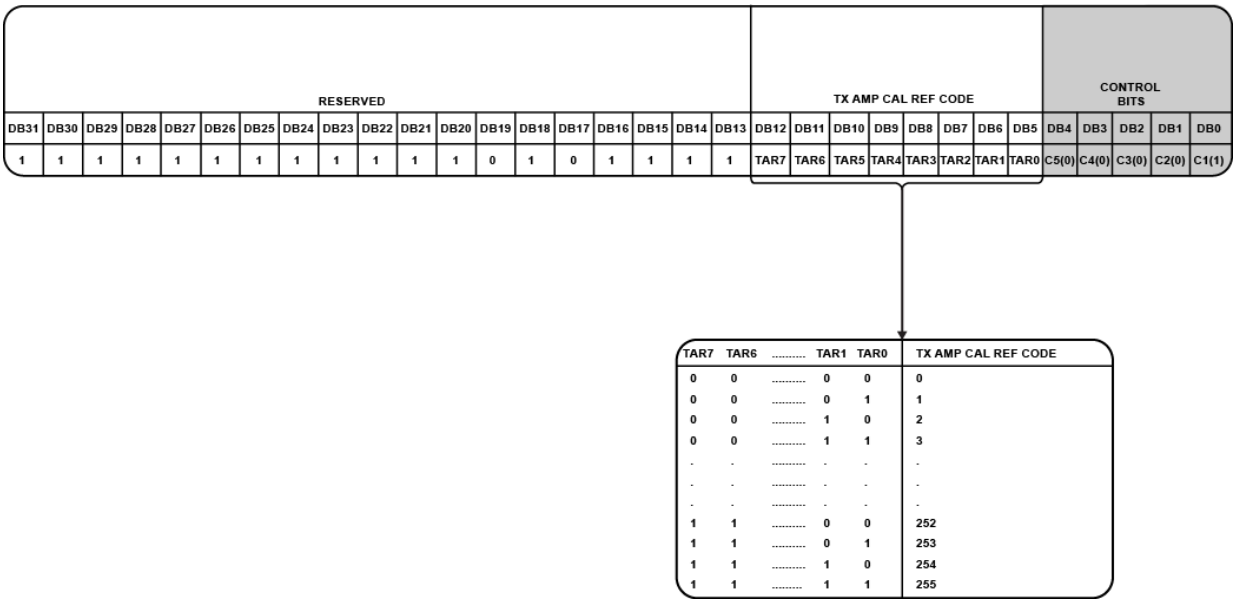


Figure 20. Register 1 (R1)

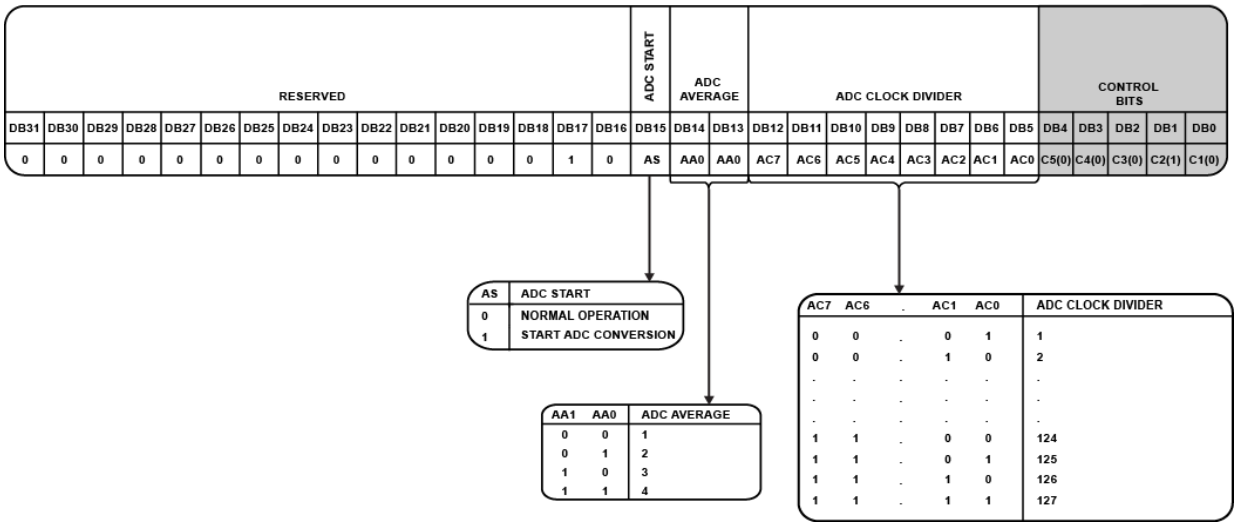


Figure 21. Register 2 (R2)

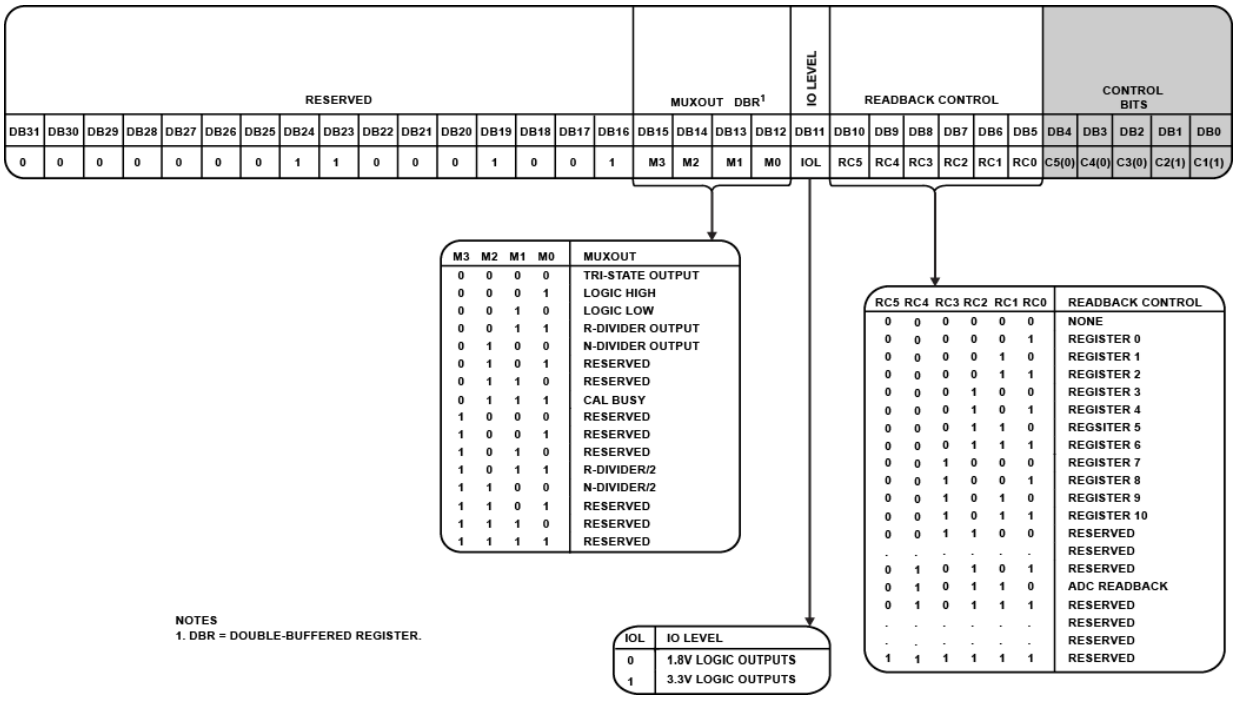


Figure 22. Register 3 (R3)

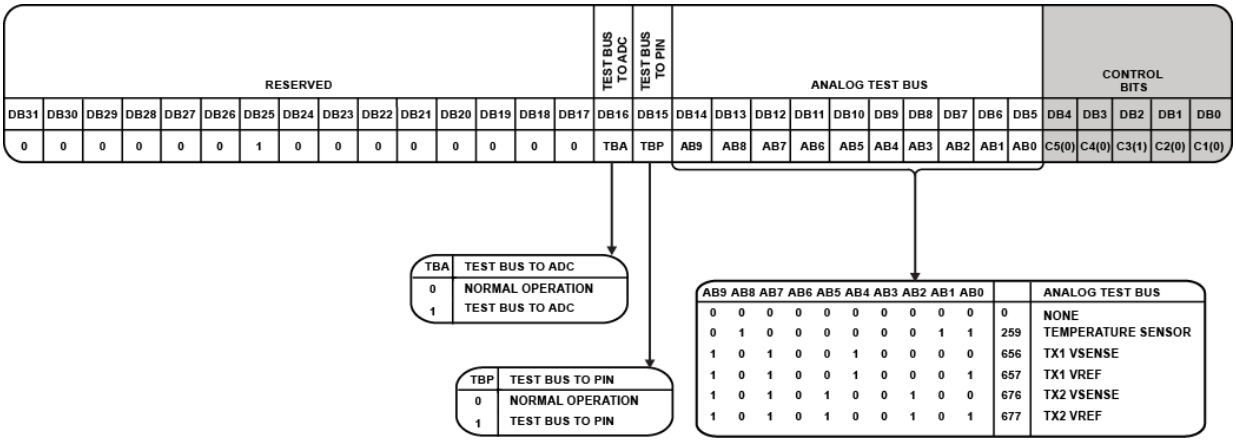


Figure 23. Register 4 (R4)

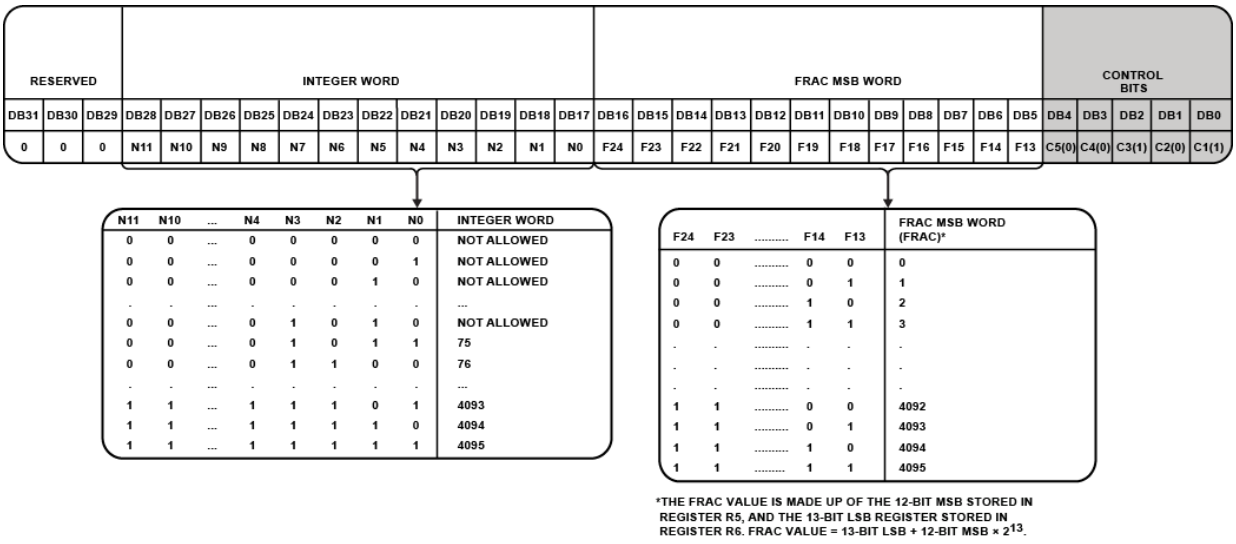


Figure 24. Register 5 (R5)

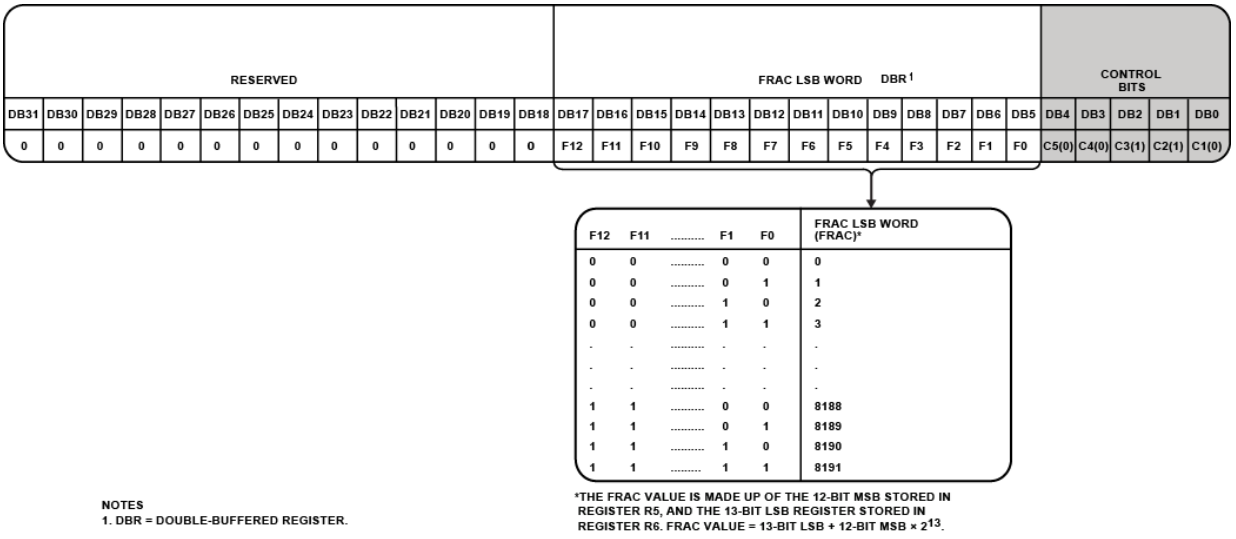


Figure 25. Register 6 (R6)

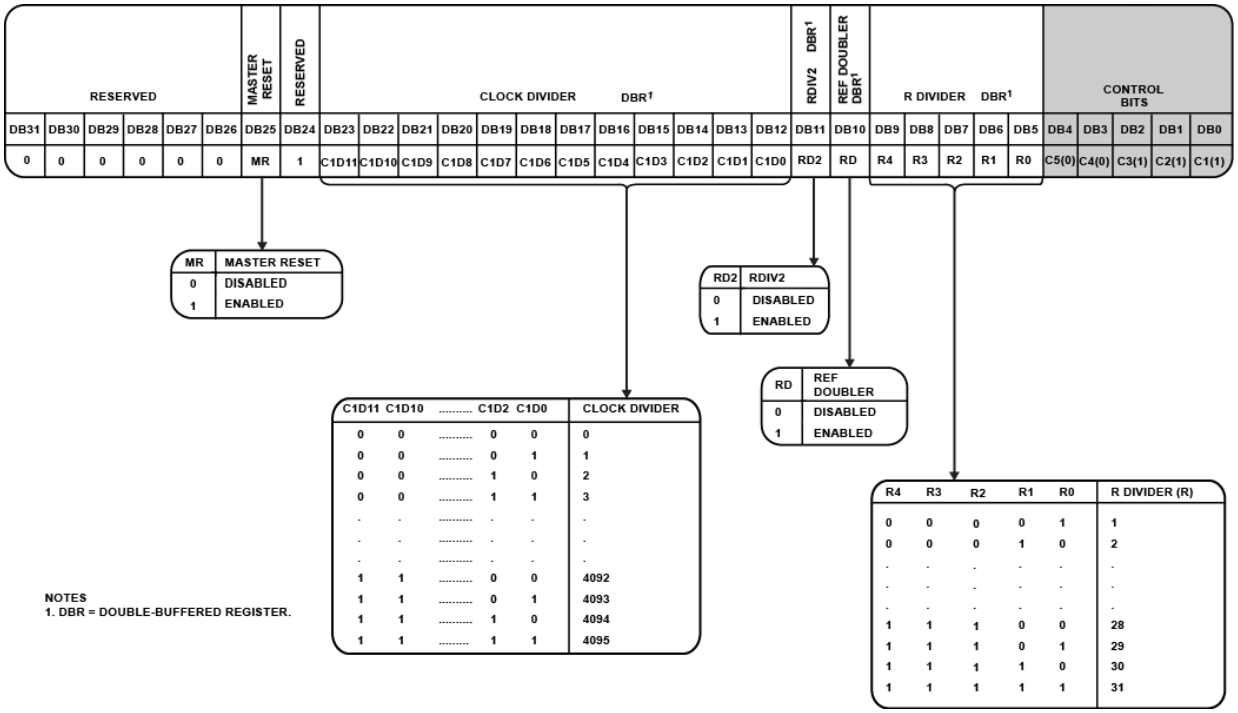


Figure 26. Register 7 (R7)

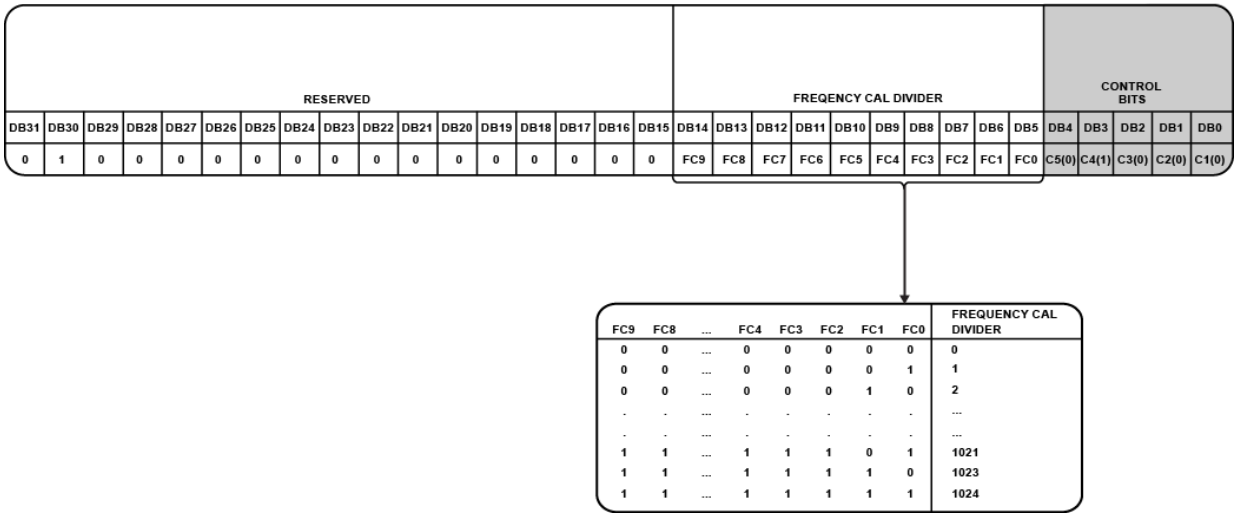


Figure 27. Register 8 (R8)

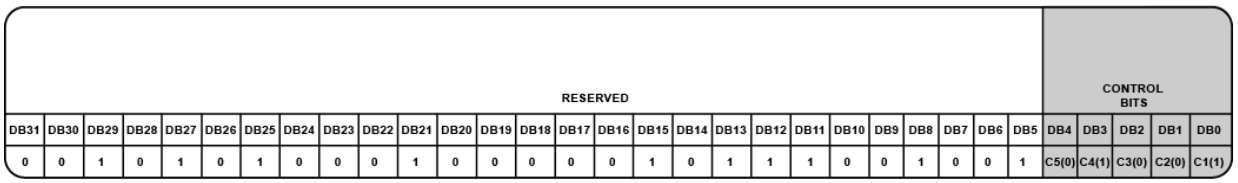
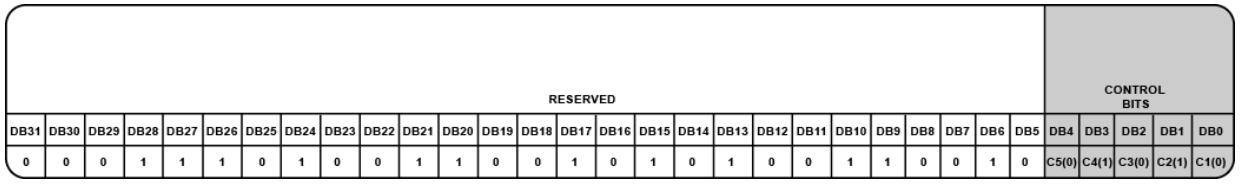
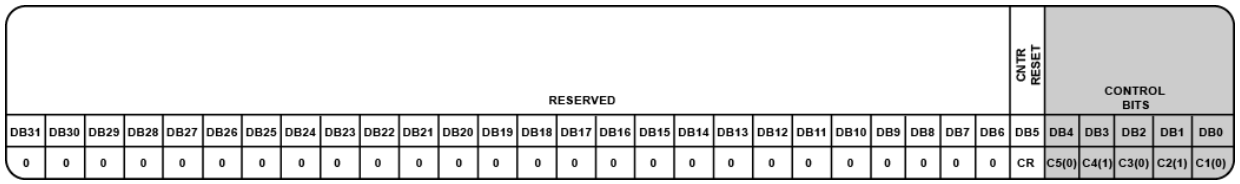


Figure 28. Register 9 (R9)



RESERVED																								CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	1	0	0	1	0	C5(0)	C4(1)	C3(0)	C2(1)	C1(0)

Figure 29. Register 10 (R10)



RESERVED																									CNTR RESET	CONTROL BITS				
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CR	C5(0)	C4(1)	C3(0)	C2(1)	C1(0)

Figure 30. Register 11 (R11)

REGISTER 0

Control Bits

With Bits[C5:C1] set to 0, 0, 0, 0, 0, Register R0 is programmed. Figure 19 shows the input data format for programming this register.

AUX Buffer Gain

Bits[DB23:DB21] set the auxiliary output buffer gain (see Figure 19).

AUX Divide-by-2

DB20 selects the auxiliary output divider. Setting this bit to 0 selects divide-by-2 (6GHz output), setting the bit to 1 selects divide-by-1 (12GHz output)

Power-Up R Counter

DB15 provides the power-up bit for the R counter block. Setting this bit to 0 performs a power-down of the counter block. Setting this bit to 1 returns the counter block to normal operation.

Power-Up N Counter

DB14 provides the power-up bit for the N counter block. Setting this bit to 0 performs a power-down of the counter block. Setting this bit to 1 returns the counter block to normal operation.

TX2 Amplitude Calibration

DB12 provides the control bit for amplitude calibration of TX2 output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of TX2 output.

TX1 Amplitude Calibration

DB11 provides the control bit for amplitude calibration of TX1 output. Set this bit to 0 for normal operation. Setting this bit to 1 performs an amplitude calibration of TX1 output.

Power-Up VCO

DB10 provides the power-up bit for the VCO. Setting this bit to 0 performs a power-down of the VCO. Setting this bit to 1 performs a power-up of the VCO.

VCO CAL

DB9 provides the control bit for frequency calibration of the VCO. Set this bit to 0 for normal operation. Setting this bit to 1 performs a VCO frequency calibration.

Power-Up ADC

DB8 provides the power-up bit for the ADC. Setting this bit to 0 performs a power-down of the ADC. Setting this bit to 1 performs a power-up of the ADC.

Power-Up TX2 Output

DB7 provides the power-up bit for TX2 output. Setting this bit to 0 performs a power-down of TX2 output. Setting this bit to 1 performs a power-up of TX2 output. Only one TX output can be powered up at any time, either TX1 DB6 or TX2 DB7.

Power-Up TX1 Output

DB6 provides the power-up bit for TX1 output. Setting this bit to 0 performs a power-down of TX1 output. Setting this bit to 1 performs a power-up of TX1 output. Only one TX output can be powered up at any time, either TX1 DB6 or TX2 DB7.

Power-Up LO Output

DB5 provides the power-up bit for LO output. Setting this bit to 0 performs a power-down of LO output. Setting this bit to 1 performs a power-up of LO output.

REGISTER 1

Control Bits

With Bits[C5:C1] set to 0, 0, 0, 0, 1, Register R1 is programmed. Figure 20 shows the input data format for programming this register.

TX Amplitude Calibration Reference Code

Bits[DB12:DB5] set TX Amplitude Calibration Reference Code (see Figure 20) for the 2 TX outputs during calibration. The output power on the TX outputs can be calibrated from -20dBm to 8dBm by setting the TX Amplitude Calibration Reference Code.

REGISTER 2

Control Bits

With bits[C5:C1] set to 0, 0, 0, 1, 0, Register R2 is programmed. Figure 21 shows the input data format for programming this register.

ADC Start

DB15 is used to start the ADC conversion. Setting this bit to 1 starts an ADC conversion.

ADC Average

Bits[14:13] program the ADC average, which is the number of averages of the ADC output. (see Figure 21)

ADC Clock Divider

DB[12:5] programs the clock divider, which is used as the sampling clock for the ADC. (see Figure 21) The output of the R divider block is the clock used to clock the ADC clock divider, a divider value should be programmed to ensure the ADC sampling clock is 1MHz.

REGISTER 3

Control Bits

With Bits[C5:C1] set to 0, 0, 0, 1, 1, Register R3 is programmed. Figure 22 shows the input data format for programming this register.

MUXOUT Control

The on-chip multiplexer of the ADF5901 is controlled by bits DB[15:12]. See Figure 22 for the truth table.

IO Level

DB[11] controls the DOUT logic levels. Setting this bit to 0 sets the DOUT logic level to 1.8v. Setting this bit to 1 sets the DOUT logic level to 3.3v.

Readback Control

Bits DB[11:5] controls the readback data to DOUT on the ADF5901. See Figure 22 for the truth table.

REGISTER 4

Control Bits

With Bits[C5:C1] set to 0, 0, 1, 0, 0, Register R4 is programmed. Figure 23 shows the input data format for programming this register.

Test Bus to ADC

DB[16] controls the ATEST pin. Set this bit to 0 for normal operation. Setting this bit to 1 connects the ADC input to the ATEST Bus.

Test Bus to Pin

DB[15] controls the ATEST pin. Setting this bit to 0 sets the ATEST pin to high impedance. Setting this bit to 1 connects the analog test bus to the ATEST pin.

Analog Test Bus

Bits DB[14:5] controls the Analog Test Bus. This allows access to internal test signals for the temperature sensor and power detectors. See Figure 23 for the truth table.

REGISTER 5

Control Bits

With Bits[C5:C1] set to 0, 0, 1, 0, 1, Register R5 is programmed. Figure 24 shows the input data format for programming this register.

12-Bit Integer Value (INT)

These 12 bits DB[28:17] set the INT value, which determines the integer part of the RF division factor. This is used in Equation 1 (see RF Synthesis: A Worked Example section). All integer values from 75 to 4095 are allowed.

12-Bit MSB Fractional Value (FRAC)

These 12 bits DB[16:5], along with bits DB[17:5] in the LSB FRAC register (Register R6), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall RF division factor. It is also used in Equation 1. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and bits DB[17:5] in the LSB FRAC register (Register R6) are the least significant bits (LSB). See the RF Synthesis: A Worked Example section for more information.

REGISTER 6

Control Bits

With Bits[C5:C1] set to 0, 0, 1, 1, 0, Register R6 is programmed. Figure 25 shows the input data format for programming this register.

13-Bit LSB FRAC Value

These 13 bits DB[17:5], along with bits DB[16:5] in the FRAC/INT register (Register R5), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall RF division factor. It is also used in Equation 1. These 13 bits are the least significant bits (LSB) of the 25-bit FRAC value, and Bits DB[14:3] in the INT/FRAC register are the most significant bits (MSB). See RF Synthesis: A Worked Example section for more information.

REGISTER 7

Control Bits

With Bits[C5:C1] set to 0, 0, 1, 1, 1, Register R7 is programmed. Figure 26 shows the input data format for programming this register.

Master Reset

DB25 provides a master reset bit for the part. Setting this bit to 1 performs a reset of the part and all the register map. Setting this bit to 0 returns the part to normal operation.

Clock Divider

Bits[DB22:DB1] set a divider for the VCO frequency calibration. The divider should be loaded such that the time base is 10usec (see Figure 26).

RDIV2

Setting the DB11 bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and VCO CAL block.

Reference Doubler

Setting DB10 to 0 feeds the REF_{IN} signal directly to the 5-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 5-bit R counter.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 50 MHz.

5-Bit R Counter

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the VCO CAL block. Division ratios from 1 to 31 are allowed.

REGISTER 8

Control Bits

With Bits[C5:C1] set to 0, 1, 0, 0, 0, Register R8 is programmed. Figure 27 shows the input data format for programming this register.

Frequency Calibration Clock

Bits[DB18:DB9] set a divider for the VCO frequency calibration clock. The divider should be loaded such that the time base is 10usec (see Figure 27).

REGISTER 9

Control Bits

With Bits[C5:C1] set to 0, 1, 0, 0, 1, Register R9 is programmed. Figure 28 shows the input data format for programming this register.

REGISTER 10

Control Bits

With Bits[C5:C1] set to 0, 1, 0, 1, 0, Register R10 is programmed. Figure 29 shows the input data format for programming this register.

REGISTER 11

Control Bits

With Bits[C5:C1] set to 0, 1, 0, 1, 1, Register R11 is programmed. Figure 30 shows the input data format for programming this register.

Counter Reset

DB5 provides a counter reset bit for the counters. Setting this bit to 1 performs a counter reset of the part counters. Setting this bit to 0 returns the part to normal operation.

INITIALIZATION SEQUENCE

After powering up the part, administer the following programming sequence. Sequence is locking the VCO to 24.125GHz with 100MHz reference and 50MHz reference divider frequency.

Step	Register	HEX Code	Description
1	R7	02000007	Master Reset
2	R11	0000002B	Counter Reset
3	R11	0000000B	Counters Enabled
4	R10	1D32A64A	
5	R9	2A20B929	
6	R8	40003E88	Frequency Calibration Divider Clock 100kHz
7	R0	809FE520	Power-Up Part and LO (10us)
8	R7	011F4827	R Counter Clock 50MHz, Calibration Clock 100kHz
9	R6	00000006	LSB FRAC = 0
10	R5	01E28005	INT = 241, MSB FRAC = 1024, => N = 240.25
11	R4	00200004	ATEST High Impedance
12	R3	01890803	IO level 3.3V
13	R2	00020642	ADC Clock 1MHz
14	R1	FFF7FFE1	TX Amplitude Level
15	R0	809FE720	VCO Frequency Calibration (800us)
16	R0	809FE560	TX1 ON, TX2 OFF, LO ON
17	R0	809FED60	TX1 Amplitude Calibration (400us)
18	R0	809FE5A0	TX1 OFF, TX2 ON, LO ON
19	R0	809FF5A0	TX2 Amplitude Calibration (400us)
20	R9	2800B929	
21	R0	809F25A0	Disabled Counters

Table 6. Initialization Sequence

RE-CALIBRATION SEQUENCE

The ADF5901 can be re-calibrated once the initialization sequence has been completed and the parts is powered up.

Step	Register	HEX Code	Description
1	R0	819FE520	Enable Counters. TX1 OFF, TX2 OFF, LO ON
2	R9	2A20B929	
3	R1	FFF7FFE1	Set TX Amplitude Level
4	R0	819FE720	VCO Frequency Calibration (800us)
5	R0	819FE560	TX1 ON, TX2 OFF, LO ON
6	R0	819FED60	TX1 Amplitude Calibration (400us)
7	R0	819FE5A0	TX1 OFF, TX2 ON, LO ON
8	R0	809FF5A0	TX2 Amplitude Calibration (400us)
9	R9	2800B929	
10	R0	819F25A0	Disabled Counters

Table 7. Re-Calibration Sequence

TEMPERATURE SENSOR

The ADF5901 has an on-chip temperature sensor that can be accessed on ATEST pin or as a digital word on DOUT following an ADC conversion. The temperature sensor operates over the full operating temperature range of −40°C to +105°C. The accuracy can be improved by doing a 1-point calibration at room temperature and storing the result in memory.

With Temperature Sensor on the Analog Test Bus and Test Bus connected to ATEST pin (Register 4 0000A064) the ATEST voltage can be converted to temperature with the following.

$$\boldsymbol{Temperature}(°C) = \frac{(\boldsymbol{V_{ATEST}} - \boldsymbol{V_{off}})}{\boldsymbol{V_{gain}}}$$

where

$\boldsymbol{V_{ATEST}}$ = Voltage on ATEST pin

$\boldsymbol{V_{off}}$ = Offset Voltage = 0.699

$\boldsymbol{V_{gain}}$= Voltage Gain 6.4m

The temperature sensor result can be converted to a digital word with the ADC and readback on DOUT with the following sequence.

Step	Register	HEX Code	Description
1	R0	809FA5A0	Enable Counters
2	R4	00012064	Test Bus to ADC and V_{TEMP} to Test Bus
3	R2	00028C82	Start ADC Conversion
4	R3	018902C3	ADC to DOUT
5			Readback DOUT
6	R0	809F25A0	Disabled Counters

Table 8. Temperature Sensor to ADC

The DOUT word can be converted to temperature with the following.

$$\boldsymbol{Temperature}(℃) = \frac{\left((\boldsymbol{ADC} \times \boldsymbol{V_{LSB}}) - \boldsymbol{V_{off}}\right)}{\boldsymbol{V_{gain}}}$$

where

$\boldsymbol{ADC}$ = ADC code read back on DOUT

$\boldsymbol{V_{LSB}}$ = ADC LSB Voltage 7.33m

$\boldsymbol{V_{off}}$ = Offset Voltage = 0.699

$\boldsymbol{V_{gain}}$= Voltage Gain 6.4m

RF SYNTHESIS: A WORKED EXAMPLE

The following equation governs how the ADF5901 should be programmed :

$$RF_{OUT} = [N + (FRAC/2^{25})] \times [f_{REF}] \times 2 \quad (4)$$

where:
RF_{OUT} is the RF frequency output.
N is the integer division factor.
$FRAC$ is the fractionality.

$$f_{REF} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (5)$$

where:
REF_{IN} is the reference frequency input.
D is the REF_{IN} doubler bit, DB10 in Register R7 (0 or 1).
R is the reference division factor.
T is the reference divide-by-2 bit, DB11 in Register R7 (0 or 1).

For example, in a system where a 24.125 GHz RF frequency output (RF_{OUT}) is required and a 100 MHz reference frequency input (REF_{IN}) is available. f_{REF} is set to 50MHz

From Equation 5,

$$f_{REF} = [100\ \text{MHz} \times (1 + 0)/(1 \times (1+1)] = 50\ \text{MHz}$$

From Equation 4,

$$24.125\ \text{GHz} = 50\ \text{MHz} \times (N + FRAC/2^{25}) \times 2$$

Calculating the N and FRAC values,

$$N = int(RF_{OUT}/(f_{REF} \times 2)) = 241$$
$$FRAC = F_{MSB} \times 2^{13} + F_{LSB}$$
$$F_{MSB} = int(((RF_{OUT}/(f_{REF} \times 2)) - N) \times 2^{12}) = 1024$$
$$F_{LSB} = int(((((RF_{OUT}/(f_{REF} \times 2)) - N) \times 2^{12}) - F_{MSB}) \times 2^{13}) = 0$$

where:
F_{MSB} is the 12-bit MSB FRAC value in Register R5.
F_{LSB} is the 13-bit LSB FRAC value in Register R6.
$int()$ makes an integer of the argument in parentheses.

APPLICATIONS INFORMATION

APPLICATION OF THE ADF5901 IN FMCW RADAR

Figure 31 shows the application of the ADF5901 in a frequency modulated continuous wave (FMCW) radar system.

In the FMCW radar system, the ADF4159 generates the sawtooth or triangle ramps necessary for this type of radar to operate.

The ADF4159 controls the VTUNE pin on the ADF5901 (Tx) monolithic microwave integrated circuit (MMIC) and thus the frequency of the voltage controlled oscillator (VCO) and the Tx output signal on TXOUT1 or TXOUT2. The LO signal from the ADF5901 is fed to the LO input on the ADF5904.

The ADF5904 downconverts the signal from the four receiver antennas to baseband with the LO signal from the Tx MMIC.

The downconverted baseband signals from the four receiver channels on the ADF5904 are fed to the ADAR7251 4-channel, continuous time (CT), Σ-Δ analog-to-digital converter (ADC).

A digital signal processor (DSP) follows the ADC to handle the target information processing.

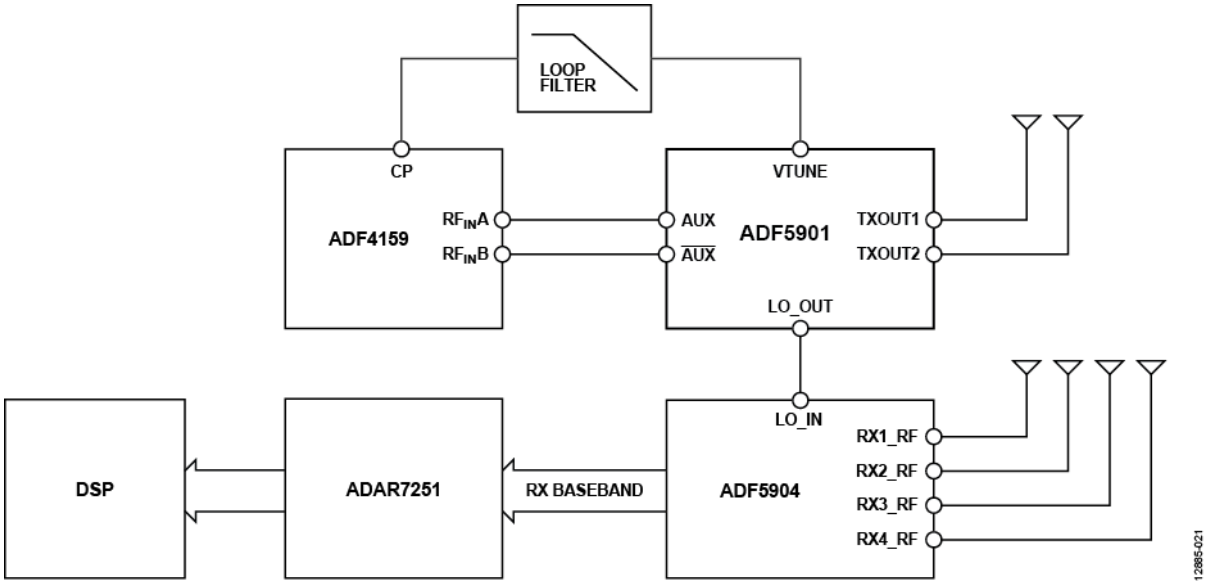


Figure 31. FMCW Radar with ADF5901

OUTLINE DIMENSIONS

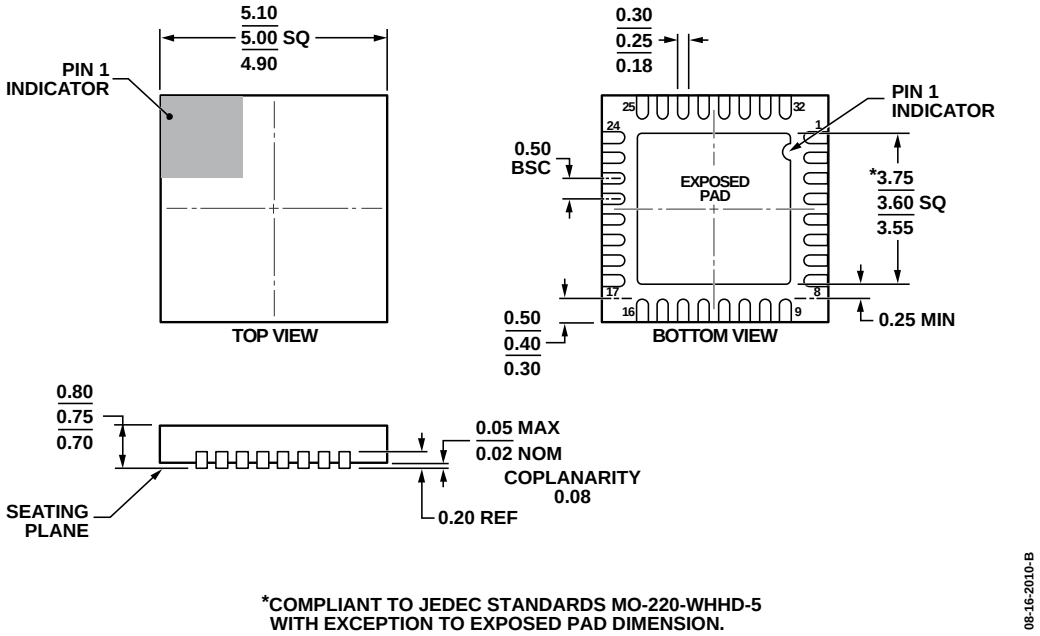


Figure 32. 32-Lead Lead Frame Chip Scale Package [LFCSP_LQ] (CP-32-12)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF5901WCCPZ-U6	–40°C to + 105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADF5901WCCPZ-U6-RL7	–40°C to + 105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EV-ADF5901SD2Z-U6		Evaluation Board	

PRODUCTS

The ADF5901W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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