Angle Sensor

GMR-Based Angle Sensor

TLE5012B

Data Sheet

V 1.1, 2012-01
Final

Sensors

Edition 2012-01

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V 1.1, 2012-01	
12	Table 1, SPC interface at pin 5 added
31	Table 16, bit[14] and bit[12] updated
33	Sensor with preset PWM added
35	Sensor with preset SPC added
37	Sensor with preset HSM added
41	Sensor with preset IIF added
general	Correction of typing errors

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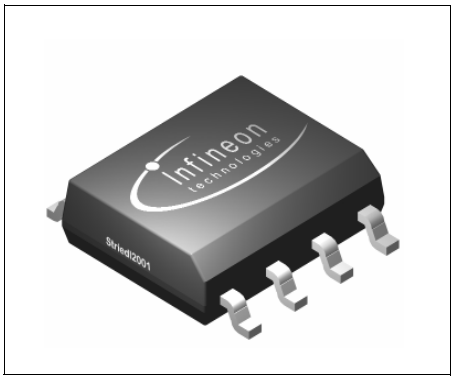
1 Product Description



1.1 Overview

The TLE5012B is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance (iGMR) elements.

Highly precise angle values are adetermined over a wide temperature range and a long lifetime using an internal autocalibration algorithm.

Data communications are accomplished with a bi-directional Synchronous Serial Communication (SSC) that is SPI-compatible.

The absolute angle value and other values are transmitted via SSC or via a Pulse-Width-Modulation (PWM) Protocol. The sine and cosine raw values can also be read out. These raw signals are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLE5012B is a pre-calibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into flip-flops, where these values can be changed by the application-specific parameters.

Online diagnostic functions are provided to ensure reliable operation.

Product Type	Marking	Ordering Code	Package
TLE5012B E1000	012B1000	SP000905682	PG-DSO-8
TLE5012B E3005	012B3005	SP000905686	PG-DSO-8
TLE5012B E5000	012B5000	SP000905690	PG-DSO-8
TLE5012B E9000	012B9000	SP000905694	PG-DSO-8

1.2 Features

- **G**iant **M**agneto **R**esistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- Full calibrated 0 - 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single bit SD-ADC
- 15 bit representation of absolute angle value on the output (resolution of 0.01°)
- 16 bit representation of sine / cosine values on the interface
- Max. 1.0° angle error over lifetime and temperature-range with activated auto-calibration
- Bi-directional SSC Interface up to 8Mbit/s
- Supports Safety Integrity Level (SIL) with diagnostic functions and status information
- Interfaces: SSC, PWM, Incremental Interface (IIF), Hall Switch Mode (HSM), Short PWM Code (SPC)
- 0.25 µm CMOS technology
- Automotive qualified: -40°C to 150°C (junction temperature)
- ESD > 4kV (HBM)
- RoHS compliant (Pb-free package)

1.3 Application Example

The TLE5012B GMR-based angle sensor is designed for angular position sensing in automotive applications such as:

- Electrical commutated motor (e.g. used in Electric Power Steering (EPS))
- Rotary switches
- Steering angle measurements
- General angular sensing

2 Functional Description

2.1 General

The Giant Magneto Resistance (GMR) sensor is implemented using vertical integration. This means that the GMR-sensitive areas are integrated above the logic portion of the TLE5012B device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

The advantage of a full-bridge structure is that the maximum GMR signal is available and temperature effects cancel out each other.

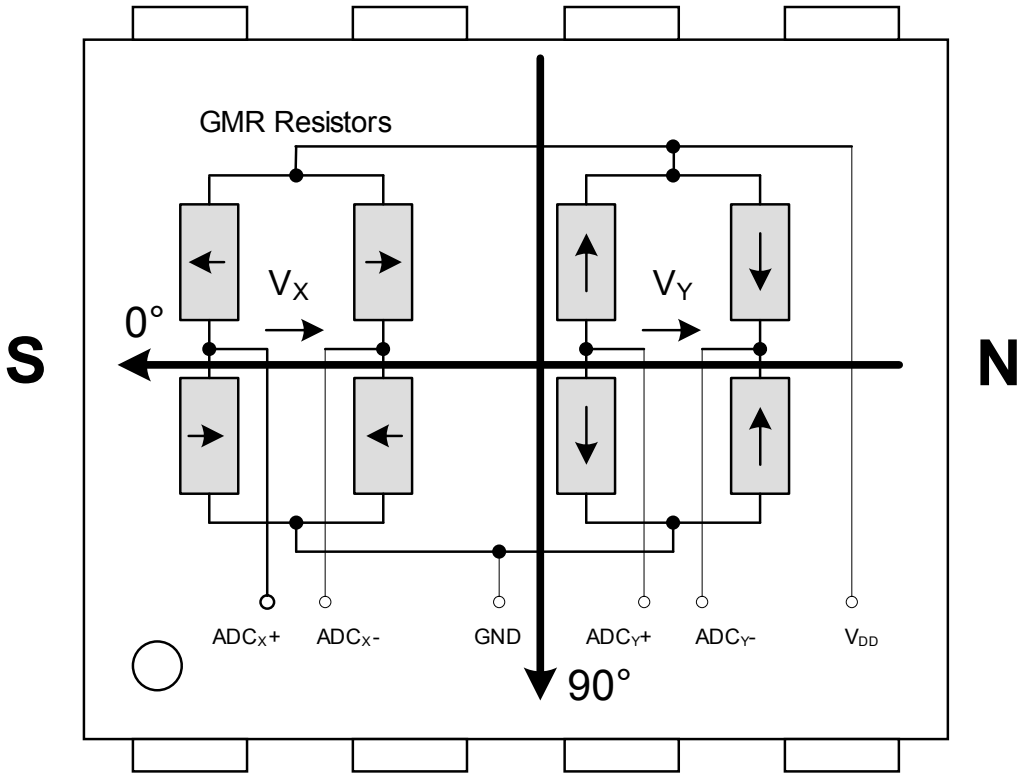


Figure 1 Sensitive bridges of the GMR sensor

*Note: In **Figure 1**, the arrows in the resistors represent the magnetic direction which is fixed in the reference layer. If the external magnetic field is parallel to the direction of the Reference Layer, the resistance is minimal. If they are anti-parallel, resistance is maximal.*

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are orientated orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN, the true 360° angle value can be calculated, based on the relationship of X and Y signals.

Because only the relative values influence the result, the absolute magnitude of the two signals is of minor importance. Therefore, it is possible to compensate for most external influences on the amplitudes.

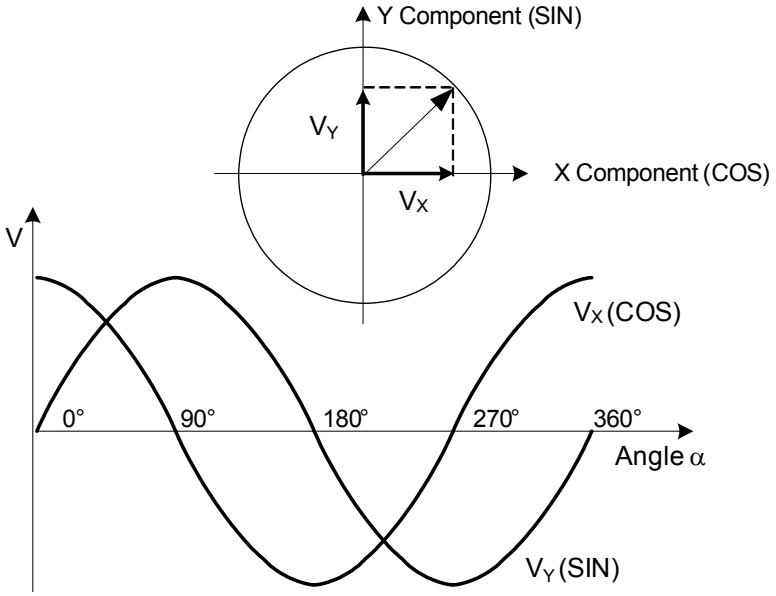


Figure 2 Ideal output of the GMR sensor bridges

2.2 Pin Configuration

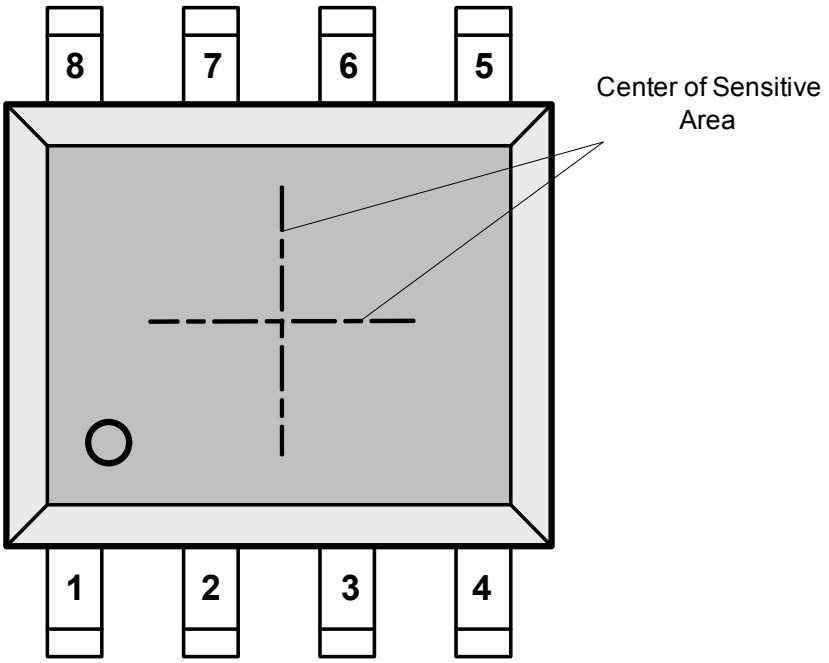


Figure 3 Pin configuration (top view)

2.3 Pin Description

Table 1 Pin Description

Pin No.	Symbol	In/Out	Function
1	IFC (CLK / IIF_IDX / HS3)	I/O	Interface C: External Clock / IIF Index / Hall Switch Signal 3
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA	I/O	SSC Data
5	IFA (IIF_A / HS1 / PWM / SPC)	O	Interface A: IIF Phase A / Hall Switch Signal 1 / PWM / SPC output
6	V_{DD}	-	Supply Voltage
7	GND	-	Ground
8	IFB (IIF_B / HS2)	O	Interface B: IIF Phase B / Hall Switch Signal 2

2.4 Block Diagram

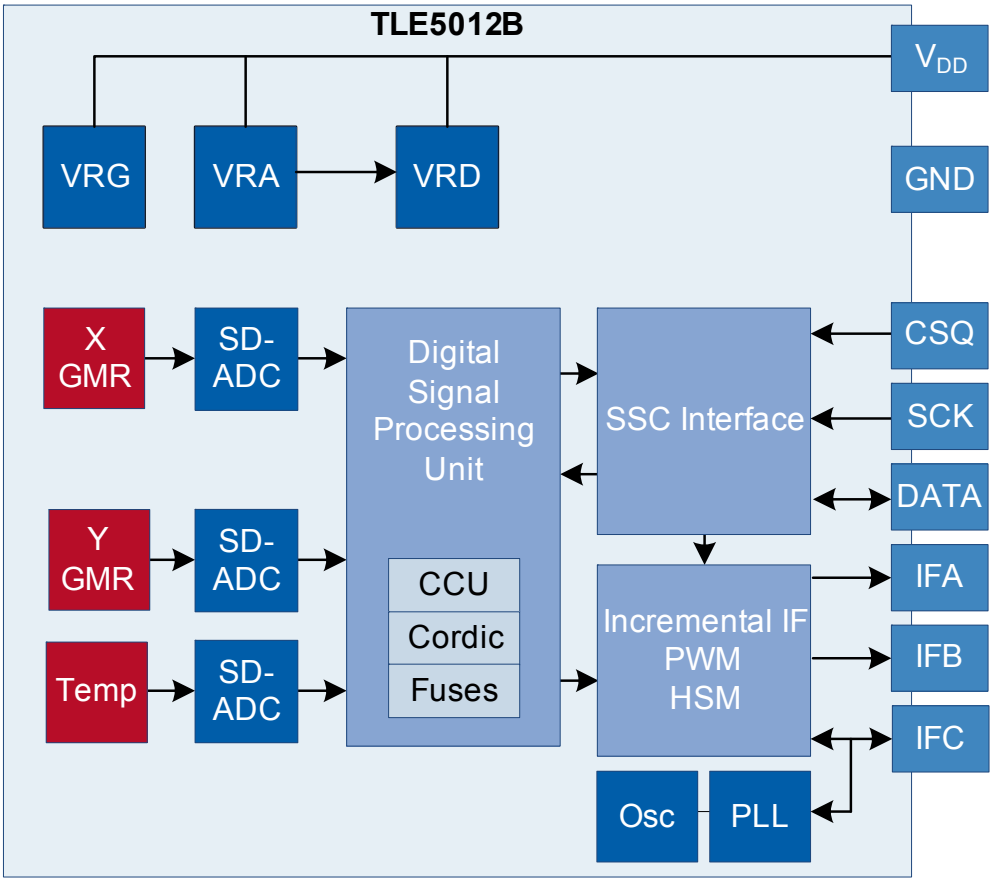


Figure 4 TLE5012B block diagram

2.5 Functional Block Description

2.5.1 Internal Power Supply

The internal stages of the TLE5012B are supplied with several voltage regulators:

- GMR Voltage Regulator, VRG
- Analog Voltage Regulator, VRA
- Digital Voltage Regulator, VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.5.2 Oscillator and PLL

The internal frequency oscillator feeds the Phase-Locked Loop (PLL). Therefore, the external clock (CLK) can also be used.

2.5.3 SD-ADC

The SD-ADCs transform the analog GMR voltages and temperature voltage into the digital domain.

2.5.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- **C**apture **C**ompare **U**nit (**CCU**), which is used to generate the PWM signal
- **CO**ordinate **R**otation **DI**gital **C**omputer (**CORDIC**), which contains the trigonometric function for angle calculation
- Fuses, which contain the calibration parameters

2.5.5 Interfaces

Various Interfaces can be selected:

- SSC Interface
- PWM
- Incremental Interface
- Hall Switch Mode
- Short PWM Code

2.5.6 Safety Features

The TLE5012B offers a multiplicity of safety features to support the Safety Integrity Level (SIL). Infineon's sensors that are intended for this purpose are identified by the following logo:

Figure 5 PRO-SIL™ Logo

Safety features are:

- Test vectors switchable to ADC input
- Inversion or combination of filter input streams
- Data transmission check via 8-bit **C**yclic **R**edundancy **C**heck (**CRC**)
- Self-test routines
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

Disclaimer

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The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.

SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency.

SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.

SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

3 Specification

3.1 Application Circuit

The application circuits in **Figure 6**, **Figure 7**, **Figure 8** and **Figure 9** show the various communication possibilities of the TLE5012B.

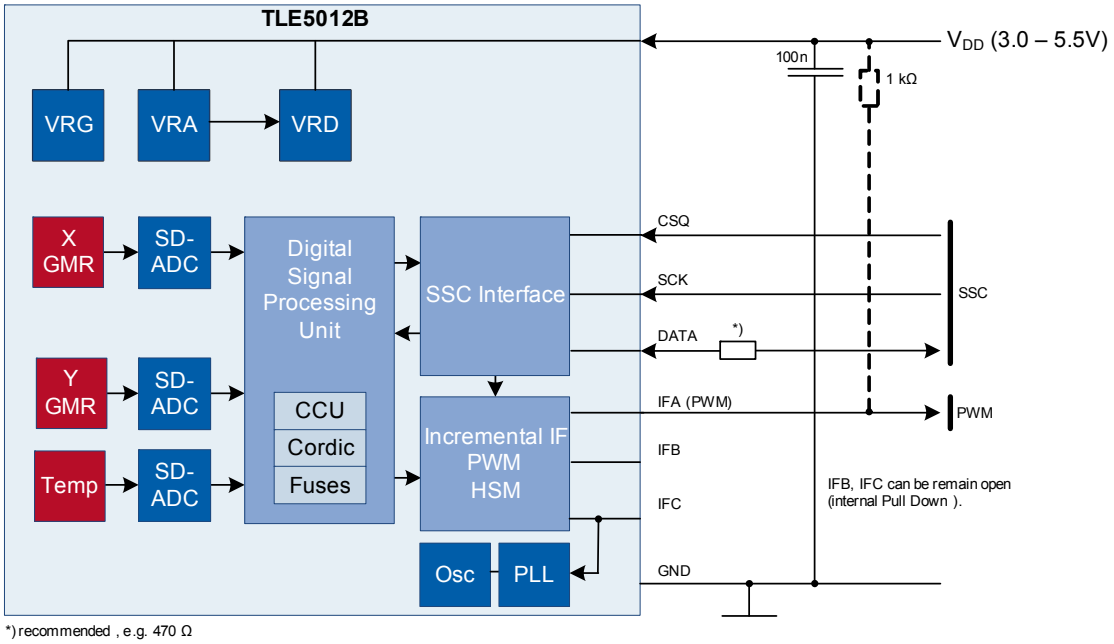

Figure 6 Application circuit for TLE5012B with SSC and PWM interface (using internal CLK)

Figure 6 shows a basic block diagram of the TLE5012B with PWM interface.In addition to the PWM interface, the SSC interface could be used. Within the SSC interface, the PWM mode is selectable between push-pull and open-drain.

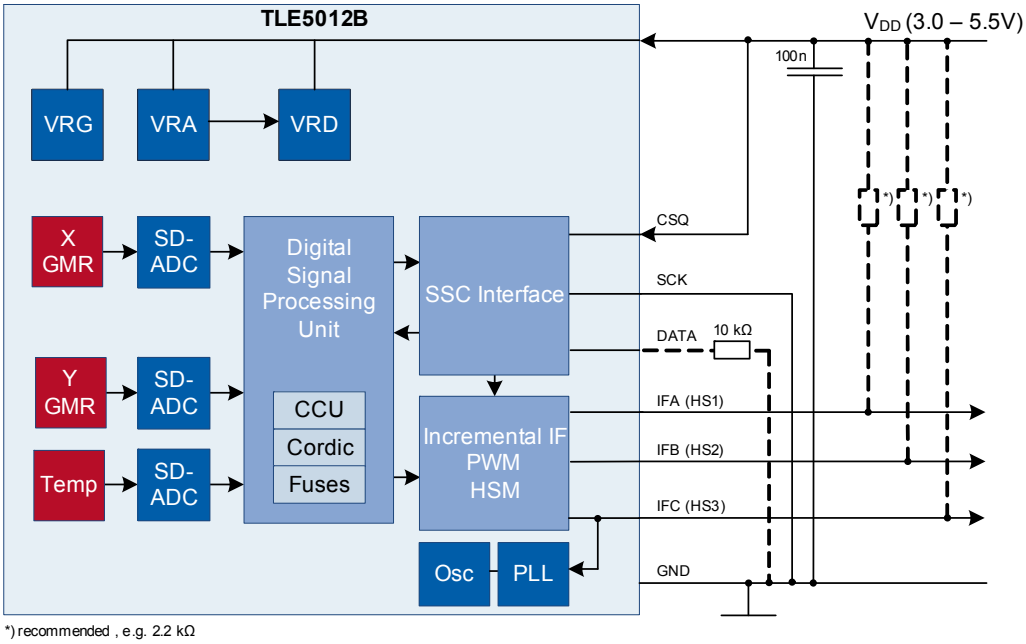

Figure 7 Application circuit for TLE5012B with HS Mode (using internal CLK)

Figure 7 shows a basic block diagram of the TLE5012B with HS Mode. In addition to the HS Mode, the SSC interface could be used in parallel. Within the SSC- Interface, the HS Mode is selectable between push-pull and open-drain.

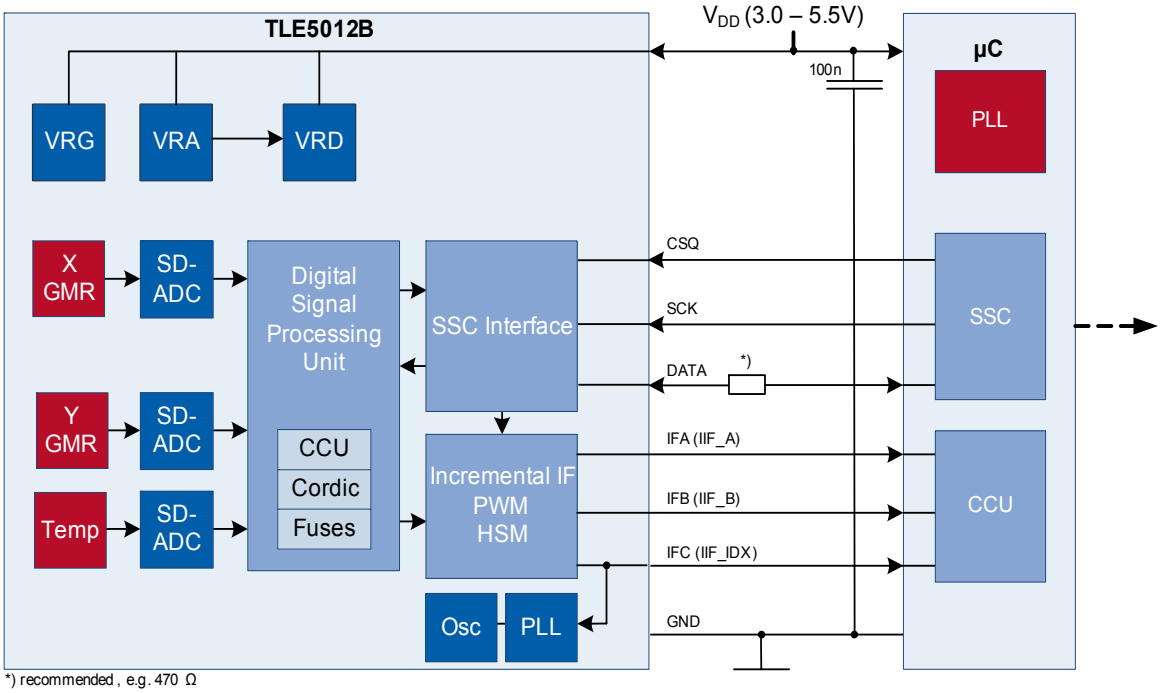

Figure 8 Application circuit for TLE5012B with SSC and IIF interface (using external CLK)

Figure 8 shows a basic block diagram of an angle-sensor system using a TLE5012B and a microcontroller for rotor positioning applications. The depicted interface configuration is needed for high-speed applications suchas electrical commutated motor drives. It is possible to connect the TLE5012B to a microcontroller via Incremental Interface and for safety reasons also via the SSC interface.

The TLE5012B can be configured with PWM only (**Figure 9**). This is only possible with the TLE5012B-E5000 type.[1)]

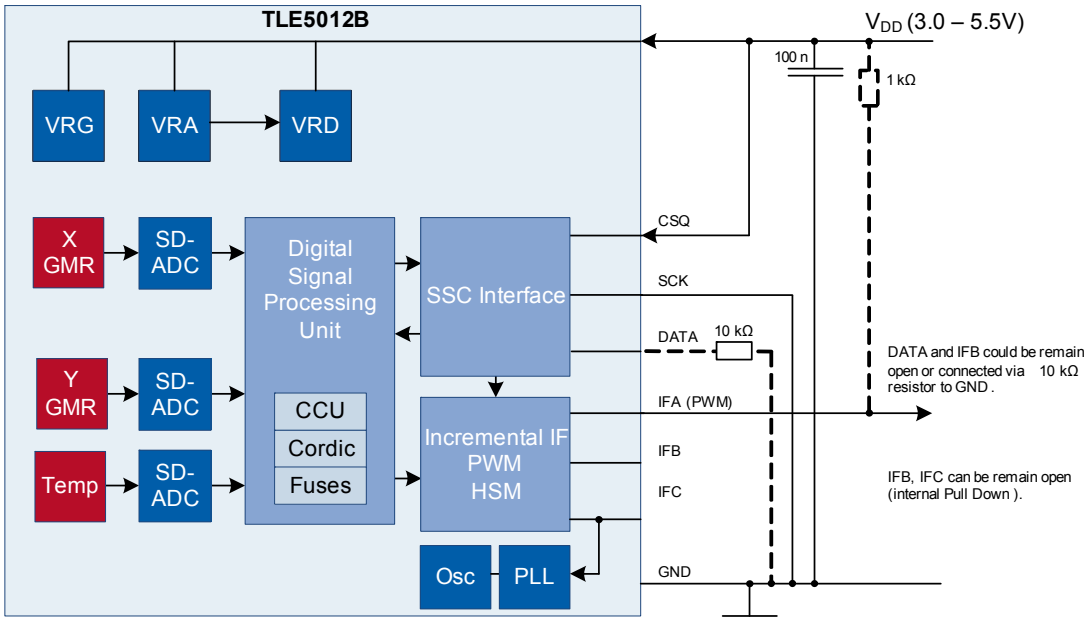

Figure 9 Application circuit for TLE5012B with only PWM interface (using internal CLK)

The TLE5012B can be configured with SPC only (**Figure 9**). This is only possible with the TLE5012B-E9000 type.[1)]

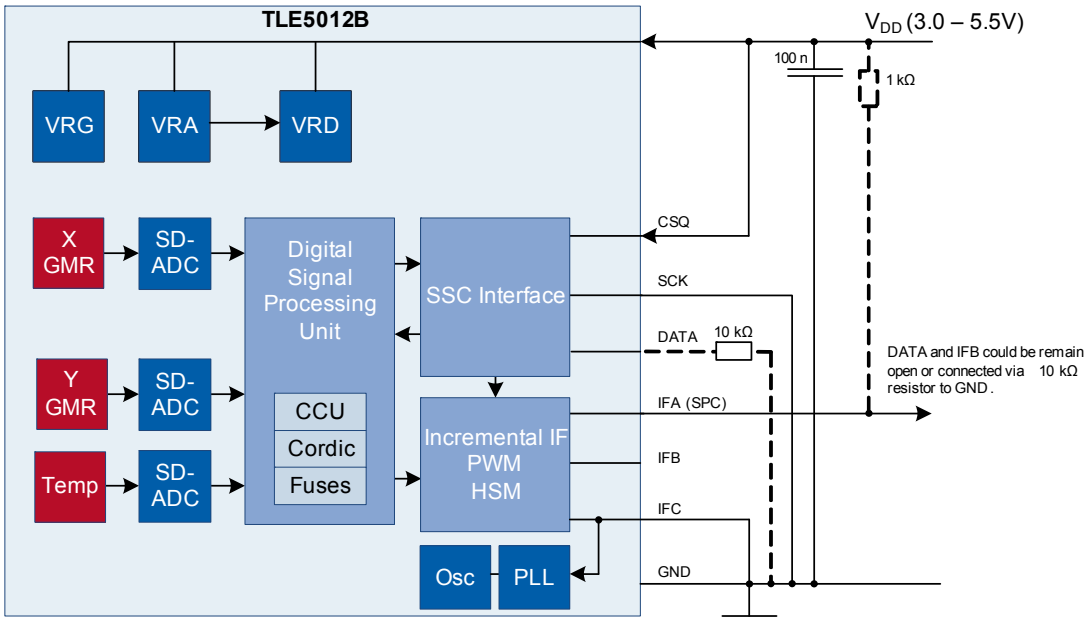

Figure 10 Application circuit for TLE5012B with only SPC interface (S_NR = 00)

1) For more information get in contact with Infineon

3.2 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5		6.5	V	Max 40 h/Lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5		6.5	V	Additionally V_{DD} + 0.5 V may not be exceeded
Junction temperature	T_J	-40		150	°C	
				150	°C	For 1000 h, not additive
Magnetic field induction	B			200	mT	Max. 5 min @ T_A = 25°C
				150	mT	Max. 5 h @ T_A = 25°C
Storage temperature	T_{ST}	-40		150	°C	Without magnetic field

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012B. All parameters specified in the following sections refer to these operating conditions, unless otherwise noted. **Table 3** is valid for -40°C < T_J < 150°C unless otherwise noted.

Table 3 Operating range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	5.0	5.5	V	1)
Output current (DATA-Pad)	I_Q			-25	mA	PAD_DRV =’0x’, sink current2)3)
				-5	mA	PAD_DRV =’10’, sink current2)3)
				-0.4	mA	PAD_DRV =’11’, sink current2)3)
Output current (IFA / IFB / IFC - Pad)	I_Q			-15	mA	PAD_DRV =’0x’, sink current2)3)
				-5	mA	PAD_DRV =’1x’, sink current2)3)
Input voltage	V_{IN}	-0.3		5.5	V	V_{DD} + 0.3 V may not be exceeded

Table 3 Operating range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Magnetic induction at T_A = 25°C 4)5)	B_{XY}	30		50	mT	-40°C < T_J < 150°C
	B_{XY}	30		60	mT	-40°C < T_J < 100°C
	B_{XY}	30		70	mT	-40°C < T_J < 85°C
Expanded magnetic induction at T_A = 25°C 4)5)6)	B_{XY}	25		30	mT	Additional angle error of 0.1°
Angle range	Ang	0		360	°	

1) Directly blocked with 100-nF ceramic capacitor
2) Max. current to GND over open-drain output
3) At V_{DD} = 5V
4) Values refer to a homogeneous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0mT).
5) See **Figure 11**
6) 0h

The field strength of a magnet can be selected within the colored area of **Figure 11**. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J=100°C, a magnet with up to 60mT at T_A = 25°C is allowed.

It is also possible to widen the magnetic field range for higher temperatures. In that case, additional angle errors have to be considered (see Application Note "GMR Angle Error Extension").

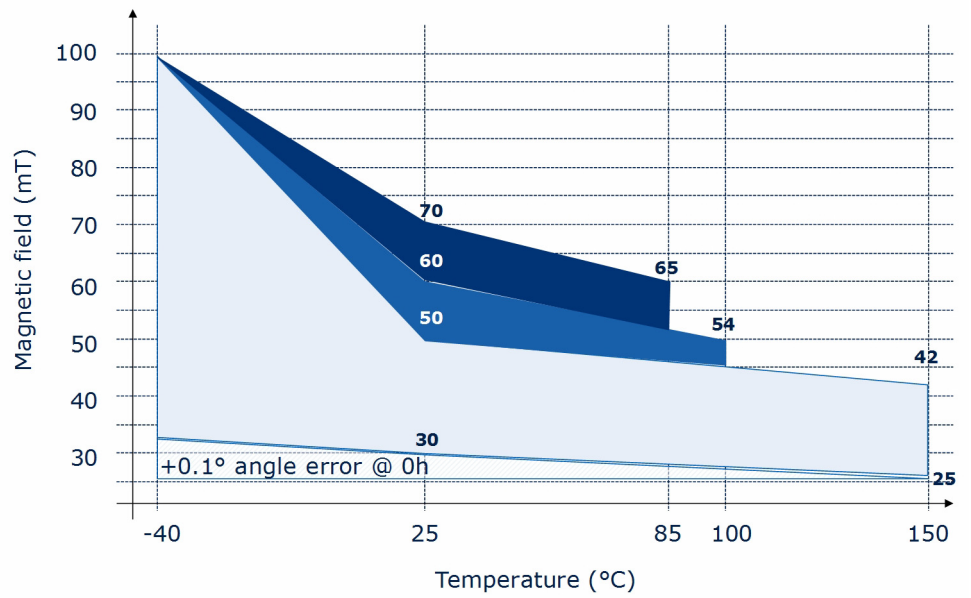

Figure 11 Magnet performance (ambient temperature)

*Note: The thermal resistances listed in **Table 29 "Package Parameters" on Page 46** must be used to calculate the corresponding ambient temperature of the sensor.*

Calculation of the Junction Temperature

The total power dissipation P_{TOT} of the chip increases its temperature above the ambient temperature.

The power multiplied by the total thermal resistance R_{thJA} (junction to ambient) leads to the final junction temperature. R_{thJA} is the sum of the addition of the values of the two components Junction to Case and Case to Ambient.

$$R_{thJA} = R_{thJC} + R_{thCA} \quad (1)$$
$$T_J = T_A + \Delta T$$
$$\Delta T = R_{thJA} \times P_{TOT} = R_{thJA} \times (V_{DD} \times I_{DD} + (V_{DD} - V_{OUT}) \times I_{OUT})$$

Example (assuming no load on V_{out}):

$$V_{DD} = 5V \quad (2)$$
$$I_{DD} = 14mA$$
$$\Delta T = 150\left[\frac{K}{W}\right] \times (5[V] \times 0.014[A] + 0[VA]) = 10.5K$$

For molded sensors, the calculation with R_{thJC} is more appropriate.

3.4 Characteristics

3.4.1 Electrical Parameters

The indicated electrical parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25 °C, unless individually specified. All other values correspond to -40 °C < T_J < 150°C.

Table 4 Electrical parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current	I_{DD}		14	16	mA	
POR level	V_{POR}	2.0		2.9	V	Power-on reset
POR hysteresis	V_{PORhy}		30		mV	
Pull-up current	I_{PU}	-10		-225	µA	CSQ
		-10		-150	µA	DATA
Pull-down current	I_{PD}	10		225	µA	SCK
		10		150	µA	IFA, IFB, IFC
Power-on time [1]	t_{Pon}		5	7	ms	$V_{DD} > V_{DDmin}$; SBIST = 1
				0.5	ms	$V_{DD} > V_{DDmin}$; SBIST = 0[2]

1) Within “Power-on time,” write access is not permitted

2) Not subject to production test - verified by design/characterization

Table 5 Electrical parameters for 4.5V < V_{DD} < 5.5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	V_{L5}			0.3 V_{DD}	V	
Input signal high level	V_{H5}	0.7 V_{DD}			V	
Output signal low level	V_{OL5}			1	V	DATA; I_Q = -25 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='10'), I_Q = -0.4 mA (PAD_DRV='11')
				1	V	IFA,IFB, IFC; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='1x')

Table 6 Electrical parameters for 3.0V < V_{DD} < 3.6V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input signal low level	V_{L3}			0.3 V_{DD}	V	
Input signal high level	V_{H3}	0.7 V_{DD}			V	
Output signal low level	V_{OL3}			0.9	V	DATA; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='10'), I_Q = -0.24 mA (PAD_DRV='11')
				0.9	V	IFA,IFB; I_Q = - 10 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='1x')

3.4.2 ESD Protection

Table 7 ESD protection

Parameter	Symbol	Values		Unit	Notes
		min.	max.		
ESD voltage	V_{HBM}		±4.0	kV	Human Body Model[1)]
	V_{SDM}		±0.5	kV	Socketed Device Model[2)]

1) Human Body Model (HBM) according to: AEC-Q100-002

2) Socketed Device Model (SDM) according to: ESDA/ANSI/ESD SP5.3.2-2008

3.4.3 GMR Parameters

All parameters apply over B_{XY} = 30mT and T_A = 25°C, unless otherwise specified.

Table 8 Basic GMR parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
X, Y output range	RG_{ADC}			±23230	digits	Operating range[1)]
X, Y amplitude [2)]	A_X, A_Y	6000	9500	15781	digits	
		3922		20620	digits	Operating range
X, Y synchronism [3)]	k	87.5	100	112.49	%	
X, Y offset [4)]	O_X, O_Y	-2048	0	+2047	digits	
X, Y orthogonality error	φ	-11.25	0	+11.24	°	
X, Y without field	X_0, Y_0	-5000		+5000	digits	Without magnet[1)]

1) Not subject to production test - verified by design/characterization
2) See **Figure 12**
3) $k = 100*(A_X/A_Y)$
4) $O_Y=(Y_{MAX} + Y_{MIN}) / 2$; $O_X = (X_{MAX} + X_{MIN}) / 2$

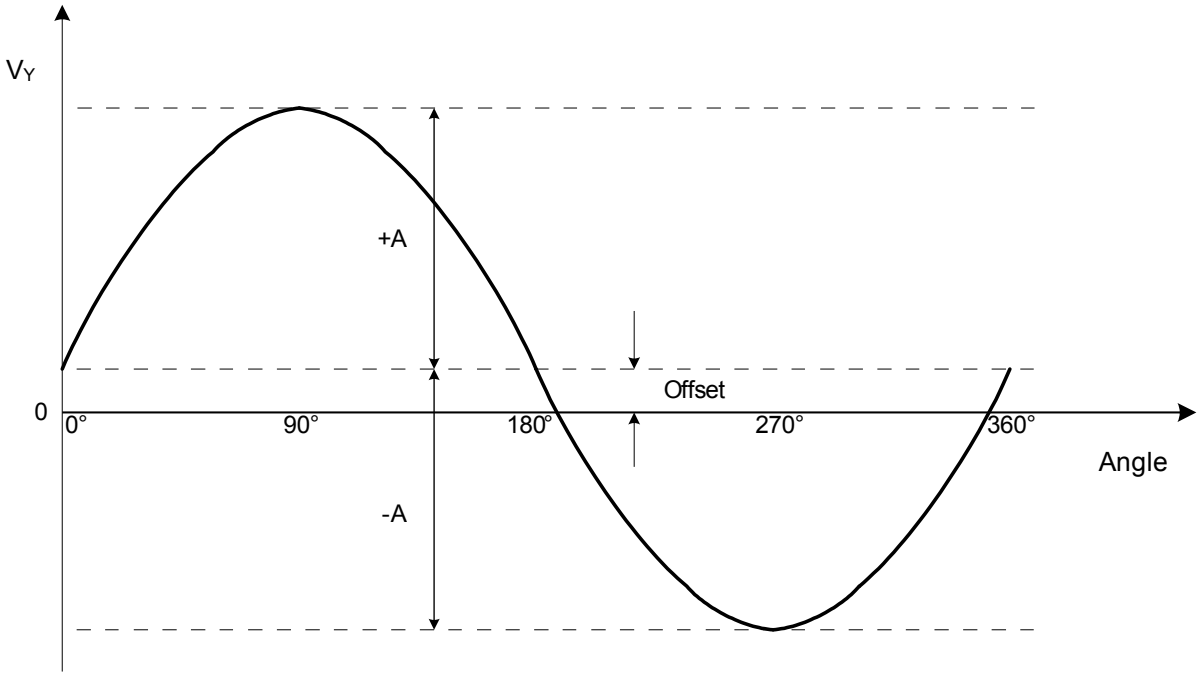

Figure 12 Offset and amplitude definition

3.4.4 Angle Performance

After internal calculation, the sensor has a remaining error, as shown in **Table 9**. The error value refers to B_Z= 0mT and the operating conditions given in **Table 3 "Operating range" on Page 18**.

The overall angle error represents the relative angle error. This error describes the deviation from the reference line after zero-angle definition.

Table 9 Angle performance

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overall angle error (with auto-calibration)	α_{Err}		0.6[1)]	1.0	°	Including lifetime and temperature drift[2)3)4)]
Overall angle error (without auto-calibration)	α_{Err}		0.6[1)]	1.6	°	Including temperature drift[2)3)5)]

1) At 25°C, B = 30mT
2) Including hysteresis error, caused by revolution direction change
3) Only with calibrated GMR-compensation parameters of customer setup; relative error after zero angle definition
4) Not subject to production test - verified by design/characterization
5) 0h

Autocalibration

The autocalibration enables online parameter calculation and therefore reduces the angle error due to temperature drifts, lifetime drifts, and misalignments.

The TLE5012B is a pre-calibrated sensor. After start-up, the parameters in the laser fuses get loaded into flip-flops. The TLE5012B needs 1.5 revolutions to generate new autocalibration parameters. The update mode can be chosen within the Interface Mode 2 register (AUTOCAL). The parameters are updated in a smooth way to avoid an angle jump on the output. Therefore only one Least-Significant Bit (LSB) will be changed within the chosen range or time. The autocalibration is done continuously.

AUTOCAL Modes:

- 00: No autocalibration
- 01: Autocalibration Mode 1. One LSB to final values within the update time t_{upd} (depending on FIR_MD setting).
- 10: Autocalibration Mode 2. Only one LSB update over one full parameter generation (1.5 revolutions). After update of one LSB, the autocalibration will calculate the parameters again.
- 11: Autocalibration Mode 3. One LSB to final values within an angle range of 11.25°

3.4.5 Signal Processing

The signal path of the TLE5012B is depicted in **Figure 13**. It consists of the GMR-bridge, ADC, filter and angle calculation. Depending on the filter configuration, a total delay times is calculated. In addition to this delay time, the delay time of the interface has to be considered. The delay time leads to an additional angle error at higher speeds. By enabling the prediction, the signal delay time can be reduced (**Figure 14**). The prediction uses the difference between current and last angle value, and calculates the output value by adding this difference to the current value. A linear prediction is achieved with following equation.

$$\alpha(t+1) = 2 \cdot \alpha(t) - \alpha(t-1) \quad (3)$$

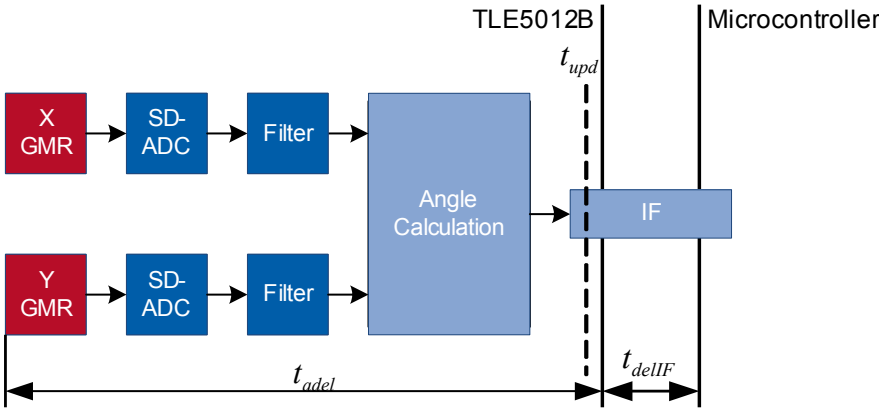

Figure 13 Signal path

At FIR_MD = '00' only raw values can be read out, due to the more time-consuming angle calculation.

Table 10 Signal processing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Update rate at interface	t_{upd}		21.3		µs	FIR_MD = 0 (only raw values)[1)2)]
			42.7		µs	FIR_MD = 1[1)2)]
			85.3		µs	FIR_MD = 2 (default)[1)2)]
			170.6		µs	FIR_MD = 3[1)2)]
Angle delay time[3)]	t_{adel}		60	70	µs	FIR_MD = 1[1)2)]
			80	95	µs	FIR_MD = 2[1)2)]
			120	140	µs	FIR_MD = 3[1)2)]
Angle delay time with prediction[3)]	t_{adel}		20	30	µs	FIR_MD = 1; PREDICT = 1 [1)2)]
			5	20	µs	FIR_MD = 2; PREDICT = 1 [1)2)]
			-40	-20	µs	FIR_MD = 3; PREDICT = 1 [1)2)]
Angle noise	N_{Angle}		0.11		°	FIR_MD = 0, (1 Sigma)[2)]
			0.08		°	FIR_MD = 1, (1 Sigma)[2)]
			0.05		°	FIR_MD = 2, (1 Sigma)[2)] (default)
			0.04		°	FIR_MD = 3, (1 Sigma)[2)]

1) Without internal oscillator frequency variation (**Section 3.4.6**)
2) Not subject to production test - verified by design/characterization
3) Valid at constant rotation speed

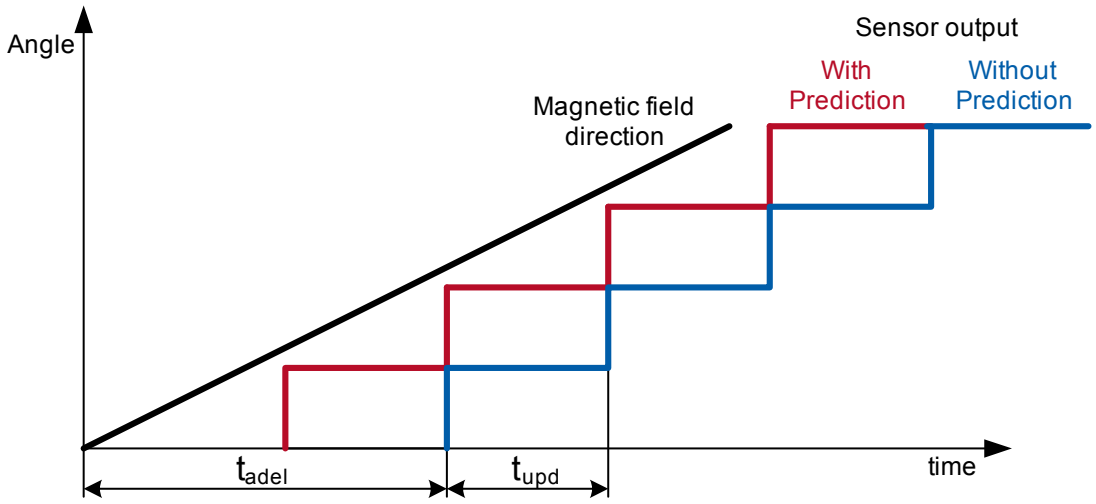

Figure 14 Delay of sensor output

3.4.6 Clock Supply (CLK Timing Definition)

If the external clock supply is selected, the clock signal input IFC must fulfill certain requirements:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike-filtered.
- The duty cycle factor should be 0.5 but can vary within the values limited by $t_{CLKh(f\_min)}$ and $t_{CLKl(f\_min)}$.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically and the sensor starts with the internal clock. This is indicated by S_RST, CLK_SEL bit, and additionally by the Safety Word.

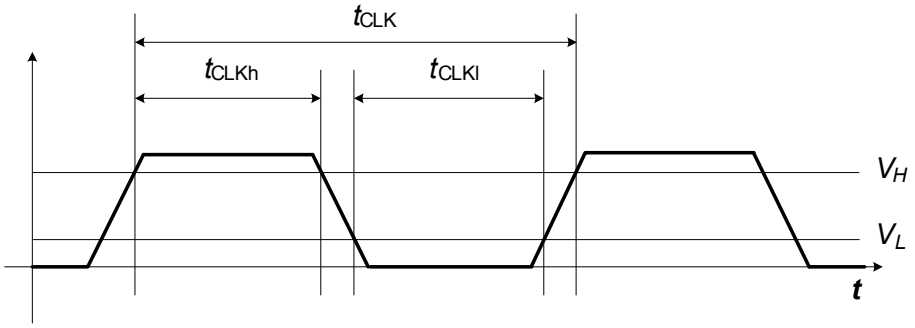

Figure 15 External CLK timing definition

Table 11 CLK timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{CLK}	3.8	4.0	4.2	MHz	
CLK duty cycle[1)2)]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}			30	ns	From V_L to V_H
CLK fall time	t_{CLKf}			30	ns	From V_H to V_L
Digital clock	f_{DIG}	22.8	24	25.2	MHz	
Internal oscillator frequency	f_{CLK}	3.8	4.0	4.2	MHz	

1)Minimum duty cycle factor: $t_{CLKh(f\_min)}$ / $t_{CLK(f\_min)}$ with $t_{CLK(f\_min)}$= 1 / $f_{CLK(f\_min)}$
2)Maximum duty cycle factor: $t_{CLKh(f\_max)}$ / $t_{CLK(f\_min)}$ with $t_{CLKh(f\_max)}$= $t_{CLK(f\_min)}$ - $t_{CLKl(min)}$

3.5 Interfaces

Within the register MOD_3, the driver strength and the slope for push-pull communication can be varied depending on the sensor output. The driver strength is specified in **Table 3** and the slope fall and rise time in **Table 12**.

Table 12 PAD characteristic

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output fall time	t_{fall}, t_{rise}			8	ns	DATA, 50 pF, PAD_DRV='00'[1)2)]
Output rise time				28	ns	DATA, 50 pF, PAD_DRV='01'[1)2)]
				45	ns	DATA, 50 pF, PAD_DRV='10'[1)2)]
				130	ns	DATA, 50 pF, PAD_DRV='11'[1)2)]
				15	ns	IFA/IFB, 20 pF, PAD_DRV='0x'[1)2)]
				30	ns	IFA/IFB, 20 pF, PAD_DRV='1x'[1)2)]

1) Valid for push-pull output

2) Not subject to production test - verified by design/characterization

3.5.1 Synchronous Serial Communication (SSC) Interface

The 3-pin SSC interface has a bi-directional push-pull data line, serial clock signal, and chip select. The SSC Interface is designed to communicate with a microcontroller peer-to-peer for fast applications.

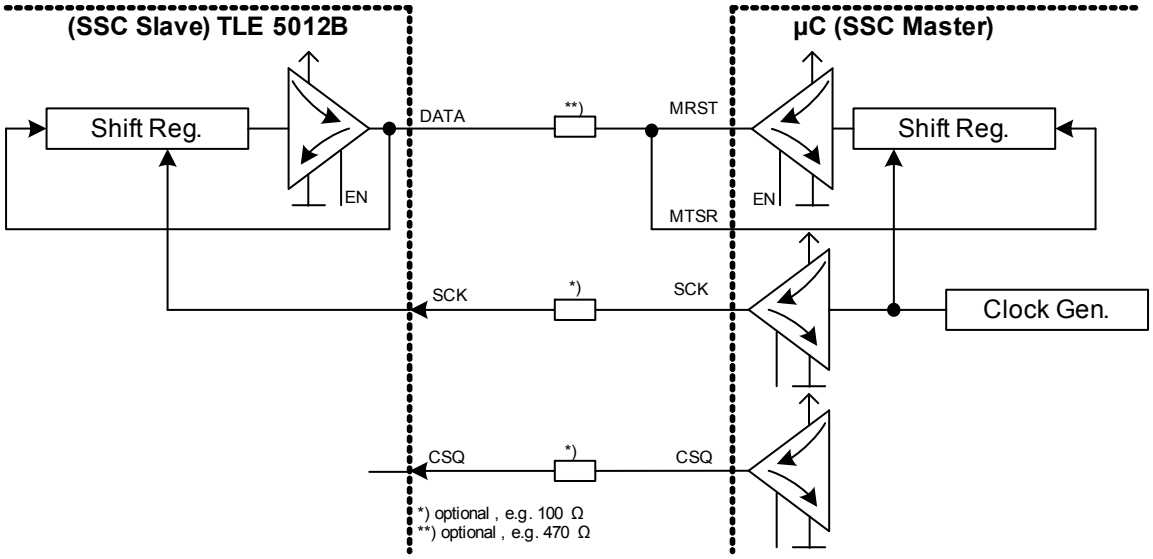

Figure 16 SSC configuration in sensor-slave mode with push-pull outputs (high-speed application)

Another possibility is a 3-pin SSC interface with bidirectional open-drain data line, serial clock signal, and chip select. This setup is designed to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLE5012B devices for redundancy reasons). This mode can be activated using bit SSC_OD.

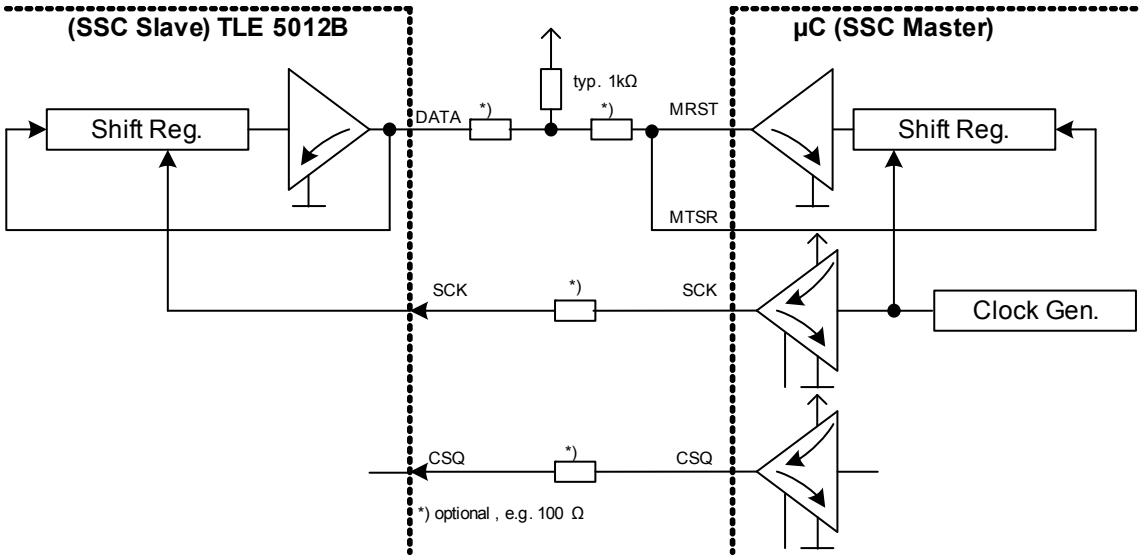

Figure 17 SSC configuration in sensor-slave mode and open drain (safe bus systems)

3.5.1.1 SSC Timing Definition

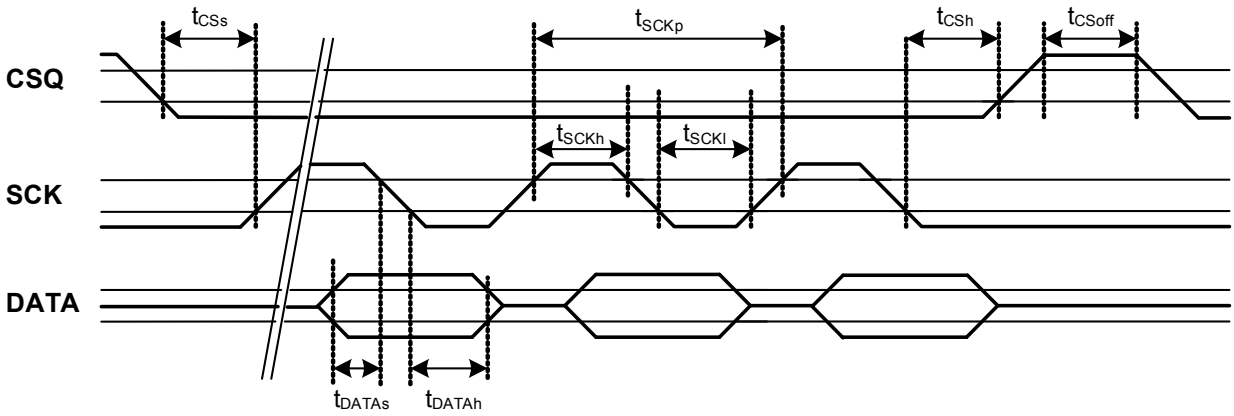

Figure 18 SSC timing

SSC Inactive Time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLE5012B can be selected again.

Table 13 SSC push-pull timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		8.0		Mbit/s	1)
CSQ setup time	t_{CSs}	105			ns	1)
CSQ hold time	t_{CSh}	105			ns	1)
CSQ off	t_{CSoff}	600			ns	SSC inactive time1)
SCK period	t_{SCKp}	120	125		ns	1)
SCK high	t_{SCKh}	40			ns	1)

Table 13 SSC push-pull timing specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCK low	t_{SCKl}	30			ns	1)
DATA setup time	t_{DATAs}	25			ns	1)
DATA hold time	t_{DATAh}	40			ns	1)
Write read delay	t_{wr_delay}	130			ns	1)
Update time	$t_{CSupdate}$	1			µs	see Figure 22 1)
SCK off	t_{SCKoff}	170			ns	1)

1) Not subject to production test - verified by design/characterization

Table 14 SSC open-drain timing specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		2.0		Mbit/s	Pull-up Resistor = 1kΩ 1)
CSQ setup time	t_{CSs}	300			ns	1)
CSQ hold time	t_{CSh}	400			ns	1)
CSQ off	t_{CSoff}	600			ns	SSC inactive time 1)
SCK period	t_{SCKp}	500			ns	1)
SCK high	t_{SCKh}		190		ns	1)
SCK low	t_{SCKl}		190		ns	1)
DATA setup time	t_{DATAs}	25			ns	1)
DATA hold time	t_{DATAh}	40			ns	1)
Write read delay	t_{wr_delay}	130			ns	1)
Update time	$t_{CSupdate}$	1			µs	see Figure 22 1)
SCK off	t_{SCKoff}	170			ns	1)

1) Not subject to production test - verified by design/characterization

3.5.1.2 SSC Data Transfer

The SSC data transfer is word-aligned. The following transfer words are possible:

- Command Word (to access and change operating modes of the TLE5012B)
- Data words (any data transferred in any direction)
- Safety Word (confirms the data transfer and provides status information)

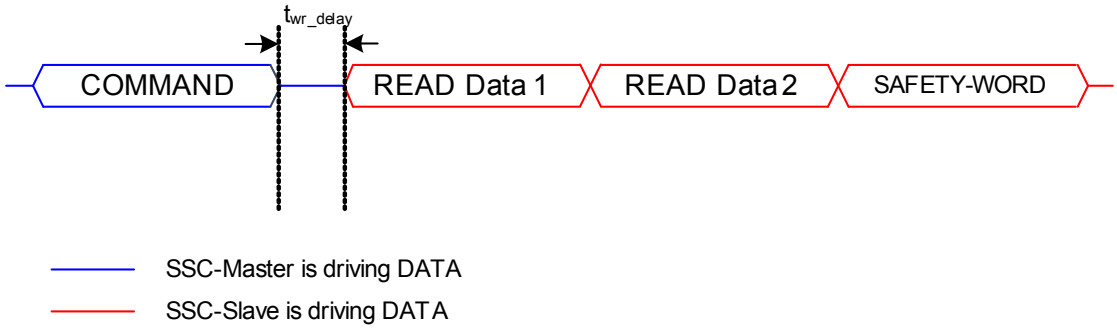

Figure 19 SSC data transfer (data-read example)

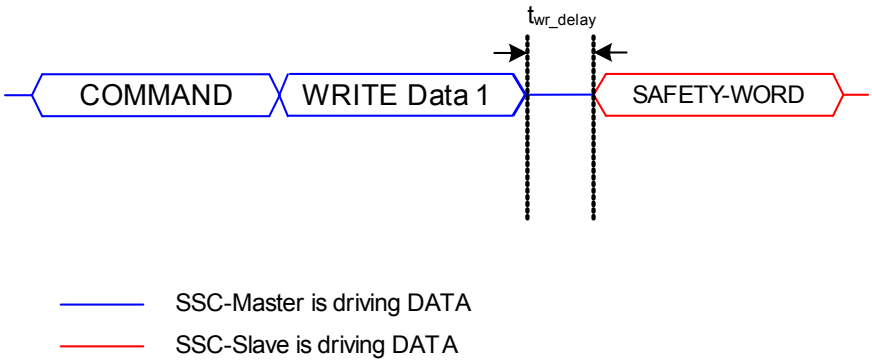

Figure 20 SSC data transfer (data-write example)

Command Word

The TLE5012B is controlled by a command word. It is sent first at every data transmission.The structure of the command word is shown in **Table 15**, where the Update (UPD) bit allows the access to current values or updated values. If an update command is issued and the UPD is set, the immediate values are stored in the update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time. Bits with an update buffer are marked by an “u” in the Type column in register descriptions. The initialization of such an update is described on page **32**.

Table 15 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0: Write 1: Read
Lock	[14..11]	4-bit Lock Value 0000_B: Default operating access for addresses 0x00:0x04 1010_B: Configuration access for addresses 0x05:0x11

Table 15 Structure of the Command Word

Name	Bits	Description
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to updated values
ADDR	[9..4]	6-bit Address
ND	[3..0]	4-bit Number of Data Words

Safety Word

The safety word consists of the following bits:

Table 16 Structure of the Safety Word

Name	Bits	Description
STAT	Chip and Interface Status	
	[15]	Indication of chip reset or watchdog overflow (resets after readout) via SSC 0: Reset occurred 1: No reset Reset: 1_B
	[14]	System error (e.g. overvoltage; undervoltage; V_{DD}-, GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_FUSE; S_ROM; S_ADCT) 1: No error
	[13]	Interface access error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid angle value (NO_GMR_A = 0; NO_GMR_XY = 0) 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor number response indicator The sensor number bit is pulled low and the other bits are high
CRC	[7..0]	Cyclic Redundancy Check (CRC)

Bit Types

The types of bits used in the registers are listed here:

Table 17 Bit Types

Abbreviation	Function	Description
r	Read	Read-only registers
w	Write	Read and write registers
u	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This enables a snapshot of all necessary system parameters at the same time.

Data communication via SSC

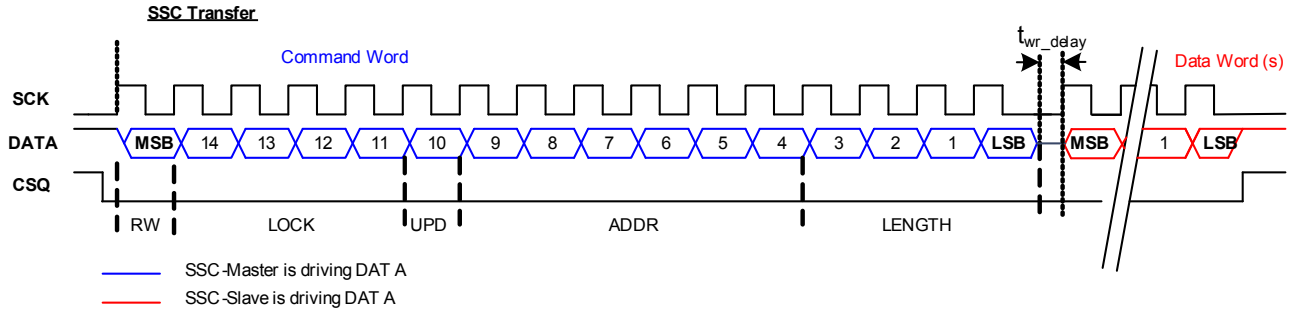

Figure 21 SSC bit ordering (read example)

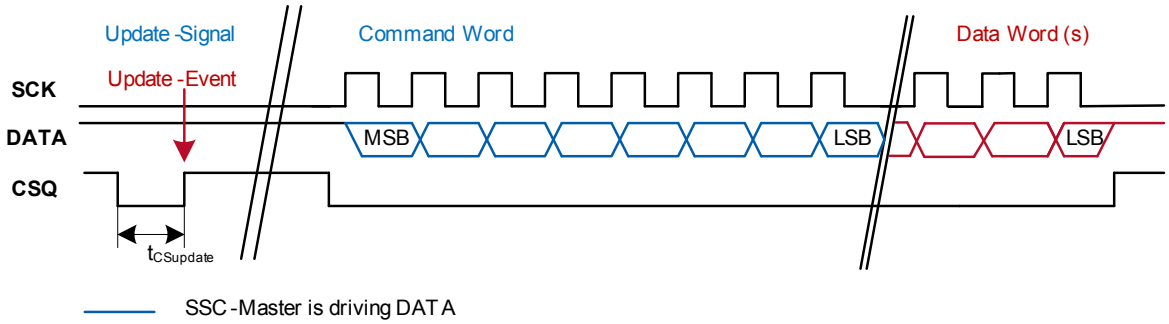

Figure 22 Update of update registers

The data communication via SSC interface has the following characteristics:

- The data transmission order is Most-Significant Bit (MSB) first.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- A “high” condition on the negated Chip Select pin (CSQ) of the selected TLE5012B interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay (t_{wr_delay}) has to be implemented before continuing the data transfer. This is necessary for internal register access.
- Every access to the TLE5012B with the number of data (ND) ≥ 1 is performed with address auto-increment.
- At an overflow at address $3F_H$, the transfer continues at address 00_H.
- With ND = 0, no auto-increment is done and a continuous readout of the same address can take place. Afterwards no Safety Word is sent, and the transfer ends with high condition on CSQ.
- After every data transfer with ND ≥ 1, the 16-bit Safety Word will be appended by the selected TLE5012B.
- At a rising edge of CSQ without a preceding data transfer (no SCK pulse), the update registers are updated with according values (**Figure 22**).
- After sending the Safety Word, the transfer ends. To start another data transfer, the CSQ has to be deselected once for t_{CSoff}.
- The SSC is default push-pull. The push-pull driver is active only if the TLE5012B has to send data, otherwise the push-pull is disabled and cannot receive data from the microcontroller.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus Specification.
- Every new transfer restarts the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).

- Generator polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast-CRC generation circuit is used (see **Figure 23**)
- The remainder of the fast CRC circuit is initial set to '11111111_B'.
- The remainder is inverted before transmission.

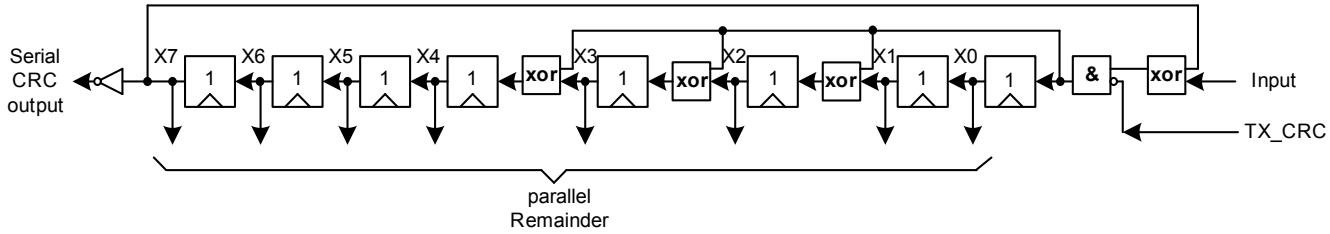

Figure 23 Fast CRC polynomial division circuit

3.5.1.3 Registers Chapter

The registers of the TLE5012B are described in the application note "TLE5012B Register Setting".

3.5.2 Pulse Width Modulation Interface

The Pulse Width Modulation (PWM) interface can be selected via SPI (IF_MD = '001').

The PWM update rate can be programmed within the register $0E_H$ (IFAB_RES) in the following steps:

- ~0.25 kHz with 12-bit resolution
- ~0.5 kHz with 12-bit resolution
- ~1.0 kHz with 12-bit resolution
- ~2.0 kHz with 12-bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated, resulting in an average value of the waveform.

Figure 24 shows the principal behavior of a PWM with various duty cycles and the definition of timing values. The duty cycle of a PWM is defined by the following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}} \quad (4)$$

The range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. More details are given in **Table 18**.

Sensors with preset PWM are available as TLE5012B E5xxx. The register settings for these sensors can be found in the latest **Application Note TLE5012B Register Setting; section 4**.

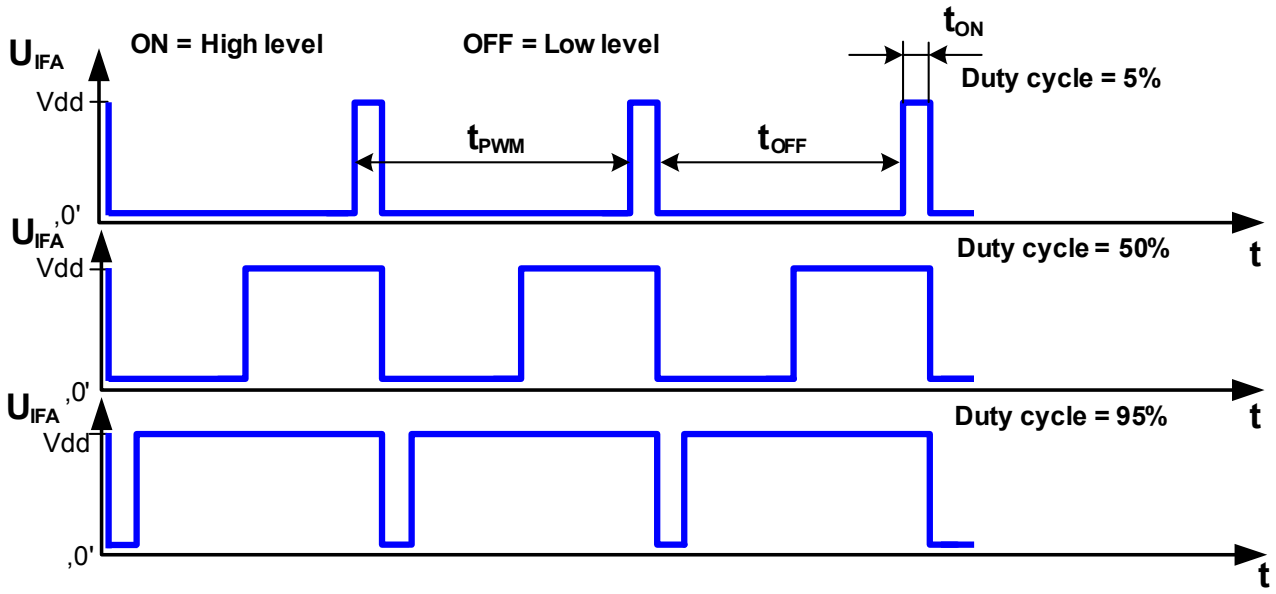

Figure 24 Typical example of a PWM signal

Table 18 PWM interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM output frequency	f_{PWM}	244		1953	Hz	Selectable by IFAB_RES[1)2)]
Output duty cycle range	DY_{PWM}	6.25		93.75	%	Absolute angle[2)]
			2		%	Electrical Error (S_RST; S_VR)[2)]
			98		%	System error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)[2)]
		0		1	%	Short to GND[2)]
		99		100	%	Short to V_{DD}, power loss[2)]
PWM period variation	t_{PWMvar}	-5		5	%	[2)3)]

1) $f_{PWM} = (f_{DIG} * 2^{IFAB\_RES}) / (24 * 4096)$

2) Not subject to production test - verified by design/characterization

3) Depends on internal oscillator frequency variation (**Section 3.4.6**)

3.5.3 Short PWM Code

The Short PWM Code (SPC) is a synchronized data transmission based on the SENT protocol (Single Edge Nibble Transmission) defined by SAE J2716. SPC enables the use of enhanced protocol functionality due to the ability to select between various sensor slaves (ID selection). The slave number (S_NR) can be given by the external circuit of SCK and IFC pin. In case of V_{DD} on SCK, the S_NR[0] can be set to 1 and in the case of GND on SCK the S_NR[0] is equal to 0. S_NR[1] can be adjusted in the same way by the IFC pin.

As in SENT, the time between two consecutive falling edges defines the value of a 4-bit nibble, thus representing numbers between 0 and 15. The transmission time therefore depends on the transmitted data values. The single edge is defined by a 3 Unit Time (UT) low pulse on the output, followed by the high time defined in the protocol (nominal values, may vary depending on the tolerance of the internal oscillator and the influence of external circuitry). All values are multiples of a unit time frame concept. A transfer consists of the following parts (**Figure 25**):

- A trigger pulse by the master, which initiates the data transmission
- A synchronization period of 56 UT (in parallel, a new sample is calculated)
- A status nibble of 12-27 UT
- Between 3 and 6 data nibbles of 12-27 UT
- A CRC nibble of 12-27 UT
- An end pulse to terminate the SPC transmission

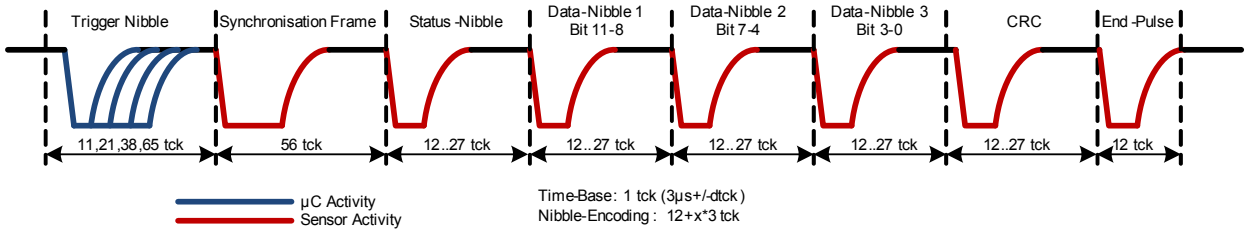

Figure 25 SPC frame example

The CRC checksum includes the status nibble and the data nibbles, and can be used to check the validity of the decoded data. The sensor is available for next sample 90µs after the falling edge of the end pulse.

In parallel to the SPC, the SPI can be used for individual configuration. The number of transmitted SPC nibbles can be changed to customize the amount of information sent by the sensor. The frame contains a 16-bit angle value and an 8-bit temperature value in the full configuration (**Table 19**).

Sensors with preset SPC are available as TLE5012B E9xxx. The register settings for these sensors can be found in the latest **Application Note TLE5012B Register Setting; section 4**.

Table 19 Frame configuration

Frame type	IFAB_RES	Data nibbles
12-bit angle	00	3 nibbles
16-bit angle	01	4 nibbles
12-bit angle, 8-bit temperature	10	5 nibbles
16-bit angle, 8-bit temperature	11	6 nibbles

The status nibble makes it possible to check internal states and conditions of the sensor.

Table 20 Structure of status nibble

Name	Bits	Description
SYS_ERR	[3]	Indication of system error (S_FUSE, S_OV, S_XYOL, S_MAGOL, S_ADCT) 0: No system error 1: System error occurred
ELEC_ERR	[2]	Indication of electrical error (S_RST, S_VR) 0: No electrical error 1: Electrical error occurred
S_NR	[1]	Slave number bit 1 (level on IFC)
	[0]	Slave number bit 0 (level on SCK)

3.5.3.1 Unit Time Setup

The basic SPC protocol unit time granularity is defined as 3 µs. Every timing is a multiple of this basic time unit.To achieve more flexibility, trimming of the unit time can be done within IFAB_HYST. This enables a setup of different unit times.

Table 21 Predivider setting

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Unit time	t_{Unit}		3.0		µs	IFAB_HYST = 00[1)]
			2.5			IFAB_HYST = 01[1)]
			2.0			IFAB_HYST = 10[1)]
			1.5			IFAB_HYST = 11[1)]

1) Not subject to production test - verified by design/characterization

3.5.3.2 Master Pulse Requirements

An SPC transmission is initiated by a master pulse on the IFA pin. To detect a low level on the IFA pin, the voltage must be below a threshold V_{thf}. The sensor detects that the IFA line has been released as soon as V_{thr} is crossed. **Figure 26** shows the timing definitions for the master pulse. The master low time t_{mlow} as well as the total trigger time t_{mtr} are given in **Table 22**.

If the master low time exceeds the maximum low time, the sensor does not respond and is available for a next triggering 30 µs after the master pulse crosses V_{thr}. $t_{md,tot}$ is the delay between internal triggering of the falling edge in the sensor and the triggering of the ECU.

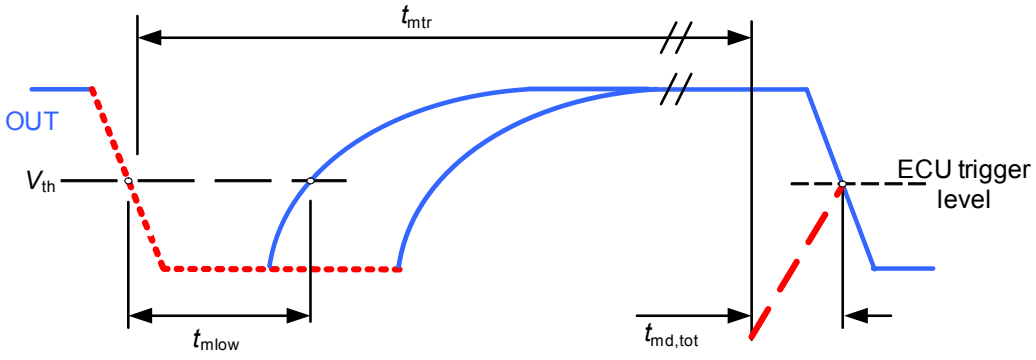

Figure 26 SPC Master pulse timing

Table 22 Master pulse parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Threshold	V_{th}		50		% of V_{DD}	1)
Threshold hysteresis	V_{thhyst}		8		% of V_{DD}	V_{DD} = 5V 1)
			3			V_{DD} = 3V 1)
Total trigger time	t_{mtr}		90		UT	SPC_Trigger = 0; 1)2)
			t_{mlow} +12		UT	SP_Trigger = 1 1)
Master low time	t_{mlow}	8	12	14	UT	S_NR =00 1)
		16	22	27		S_NR =01 1)
		29	39	48		S_NR =10 1)
		50	66	81		S_NR =11 1)
Master delay time	$t_{md,tot}$		5.8		µs	1)

1) Not subject to production test - verified by design/characterization

2) Trigger time in the sensor is fixed to the number of units specified in the “typ.” column, but the effective trigger time varies due to the sensor’s clock variation

3.5.3.3 Checksum nibble details

The checksum nibble is a 4-bit CRC of the data nibbles including the status nibble. The CRC is calculated using a polynomial $x^4+x^3+x^2+1$ with a seed value of 0101. The remainder after the last data nibble is used are transferred as CRC.

3.5.4 Hall Switch Mode

The **H**all **S**witch **M**ode (**HSM**) within the TLE5012B makes it possible to emulate the output of 3 Hall switches. Hall switches are often used in electrical commutated motors to determine the rotor position. With these 3 output signals, the motor will be commutated in the right way. Depending on which pole pairs of the rotor are used, various electrical periods have to be controlled. This is selectable within $0E_H$ (HSM_PLP). **Figure 27** depicts the three output signals with the relationship between electrical angle and mechanical angle. The mechanical 0° point is always used as reference.

The HSM is generally used with push-pull output, but it can be changed to open-drain within IFAB_OD.

Sensors with preset HSM are available as TLE5012B E3xxx. The register settings for these sensors can be found in the latest **Application Note TLE5012B Register Setting; section 4**.

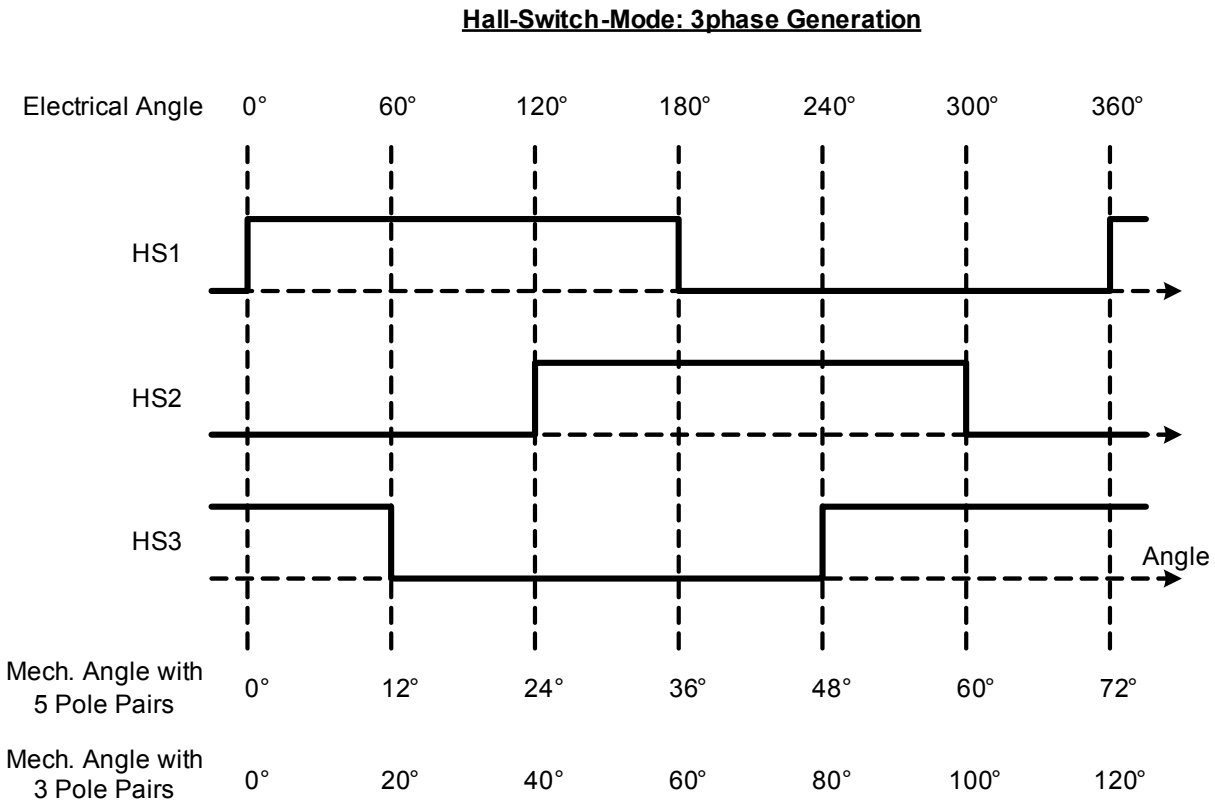

Figure 27 Hall Switch Mode

The HSM Interface can be selected via SPI (IF_MD = 010).

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rotation speed	n			10000	rpm	Mechanical[2)]

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical angle accuracy	α_{elect}		0.6	1	°	1 pole pair with autocalibration[1)2)]
			1.2	2		2 pole pairs with autocal.[1)2)]
			1.8	3		3 pole pairs with autocal.[1)2)]
			2.4	4		4 pole pairs with autocal.[1)2)]
			3.0	5		5 pole pairs with autocal.[1)2)]
			3.6	6		6 pole pairs with autocal.[1)2)]
			4.2	7		7 pole pairs with autocal.[1)2)]
			4.8	8		8 pole pairs with autocal.[1)2)]
			5.4	9		9 pole pairs with autocal.[1)2)]
			6.0	10		10 pole pairs with autocal.[1)2)]
			6.6	11		11 pole pairs with autocal.[1)2)]
			7.2	12		12 pole pairs with autocal.[1)2)]
			7.8	13		13 pole pairs with autocal.[1)2)]
			8.4	14		14 pole pairs with autocal.[1)2)]
			9.0	15		15 pole pairs with autocal.[1)2)]
			9.6	16		16 pole pairs with autocal.[1)2)]
Mechanical angle switching hysteresis	$\alpha_{HShystm}$	0		0.703	°	Selectable by IFAB_HYST[2)3)4)]

Table 23 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Electrical angle switching hysteresis[5]	$\alpha_{HShystel}$		0.70		°	1 pole pair; IFAB_HYST=11[1)2)]
			1.41			2 pole pairs; IFAB_HYST=11[1)2)]
			2.11			3 pole pairs; IFAB_HYST=11[1)2)]
			2.81			4 pole pairs; IFAB_HYST=11[1)2)]
			3.52			5 pole pairs; IFAB_HYST=11[1)2)]
			4.22			6 pole pairs; IFAB_HYST=11[1)2)]
			4.92			7 pole pairs; IFAB_HYST=11[1)2)]
			5.62			8 pole pairs; IFAB_HYST=11[1)2)]
			6.33			9 pole pairs; IFAB_HYST=11[1)2)]
			7.03			10 pole pairs; IFAB_HYST=11[1)2)]
			7.73			11 pole pairs; IFAB_HYST=11[1)2)]
			8.44			12 pole pairs; IFAB_HYST=11[1)2)]
			9.14			13 pole pairs; IFAB_HYST=11[1)2)]
			9.84			14 pole pairs; IFAB_HYST=11[1)2)]
			10.55			15 pole pairs; IFAB_HYST=11[1)2)]
			11.25			16 pole pairs; IFAB_HYST=11[1)2)]
Fall time	t_{HSfall}		0.02	1	µs	R_L = 2.2kΩ; C_L < 50pF[2)]
Rise time	t_{HSrise}		0.4	1	µs	R_L = 2.2kΩ; C_L < 50pF[2)]

1) Depends on internal oscillator frequency variation (**Section 3.4.6**)
2) Not subject to production test - verified by design/characterization
3) GMR hysteresis not considered
4) Minimum hysteresis without switching
5) The hysteresis has to be considered only at change of rotation direction

To avoid switching due to mechanical vibrations of the rotor, an artificial hysteresis is recommended (**Figure 28**).

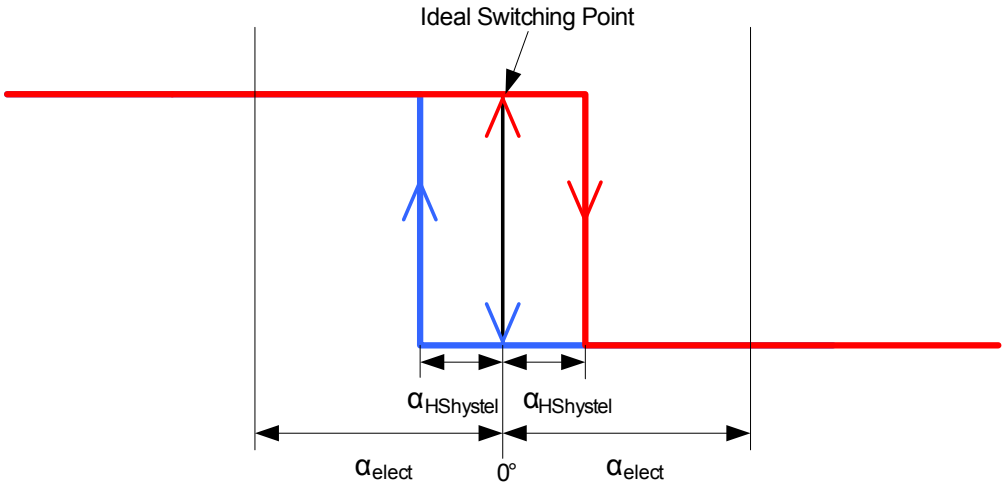

Figure 28 HS hysteresis

3.5.5 Incremental Interface

The **I**ncremental **I**nterface (**IIF**) uses an up/down counter of a microcontroller for the angle transmission. The synchronization is done by the parallel active SSC interface. The angle value read out by the SSC interface can be compared to the stored counter value. In case of a non-synchronization, the microcontroller adds the difference to the actual counter value to synchronize the TLE5012B with the microcontroller. The resolution of the IIF can be selected within the interface mode4 register (MOD_4) under IFAB_RES.

After startup, the IIF pulses out the actual absolute angle value. Thus, the microcontroller gets the information about the absolute position. The Index Signal that indicates the zero crossing is available on the IFC pin.

In register MOD_1, the incremental interface can be chosen between A/B mode and Step/Direction mode (IIF_MOD).

Within the TLE5012B, the incremental interface is implemented like a quadrature encoder with a 50% duty cycle.

Sensors with preset IIF are available as TLE5012B E1xxx. The register settings for these sensors can be found in the latest **Application Note TLE5012B Register Setting; section 4**.

A/B Mode

The phase shift between phases A and B indicates either a clockwise (A follows B) or a counterclockwise (B follows A) rotation of the magnet.

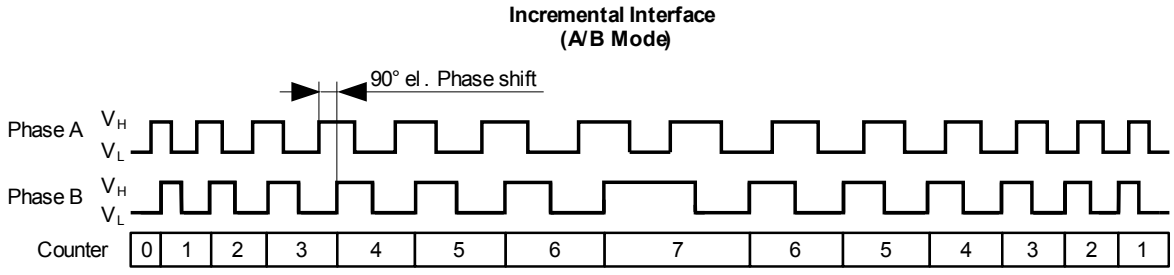

Figure 29 Incremental interface with A/B mode

Step/Direction Mode

Phase A pulses out the increments and phase B indicates the direction (**Figure 30**).

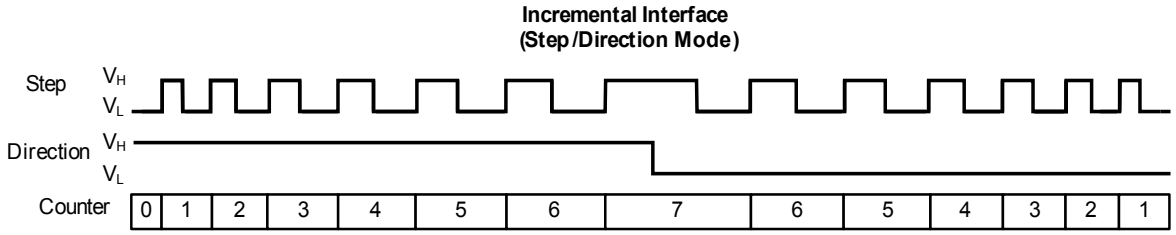

Figure 30 Incremental interface with Step/Direction mode

Table 24 Incremental Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Incremental output frequency	f_{Inc}			1.0	MHz	Frequency of phase A and phase B[1)]
Index	$t_{0°}$		5		µs	0°[1)]

1) Not subject to production test - verified by design/characterization

3.6 Test Structure

3.6.1 ADC Test Vectors

It is possible to feed the ADCs with appropriate values to simulate a certain magnet position and other GMR effects. This test can be activated within the SIL register (ADCTV_EN). With ADCTV_Y and ADCTV_X, the vector length can be adjusted as shown in **Figure 31**.

The values are generated with resistors on the chip.

The following X/Y ADC values can be programmed:

- 4 points, circle amplitude = 70% (0°,90°, 180°, 270°)
- 8 points, circle amplitude = 100% (0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1% (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4% (45°, 135°, 225°, 315°)

Note: The 100% values typically correspond to 21700 digits and the 70% values to 15500 digits.

Table 25 ADC test vectors

Register bits	X/Y values (decimal)		
	Min.	Typ.	Max.
000		0	
001		15500	
010		21700	
011		32767	
100[1)]		0	
101		-15500	
110		-21700	
111		-32768	

1) Not allowed to use

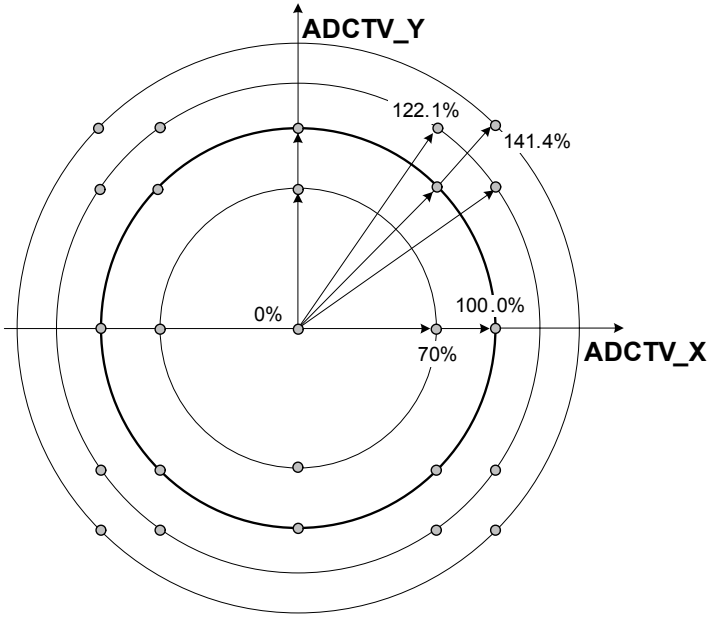

Figure 31 ADC test vectors

Examples of ADC test vector check

The sensor has to be selected first via CSQ and SCK must be available for the communication. Table 26 shows the structure of the communication to enable the ADC test vector for 54.7°.

Table 26 SSC Command to enable ADC test vector check

SSC Word No.	Description	Master transmitting	TLE5012B transmitting	Note
1	Command	0_1010_0_000111_0001		
2	Write Data	0_0_000_0_000_1_010_001		Check of 54.7°
3	Safety Word		1_1_1_0_xxxx_xxxxxxxx	

Table 27 Structure of Write Data for various test vectors

SSC Word No.	Description	Master transmitting	TLE5012B transmitting	Note
1	Write Data	0_0_000_0_000_1_001_101		~135°
2	Write Data	0_0_000_0_000_1_010_110		~135°
3	Write Data	0_0_000_0_000_1_101_110		~215.3°
4	Write Data	0_0_000_0_000_1_101_000		~270°
5	Write Data	0_0_000_0_000_1_101_010		~324.7°

3.7 Overvoltage Comparators

Various comparators monitor the voltage in order to ensure error-free operation. The overvoltages must be active at least 256 periods of t_{DIG} to set the test comparator bits in the SSC interface registers. This works as digital spike suppression.

Table 28 Test comparators

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overvoltage detection	V_{OVG}		2.80		V	1)
	V_{OVA}		2.80		V	1)
	V_{OVD}		2.80		V	1)
V_{DD} overvoltage	V_{DDOV}		6.05		V	1)
V_{DD} undervoltage	V_{DDUV}		2.70		V	1)
GND - off voltage	V_{GNDoff}		-0.55		V	1)
V_{DD} - off voltage	V_{VDDoff}		0.55		V	1)
Spike filter delay	t_{DEL}		10		µs	1)

1) Not subject to production test - verified by design/characterization

3.7.1 Internal Supply Voltage Comparators

Every voltage regulator has an overvoltage (OV) comparator to detect malfunctions. If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated.

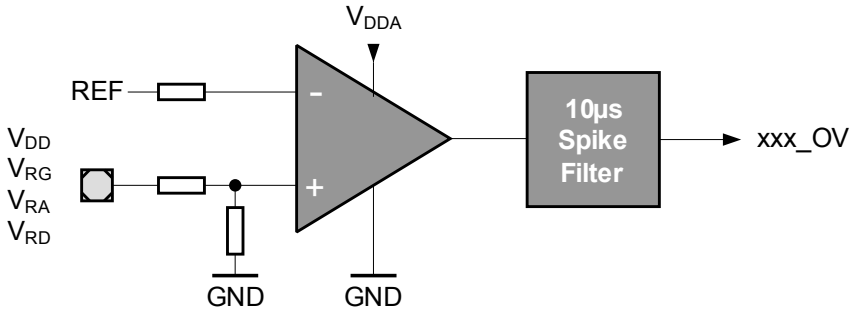

Figure 32 OV comparator

3.7.2 V_{DD} Overvoltage Detection

The overvoltage detection comparator monitors the external supply voltage at the V_{DD} pin. It activates the S_VR bit.(**Figure 32**)

3.7.3 GND - Off Comparator

The GND - Off comparator is used to detect a voltage difference between the GND pin and SCK. It activates the S_VR bit of the SSC - Interface. This circuit can detect a disconnection of the supply GND Pin.

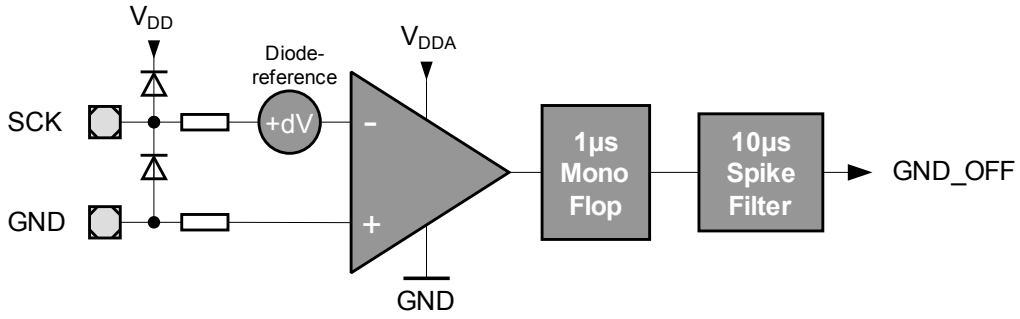

Figure 33 GND - off comparator

3.7.4 V_{DD} - Off Comparator

The V_{DD} - Off comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLE5012B is supplied by the SCK and CSQ input pins via the ESD structures. It activates the S_VR bit.

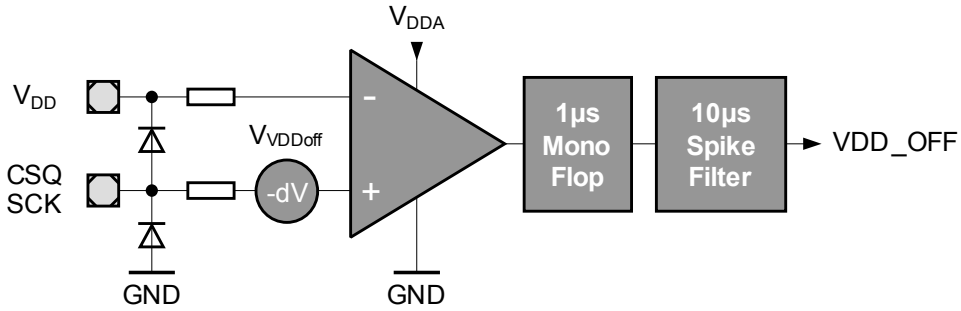

Figure 34 V_{DD} - off comparator

4 Package Information

4.1 Package Parameters

Table 29 Package Parameters

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Thermal resistance	R_{thJA}		150	200	K/W	Junction to air[1)]
	R_{thJC}			75	K/W	Junction to case
	R_{thJL}			85	K/W	Junction to lead
Soldering moisture level	MSL 3					260°C
Lead Frame	Cu					
Plating	Sn 100%					> 7 µm

1) according to Jedec JESD51-7

4.2 Package Outline

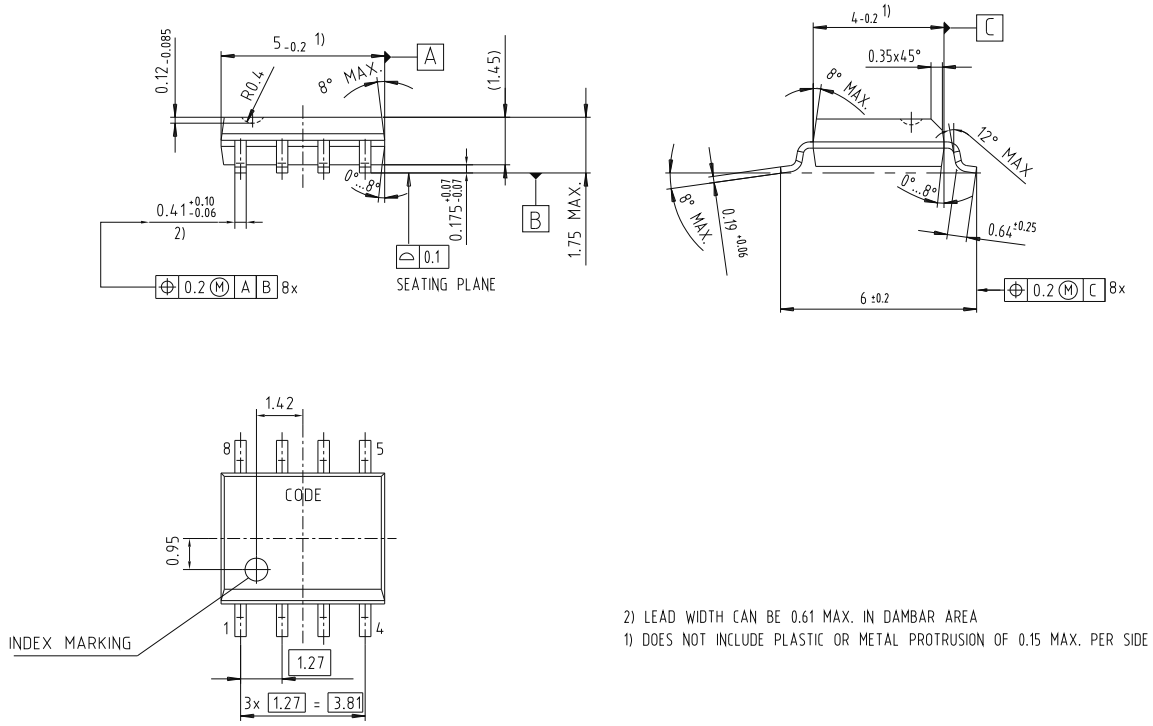

Figure 35 PG-DSO-8 package dimension

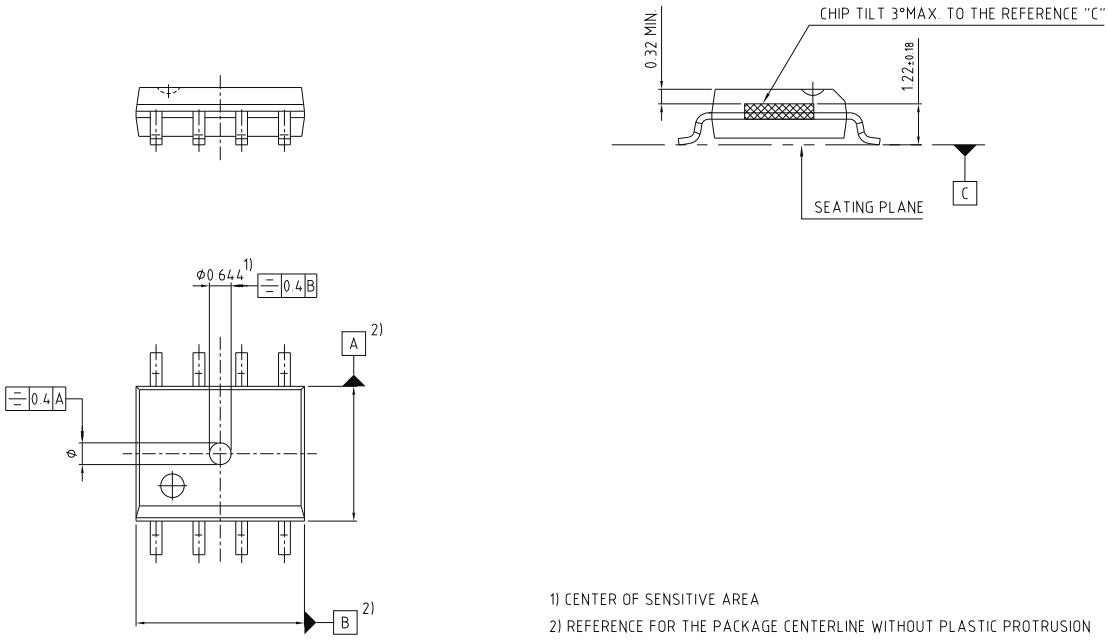

Figure 36 Position of sensing element

4.3 Footprint

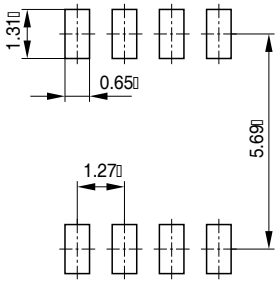

Figure 37 Footprint of PG-DSO-8

4.4 Packing

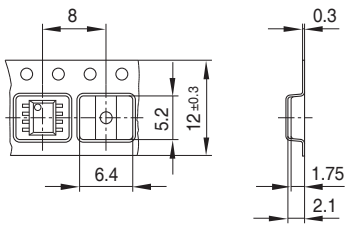

Figure 38 Tape and Reel

4.5 Marking

Position	Marking	Description
1st Line	012Bxxxx	See ordering table on **Page 8**
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon's Notes on processing

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