Features

- Fully Integrated Low IF Receiver
- Fully Integrated GFSK Modulator for 72, 144, 288, 576 and 1152 Kbits/s
- High Sensitivity of Typically –93 dBm Due to Integrated LNA
- High Output Power of Typically +4 dBm
- Multi-channel Operation
  - 95 Channels
  - Support Frequency Hopping (ETSI) and Digital Modulation (FCC)
- Supply-voltage Range 2.9V to 3.6V (Unregulated)
- Auxiliary Voltage Regulator on Chip (3.2V to 4.6V)
- Low Current Consumption
- Few Low-cost External Components
- Integrated Ramp-signal Generator and Power Control for an Additional Power Amplifier
- Low Profile Lead-free Plastic Package QFN32 (5 mm × 5 mm × 0.9 mm)
- RoHs Compliant

Applications

- High-tech Multi-user Toys
- Wireless Game Controllers
- Telemetry
- Wireless Audio/Video
- Electronic Point of Sales
- Wireless Head Set
- FCC CFR47, Part 15, ETSI EN 300 328, EN 300 440 and ARIB STD-T-66 Compliant Radio Links

1. Description

The ATR2406 is a single chip RF transceiver intended for applications in the 2.4-GHz ISM band. The QFN32-packaged IC is a complete transceiver including image rejection mixer, low IF filter, FM demodulator, RSSI, TX preamplifier, power-ramping generator for external power amplifier, integrated synthesizer, and a fully integrated VCO and TX filter. No mechanical adjustment is necessary in production.

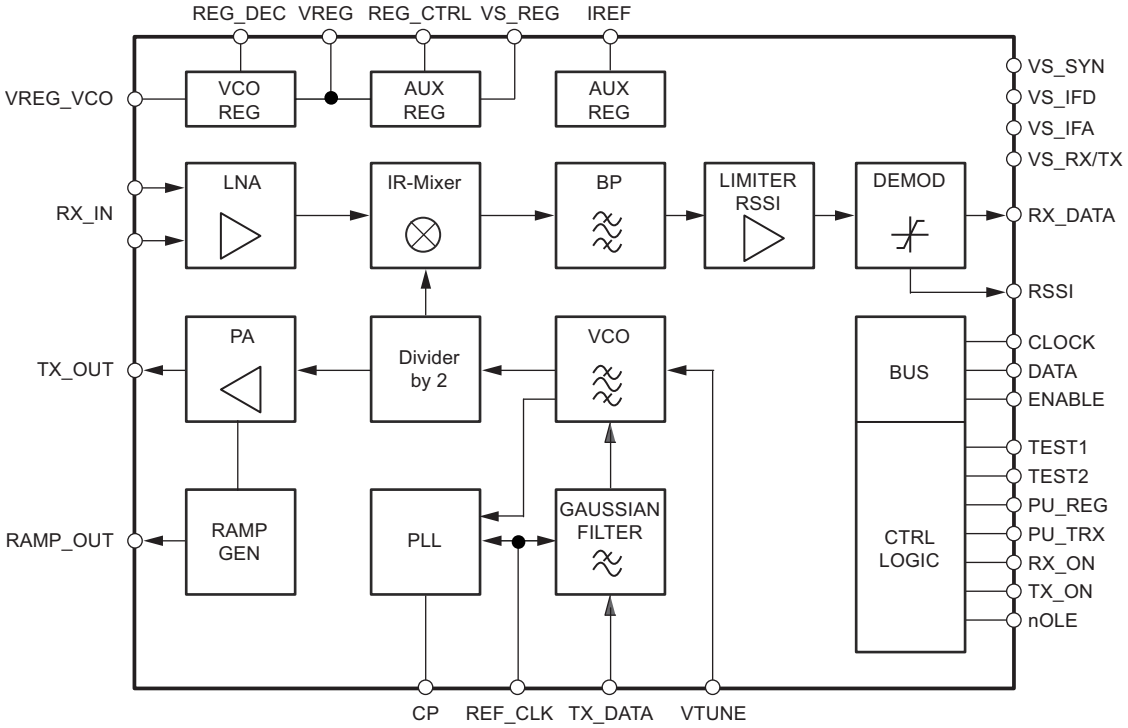
The RF transceiver offers a clock recovery function on-chip.

Low-IF 2.4-GHz ISM Transceiver

ATR2406

4779N–ISM–12/08

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN32 - 5 × 5

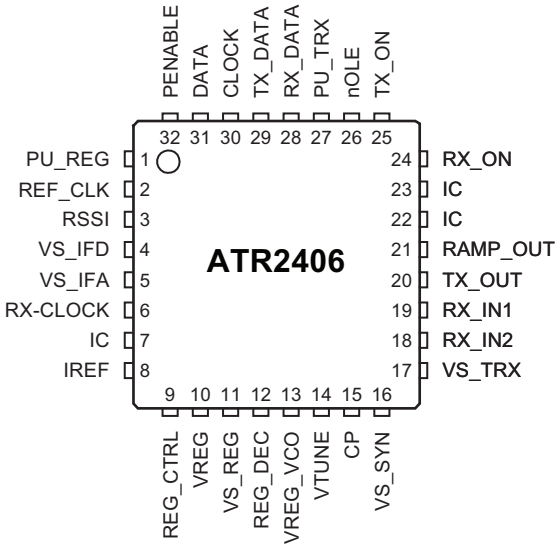


Table 2-1. Pin Description

Pin	Symbol	Function
1	PU_REG	Power-up input for auxiliary regulator
2	REF_CLK	Reference frequency input
3	RSSI	Received signal strength indicator output
4	VS_IFD	Digital supply voltage
5	VS_IFA	Analog supply voltage for IF circuits
6	RX-CLOCK	RX-CLOCK, if RX mode with clock recovery is active
7	IC	Internally connected. Connect to V_S if internal AUX regulator is not used
8	IREF	External resistor for band-gap reference
9	REG_CTRL	Auxiliary voltage regulator control output
10	VREG	Auxiliary voltage regulator output
11	VS_REG	Auxiliary voltage regulator supply voltage
12	REG_DEC	Decoupling pin for VCO_REG
13	VREG_VCO	VCO voltage regulator
14	VTUNE	VCO tuning voltage input
15	CP	Charge-pump output
16	VS_SYN	Synchronous supply voltage
17	VS_TRX	Transmitter receiver supply voltage
18	RX_IN2	Differential receiver input 2
19	RX_IN1	Differential receiver input 1
20	TX_OUT	TX driver amplifier output
21	RAMP_OUT	Ramp generator output for PA power ramping
22	IC	Internally connected, do not connect on PCB
23	IC	Internally connected, do not connect on PCB
24	RX_ON	RX control input
25	TX_ON	TX control input
26	nOLE	Open loop enable input
27	PU_TRX	RX/TX/PLL/VCO power-up input
28	RX_DATA	RX data output
29	TX_DATA	TX data input
30	CLOCK	3-wire-bus: Clock input
31	DATA	3-wire-bus: Data input
32	ENABLE	3-wire-bus: Enable input
Paddle	GND	Ground

3. Functional Description

3.1 Receiver

The RF signal at RF_IN is differentially fed through the LNA to the image rejection mixer IR_MIXER, driving the integrated low-IF band-pass filter. The IF frequency is 864 kHz. The limiting IF_AMP with an integrated RSSI function feeds the signal to the digital demodulator DEMOD. No tuning is required. Data slicing is handled internally.

3.2 Clock Recovery

For a 1152-kBit/s data rate, the receiver has a clock recovery function on-chip.

The receiver includes a clock recovery circuit which regenerates the clock out of the received data. The advantage is that this recovered clock is synchronous to the clock of the transmitting device (and thus to the transmitted data), which significantly reduces the load of the processing microcontroller.

The falling edge of the clock is the optimal sampling position for the RX_Data signal, so at this event the data must be sampled by the microcontroller. The recovered clock is available at pin 6.

3.3 Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian filter (GF) and fed to the fully integrated VCO operating at twice the output frequency. After modulation, the signal is frequency divided by 2 and fed to the internal preamplifier PA. This preamplifier supplies typically +4 dBm output power at TX_OUT.

A ramp-signal generator RAMP_GEN, providing a ramp signal at RAMP_OUT for the external power amplifier, is integrated. The slope of the ramp signal is controlled internally so that spurious requirements are fulfilled.

3.4 Synthesizer

The IR_MIXER, the PA, and the programmable counter (PC) are driven by the fully integrated VCO, using on-chip inductors and varactors. The output signal is frequency divided to supply the desired frequency to the TX_DRIVER, the 0/90 degree phase shifter for the IR_MIXER, and to be used by the PC for the phase detector (PD) (f_{PD} = 1.728 MHz). Open loop modulation is supported.

3.5 Power Supply

An integrated band-gap–stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage auxiliary regulator	V_S	–0.3	+4.7	V
Supply voltage	V_S	–0.3	+3.6	V
Control voltages	V_{contr}	–0.3	V_S	V
Storage temperature	T_{stg}	–40	+125	°C
Input RF level	P_{RF}		+10	dBm
ESD protection	V_{ESD_ana}		TBD	V
	V_{ESD_dig}		TBD	V

Electrostatic sensitive device.
Observe precautions for handling.

5. Operating Range

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S	2.9	3.6	V
Auxiliary regulator supply voltage	V_{S_BATT}	3.2	4.6	V
Temperature ambient	T_{amb}	–10	+60	°C
Input frequency range	f_{RX}	2400	2483	MHz

6. Electrical Characteristics

V_S = 3.6V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
1	**Supply**						
1.1	Supply voltage	With AUX regulator	V_S	3.2	3.6	4.6	V
1.2	Supply voltage	Without AUX regulator	V_S	2.9	3.0	3.6	V
1.3	RX supply current	CW mode (peak current)	I_S		57		mA
		Burst mode at 10 Kbits/s(4)	I_S		625		µA
1.4	TX supply current	CW mode (peak current)	I_S		42		mA
		Burst mode at 10 Kbits/s(4)	I_S		500		µA
1.5	Battery lifetime of a remote control application using an AVR®	See Section 10. "Appendix: Current Calculations for a Remote Control" on page 20					
1.6	Supply current in power-down mode	With AUX regulator PU_TRX = 0; PU_REG = 0	I_S		< 1		µA
1.7	Supply current in power-down mode	Without AUX regulator PU_TRX = 0; PU_REG = 0	I_S		< 1		µA
2	**Voltage Regulator**						
2.1	AUX regulator		VREG		3.0		V
2.2	VCO regulator		VREG_VCO		2.7		V
3	**Transmitter Part**						
3.1	TX data rate			72/144/288/576/1152			kBits/s
3.2	Output power		PTX		4		dBm
3.3	TX data filter clock	9 taps in filter	f_{TXFCLK}	10.368/13.824			MHz
3.4	Frequency deviation	To be tuned by GFCS bits	GF_{FM_nom}		±400		kHz
3.5	Frequency deviation scaling(3)	GFFM = GF_{FM_nom} × GFCS (Refer to bus protocol D9 to D11)	GFCS	60		130	%
3.6	Frequency drift	With standard loop filter and slot length of 1400 µs (Refer to the application note "ATR2406 Loop Filter and Data Rates")	Δfo (drift)			±40	kHz
3.7	Harmonics	BW = 100 kHz(1)				–41.2	dBm
3.8	Spurious emissions 30 – 1000 MHz 1 – 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.3 GHz	BW = 100 kHz(1)				 –57 –57 –57 –57	 dBm dBm dBm dBm
4	**Ramp Generator, Pin 21**						
4.1	Minimum output voltage	TX_ON = low	V_{min}		0.7		V
4.2	Maximum output voltage	Refer to bus protocol D12 to D13	V_{max}	1.1		1.9	V
4.3	Rise time		t_r		5		µs
4.4	Fall time		t_f		5		µs

Notes:
1. Measured and guaranteed only on the Atmel® evaluation board, including microstrip filter, balun, and Smart Radio Frequency (Smart RF) firmware. Conducted measured.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of the loop filter. For further information refer to the application notes.
3. The Gaussian filter control setting (GFCS) is used to compensate production tolerances by tuning the modulation deviation in production to the nominal value of 400 kHz.
4. Burst mode with 0.9% duty cycle

6. Electrical Characteristics (Continued)

V_S = 3.6V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
5	**Receiver Part**						
5.1	RX input impedance	Differential	Z_{in}		170 + j0		Ω
5.2	Sensitivity	At input for BER ≤ 10^{-3} at 1152 kBits/s(1)			–93		dBm
5.3	Third order input intercept point		IIP3		–15		dBm
5.4	Intermodulation rejection	BER < 10^{-3}, wanted at -83 dBm, level of interferers in channels N + 2 and N + 4(1)	IM_3	32			dBc
5.5	Co-channel rejection	BER < 10^{-3}, wanted at –76 dBm(1)	R_{CO}	–11			dBc
5.6	Adjacent channel rejection ±1.728 MHz	BER < 10^{-3}, wanted at –76 dBm, adjacent level referred to wanted channel level(1)	$R_{i\,(N-1)}$	14			dBc
5.7	Bi-adjacent channel rejection ±3.456 MHz	BER < 10^{-3}, wanted at –76 dBm, bi-adjacent level referred to wanted channel level(1)	$R_{i\,(N-2)}$	30			dBc
5.8	Rejection with ≥ 3 channels separation ≥ ±5.128 MHz	BER < 10^{-3}, wanted at –76 dBm, n ≥ 3 adjacent level referred to wanted channel level(1)	$R_{i\,(n\geq 3)}$	40			dBc
5.9	Out of band rejection > 6 MHz	BER < 10^{-3}, wanted at –83 dBm at 2.45 GHz(1)	$BI_{df>6MHz}$	38			dBc
5.10	Out of band rejection 2300 MHz to 2394 MHz 2506 MHz to 2600 GHz	BER < 10^{-3}, wanted at –83 dBm at 2.45 GHz(1)	BI_{near}	47			dBc
5.11	Out of band rejection 30 MHz to 2300 MHz 2600 MHz to 6 GHz	BER < 10^{-3}, wanted at –83 dBm at 2.45 GHz(1)	BI_{far}	57			dBc
6	**RSSI Part**						
6.1	Maximum RSSI output voltage	Under high RX input signal level	$V_{RSSImax}$		2.1		V
6.2	RSSI output voltage, monotonic over range –96 dBm to –36 dBm	With –33 dBm at RF input With –96 dBm at RF input	V_{RSSI}		1.9 0.1		V V
7	**VCO**						
7.1	Oscillator frequency defined at TX output	Over full temperature range(1)		2400		2483	MHz
7.2	Frequency control voltage range		V_{VTUNE}	0.5		V_{CC} – 0.5	V
7.3	VCO tuning input gain defined at TX output		G_{VCO}		240		MHz/V

Notes:
1. Measured and guaranteed only on the Atmel® evaluation board, including microstrip filter, balun, and Smart Radio Frequency (Smart RF) firmware. Conducted measured.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of the loop filter. For further information refer to the application notes.
3. The Gaussian filter control setting (GFCS) is used to compensate production tolerances by tuning the modulation deviation in production to the nominal value of 400 kHz.
4. Burst mode with 0.9% duty cycle

6. Electrical Characteristics (Continued)

V_S = 3.6V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
8	**Synthesizer**						
8.1	External reference input frequency	D7 = 0 D7 = 1	REF_CLK		10.368 13.824		MHz MHz
8.2	Sinusoidal input signal level (peak-to-peak value)	AC-coupled sine wave	REF_CLK	500		1000	mV_{PP}
8.3	Scaling factor prescaler		S_{PSC}		32/33		-
8.4	Scaling factor main counter		S_{MC}		86/87/88/89		-
8.5	Scaling factor swallow counter		S_{SC}	0		31	-
9	**Phase Detector**						
9.1	Phase detector comparison frequency		f_{PD}		1728		kHz
10	**Charge-pump Output**						
10.1	Charge-pump output current	V_{CP} = 1/2 V_{CC}	I_{CP}		±2		mA
10.2	Leakage current	V_{CP} = 1/2 V_{CC}	I_L		±100	1000	pA
11	**Timing Conditions[1][2]**						
11.1	Transmit to receive time	Reference clock stable	TX → RX time		200		µs
11.2	Receive to transmit time	Reference clock stable	RX → TX time		200		µs
11.3	Channel switch time	Reference clock stable	CS time		200		µs
11.4	Power down to transmit	Reference clock stable	PD → TR time		250		µs
11.5	Power down to receive	Reference clock stable	PD → RX time		200		µs
11.6	Programming register	Reference clock stable	PRR time		3		µs
11.7	PLL settling time	Reference clock stable	PLL set time		200		µs
12	**Interface Logic Input and Output Signal Levels, Pin DATA, CLOCK, ENABLE**						
12.1	HIGH-level input voltage	Logic 1	V_{IH}	1.4		3.1	V
12.2	LOW-level input voltage	Logic 0	V_{IL}	–0.3		+0.4	V
12.3	HIGH-level output voltage	Logic 1	V_{OH}			3.1	V
12.4	LOW-level output voltage	Logic 0	V_{OL}	0			V
12.5	Input bias current	Logic 1 or logic 0	I_{bias}	–5		+5	µA
12.6	3-wire bus clock frequency		f_{CLKmax}			10	MHz

Notes:
1. Measured and guaranteed only on the Atmel® evaluation board, including microstrip filter, balun, and Smart Radio Frequency (Smart RF) firmware. Conducted measured.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of the loop filter. For further information refer to the application notes.
3. The Gaussian filter control setting (GFCS) is used to compensate production tolerances by tuning the modulation deviation in production to the nominal value of 400 kHz.
4. Burst mode with 0.9% duty cycle

7. PLL Principle

Figure 7-1. PLL Principle

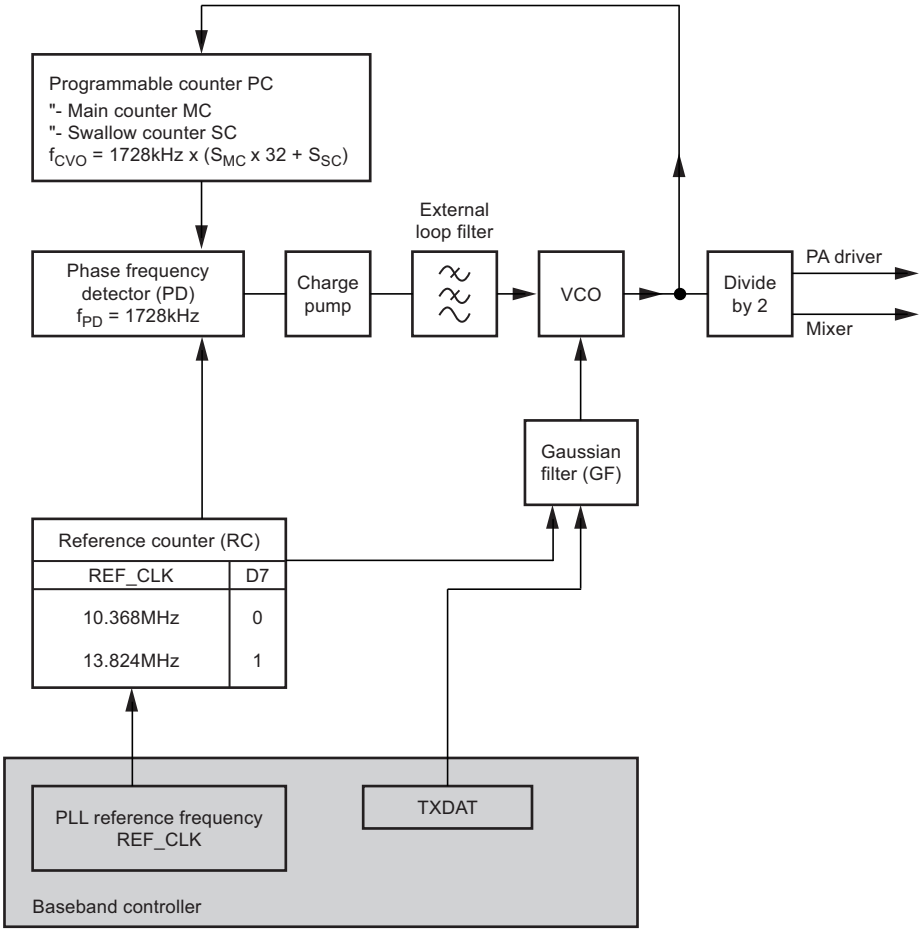


Table 7-1 shows the LO frequencies for RX and TX in the 2.4-GHz ISM band. There are 95 channels available. Since the ATR2406 supports wideband modulation with 400-kHz deviation, every second channel can be used without overlap in the spectrum.

Table 7-1. LO Frequencies

Mode	f_{IF} / kHz	Channel	f_{ANT} / MHz	f_{VCO} / MHz divided by 2	S_{MC}	S_{SC}	N
TX		C0	2401.056	2401.056	86	27	2779
		C1	2401.920	2401.920	86	28	2780
		...	...	...	...	...	...
		C93	2481.408	2481.408	89	24	2872
		C94	2482.272	2482.272	89	25	2873
RX	864	C0	2401.056	2401.920	86	28	2780
		C1	2401.920	2402.784	86	29	2781
		...	...	...	...	...	...
		C93	2481.408	2482.272	89	25	2873
		C94	2482.272	2483.136	89	26	2874

7.1 TX Register Setting

The following 16-bit word has to be programmed for TX.

MSB															LSB
Data bits															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PA		GFCS			1	RC	MC		SC				

Note: D12 and D13 are only relevant if ramping generator in conjunction with external PA is used, otherwise it can be programmed 0 or 1.

Table 7-2. Output Power Settings with Bits D12 - D13

PA (Output Power Settings)		
D13	**D12**	**RAMP_OUT (Pin 21)**
0	0	1.3V
0	1	1.35V
1	0	1.4V
1	1	1.75V

The VRAMP voltage is used to control the output power of an external power amplifier. The voltage ramp is started with the TX_ON signal.

These bits are only relevant in TX mode.

7.2 RX Register Setting

There are two RX settings possible. For a data rate of 1152 kBits/s, an internal clock recovery function is implemented.

7.3 Register Setting Without Clock Recovery

Must be used for data rates below 1.152 Mbits/s.

MSB															LSB
Data bits															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	X	X	X	X	X	0	RC	MC		SC				

Note: X values are not relevant and can be set to 0 or 1.

7.4 RX Register Setting with Internal Clock Recovery

Recommended for 1.152-Mbit/s data rate.

The output pin of the recovered clock is pin 6. The falling edge of the recovered clock signal samples the data signal.

MSB								
Data bits								
D24	D23	D22	D21	D20	D19	D18	D17	D16
1	0	1	0	0	0	0	0	0

															LSB
Data bits															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	X	X	X	X	X	0	RC	MC		SC				

Note: X values are not relevant and can be set to 0 or 1.

7.5 PLL Settings

RC, MC and SC bits control the synthesizer frequency as shown in Table 7-3, Table 7-4 on page 12 and Table 7-5 on page 12.

Formula for calculating the frequency:

TX frequency: $f_{ANT} = 864\ kHz \times (32 \times S_{MC} + S_{SC})$
RX frequency: $f_{ANT} = 864\ kHz \times (32 \times S_{MC} + S_{SC} - 1)$

Table 7-3. PLL Settings of the Reference Counter Bit D7

RC (Reference Counter)	
D7	**CLK Reference**
0	10.368 MHz
1	13.824 MHz

Table 7-4. PLL Settings of the Main Counter Bits D5 to D6

MC (Main Counter)		
D6	**D5**	**S_{MC}**
0	0	86
0	1	87
1	0	88
1	1	89

Table 7-5. PLL Settings of the Swallow Counter Bits D0 to D4

SC (Swallow Counter)					
D4	**D3**	**D2**	**D1**	**D0**	**S_{SC}**
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

7.6 GFCS Adjustment

The Gaussian filter control setting (GFCS) is used to compensate for production tolerances by tuning the modulation deviation in production to the nominal value of 400 kHz. These bits are only relevant in TX mode.

Table 7-6. GFCS Adjustment of Bits D9 - D11

GFCS			
D11	**D10**	**D9**	**GFCS**
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

7.7 Control Signals

The various transceiver functions are activated by the following control signals. A timing proposal is shown in Figure 7-3 on page 14

Table 7-7. Control Signals and Functions

Signal	Functions
PU_REG	Activates AUX voltage regulator and the VCO voltage regulator supplying the complete transceiver
PU_TRX	Activates RX/TX blocks
RX_ON	Activates RX circuits: DEMOD, IF AMP, IR MIXER
TX_ON	Activates TX circuits: PA, RAMP GEN, Starts RAMP SIGNAL at RAMP_OUT
nOLE	Disables open loop mode of the PLL

7.8 Serial Programming Bus

The transceiver is programmed by the SPI (CLOCK, DATA and ENABLE).

After setting the enable signal to low, the data is transferred bit by bit into the shift register on the rising edge of the clock signal, starting with the MSBit. When the enable signal has returned to high, the programmed information is active. Additional leading bits are ignored and there is no check made of how many clock pulses arrived during enable low.

The programming of the transceiver is done by a 16-bit or 25-bit data word (for the RX clock recovery mode).

7.9 3-wire Bus Timing

Figure 7-2. 3-wire Bus Protocol Timing Diagram

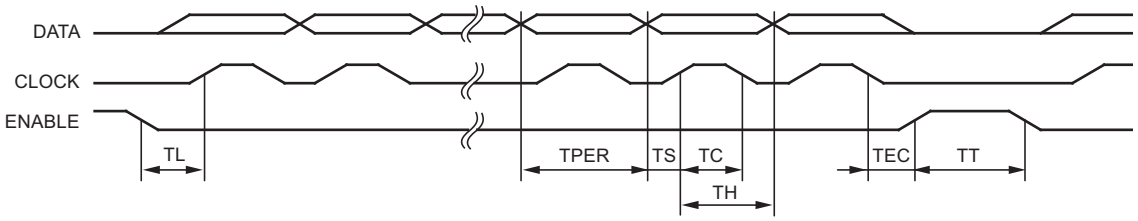


Table 7-8. 3-wire Bus Protocol Table

Description	Symbol	Minimum Value	Unit
Clock period	TPER	100	ns
Set time data to clock	TS	20	ns
Hold time data to clock	TH	20	ns
Clock pulse width	TC	60	ns
Set time enable to clock	TL	100	ns
Hold time enable to data	TEC	0	ns
Time between two protocols	TT	250	ns

Figure 7-3. Example TX and RX Timing Diagram

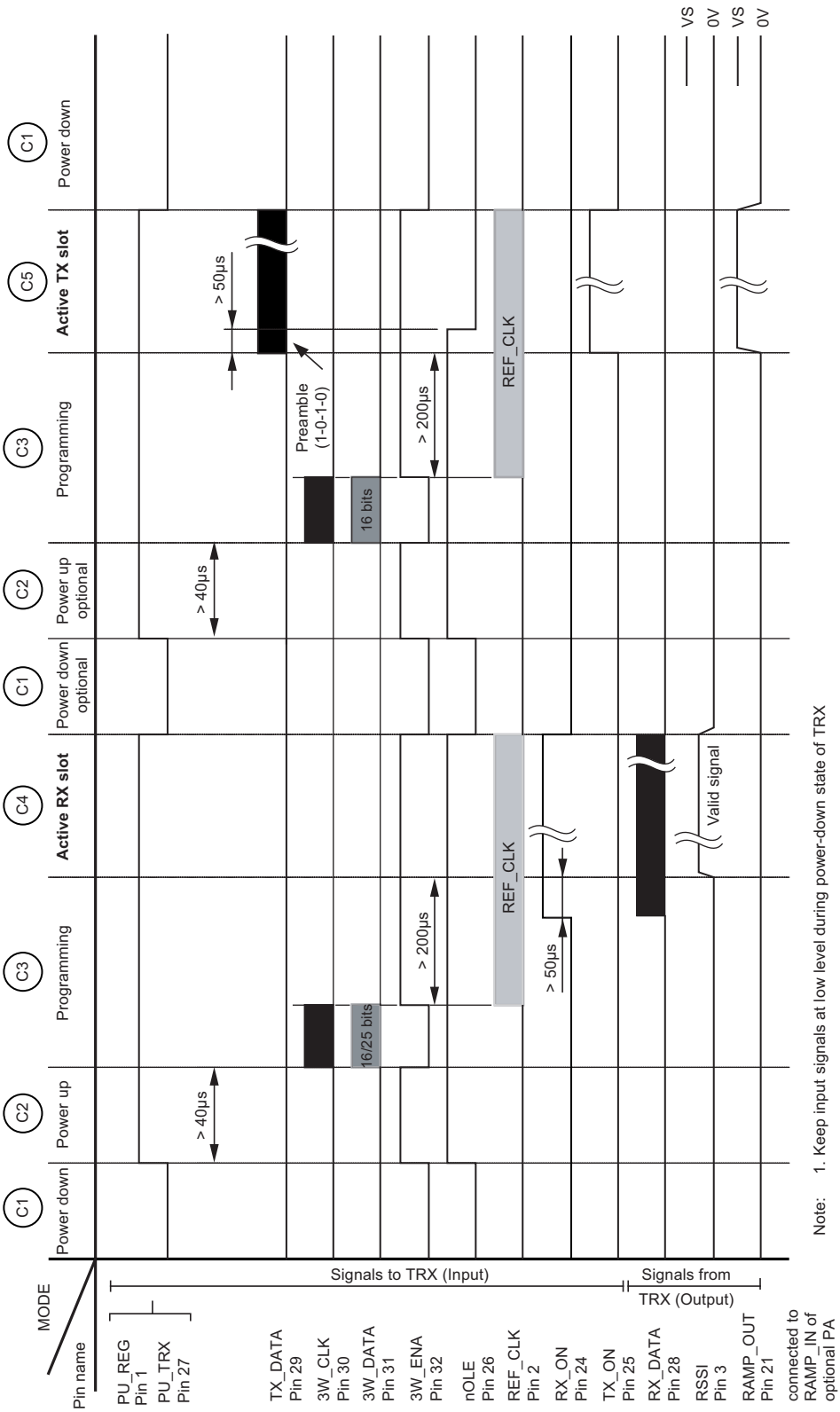


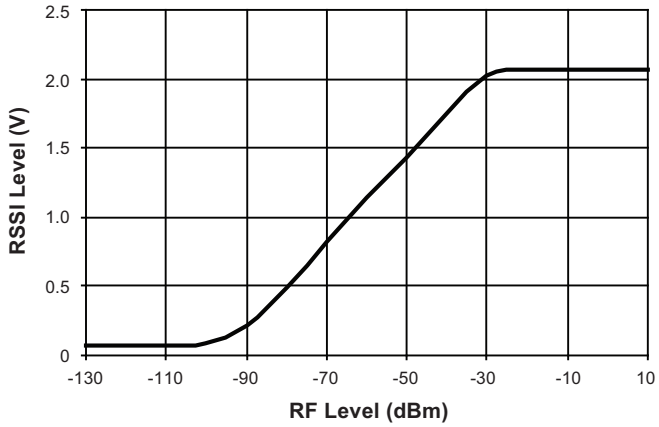
Table 7-9. Description of the Conditions/States

Condition	Description
C1	Power down ATR2406 is switched off and the supply current is lower than 1 µA.
C2	Power up ATR2406 is powered up by toggling PU_REG and PU_TRX to high. PU_REG enables the external AUX regulator transistor including VCO regulator. PU_TRX enables internal blocks like the PLL and the VCO. Depending on the value of the external capacitors (for example, at the AUX regulator, if one is used), it is necessary to wait at least 40 µs until the different supply voltages have settled.
C3	Programming The internal register of the ATR2406 is programmed via the three-wire interface. At TX, this is just the PLL (transmit channel) and the deviation (Gaussian filter). At RX, this is just the PLL (receive channel) and, if the clock recovery is used, also the bits to enable this option. At the start of the three-wire programming, the enable signal is toggled from high to low to enable clocking the data into the internal register. When the enable signal rises again to high, the programmed data is latched. This is the time point at which the settling of the PLL starts. It is necessary to wait the settling time of 200 µs so that the VCO frequency is stable. The reference clock needs to be applied to ATR2406 for at least the time when the PLL is in operation, which is the programming state (C3) and the active slot (C4, C5). Out of the reference clock, several internal signals are also derived, for example, the Gaussian filter circuitry and TX_DATA sampling.
C4	This is the receive slot where the transmit burst is received and data as well as recovered clock are available.
C5	This is the active transmit slot. As soon as TX_DATA is applied to ATR2406, the signal nOLE toggles to low which enables modulation in open-loop mode. The preamble (1-0-1-0 pattern) should start being sent at the start of TX_ON.

7.10 Received Signal Strength Indication (RSSI)

The RSSI is given as an analog voltage at the RSSI pin. A typical plot of the RSSI value is shown in Figure 7-4.

Figure 7-4. Typical RSSI Value versus Input Power



8. Application Circuit

The ATR2406 requires only a few low-cost external components for operation. A typical application is shown in Figure 8-3 on page 17.

8.1 Typical Application Circuit

Figure 8-1. Microcontroller Interfacing with General Purpose MCU, Pin Connections between Microcontroller and ATR2406

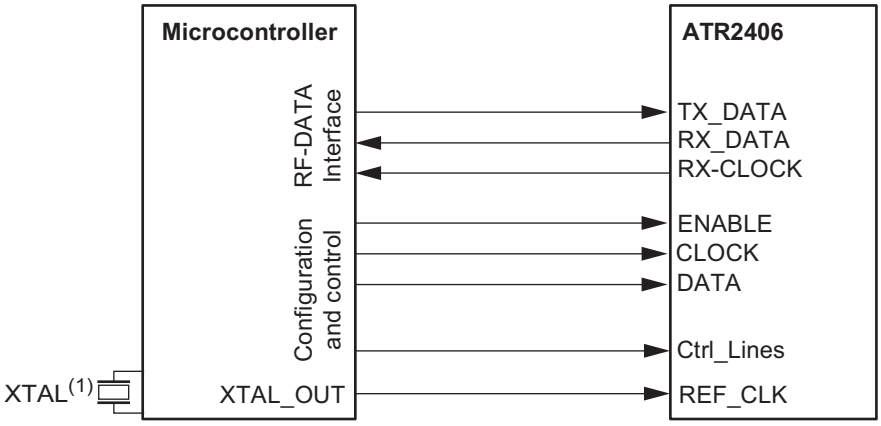
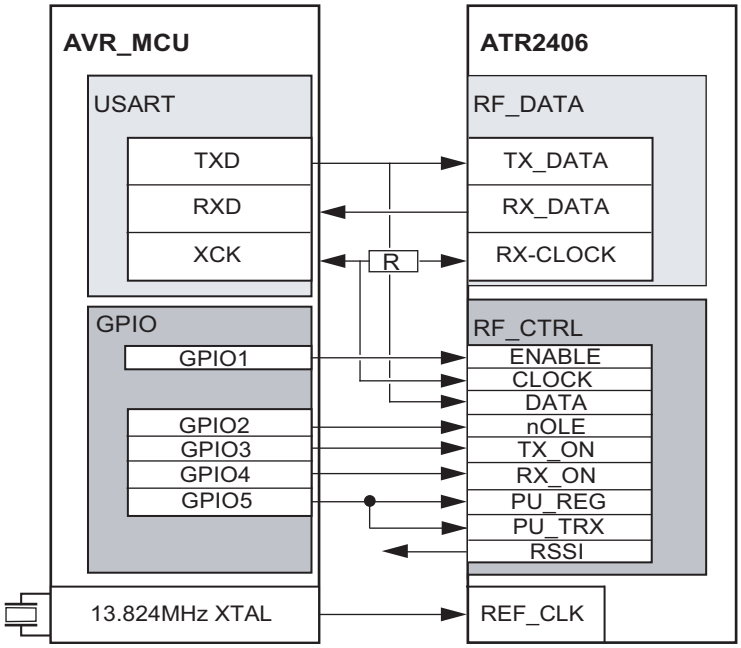
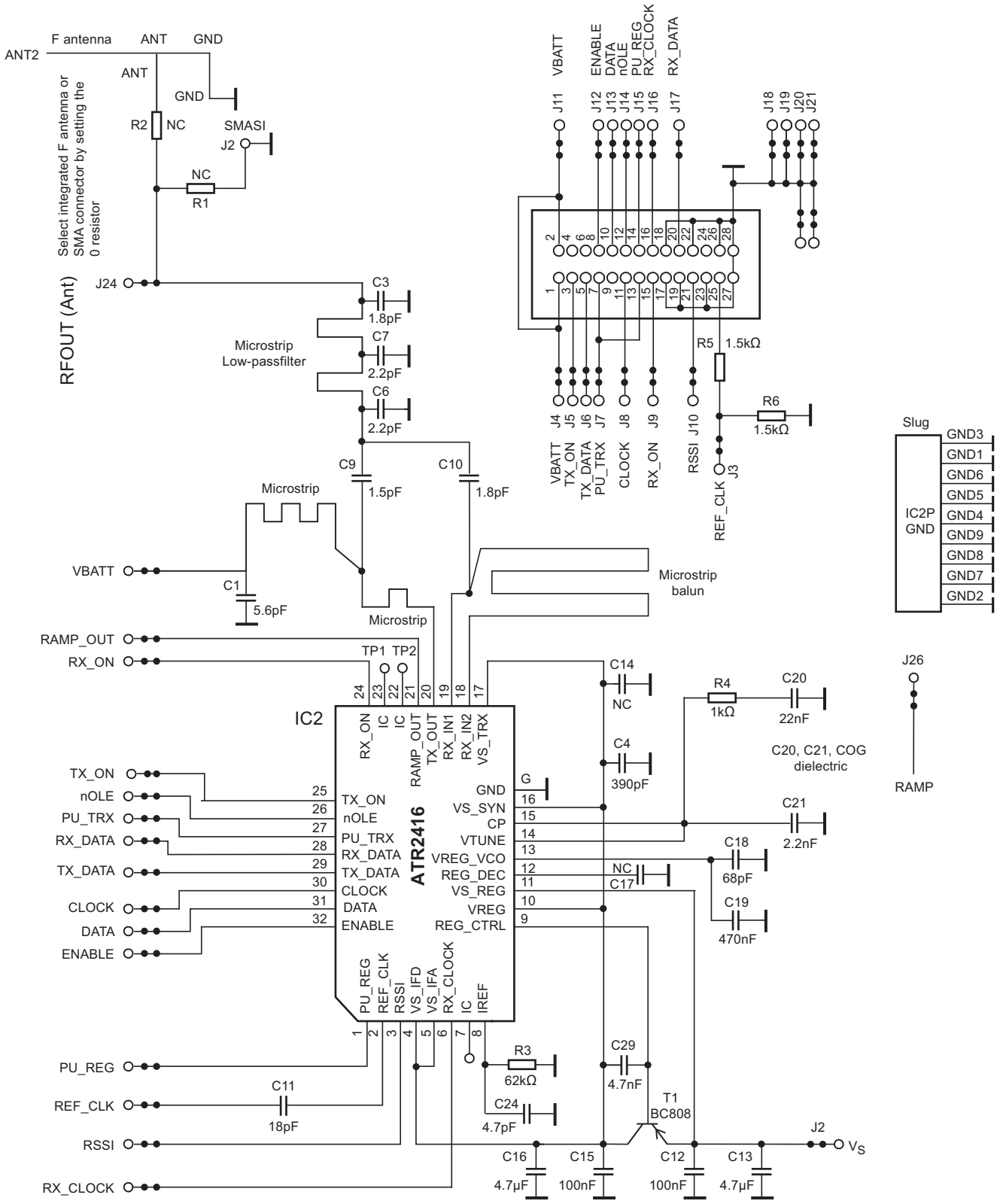


Figure 8-2. Example with AVR MCU



Note: 1. XTAL: for example, XRFBCC-NANL; 13.824 MHz, 10 ppm
Order at: Taitien Electronic, Taitien Specific No.: A009-x-B26-3, SMD

Figure 8-3. Application Circuit for ATR2406-DEV-BOARD



9. PCB Layout Design

Figure 9-1. PCB Layout ATR2406-DEV-BOARD

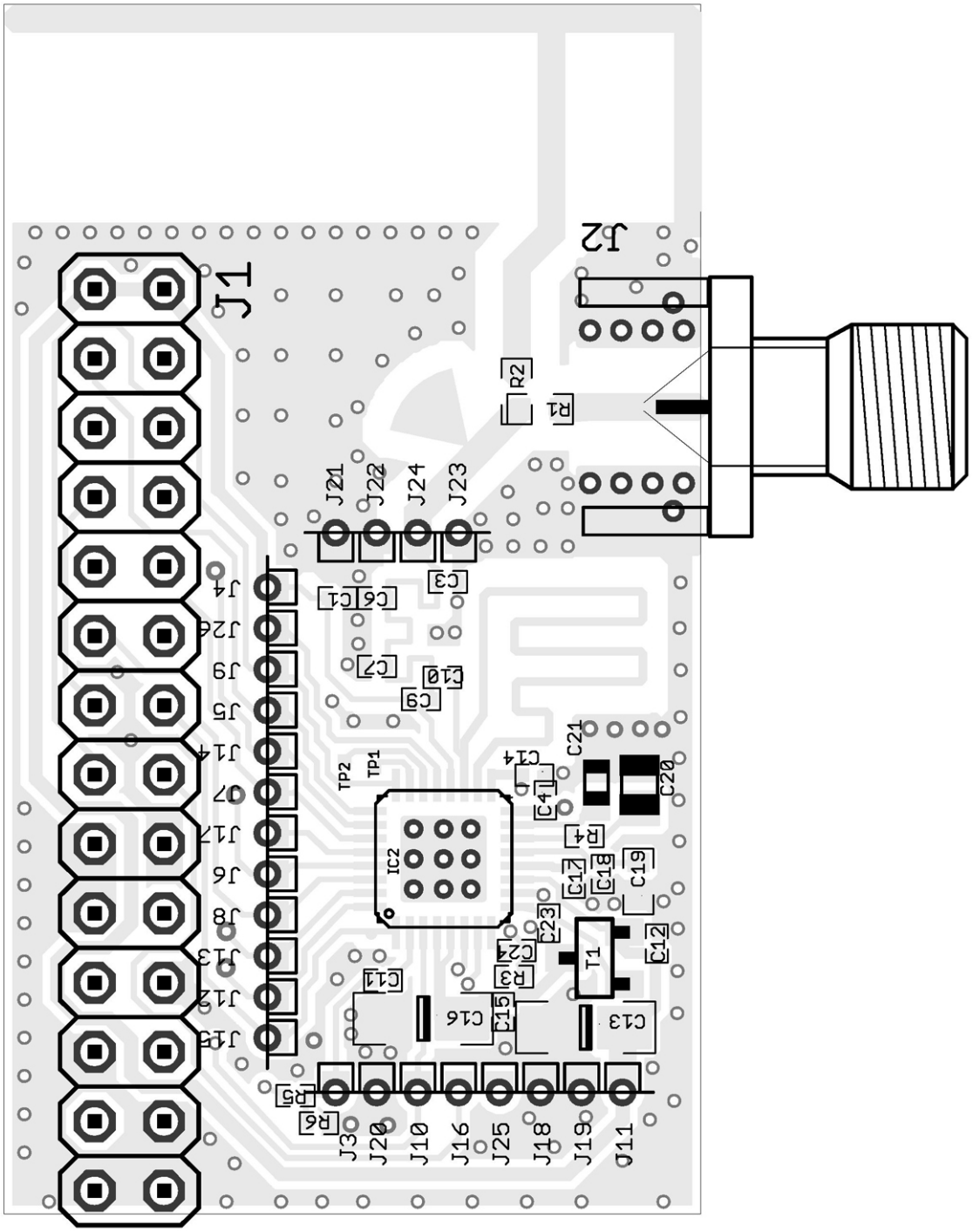


Table 9-1. Bill of Materials

Part	Value	Part Number	Vendor	Package	Comment
C1	5.6 pF			0402	
C3, C10	1.8 pF			0402	
C4	390 pF			0402	
C5	4.7 pF			0402	NC
C6, C7	2.2 pF			0402	
C9	1.5 pF			0402	
C11	18 pF			0402	
C12, C15	100 nF			0402	
C13, C16	4.7 µF	B45196H2475M109	Epcos®	3216	Optional(2)
C14	1 nF			0402	NC
C17	3.3 nF			0402	NC
C18	68 pF			0402	
C19	470 nF			0402/0603	
C20	22 nF, COG	GRM21B5C1H223JA01	Murata	0805	COG, important for good RF performance
C21	2.2 nF, COG	GRM1885C1H222JA01	Murata	0603	COG, important for good RF performance
C23	4.7 nF			0402	
C24	4.7 pF			0402	
R3	62 kΩ	62k, ≤ 5%		0402	
R4	1.0 kΩ	1k0, ≤ 5%		0402	
R5	1.5 kΩ	1k5, ≤ 5%		0402	Ref_Clk level, optional(1)
R6	1.5 kΩ	1k5, ≤ 5%		0402	Ref_Clk level, optional(1)
IC2	ATR2406	ATR2406	Atmel	MLF32	
T1	BC808-40	BC808-40, any standard type can be used, but it is important that be “–40”!	Vishay®, Philips®, etc.	SOT-23	Optional(2)
MSUB	FR4	FR4, e_r = 4.4 at 2.45 GHz, H = 500 µm, T = 35 µm, t_{and} = 0.02, surface, that is, chem. tin or chem. gold			

Notes: 1. Not necessary if supplied RefClk level is within specification range

2. If no AUX regulator is used, then T1 and C16 can be removed and a jumper is needed from the collector to the emitter pad. Additionally, pin 7 of the ATR2406 has to be connected to pin 4 or pin 5 to use the integrated F antenna, set jumper R2 (0R resistor 0603)

Table 9-2. Parts Count Bill of Materials

Parts Count	Required (Minimal BOM)	Optional (Depending on Application)
Capacitors 0402	14	14
Capacitors >0402	2	4
Resistors 0402	2	2
Inductors 0402	–	–
Semiconductors	1	2

10. Appendix: Current Calculations for a Remote Control

Assumptions:

Protocol	A data packet consists of 24 bytes. 24 bytes = 240 bits (USART connection) T_{packet_length} = 210 µs at 1.152 Mbits/s
Channel	The system will use five predefined channels for frequency hopping spread spectrum (FHSS) which gives improved immunity against interferers
Loop filter	Loop filter settling time will be 110 µs
Handheld device	If not in use, the handheld device will be in power-down mode with the AVR's watchdog timer disabled. The AVR power-down current is typically 1.25 µA. If an external voltage regulator is used, additional power-down current has to be taken into account
Base station device	The base station will periodically scan all the channels of the used subset. The base station will stay on one channel for 2 seconds. If the base station receives a correct packet, an acknowledge will be returned to the handheld device. The power consumption of the base station device is not power-sensitive, as this part of the application is normally mains powered

Basic Numbers:

Peak current ATR2406 in TX at 1.152 Kbits/s	42 mA
Peak current ATR2406 in RX at 1.152 Kbits/s	57 mA
Peak current ATR2406 with synthesizer running	26 mA
Current ATmega88 active	5 mA
Current ATmega88 power down (no WDT)	1.25 µA
Current ATmega88 power down (+ WDT)	5 µA
Loop settling time of ATR2406	110 µs
Configuration of ATR2406	30 µs
Time needed for exchanging a packet at 1.152 Kbits/s	210 µs

Amount of Current Needed to Transmit One Packet:

Q1 = (0.005A + 0.026A) × 5030 µs = 155 µAs (charge up time ATR2406 + AVR internal calculations)
Q2 = (0.005A + 0.026A) × 30 µs = 0.93 µAs (charge for configuring the ATR2406)
Q3 = (0.005A + 0.026A) × 110 µs = 3.41 µAs (charge for settling the loop filter)
Q4 = (0.005A + 0.042A) × 210 µs = 9.87 µAs (charge for transmitting the packet)
Q5 = (0.005A) × 250 µs = 1.25 µAs (charge for turn around (TX to RX, RX to TX, etc.))
Q6 = (0.005A + 0.026A) × 30 µs = 0.93 µAs (charge for configuring the ATR2406)
Q7 = (0.005A + 0.026A) × 60 µs = 1.86 µAs (charge for settling the loop filter)
Q8 = (0.005A + 0.057A) × 50 µs = 3.10 µAs (charge until valid data can be received)
Q9 = (0.005A + 0.057A) × 210 µs = 13.02 µAs (charge for receiving the packet)
Q10 = (0.005A + 0.057A) × 50 µs = 3.1 µAs (charge for latency before receiving)

A successful packet exchange needs the following charge
Q = Q1 + Q2 + Q3 + Q4 + Q5 + Q6 + Q7 + Q8 + Q9 + Q10 = 192.47 µAs

As the described system is a FHSS system with 5 different channels, the system has to do this up to five times before the packet is acknowledged by the base station. The average will be 2.5 times. In the case of an interfered environment, some more retries may be required; therefore, it is assumed the factor will be 3. The power-up time is included only once, as the cycle will be completed without powering up and down the handheld in order to be as power efficient as possible.

Average current needed for a packet exchange:

155 µAs + (37.5 µAs × 3) = 267.5 µAs
If the device will be used 1000 times a day → 3.1 µA

Average current in active mode:

→ System Power Down current:

Current ATmega88:	1.25 µA
Current ATR2406:	1.0 µA
Current VREG (+ ShutDown):	2.75 µA

Assumed average power-down current is 5 µA.

→ Overall power consumption is 8.1 µA

It is assumed the system uses a small battery with a capacity of 100 mAh. This is 100.000 µAh.

→ Battery lifetime will be around: 12345 hours = 514 days = 1.4 years.

The most important factor is to get the power-down current as low as possible!

Example:

Assume a system where the handheld is used just 10 times per day.
→ I_{active} = 0.031 µA

and assuming the power-down current of this device is just 4 µA.

→ I = 0.031 µA + 4 µA = 4.03 µA

→ Battery lifetime will be around 24807 hours = 1033 days = 2.83 years.

→ Power-down current is the main factor influencing the battery lifetime.

11. Ordering Information

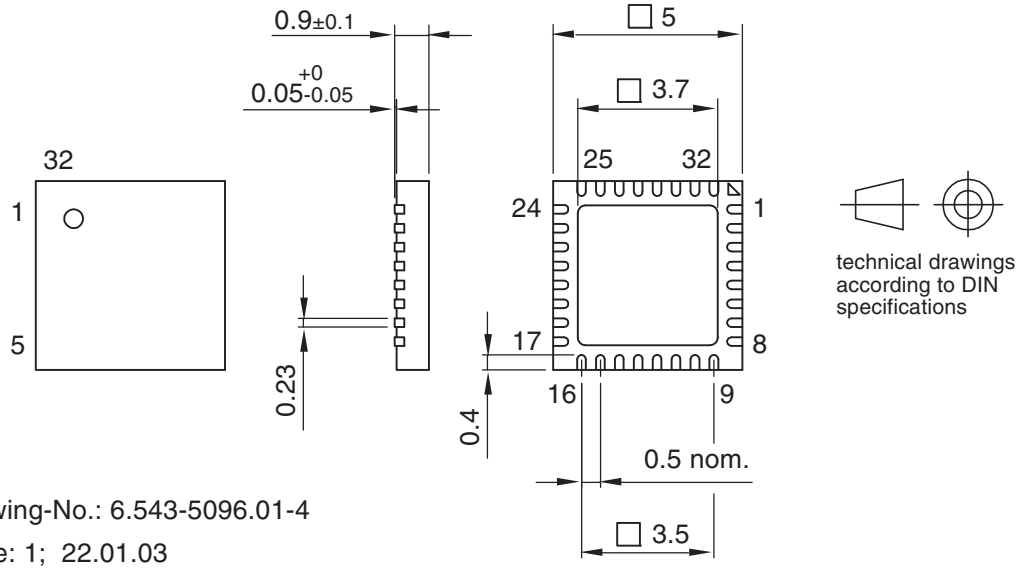
Extended Type Number	Package	Remarks	MOQ
ATR2406-PNQG	QFN32 - 5x5	Taped and reeled, Pb-free	4000
ATR2406-DEV-BOARD	–	RF module	1
ATR2406-DEV-KIT2	–	Complete evaluation kit and reference design ATR2406 + ATmega88	1

12. Package Information

Package: QFN 32 - 5 x 5
Exposed pad 3.7 x 3.7

Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5096.01-4
Issue: 1; 22.01.03

13. Recommended Footprint/Landing Pattern

Figure 13-1. Recommenced Footprint/Landing Pattern

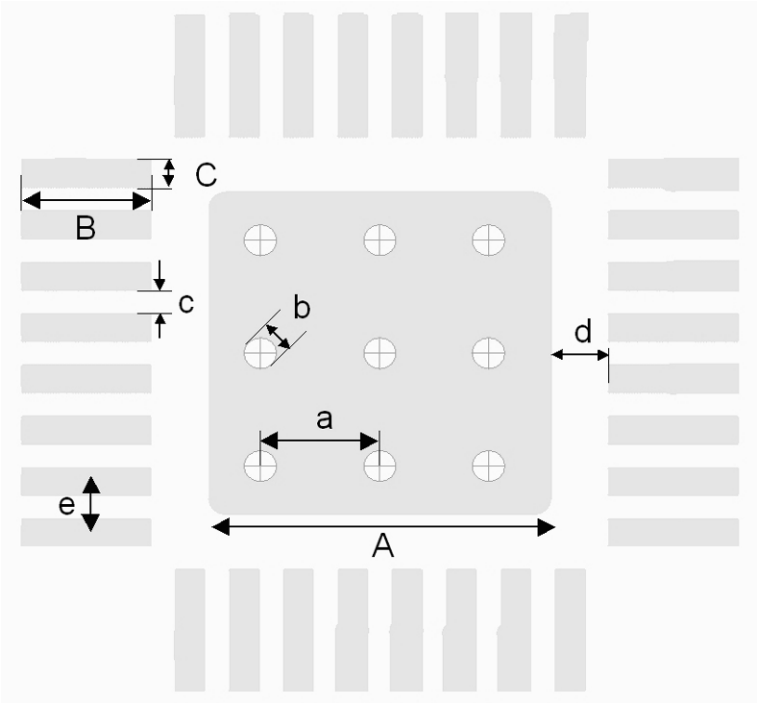


Table 13-1. Recommended Footprint/Landing Pattern Signs

Sign	Size
A	3.2 mm
B	1.2 mm
C	0.3 mm
a	1.1 mm
b	0.3 mm
c	0.2 mm
d	0.55 mm
e	0.5 mm

14. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4779N-ISM-12/08	• Put datasheet in a new template • Section 12 “Package Information” on page 22 changed
4779M-ISM-02/07	• Put datasheet in a new template • Table 9-1 “Bill of Materials” on page 19 changed
4779L-ISM-08/06	• Table “Electrical Characteristics” on pages 6 to 8 changed • Section 10 “Appendix: Current Calculations for a Remote Control” on pages 20 to 21 changed • Table “Ordering Information” on page 22 changed • Minor corrections to grammar and style throughout document
4779K-ISM-06/06	• Put datasheet in a new template • Table “Electrical Characteristics” on pages 6 to 8 changed • Section 10 “Appendix: Current Calculations for a Remote Control” on pages 20 to 21 added • Ordering Information on page 22 changed

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