Amulet Technologies

GUI Engines for Embedded Systems

Easy GUI™ Browser Chip

AGB64LV01-QC

General Description

Amulet Easy GUI Browser Chip is a special purpose micro controller that is optimized to execute Amulet's GUI kernel and component based GUI firmware, The chip is a combination LCD controller chip and a user interface chip. This chip eliminates the need for complex code to draw each pixel on a LCD. The chip renders GUI pages containing graphic images, Amulet Widgets, and other UI objects directly to the LCD. This lets your embedded micro do it's job more efficiently. Thus, the main application can run on a smaller processor with less RAM and ROM, and code development and maintenance time is Significantly reduced.

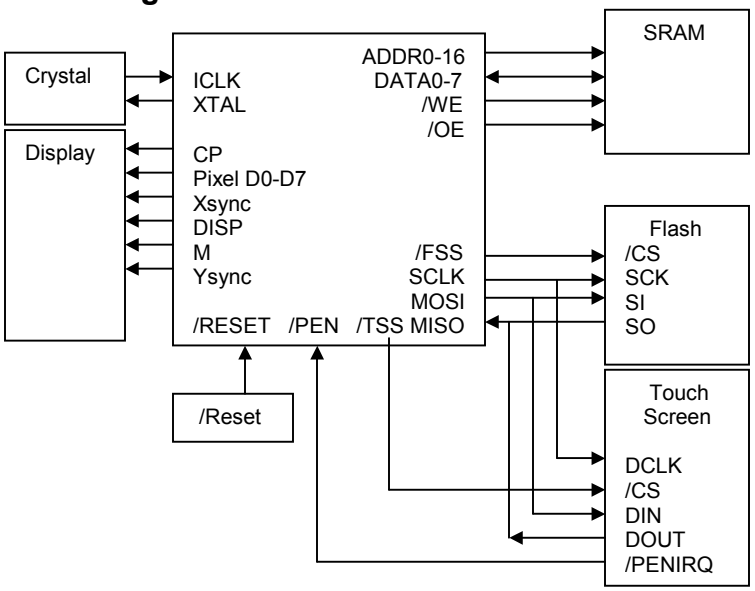
Features

- **Dedicated GUI Chip -** Manages the GUI, Interacts with the user, and controls the LCD – Frees up your Micro!
- **HTML-Based GUI Creation** – Create and edit Quickly using drag-and-drop HTML tools
- **Compiler Included** – Converts from HTML, JPEG, and GIF into small, quickly-executable Amulet ᑊHTML pages
- **Processor Independent** – Easily interfaces to Most micro controllers (8/16/32-bit and DSPs)
- **Replaces Traditional GUI Library** – No Library porting, complex GUI programming, or RTOS required
- **RS232 Interface** – Up to 115,200 bps

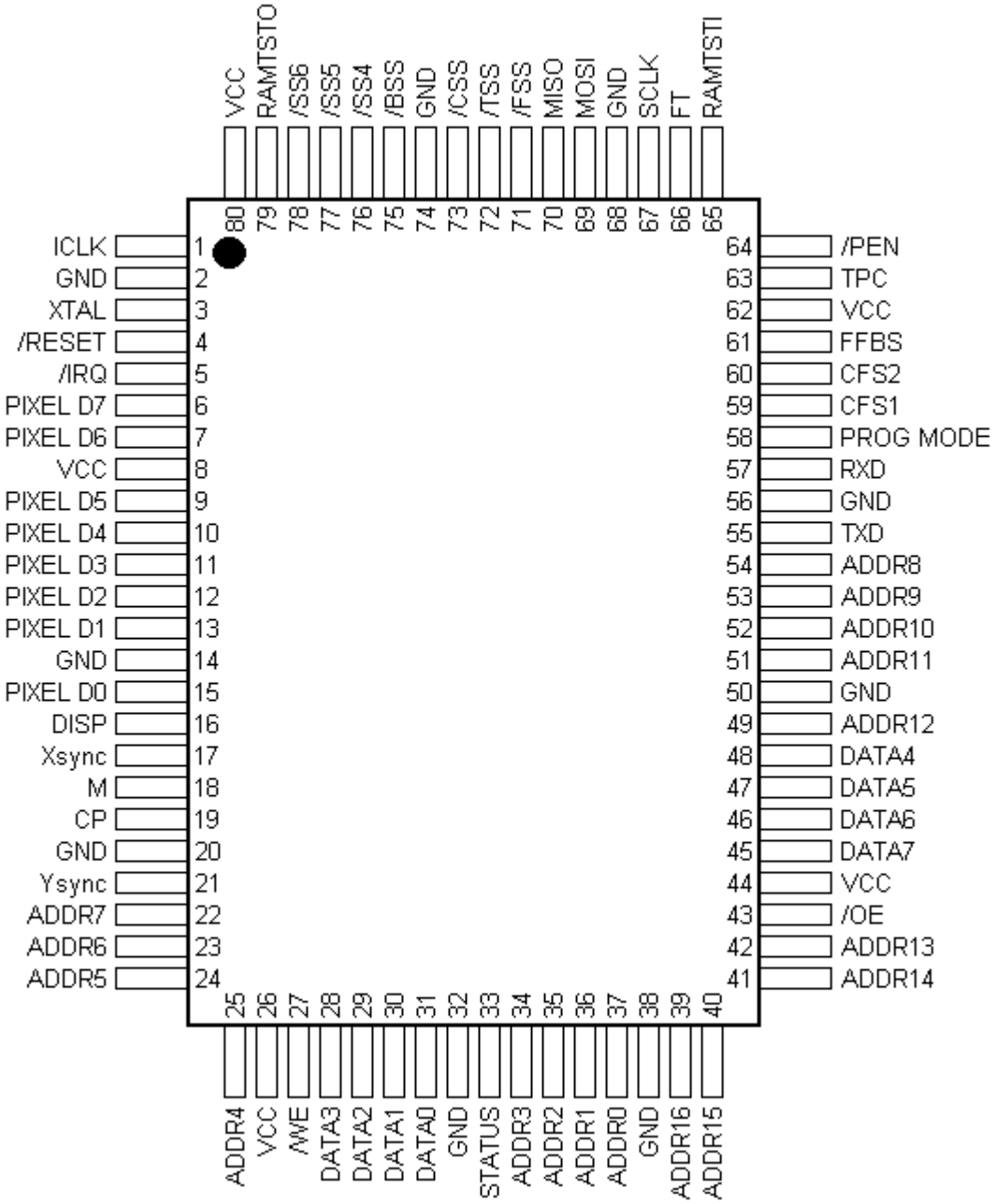
Requirements

- 3.3V Power Supply
- Serial Flash (Atmel 4 Megabit recommended)
- Asynchronous SRAM (128Kx8 Minimum)
- Clock/Crystal (up to 20 MHz.)

Typical Circuit Block Diagram



Pin Configurations



Overview

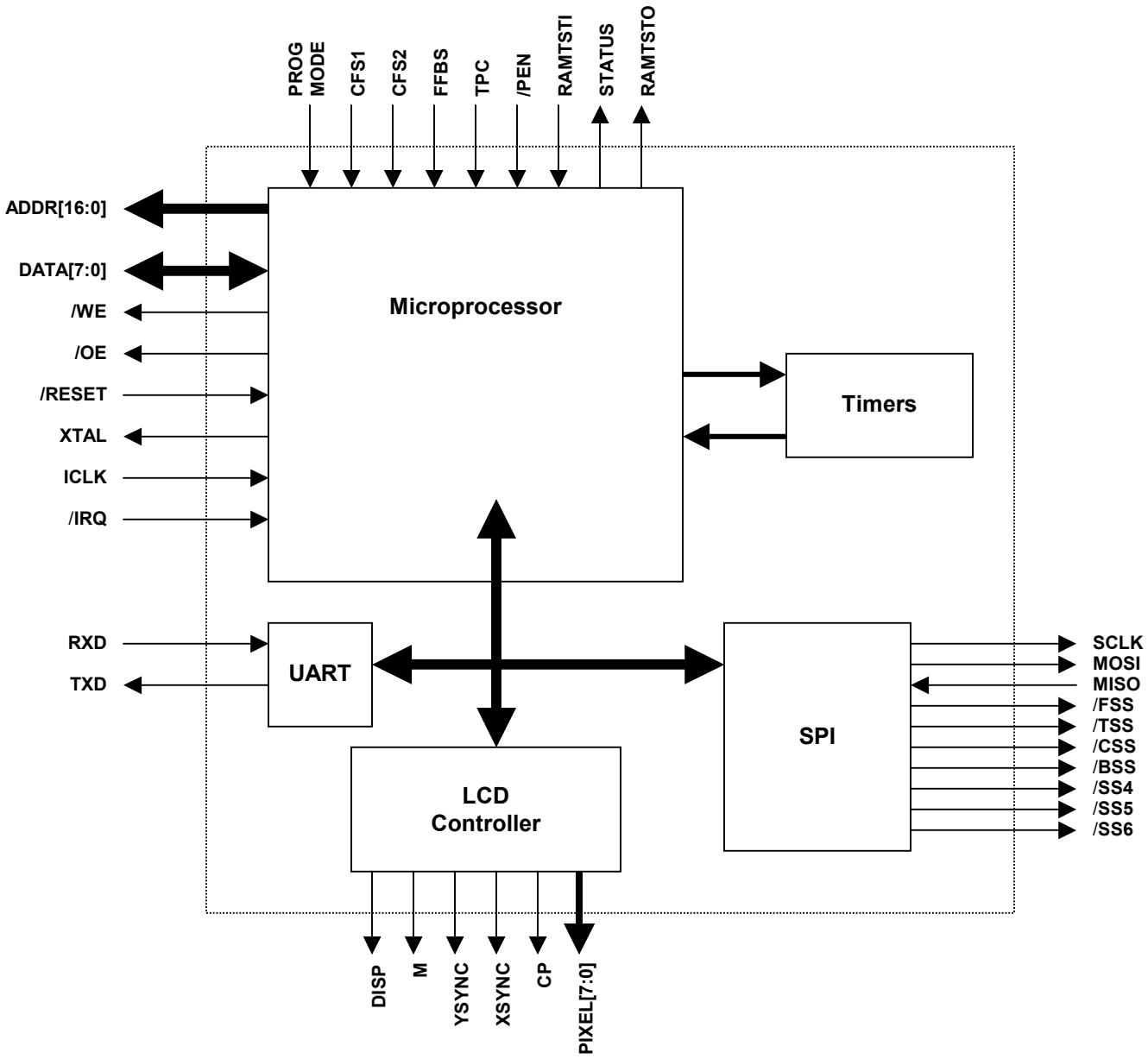
The Amulet is a powerful 8-bit microcontroller featuring task specific opcodes, registers, and memory segments allowing for optimization of graphics rendering, I/O processing, and general purpose computing. The Amulet is equipped with the following built-in peripherals:

- LCD Controller
- Microprocessor
- UART
- Timers
- SPI Master

The Easy GUI Browser chip has 13 dedicated output lines for LCD control of various sized sub-VGA displays. The chip is able to drive different size displays because the bias voltage, which determines the LCD driving voltage, is supplied from an external source.

- Supply voltage: 3.3V +/- 10%
- Applicable LCD duty: up to 1/640
  (adjustable in single increments)

Block Diagram



Pin Descriptions

I = [1]CMOS Input
O = [1]CMOS Output
I/O = [1]CMOS Input & Output
P = Power Supply

[1] The I/O pins are only VCC tolerant and must adhere to the voltage levels depicted in the DC CHARACTERISTICS section. All input pins have an internal pull-up resistor.

Pin Name	Type	Pin Number	Description
VCC	P	8, 26, 44, 62, 80	Supply voltage. 3.3V
GND	P	2, 14, 20, 32, 38, 50, 56, 68, 74	Ground.
ICLK	I	1	[1]System clock. Reference Recommended XTAL Connections section.
XTAL	O	3	[1]System clock. Reference Recommended XTAL Connections section.
/RESET	I	4	[1,5,6]System reset. A low level of 10us or longer will generate a system reset.
/IRQ	I	5	[1]System interrupt. This pin should be left unconnected.
PIXELD0 - PIXELD7	O	6-7, 9-13, 15	[1]LCD pixel data. The LCD pixel data bus width can be set to 1, 2, 4, or 8 data bits via the HTMLCompiler software.
DISP	O	16	[1]LCD control signal (High = LCD on, Low = LCD off).
Xsync	O	17	[1]LCD data latch. Xsync goes active for one clock period after all the LCD pixel data for the current line has been shifted out. The Xsync polarity can be set via the HTMLCompiler software.
M	O	18	[1]LCD crystal polarization clock.
CP	O	19	[1]LCD pixel clock. The CP's active edge can be set to a rising or falling edge via the HTMLCompiler software.
Ysync	O	21	[1]LCD first frame synchronization.
ADDR0 - ADDR16	O	22-25, 34-37, 39-42, 49, 51-54	[1]System address bus.
DATA0 - DATA7	I/O	28-31, 45-48	[1]System data bus.
/WE	O	27	[1]Memory write enable to data bus (Low = write).
/OE	O	43	[1]Memory output enable from data bus (Low = read).
STATUS	O	33	[1]Internal operational status. This pin should be left unconnected.
TXD	O	55	[1] UART data output.
RXD	I	57	[1,5]UART data input.
PROG MODE	I	58	[1,2,5]System power up mode. A low level boots Amulet in run mode. A high level boots Amulet in program mode.
CFS1	I	59	[1]Crystal frequency selection 1. Reference Recommended XTAL Component Selections section.
CFS2	I	60	[1]Crystal frequency selection 2. Reference Recommended XTAL Component Selections section.
FFBS	I	61	[1,3,5]Flash programming baud rate. A low level sets the flash programming rate to 19,200 bps. A high level sets the flash programming rate to 115,200 bps.
TPC	I	63	[1,4,5]Touch panel calibration mode. A low level does not perform a calibration session. A high level performs a calibration session.
/PEN	I	64	[1,5]Touch panel status if a touch panel is used. A low level indicates touch panel is pressed. A high level indicates touch panel is not pressed. This pin should be left unconnected if no touch panel is used.
RAMTSTI	I	65	[1,4]External SRAM test. A low level instructs Amulet to perform an external SRAM test. A high level instructs Amulet to not perform an external SRAM test. When applicable, results of external SRAM test are output on pin 79 (RAMTSTO).
FT	I	66	[1]Factory test. This pin should be left unconnected.
SCLK	O	67	[1]SPI clock.
MOSI	O	69	[1]SPI data out.
MISO	I	70	[1,5]SPI data in.

/FSS	O	71	[1]Flash slave select.
/TSS	O	72	[1]Touch panel slave select.
/CSS	O	73	[1]Contrast slave select.
/BSS	O	75	[1]Backlight slave select.
/SS4	O	76	[1]SPI slave select 4. This pin is for future use and should be left unconnected.
/SS5	O	77	[1]SPI slave select 5. This pin is for future use and should be left unconnected.
/SS6	O	78	[1]SPI slave select 6. This pin is for future use and should be left unconnected.
RAMTSTO	O	79	[1]External SRAM test results. A low level indicates external SRAM test failed. A high level indicates external SRAM test passed. Results are only valid if external SRAM test was performed. See input pin RAMTSTI description above.

[1] The I/O pins are only Vcc tolerant and must adhere to the voltage levels depicted in the DC CHARACTERISTICS section.
[2] Input pin is read upon power up, a system reset, or when writing to flash.
[3] Input pin is only read when a flash programming session has been initiated.
[4] Input pin is read upon power up or a system reset.
[5] Internally pulled high. If pin is externally connected, interface it to an open collector output.
[6] The /RESET pin should be held low for a minimum of 140ms after applying VCC.

DC Characteristics

Absolute Maximum Ratings

Voltage on Vcc with respect to ground…….….....	- 0.3 to + 6.5V
Operating temperature……..…..….	-20 to +75ºC
Storage temperature……...……..	-60 to +150ºC
Soldering lead temperature……...…..	210ºC
Soldering 10 Sec.	

DC Characteristics For Vcc = 3.3V

Item	Symbol	Minimum	Typical	Maximum	Unit
CMOS INPUT		**(Vcc tolerant only)**			
Input "High" Voltage	V_{IH}	2.0	-	-	V
Input "Low" Voltage	V_{IH}	-	-	0.8	V
Input Leakage current	I_L	-	-	5	uA
CMOS OUTPUT		**(Vcc tolerant only)**			
Output "High" Voltage	V_{OH}	2.8	-	-	V
Output "Low" Voltage	V_{OL}	-	-	0.2	V
Operating Frequency	F_{opr}	10	16	20	MHz
Pull-up Resistor	R_I	37K	-	202K	Ω

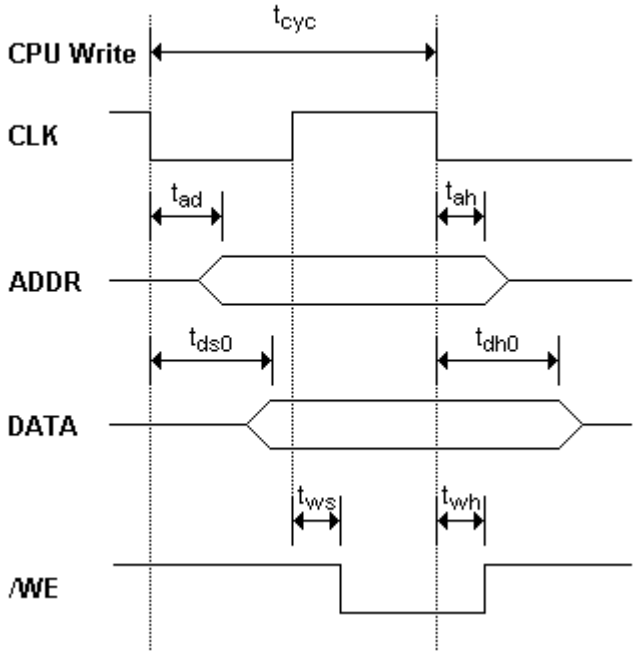
Current

Vcc = 3.3V +/-10%, Ground = 0, Temperature = -20ºC to +75ºC

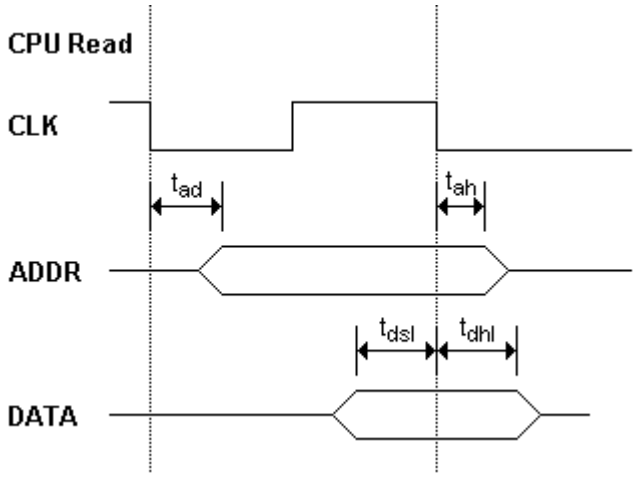
Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Operating Current	I_{CC}	10MHz	-	10	-	mA
Operating Current	I_{CC}	10MHz Reset	-	7	-	mA
Operating Current	I_{CC}	16MHz	-	16	-	mA
Operating Current	I_{CC}	16MHz Reset	-	10	-	mA

CPU Memory Access Timing

The CPU performs both Read and Write accesses to memory. In either case, all timing parameters for CPU accesses are relative to the falling edge of CLK. All input signals are sampled at the falling edge of CLK and all output signals transition after some delay relative to the falling edge of CLK. Input Hold times are the amount of time after the falling edge of CLK that a signal must remain stable. Output Hold times are the minimum delay that the signal will remain stable after the falling edge of CLK.



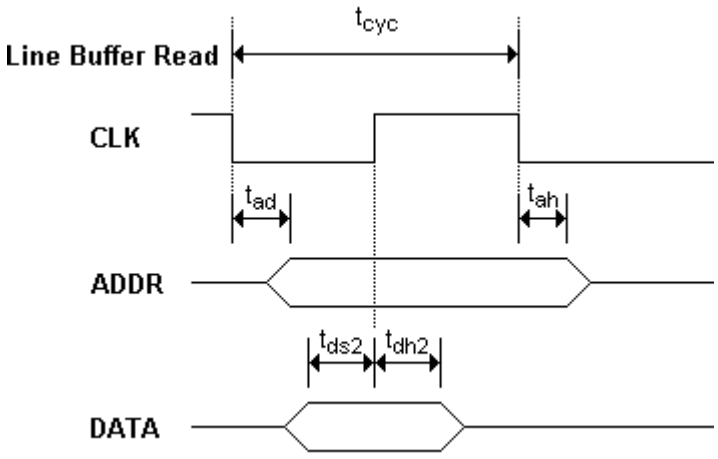
Label	Description	Value	Units
tcyc	Clock Cycle Period	1/Crystal	nS
tad	Address Delay	10	nS
tah	Address Hold	5	nS
tds0	Write Data Delay	10	nS
tdh0	Write Data Hold	5	nS
tws	Write Enable Delay	8	nS
twh	Write Enable Hold	3	nS



Label	Description	Value	Units
tad	Address Delay	10	nS
tah	Address Hold	5	nS
tdsl	Read Data Setup	5	nS
tdhl	Read Data Hold	0	nS

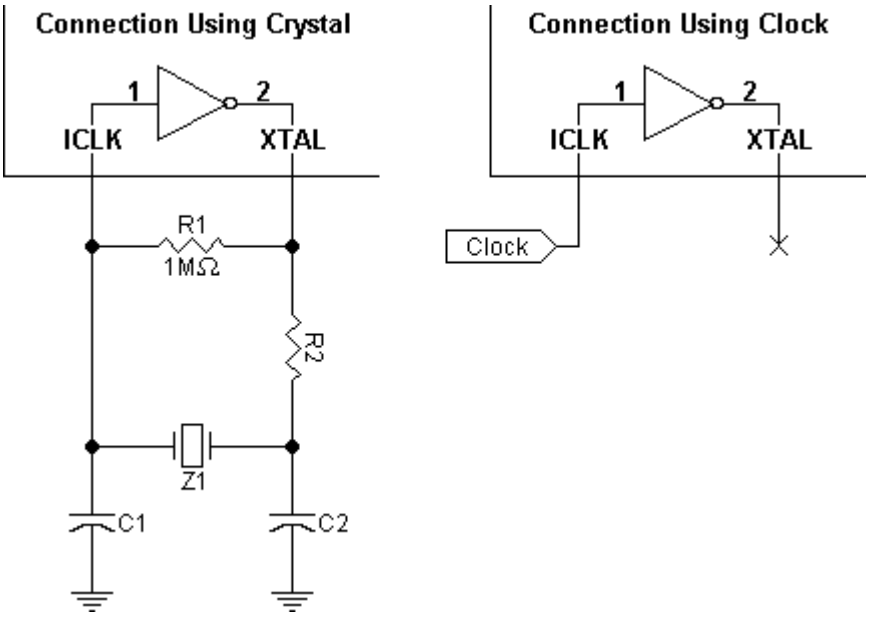
Line Buffer Memory Access Timing

The Line buffer only performs Read accesses to memory. Timing parameters for Line buffer reads are relative to both edges of CLK. All input signals are sampled at the rising edge of CLK and all output signals transition after some delay relative to the falling edge of CLK. Input Hold times are the amount of time after the rising of CLK that a signal must remain stable. Output Hold times are the minimum delay that the signal will remain stable after the falling edge of CLK.



Label	Description	Value	Units
tad	Address Delay	10	nS
tah	Address Hold	5	nS
tds2	Read Data Setup	5	nS
tdh2	Read Data Hold	5	nS

Recommended XTAL Connections



Recommended Crystal Component Selections

CFS1 = [1]Amulet Pin 59
CFS2 = [1]Amulet Pin 60
R1, R2 = Resistor (+/- 10%)
C1, C2 = Capacitor (+/- 10%)

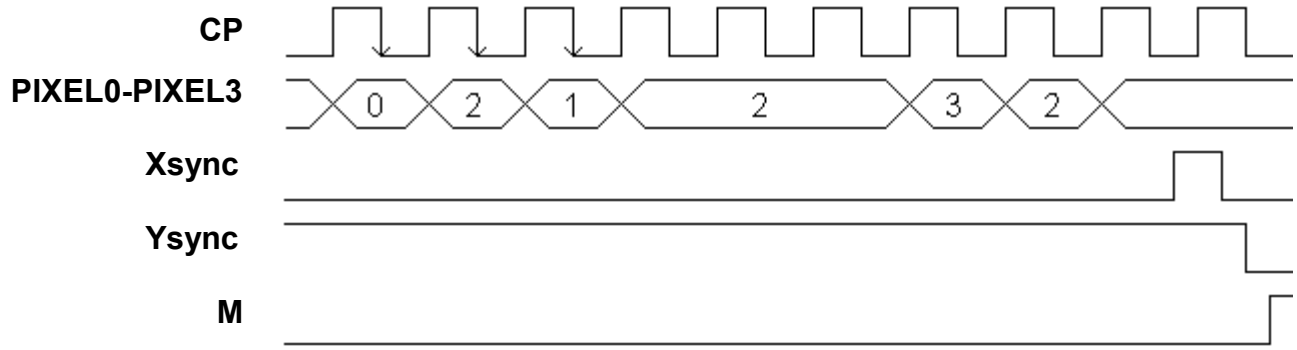
Z1	CFS1	CFS2	R1	R2	C1	C2
10 MHz.	High	High	1 MΩ	1.8 kΩ	18 pF	18 pF
12 MHz.	Low	High	1 MΩ	1.0 kΩ	18 pF	18 pF
16 MHz.	High	Low	1 MΩ	560 Ω	15 pF	15 pF
20 MHz.	Low	Low	1 MΩ	560 Ω	12 pF	12 pF

[1] By default, CFS1 and CFS2 are internally pulled high.

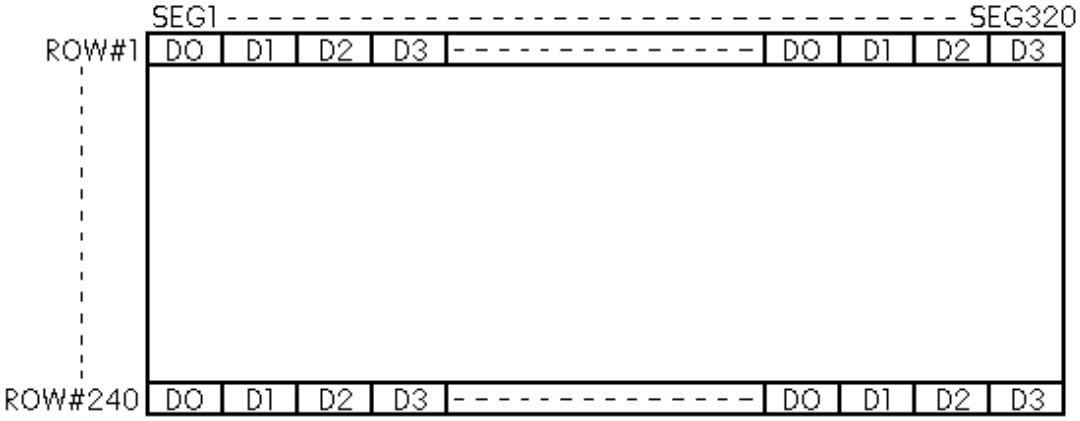
LCD Timing Chart of Signals

The following signal timing assumes:

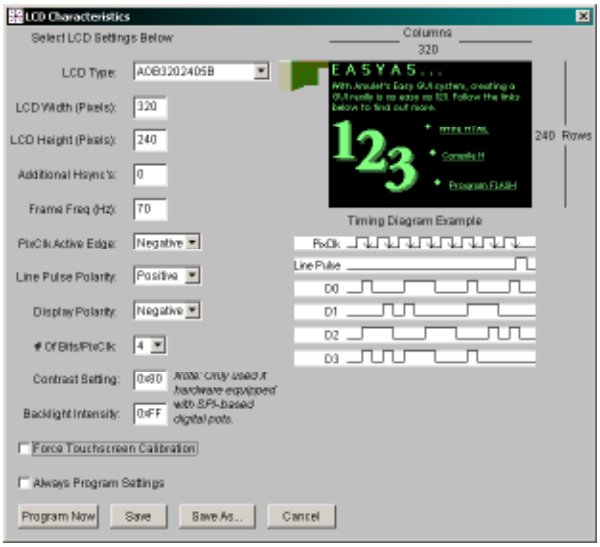
CP = Negative Edge (Adjustable in HTMLCompiler Software).
# of Data Bits = 4 (Adjustable in HTMLCompiler Software).
Xsync = Positive Polarity (Adjustable in HTMLCompiler Software).
MAXBYTE = 4 bytes of data per line and with the following data in the line buffer: 20, 21, 22, 23…



Display Data Pattern



The LCD Characteristics settings within the HTMLCompiler software let you specify a display either by manufacturer or by size (up to full VGA resolution).

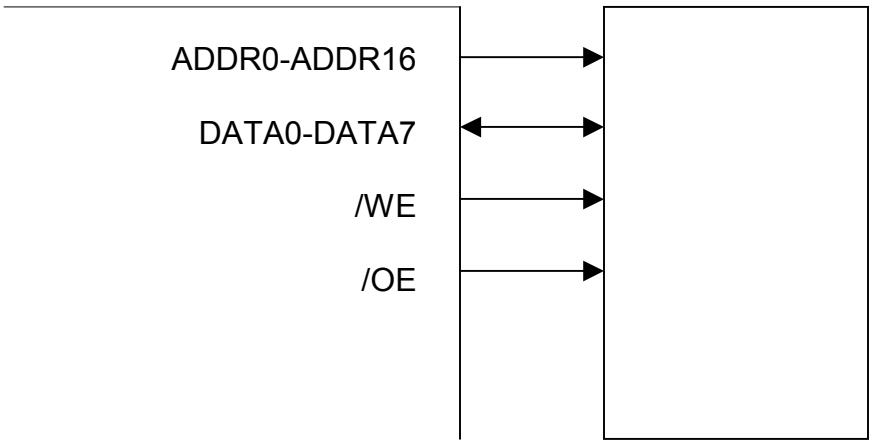


External Asynchronous SRAM

Size and speed are the two most important factors to consider when selecting an external SRAM device. The minimum size of the SRAM must be at least 128K x 8. The minimum speed of the SRAM will be a function of the system clock. Use the following formula to calculate the minimum speed:

1 / (2 * system clock)

For example, a design utilizing a system clock of 16 MHz. would require an SRAM device with a speed grade of at least 31 nS.



Flash SPI Interface

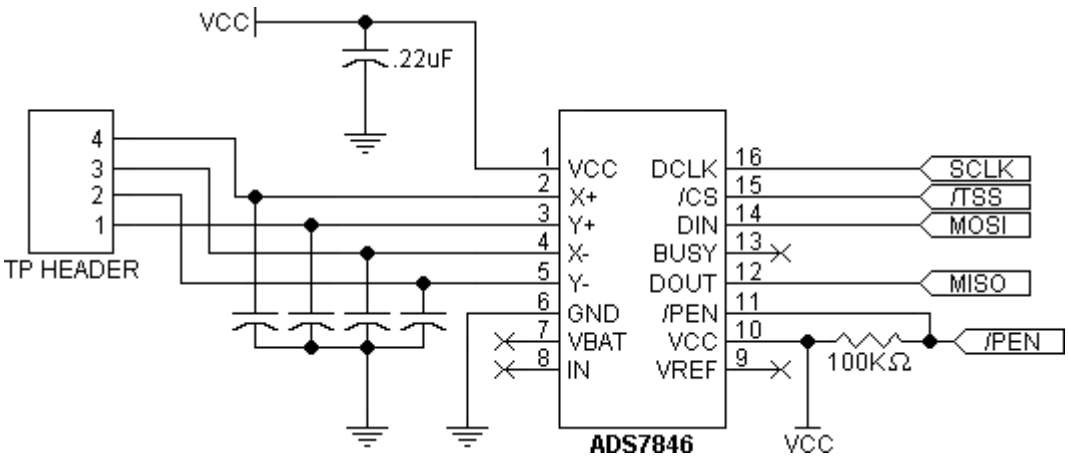
The Amulet supports Atmel DataFlash for storage of uHTML pages. The DataFlash must be organized with a minimum of 512 pages of 264 bytes each, plus one SRAM data buffer of 264 bytes like the AT45DB011B-SC device from Atmel. The DataFlash is enabled through a chip select pin (/CS) and accessed via a three wire serial interface consisting of a serial input (SI), serial output (SO), and a serial clock (SCK). The DataFlash is controlled by instructions from the Amulet. The list of instructions Amulet uses to interface to the DataFlash is as follows:

Main Memory Page Read (52H)
Main Memory Page to Buffer Transfer (53H)
Buffer Write (84H)
Buffer to Main Memory Page Program (83H)
Status Register (57H)

If you decide to use a flash device other than the recommended Atmel DataFlash, then the device must support the DataFlash organization as well as the five instructions above. Please check the Atmel DataFlash datasheet for more information on the device.

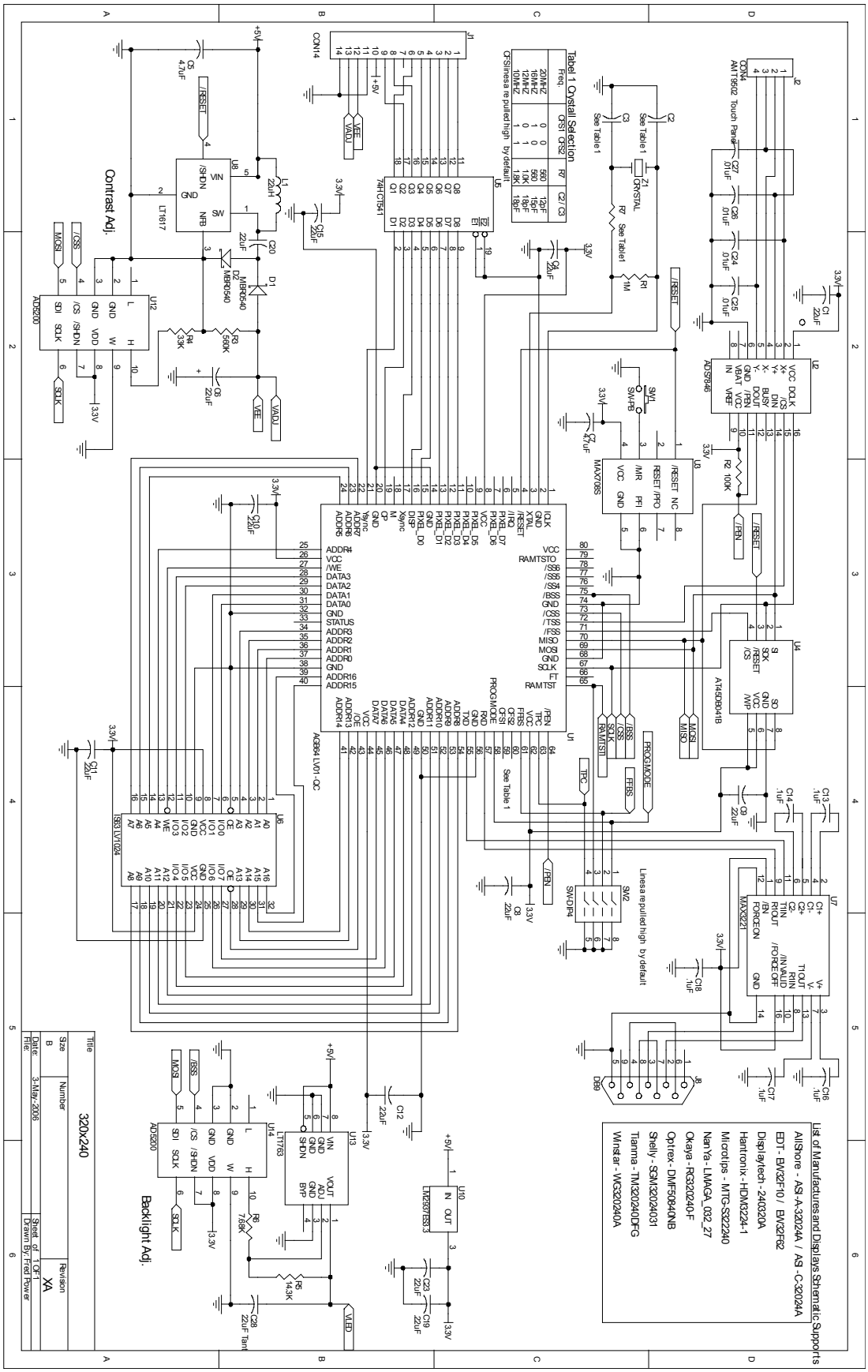
Touch-Screen SPI Interface

Amulet's Easy GUI Browser Chip supports Burr-Brown touch-screen controllers (ADS7843 and ADS7846) for decoding 4-wire resistive touch panels. The touch-screen controller is enabled through a chip select pin (/CS) and accessed via a three-wire serial interface consisting of a serial input (DIN), serial output (DOUT), and a serial clock (DCLK). The firmware to decode a Burr-Brown touch-screen controller is included with the Amulet OS. Below is a sample schematic on how a Burr-Brown touch-screen controller should be interfaced in a typical application requiring the use of a 4-wire resistive touch panel for user input.



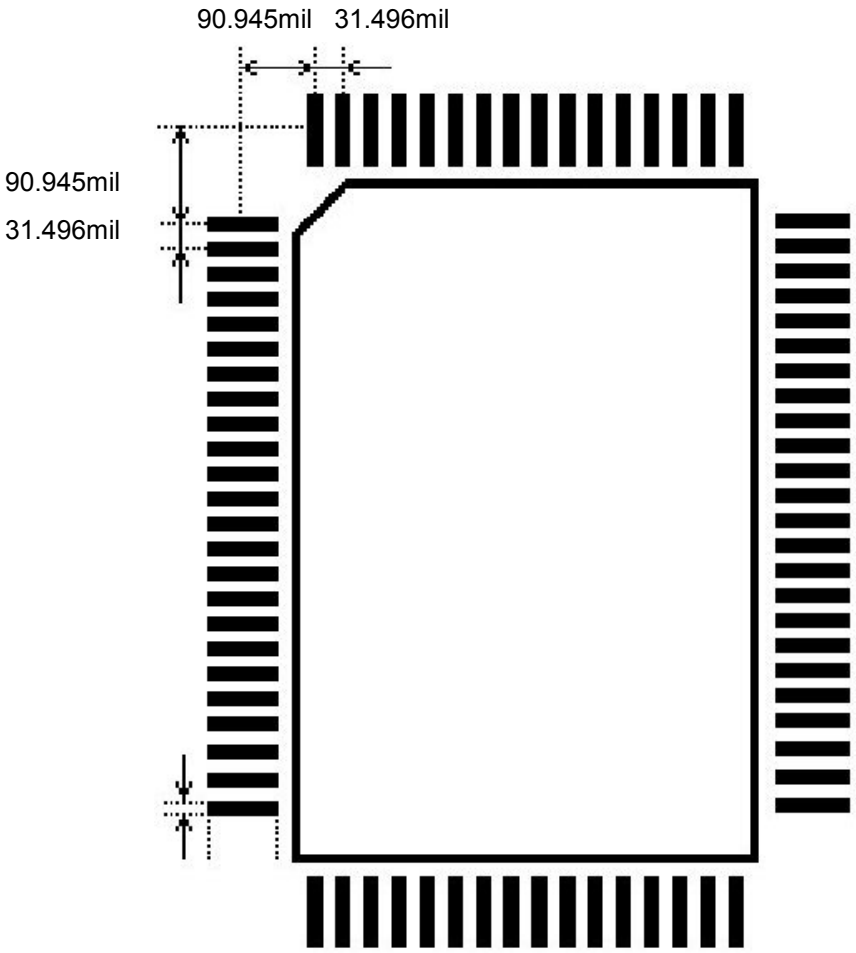
The 4 noise filtering capacitors between the TP HEADER and Burr-Brown device may or may not be needed, but it is recommended you design them in because you can always leave them unpopulated. Whether or not you need the noise filtering capacitors will depend on the size of the touch panel, as well as the environment in which the product will be used. For applications requiring the use of the noise filtering capacitors, .01uF (+/- 10%) capacitors will normally address the problem.

Appendix: Sample Reference Design

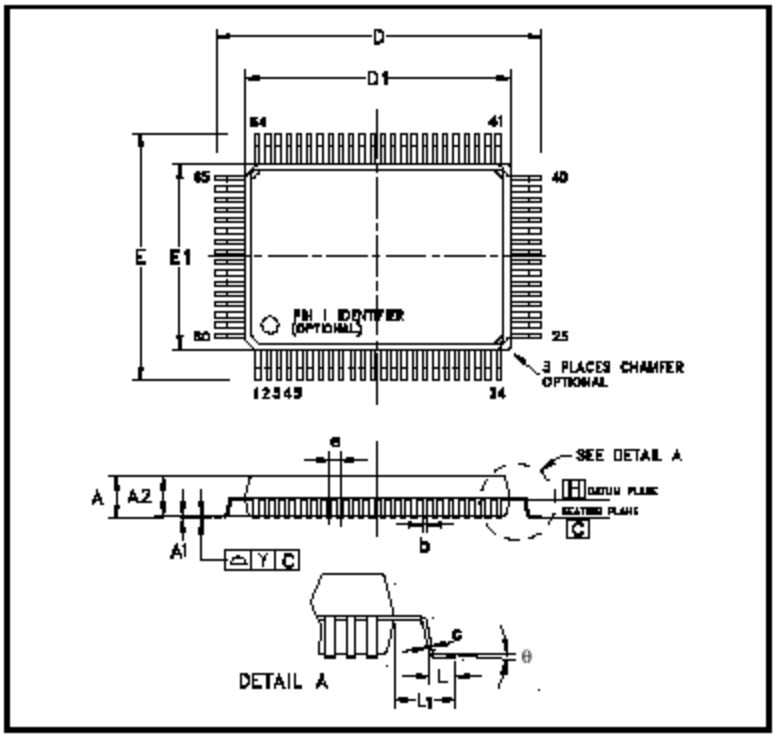


ITEM	QTY	REFERENCE LOCATIONS	PACKAGE	DESCRIPTION	MANUFACTURER	MANUFACTURER PART #
1	1	R1	805	RES, 1M, 1/10W, 5%	AVX	CR21-105J-T
					VISHAY / DALE	CRCW0805-105JRT1
					KOA	RM73B2AT105J
2	1	R2	805	RES, 100K, 1/10W, 5%	AVX	CR21-104J-T
					VISHAY / DALE	CRCW0805-104JRT1
					KOA	RM73B2AT104J
3	1	R3	805	RES, 560K, 1/10W, 5%	AVX	CR21-564J-T
					VISHAY / DALE	CRCW0805-564JRT1
					KOA	RM73B2AT564J
4	1	R4	805	RES, 33K, 1/10W, 5%	AVX	CR21-333J-T
					VISHAY / DALE	CRCW0805-333JRT1
					KOA	RM73B2AT333J
5	1	R5	805	RES, 14.3K, 1/10W, 1%	VISHAY / DALE	CRCW0805-1432FRT1
6	1	R6	805	RES, 7.68K, 1/10W, 1%	VISHAY / DALE	CRCW0805-7681FRT1
7	1	R7	805	See Table on Schematic		
8	10	C1,C4,C8-C12,	1206	CAP, .22uF, 16V, Z5U, 20%	PANASONIC	ECP-U1C224MA5
		C19, C20, C15			SAMSUNG	CL31F224ZAAD
					VITRAMON	VJ12066224MXAMT
					AVX	12065E224MAT2A
9	2	C6, C23	C	CAP, 22uF, 50V, Elect	Nippon	NACE220M50V6.3x6.3TR13
10	1	C5, C7	4X5.5CAN	CAP, 4.7uF, 25V, Electrolitic, 20%	NIC	NACE4R7M35V 4X5.5 TR13
					NICHICON	UWX1E4R7MCR1GB
11	2	C2,C3	1206	See Table on Schematic		
					AVX	12065A200JAT2A
12	5	C13, C14, C16	1206	CAP,.1uF,50V,5%	PANASONIC	ECU-V1H104KBW
		C17, C18			VITRAMON	VJ1206Y10JXAMT
13	4	C24 - C27	1206	CAP, .01uF, 50V	VITRAMON	VJ1206Y103KXAMT
14	1	C28	1206	CAP, 22uF, 10V, 10%, Tant	Vishay	293D226X9010C2T
15	2	D1, D2	SOD-123	Diode, Schottky, .5A, 40V	ON	MBR0540LT1
					SPECIALTY ELECT.	FPCHB04TT
16	1	L1	SMD	22 uH	JW MILLER	PM43-220M
17	1	Z1	CSM-7	CRYSTAL, 16MHz, 20pF	ECS	ECS-160-20-5P
					FOX	FOXSD/160-20/TR-1K
18	1	SW1	6X3.7	Momentary Push Button	PANASONIC	EVG-PPBA25
					C&K	PTS635SL25SM
19	1	SW2	SMD	4-Pos Dip Switch	CTS	219-4LPST
					C&K	SDA04H0SK
20	1	J1	SMD	Con, 14pin ZIF	JST	14FE-ST-VK-N
21	1	J2	SMD	Con, 4pin Header		
22	1	J8		DB-9 Female Connector	SMP	3170-09-F
					ADAM TECH	DE09-SL-24
23	1	U8	SOT-23	LCD Power Supply	LINEAR	LT1617ES5
24	1	U2	SSOP-16	Touch Panel A/D	BURR-BROWN	ADS7846E
25	1	U4	SOIC-8	DATA FLASH, 4MB, 2.7V	ATMEL	AT45DB041B-SC
						AT45DB041B-SI
26	1	U1	PQFP-80	Amulet Controller	AMULET	AGB64LV01-QC
27	1	U6	SOJ-32	SRAM, 128K X 8, 15ns	ISSI	IS63LV1024-15K
28	1	U7	SSOP-16	RS-232 Transceiver	INTERSIL	ICL3221CA
29	1	U3	SOIC-8	Under Voltage Detector	ON-SEMI	MAX708SESA-T
30	1	U13	8-MSOP	Linear Regulator	LINEAR	LT1763CS8
31	1	U10	SOT-223	3.3V Regulator	NATIONAL	LM2937IMP-3.3
32	2	U12, U14	8-MSOP	SPI, 10K POT	ANALOG DEVICES	AD5200BRM10
33	1	U5	SOIC-20	74HCT541, Buffer Driver	ST	74HCT541M1R

Recommended Chip Pad Dimensions



Chip Mechanicals 80 PQFP (14x20x2.7mm)



Symbol	inch
A	134mil MAX
A1	10.0mil MIN
A2	106mil NOM
b	15.0mil NOM
c	7.0mil NOM
D	913mil NOM
E	677mil NOM
e	31.496mil NOM
D1	787mil NOM
E1	551mil NOM
L	35.0mil NOM
L1	63.0mil NOM
Y	4.0mil NOM

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