

NB7NPQ702M

3.3 V USB 3.1 Dual Channel Re-driver

Description

The NB7NPQ702M is a 3.3 V dual channel re-driver for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter-symbol interference (ISI). The NB7NPQ702M compensates for these losses by engaging varying levels of equalization at the input receiver. The output transmitter circuitry provides user selectable de-emphasis settings to create the best eye openings for the outgoing data signals.

The NB7NPQ702M features an intelligent LFPS circuit. This senses the low frequency signals and automatically disables driver de-emphasis to meet full USB 3.1 Gen 1 and USB 3.1 Gen 2 compliances.

After power up, the NB7NPQ702M periodically checks both of the TX output pairs for a receiver connection. When the receiver is detected the RX termination becomes enabled and the NB7NPQ702M is set to perform the re-driver function.

The NB7NPQ702M comes in a small 3 x 3 mm UQFN16 package and is specified to operate across the entire industrial temperature range, -40°C to 85°C.

Features

- 3.3 V ± 5% Power Supply
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic LFPS De-Emphasis Control
- Automatic Receiver Termination Detection
- Integrated Input and Output Termination
- Selectable Equalization and De-Emphasis
- Hot-Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range: -40°C to 85°C
- Small 3 x 3 x 0.5 mm UQFN16 Package
- This is a Pb-Free Device

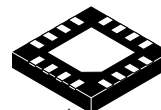
Typical Applications

- USB3.1 Type-C Signal Routing
- Mobile Phone and Tablet
- Computer and Laptop
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.



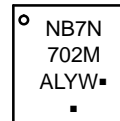
ON Semiconductor®

www.onsemi.com



UQFN16
CASE 523AF

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NB7NPQ702MMUTXG	UQFN16 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7NPQ702M

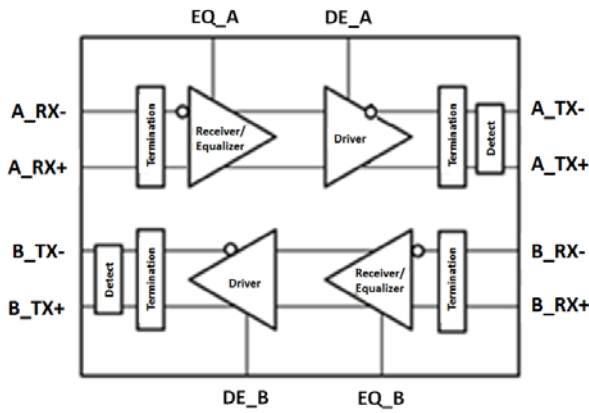


Figure 1. Logic Diagram of NB7NPQ702M

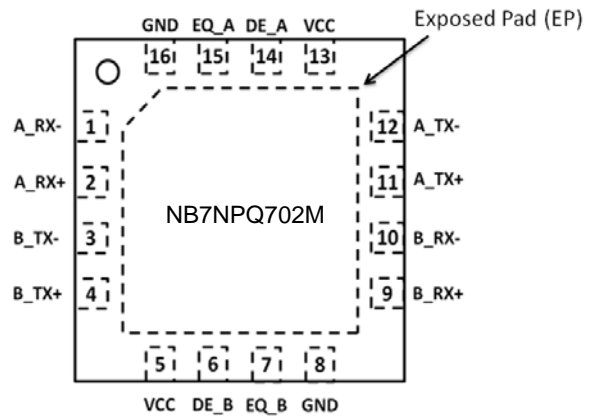


Figure 2. UQFN16 Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	A_RX-	DIFF IN	Channel A Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC-coupled.
2	A_RX+		
3	B_TX-	DIFF OUT	Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC-coupled.
4	B_TX+		
5	VCC	Power	3.3-V power supply. VCC pins must be externally connected to power supply to guarantee proper operation.
6	DE_B	LVC MOS IN	Sets the output de-emphasis gain on Channel B. 3-state input with integrated 250 kΩ pull-up and pull-down resistors.
7	EQ_B	LVC MOS IN	Sets the receiver equalizer gain on Channel B. 3-state input with integrated 250 kΩ pull-up and pull-down resistors.
8	GND	GND	Reference Ground. GND pins must be externally connected to power supply to guarantee proper operation.
9	B_RX+	DIFF IN	Channel B Differential input pair for 5 / 10 Gbps USB signals. Must be externally AC-coupled.
10	B_RX-		
11	A_TX+	DIFF OUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC-coupled.
12	A_TX-		
13	VCC	Power	3.3-V power supply. VCC pins must be externally connected to power supply to guarantee proper operation.
14	DE_A	LVC MOS IN	Sets the output de-emphasis gain on Channel A. 3-state input with integrated 250 kΩ pull-up and pull-down resistors.
15	EQ_A	LVC MOS IN	Sets the receiver equalizer gain on Channel A. 3-state input with integrated 250 kΩ pull-up and pull-down resistors.
16	GND	GND	Reference Ground. GND pins must be externally connected to power supply to guarantee proper operation.
EP	GND	GND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is not electrically connected to the die, but is recommended to be soldered to GND on the PC Board.

NB7NPQ702M

DEVICE CONFIGURATION

Table 2. CONTROL PIN EFFECTS (Typical Values)

Pin	Description	Logic State	Equalization Gain
EQ	Equalization Amount	Low	3 dB
		Mid	6 dB
		High	9 dB
Pin	Description	Logic State	De-emphasis Ratio (Note 1)
DE	De-Emphasis Amount	Low	0 dB
		Mid	-3.5 dB
		High	-5.5 dB

1. dB Decrease = $20 \log * (VTX-DE / VTX-DIFF-PP)$

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	> 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-O @ 0.125 in
Transistor Count		1828
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 3)	V_{CC}	-0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	-0.5	1.89	V
	LVC MOS inputs	-0.5	$V_{CC} + 0.5$	V
Storage Temperature Range, T_{SG}		-65	150	°C
Maximum Junction Temperature, T_J			125	°C
Operating Ambient Temperature Range, T_A		-40	85	°C
Junction-to-Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 4)			34	°C/W
Wave Solder, Pb-Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All voltage values are with respect to the GND terminals.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Min	Nom	Max	Unit
V_{CC}	Main power supply	3.135	3.3	3.465	V
T_A	Operating free-air temperature	-40		+85	°C
C_{AC}	AC coupling capacitor	75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NB7NPQ702M

Table 6. POWER SUPPLY CHARACTERISTICS

Parameter		Test Conditions	Min	Typ (Note 5)	Max	Unit
I _{CC}	Active	Link in U0 with Super Speed Plus data transmission DE = low 0 dB, EQ = low 3 dB		150		mA
	Idle State	Link has some activity, not in U0 DE = mid -3.5 dB, EQ = mid 6dB		105		mA
	U2/U3	Link in U2 or U3 power saving state DE = mid -3.5 dB, EQ = mid 6 dB		12.9		mA
	No USB Connection	No connection state, termination disabled DE = mid -3.5 dB, EQ = mid 6 dB		12.7		mA

5. TYP values use V_{CC} = 3.3 V, T_A = 25°C.

Table 7. LVCMOS CONTROL PIN CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
-----------	--	-----------------	-----	-----	-----	------

3-State LVCMOS Inputs (EQ, DE)

V _{IH}	High-level input voltage		0.8 * V _{CC}		V _{CC}	V
V _{IM}	Mid-level input voltage		0.4 * V _{CC}	V _{CC} / 2	0.6 * V _{CC}	V
V _{IL}	Low-level input voltage		GND		0.2 * V _{CC}	V
V _F	Floating voltage	V _{IN} = High impedance		V _{CC} / 2		V
R _{PU}	Internal pull-up resistance			250		kΩ
R _{PD}	Internal pull-down resistance			250		kΩ
I _{IH}	High-level input current	V _{IN} = 3.465 V			20	μA
I _{IL}	Low-level input current	V _{IN} = GND, V _{CC} = 3.465 V	-20			μA

Table 8. RECEIVER AC/DC CHARACTERISTICS Over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
V _{RX-DIFF-pp}	Input differential voltage swing	AC-coupled, peak-to-peak	250		1200	mV _{PP}
V _{RX-CM}	Common-mode voltage bias in the receiver (DC)			V _{CC} -0.25		V
Z _{RX-DIFF}	Differential input impedance (DC)	Present after an USB device is detected on TX+/TX-	80	100	120	Ω
Z _{RX-CM}	Common-mode input impedance (DC)	Present after an USB device is detected on TX+/TX-	20	25	30	Ω
Z _{RX-HIGH-IMP}	Common-mode input impedance with termination disabled (DC)	Present when no USB device is detected on TX+	25	190		kΩ
V _{TH-LFPS-pp}	Low Frequency Periodic Signaling (LFPS) Detect Threshold	Output voltage is considered squelched below this threshold voltage.			300	mV _{PP}

NB7NPQ702M

Table 9. TRANSMITTER AC/DC CHARACTERISTICS Over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Output differential voltage swing	50 Ω to V_{CC} , DE = Low 0 dB, EQ = Low 3 dB		1000		mV _{PP}
C_{TX}	TX input capacitance to GND	At 2.5 GHz		1.25		pF
$Z_{TX-DIFF}$	Differential output impedance (DC)	Present after an USB device is detected on TX+/TX-	80	100	120	Ω
Z_{TX-CM}	Common-mode output impedance (DC)	Present after an USB device is detected on TX+/TX-	20		30	Ω
I_{TX-SC}	TX short circuit current	TX+ or TX- shorted to GND		60		mA
V_{TX-CM}	Common-mode voltage bias in the transmitter (DC)			$V_{CC}-0.6$	V_{CC}	V
$V_{TX-CM-ACpp}$	AC common-mode peak-to-peak voltage swing in active mode	Within U0 and within LFPS			100	mV _{PP}
$V_{TX-IDLE-DIFF-ACpp}$	Differential voltage swing during electrical idle	Tested with a high-pass filter	0		10	mV _{PP}
$V_{TX-RXDET}$	Voltage change to allow receiver detect	Positive voltage to sense receiver termination			600	mV
t_R, t_F	Output rise, fall time	20% – 80% of differential voltage measured 1 inch from the output pin		45		ps
t_{RF-MM}	Output rise, Fall time mismatch	20% – 80% of differential voltage measured 1 inch from the output pin			5	ps
$t_{diff-LH}, t_{diff-HL}$	Differential propagation delay	De-emphasis = -3.5 dB, propagation delay between 50% level at input and output		150		ps
$t_{idleEntry}, t_{idleExit}$	Idle entry and exit times			30		ns

NB7NPQ702M

Table 10. TIMING AND JITTER CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Unit
-----------	-----------------	-----	-----	-----	------

TIMING

t _{READY}	Time from power applied until RX termination is enabled	Apply 0 V to V _{CC} , connect USB termination to TX±, apply 3.3 V to V _{CC} , and measure when Z _{RX-DIFF} is enabled		10		ms
--------------------	---	--	--	----	--	----

JITTER FOR 5 Gbps

T _{JTX-EYE}	Total jitter (Notes 6, 7)	EQ = Low 3 dB, DE = Low 0 dB		0.038		UI (Note 8)
D _{JTX}	Deterministic jitter (Note 7)			0.018		UI (Note 8)
R _{JTX}	Random jitter (Note 7)			0.003		UI (Note 8)

JITTER FOR 10 Gbps

T _{JTX-EYE}	Total jitter (Notes 6, 7)	EQ = Low 3 dB, DE = Low 0 dB		0.084		UI (Note 8)
D _{JTX}	Deterministic jitter (Note 7)			0.047		UI (Note 8)
R _{JTX}	Random jitter (Note 7)			0.006		UI (Note 8)

6. Includes RJ at 10⁻¹².

7. Measured at the ends of reference channel with a K28.5 pattern, VID = 1000 mVpp, -3.5 dB de-emphasis from source.

8. 5 Gbps, UI = 200 ps for 10 Gbps, UI = 100 ps

NB7NPQ702M

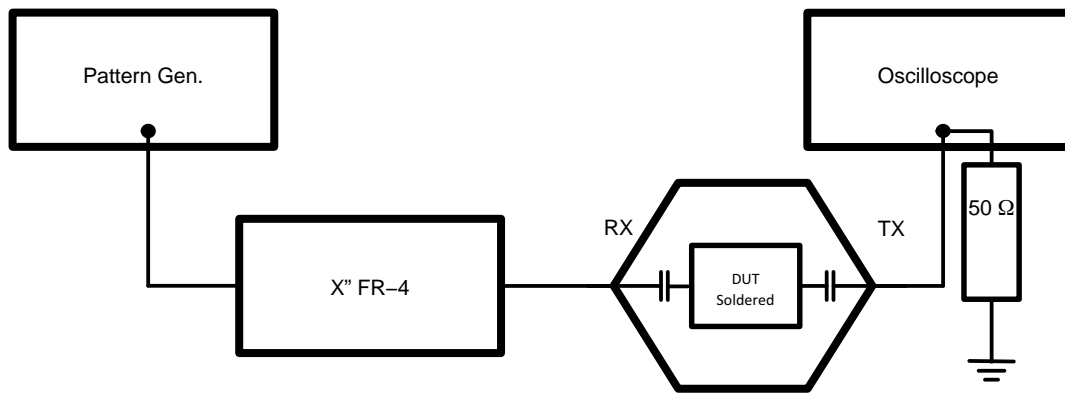


Figure 3. Equalization Measurement Setup

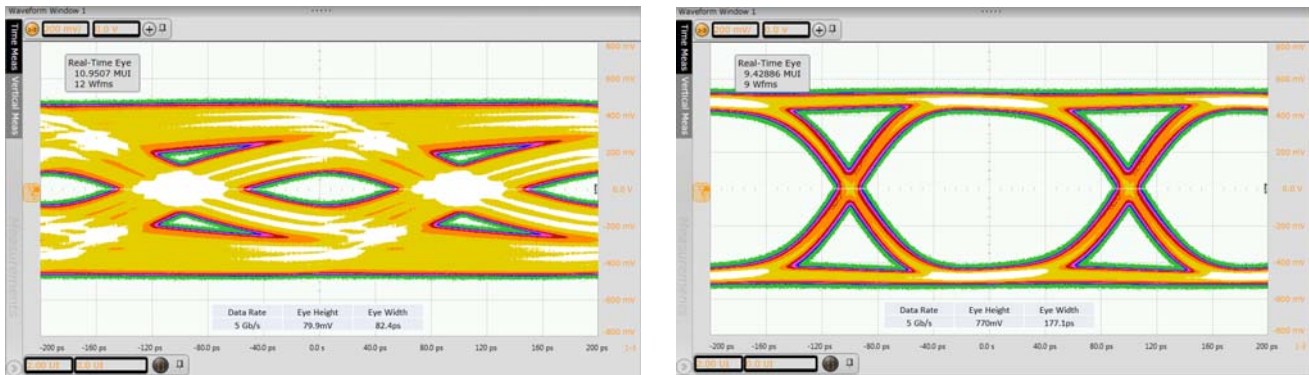


Figure 4. 5 Gbps Signal with 24 inches of FR4 Before Input to NB7NPQ702M and After Using High EQ Setting

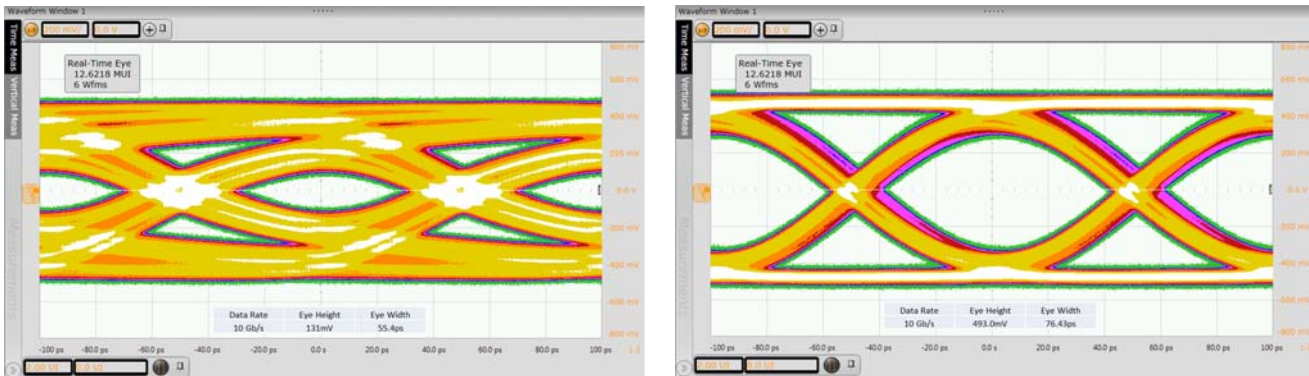


Figure 5. 10 Gbps Signal with 12 inches of FR4 Before Input to NB7NPQ702M and After with EQ Floating (Mid)

NB7NPQ702M

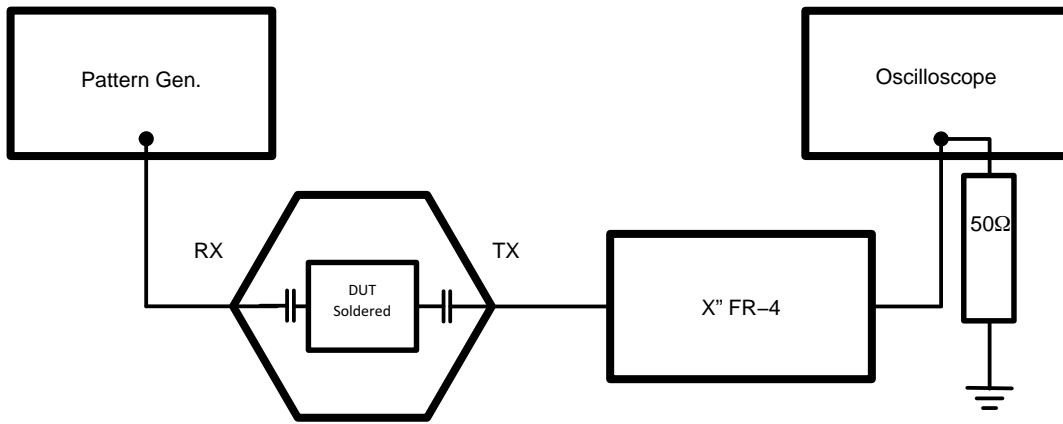


Figure 6. De-Emphasis Measurement Setup

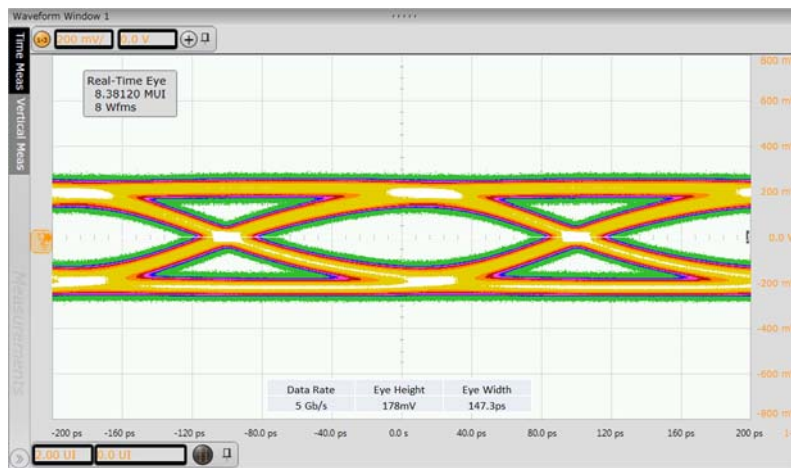


Figure 7. 5 Gbps Signal After 24 inches of FR4 at Output with High DE Setting to NB7NPQ702M

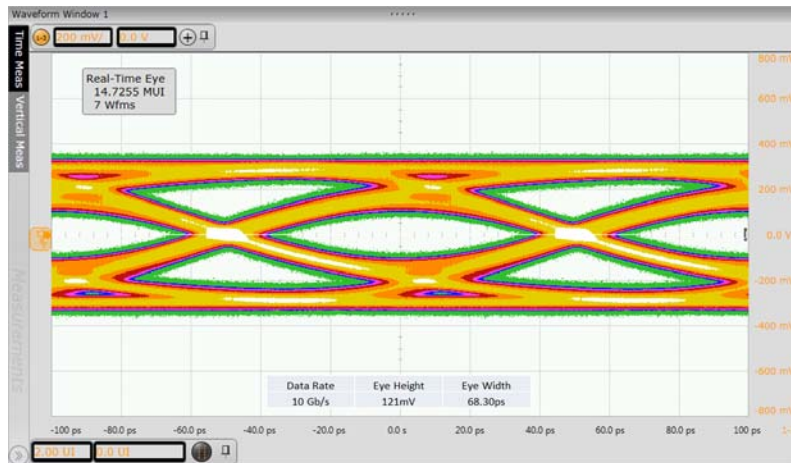


Figure 8. 10 Gbps Signal After 9 inches of FR4 at Output with Mid DE Setting to NB7NPQ702M

PARAMETER MEASUREMENT DIAGRAMS

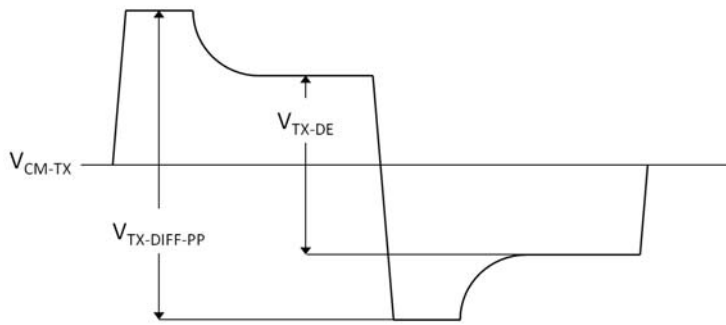


Figure 9. Transmitter Differential Voltage
 $\text{dB Decrease} = 20 \log * (V_{TX-DE} / V_{TX-DIFF-PP})$

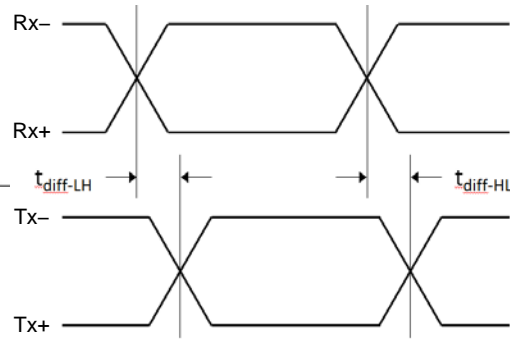


Figure 10. Propagation Delay

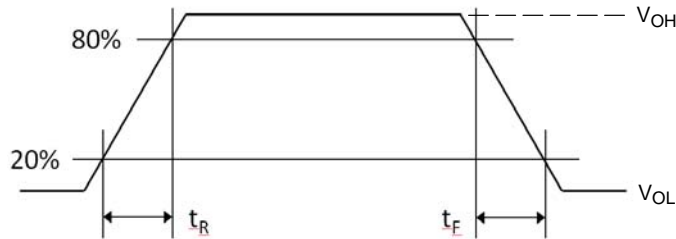


Figure 11. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. When using a real-time oscilloscope to capture this data, *the scope's trigger must be below 0 V when making single-ended measurements.* Although the differential signal is identical to that which is expected by the USB 3.1 system, the AC common mode voltage for LFPS may fall below 0 V during short bursts of switching signal, which is still within the spec's limit.

LFPS Functionality

USB 3.1 links use Low Frequency Periodic Signaling (LFPS) to implement functions like exiting low-power modes, performing warm resets and providing link training

between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

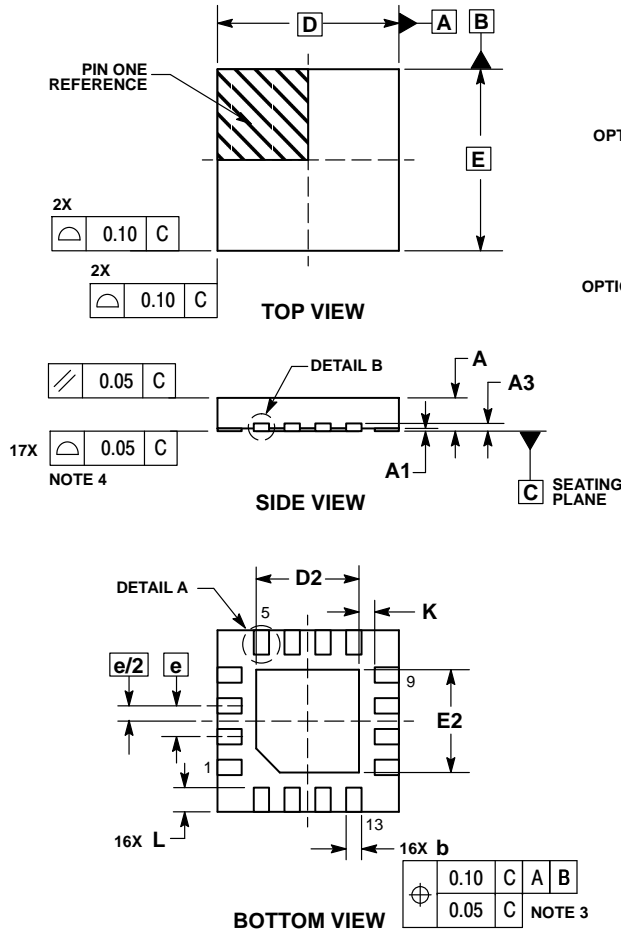
Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB-IF. In order to toggle through these patterns for various tests, the receiver must receive a ping. LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100ns at 20 MHz. In order to pass this signal through NB7NPQ702M, *the duration of the burst must be extended to at least 200 ns.*

NB7NPQ702M

PACKAGE DIMENSIONS

UQFN16 3x3, 0.5P
CASE 523AF
ISSUE B

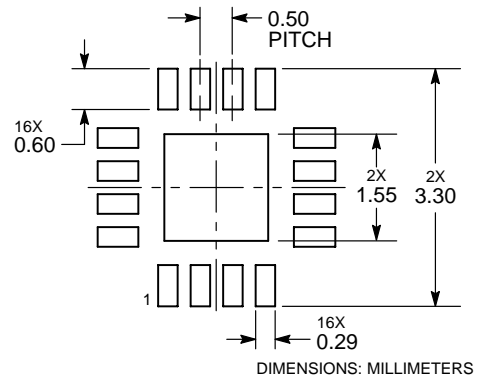


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	—
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative