

# 适用于 EV 和 HEV 的 bq76PL536A-Q1 3 至 6 节锂离子电池监控器和二级保护 IC 单元

## 1 特性

- 符合汽车应用 应用认证
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 2 级：-40°C 至 +105°C 的环境运行温度范围
  - 器件人体模型 (HBM) 分类等级 2
  - 器件充电器件模型 (CDM) 分类等级 C4B
- 3 节至 6 节电池支持，所有化合物
- 热插拔
- 用于数据通信的高速串行外设接口 (SPI)
- 支持垂直堆叠的接口
- 器件之间无需隔离组件
- 高精度模数转换器 (ADC)：
  - ±1mV 典型精度
  - 14 位分辨率，6μs 转换时间
  - 九个 ADC 输入
  - 支持同步测量的专用引脚
- 配置数据存储在有差错校验/纠正 (ECC) 功能的一次性可编程 (OTP) 寄存器中
- 内置比较器 (二级保护器) 支持：
  - 过压和欠压保护
  - 过热保护
  - 可编程的阈值和延迟时间
  - 专用故障信号
- 支持安全超时功能的电芯均衡控制输出
  - 通过外部组件设置均衡电流
- 电源电压范围：7.2V 至 27V 连续电压以及 36V 峰值
- 低功耗：
  - 休眠电流典型值为 12μA，空闲电流典型值为 45μA
- 集成 5V、3mA 高精度 LDO

## 2 应用

- 电动车与混合动力电动车
- 不间断电源系统 (UPS)
- 电动自行车和电动踏板车
- 大型电池系统

## 3 说明

bq76PL536A-Q1 器件是用于三至六节串联锂离子电池的可堆叠电池监控器和保护器。bq76PL536A-Q1 集成了模拟前端 (AFE) 以及精密模数转换器 (ADC)，用于精确测量电池电压。使用一个单独的 ADC 来测量温度。

除测量温度外，该器件还对各通道提供过压和欠压监控保护。通过非易失性存储器来存储用户可编程的保护阈值和延迟时间。一旦超出其中某个阈值，就会输出故障信号。

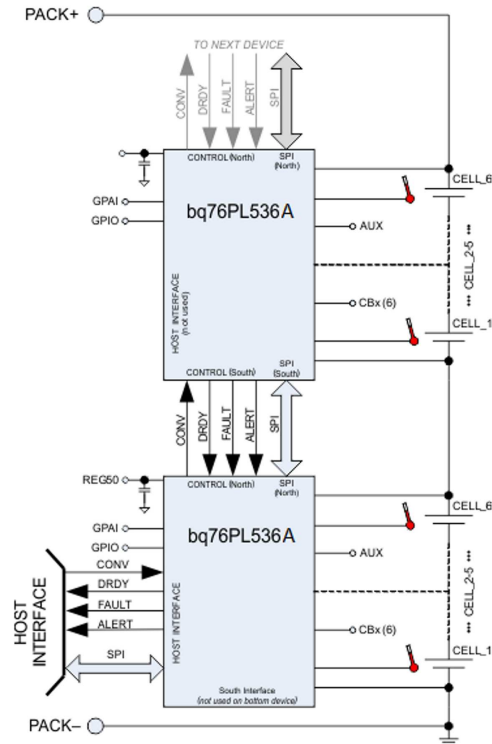
可通过堆叠式 bq76PL536A-Q1 器件来实现对由 192 节电池组成的电池组的支持。所有器件通过高速 SPI 接口进行连接。

### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
bq76PL536A-Q1	HTQFP (64)	10.00mm x 10.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

### 简化的系统连接



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

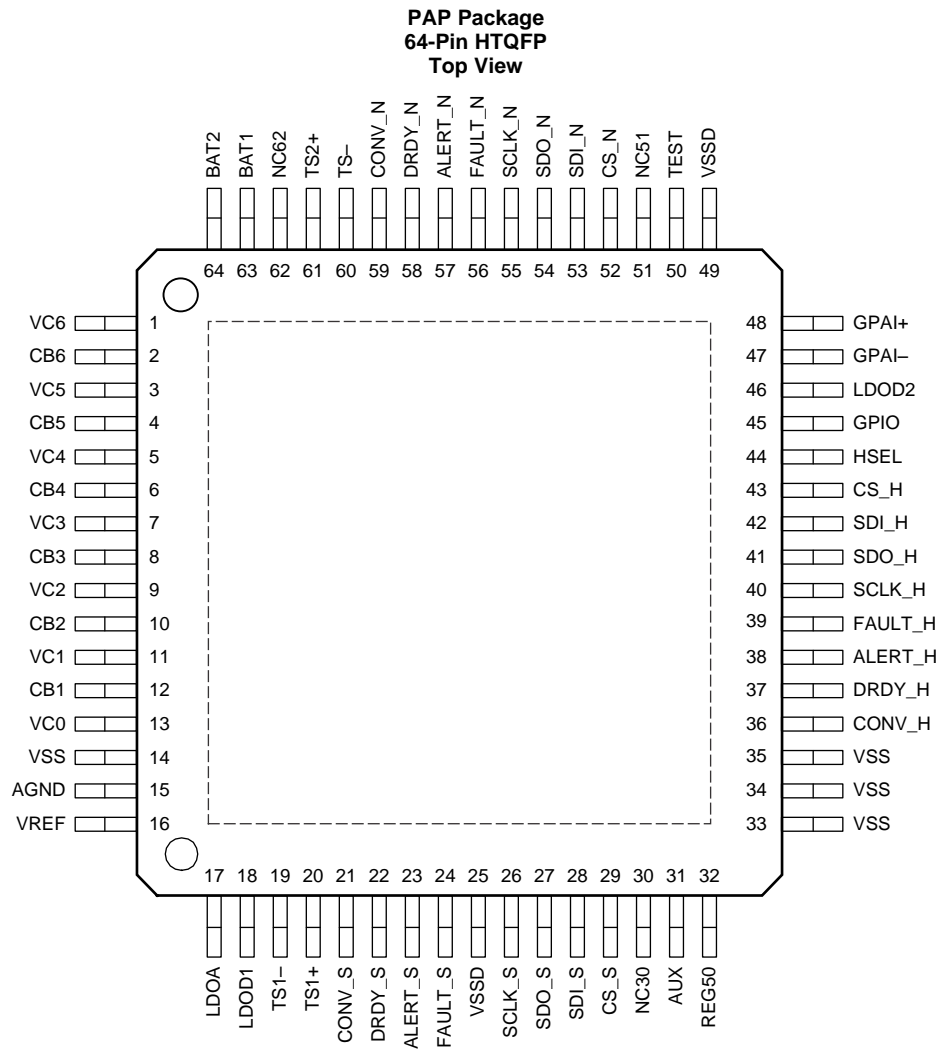
Changes from Original (May 2011) to Revision A	Page
• 已添加 ESD 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分 .....	1
• 已更改 将电源电压范围从“6V 至 30V”更改为“7.2V 至 27V”（特性部分） .....	1
• 已更改 描述 以使其更为简洁 .....	1
• Changed graphic pin 54 alignment and part number .....	4
• Changed AUX description .....	4
• Listed values and removed VCn to VCn-1 row and updated Input Voltage Range and Output Voltage Range information	6
• 已更改 "V <sub>BAT</sub> = 20 V" to "V <sub>BAT</sub> = 22 V" throughout data sheet .....	7
• 已更改 value to 27 V .....	7
• Combined <i>Electrical Characteristics</i> tables into one table .....	8
• 已更改 lower range to 7.2 .....	8
• 已更改 format of bottom two rows and added notes .....	9
• 已删除 MAX value for V <sub>IH</sub> .....	9
• 已删除 MIN value for V <sub>IL</sub> .....	9
• 已更改 120 to 125 .....	9
• 已更改 test condition .....	9
• 已删除 note .....	10
• 已添加 error range .....	10
• 已更改 table values and format .....	10
• 已更改 min value .....	10
• 已更改 test conditions, Min and Nom values, and added note 4 .....	10
• 已更改 the section to be switching characteristics .....	11
• 已更改 units in equations to match unit in corresponding row .....	11
• Moved figure after timing requirements .....	13
• 已更改 name from VC0 to VSS .....	17

**修订历史记录 (接下页)**

• 已添加 TNOM table note .....	25
• 已更改 note wording for LDODx .....	27
• 已更改 warning to caution.....	28
• 已更改 text to a warning .....	29
• 已更改 text to a caution and added SLEEP State in text .....	34
• 已更改 TS1(2) to TS1:TS2 throughout document .....	34
• 已更改 SHADOW_LOAD to REFRESH .....	37
• 已更改 paragraph text and added cross-reference to section .....	42
• 已更改 definition of 1 value .....	46
• 已更改 text to Caution format. ....	47
• 已更改 anti-aliasing VCn input to VC6-VC1 .....	52
• 已更改 "SN76PL536-Q1" to "bq76PL536A-Q1" in <i>Power Supply Decoupling</i> .....	59
• 已更改 note wording for LDODx .....	59

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## 5 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
AGND	15	AI	Internal analog $V_{REF}$ (-)
ALERT_H	38	O	Host-to-device interface – ALERT condition detected in this or higher (North) device
ALERT_N	57	I	Current-mode input indicating a system status change from the next-higher bq76PL536A-Q1
ALERT_S	23	OD	Current-mode output indicating a system status change to the next lower bq76PL536A-Q1
AUX	31	O	Switched current-limited output from REG50
BAT1	63	P	Power-supply voltage, connect to most-positive cell +, tie to BAT2 on PCB
BAT2	64	P	Power-supply voltage, connect to most-positive cell +, tie to BAT1 on PCB
CB1	12	O	Cell-balance control output 1
CB2	10	O	Cell-balance control output 2
CB3	8	O	Cell-balance control output 3
CB4	6	O	Cell-balance control output 4
CB5	4	O	Cell-balance control output 5
CB6	2	O	Cell-balance control output 6
CONV_H	36	I	Host-to-device interface – initiates a synchronous conversion. Pin has 250-nA internal sink to VSS.

**Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
CONV_N	59	OD	Current-mode output to the next-higher bq76PL536A-Q1 to initiate a conversion
CONV_S	21	I	Input from the adjacent lower bq76PL536A-Q1 to initiate a conversion
CS_H	43	I	Host-to-device interface – active-low chip select from host. Internal 100-k $\Omega$ pull-up resistor
CS_N	52	OD	Current-mode output used to select the next-higher bq76PL536A-Q1 for SPI communication
CS_S	29	I	Current-mode input SPI chip-select (slave-select) from the next-lower bq76PL536A-Q1
DRDY_H	37	O	Host-to-device interface – conversion complete, data-ready indication
DRDY_N	58	I	Current-mode input indicating conversion data is ready from next-higher bq76PL536A-Q1
DRDY_S	22	OD	Current-mode output indicating conversion data is ready to the next lower bq76PL536A-Q1
FAULT_H	39	O	Host-to-device interface – FAULT condition detected in this or higher (North) device
FAULT_N	56	I	Current-mode input indicating a system status change from the next-higher bq76PL536A-Q1
FAULT_S	24	OD	Current-mode output
GPAI+	48	AI	General-purpose (differential) analog input, connect to VSS if unused.
GPAI–	47	AI	General-purpose (differential) analog input, connect to VSS if unused.
GPIO	45	IOD	Digital open-drain I/O. A 10-k $\Omega$ to 2-M $\Omega$ pull-up is recommended.
HSEL	44	I	Host interface enable, 0 = enable, 1 = disable
LDOA	17	P	Internal analog 5-V LDO bypass connection, requires 2.2- $\mu$ F ceramic capacitor for stability
LDOD1	18	P	Internal digital 5-V LDO bypass connection 1, requires 2.2- $\mu$ F ceramic capacitor for stability. This pin is tied internally to LDOD2. This pin should be tied to LDOD2 externally.
LDOD2	46	P	Internal digital 5-V LDO bypass connection 2, requires 2.2- $\mu$ F ceramic capacitor for stability. This pin is tied internally to LDOD1. This pin should be tied to LDOD1 externally.
NC30	30	—	No connection
NC51	51	—	No connection
NC62	62	—	No connection
REG50	32	P	5-V user LDO output, requires 2.2- $\mu$ F ceramic capacitor for stability
SCLK_H	40	I	Host-to-device interface – SPI clock from host
SCLK_N	55	OD	Current-mode output SPI clock to the next-higher bq76PL536A-Q1
SCLK_S	26	I	Current-mode input SPI clock from the next-lower bq76PL536A-Q1
SDI_H	42	I	Host-to-device interface – data from host to device (host MOSI signal)
SDI_N	53	OD	Current-mode output for SPI data to the next-higher bq76PL536A-Q1
SDI_S	28	I	Current-mode input for SPI data from the next-lower bq76PL536A-Q1
SDO_H	41	O	Host-to-device interface – data from device to host (host MISO signal), 3-state pin, 250-nA internal pull-up
SDO_N	54	I	Current-mode input for SPI data from the next-lower bq76PL536A-Q1
SDO_S	27	OD	Current-mode output for SPI data to the next-lower bq76PL536A-Q1
TEST	50	I	Factory test pin. Connect to VSS in user circuitry. This pin includes an approximately 100-k $\Omega$ internal pull-down
TS1+	20	AI	Differential temperature sensor input
TS1–	19	AI	Differential temperature sensor input
TS2+	61	AI	Differential temperature sensor input
TS2–	60	AI	Differential temperature sensor input
VC0	13	AI	Sense-voltage input terminal for negative terminal of first cell (VSS)
VC1	11	AI	Sense voltage input terminal for positive terminal of the first cell
VC2	9	AI	Sense voltage input terminal for the positive terminal of the second cell
VC3	7	AI	Sense voltage input terminal for the positive terminal of the third cell
VC4	5	AI	Sense voltage input terminal for the positive terminal of the fourth cell
VC5	3	AI	Sense voltage input terminal for the positive terminal of the fifth cell
VC6	1	AI	Sense voltage input terminal for the positive terminal of the sixth cell

**Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VREF	16	P	Internal analog voltage reference (+), requires 10- $\mu$ F, low-ESR ceramic capacitor to AGND for stability
VSS	14, 33, 34, 35	P	V <sub>SS</sub>
VSSD	25, 49	P	V <sub>SS</sub>
Thermal pad	—	—	Thermal pad on bottom of PowerPAD™ package; this must be soldered to similar-size copper area on PCB and connected to VSS, to meet stated specifications herein. Provides heat-sinking to part.

(1) Key: I = digital input, AI = analog input, O = digital output, OD = open-drain output, T = 3-state output, P = power.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>MAX</sub>	Supply voltage	BAT1, BAT2 <sup>(2)</sup>	-0.3	36	V
V <sub>IN</sub>	Input voltage	VC1, VC2, VC3, VC4, VC5, VC6	-0.3	36	V
		VC0	-0.3	2	
		TS1+, TS1-, TS2+, TS2-	-0.3	6	
		GPAI	-0.3	6	
		GPIO	-0.3	V <sub>REG50</sub> + 0.3	
		DRDY_N, SDO_N, FAULT_N, ALERT_N	V <sub>BAT</sub> - 1	V <sub>BAT</sub> + 2	
		CONV_H, SDI_H, SCLK_H, CS_H	-0.3	6	
V <sub>O</sub>	Output voltage	CONV_S, SDI_S, SCLK_S, CS_S	-2	1	V
		CONV_N, SDI_N, SCLK_N, CS_N	-0.3	36	
		SDO_H, FAULT_H, ALERT_H, DRDY_H	-0.3	6	
		DRDY_S, SDO_S, FAULT_S, ALERT_S	-0.3	5	
		GPIO	-0.3	V <sub>REG50</sub> + 0.3	
		CB1...CB6 (CBREF = 0x00)	-0.3	36	
		REG50, AUX	-0.3	6	
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to VSS of this device, except where otherwise noted.

### 6.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins (1, 16, 33, and 48)		±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{\text{BAT}}$	Supply voltage	BAT	7.2		27	V
$V_I$	Input voltage	$\text{VCn}-\text{VC}(n-1)^{(1)}$	1		4.5	V
		GPAI	0		2.5	
		GPIO	0		$V_{\text{REG50}}$	
		$\text{CBn}^{(1)}$	$\text{VC}(n-1)$		$\text{VCn}$	
		TS1+, TS1-, TS2+, TS2-	0		$V_{\text{REG50}}/2$	
		Non-top IC in stack: DRDY_N, SDO_N, FAULT_N, ALERT_N			BAT + 1	
		Top IC in stack: DRDY_N, SDO_N, FAULT_N, ALERT_N			BAT	
		Non-bottom IC in stack: CONV_S, SDI_S, SCLK_S, CS_S			-1	
$V_O$	Output voltage	Bottom IC in stack: CONV_S, SDI_S, SCLK_S, CS_S			VSS	V
		Non-bottom IC in stack : CONV_N, SDI_N, SCLK_N, CS_N			1	
		Bottom IC in stack: CONV_N, SDI_N, SCLK_N, CS_N			VSS	
		Non-top IC in stack: DRDY_S, SDO_S, FAULT_S, ALERT_S			BAT - 1	
$C_{\text{REG50}}$	External capacitor	REG50 pin	2.2			$\mu\text{F}$
		$C_{\text{VREF}}$	External capacitor	$V_{\text{REF}}$ pin	9.2	10
$C_{\text{LDO}}$	External capacitor	LDOx pin	2.2		3.3	$\mu\text{F}$
$T_{\text{OPR}}$	Operating temperature <sup>(2)</sup>		-40		105	$^\circ\text{C}$

(1)  $n = 1$  to  $6$

(2) Device specifications stated within this range.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq76PL536A-Q1	UNIT
		PAP (HTQFP)	
		64 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	24.6	$^\circ\text{C}/\text{W}$
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	10	$^\circ\text{C}/\text{W}$
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	8.1	$^\circ\text{C}/\text{W}$
$\Psi_{\text{JT}}$	Junction-to-top characterization parameter	0.3	$^\circ\text{C}/\text{W}$
$\Psi_{\text{JB}}$	Junction-to-board characterization parameter	8	$^\circ\text{C}/\text{W}$
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	0.4	$^\circ\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$I_{\text{CCSLEEP}}$	Supply current	No load at REG50, SCLK_N, SDI_N, SDO_N, FAULT_N, CONV_N, DRDY_S, ALERT_N, TSx, AUX, or CBx; CB_CTRL = 0; CBT_CONTROL = 0; CONV_H = 0 (not converting), IO_CONTROL[SLEEP] = 1		12	22	$\mu\text{A}$
$I_{\text{CCPROTECT}}$	Supply current	No load at REG50, SCLK_N, SDI_N, SDO_N, FAULT_N, CONV_N, DRDY_S, ALERT_N, TSx, AUX, or CBx; CB_CTRL = 0; CBT_CONTROL = 0; CONV_H = 0 (not converting), IO_CONTROL[SLEEP] = 0		45	60	$\mu\text{A}$
$I_{\text{CCBALANCE}}$	Supply current	No load at REG50, SCLK_N, SDI_N, SDO_N, FAULT_N, CONV_N, DRDY_S, ALERT_N, TSx, AUX, or CBx; No DC load at CBx; CB_CTRL $\neq$ 0; CBT_CONTROL $\neq$ 0; CONV_H = 0 (not converting), IO_CONTROL[SLEEP] = 0		46	60	$\mu\text{A}$
$I_{\text{CCCONVERT}}$	Supply current	No load at REG50, SCLK_N, SDI_N, SDO_N, FAULT_N, CONV_N, DRDY_S, ALERT_N, TSx or CBx; CONV_S = 1 (conversion active), IO_CONTROL[SLEEP] = 0		10.5	15	mA
$I_{\text{CC TSD}}$	Supply current	Thermal shutdown activated; ALERT_STATUS[TSD] = 1		1.6		mA
<b>REG50, INTEGRATED 5-V LDO</b>						
$V_{\text{REG50}}$	Output voltage	$I_{\text{REG50OUT}} \leq 0.5\text{ mA}$ , $C = 2.2\text{ }\mu\text{F}$ to $22\text{ }\mu\text{F}$	4.9	5	5.1	V
$\Delta V_{\text{REG50LINE}}$	Line regulation	$7.2\text{ V} \leq \text{BAT} \leq 27\text{ V}$ , $I_{\text{REG50OUT}} = 2\text{ mA}$		10	25	mV
$\Delta V_{\text{REG50LOAD}}$	Load regulation	$0.2\text{ mA} \leq I_{\text{REG50OUT}} \leq 2\text{ mA}$			15	mV
		$0.2\text{ mA} \leq I_{\text{REG50OUT}} \leq 5\text{ mA}$			25	
$I_{\text{REG50MAX}}$	Current limit		12	25	35	mA
$I_{\text{AUXMAX}}$	Maximum load	AUX pin			5	mA
$R_{\text{AUX}}$	AUX output	$I = 1\text{ mA}$ , max. capacitance = $V_{\text{REG50}}$ Capacitor: $C_{\text{VAUX}} \leq C_{\text{VREG50}} / 10$			50	$\Omega$
<b>LEVEL SHIFT INTERFACE</b>						
$I_{\text{NTX1}}$	North 1 transmitter current	SCLK_N, CS_N, SDI_N, CONV_N	1000	1350	1800	$\mu\text{A}$
$I_{\text{NTX0}}$	North 0 transmitter current	CS_N, CONV_N			1	$\mu\text{A}$
$I_{\text{NTX0A}}$	North 0 transmitter current	SCLK_N, SDI_N (BASE device CS_H = 1)			1	$\mu\text{A}$
$I_{\text{NTX0B}}$	North 0 transmitter current	SCLK_N, SDI_N (BASE device CS_H = 0)	50	75	110	$\mu\text{A}$
$I_{\text{SRX}}$	South 1 receiver threshold	SCLK_S, CS_S, SDI_S, CONV_S	430	550	680	$\mu\text{A}$
$I_{\text{SRXH}}$	South receiver hysteresis	SCLK_S, CS_S, SDI_S, CONV_S		100	200	$\mu\text{A}$
$I_{\text{STX1}}$	South 1 transmitter current	ALERT_N, FAULT_S, DRDY_S	800	1100	1400	$\mu\text{A}$
$I_{\text{STX0}}$	South 0 transmitter current	ALERT_S, FAULT_S, DRDY_S			1	$\mu\text{A}$
$I_{\text{STX0A}}$	South 0 transmitter current	SDO_S (BASE device CS_H = 1)			1	$\mu\text{A}$
$I_{\text{STX0B}}$	South 0 transmitter current	SDO_S (BASE device CS_H = 0)	1	4	7	$\mu\text{A}$
$I_{\text{NRX}}$	North 1 receiver threshold	SDO_N, ALERT_N, FAULT_N, DRDY_N	420	580	720	$\mu\text{A}$
$I_{\text{NRXH}}$	North receiver hysteresis	SDO_N, ALERT_N, FAULT_N, DRDY_N	50	100	200	$\mu\text{A}$
$C_{\text{IN}}$	Input capacitance			15		pF



## Electrical Characteristics (接下页)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>HOST INTERFACE</b>						
$V_{\text{OH}}$	Logic-level output voltage, high; SDO_H, FAULT_H, ALERT_H, DRDY $C_L = 20\text{ pF}$ , $I_{\text{OH}} < 5\text{ mA}^{(1)}$	4.5		$V_{\text{LDOD}}$	V	
$V_{\text{OL}}$	Logic-level output voltage, low; SDO_H, FAULT_H, ALERT_H, DRDY $C_L = 20\text{ pF}$ , $I_{\text{OL}} < 5\text{ mA}^{(1)}$	VSS		0.5	V	
$V_{\text{IH}}$	Logic-level input voltage, high; SCLK_H, SDI_H, CS_H, CONV	2			V	
$V_{\text{IL}}$	Logic-level input voltage, low; SCLK_H, SDI_H, CS_H, CONV			0.8	V	
$C_{\text{IN}}$	Input Capacitance CONV_H <sup>(2)</sup> Input Capacitance CS_H <sup>(3)</sup> Input Capacitance SCLK_H, SDI_H		5		pF	
$I_{\text{LKG}}$	Input leakage current CONV_H <sup>(2)</sup> Input leakage current CS_H <sup>(3)</sup> Input leakage current SCLK_H, SDI_H			1	$\mu\text{A}$	
<b>GENERAL PURPOSE INPUT/OUTPUT (GPIO)</b>						
$V_{\text{IH}}$	Logic-level input voltage, high $V_{\text{in}} \leq V_{\text{REG50}}$	2			V	
$V_{\text{IL}}$	Logic-level input voltage, low			0.8	V	
$V_{\text{OH}}$	Output high-voltage pull-up voltage Supplied by external approximately 100-k $\Omega$ resistor			$V_{\text{REG50}}$	V	
$V_{\text{OL}}$	Logic-level output voltage, low $I_{\text{OL}} = 1\text{ mA}$	0.3			V	
$C_{\text{IN}}$	Input capacitance(1)		5		pF	
$I_{\text{LKG}}$	Input leakage current			1	$\mu\text{A}$	
<b>CELL BALANCING CONTROL OUTPUT (CBx)</b>						
$\text{CB}_z$	Output impedance $1\text{ V} < V_{\text{CELL}} < 5\text{ V}$	80	100	125	k $\Omega$	
$V_{\text{RANGE}}$	Output V	$V_{\text{Cn-1}}$		$V_{\text{Cn}}$	V	
<b>ADC COMMON SPECIFICATIONS</b>						
$t_{\text{CONV\_START}}$	CONV high to conversion start <sup>(4)</sup> <sup>(5)</sup>	ADC_CONTROL[ADC_ON] = 1	5.4	6	6.6	$\mu\text{s}$
		ADC_CONTROL[ADC_ON] = 0		500		$\mu\text{s}$
$t_{\text{CONV}}$	Conversion time per selected channel <sup>(6)</sup>	ADC_CONTROL[ADC_ON] = 1	5.4	6	6.6	$\mu\text{s}$
$I_{\text{LKG}}$	Input leakage current	Not converting, measured differentially		<10	100	nA
<b>V<sub>Cn</sub> (CELL) INPUTS<sup>(7)</sup></b>						
$V_{\text{IN}}$	Input voltage range <sup>(8)</sup>	$V_{\text{Cn}} - V_{\text{Cn-1}}$ , where $n = 1$ to $6$	0		6	V
$V_{\text{RES}}$	Voltage resolution <sup>(9)</sup>	14 bits		~378		$\mu\text{V}$
$V_{\text{ACC}}$	Voltage accuracy, total error, $V_{\text{IN}} = V_{\text{Cn}}$ to $V_{\text{Cn-1}}$	$-10^\circ\text{C} \leq T_A \leq 50^\circ\text{C}$ , $1.2\text{ V} < V_{\text{IN}} < 4.5\text{ V}$	-2.5	$\pm 1$	2.5	mV
		$-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ , $1.2\text{ V} < V_{\text{IN}} < 4.5\text{ V}$	-5		5	
$R_{\text{IN}}$	Effective input resistance	Converting		2		M $\Omega$
$C_{\text{IN}}$	Input capacitance	Converting		1		pF
$E_{\text{N}}$	Noise	$V_{\text{IN}} = 3\text{ V}$			250	$\mu\text{V}_{\text{RMS}}$

(1) Total simultaneous current drawn from all pins is limited by LDOD current to  $\leq 10\text{ mA}$ .

(2) Pin has 250-nA internal sink to VSS.

(3) Pin has 100-k $\Omega$  internal pull-up resistor.

(4) If ADC\_CONTROL[ADC\_ON] = 0, add 500  $\mu\text{s}$  to conversion time to allow ADC subsystem to stabilize. This is self-timed by the part.

(5) Additional 50 ms (POR) is required before first conversion after a) initial cell connection; or b)  $V_{\text{BAT}}$  falls below  $V_{\text{POR}}$ .

(6) Plus  $t_{\text{CONV\_START}}$ , that is, if device is programmed for six channel conversions, total time is approximately  $6 \times 6 + 6 = 42\ \mu\text{s}$ .

(7) FUNCTION\_CONFIG[] = 01xxxx00b for all test conditions (6- $\mu\text{s}$  conversion time selected).

(8) 0 V may not lie within the range of measured values due to offset voltage limit and device calibration.

(9) See text for specific conversion formula.

## Electrical Characteristics (接下页)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b><math>V_{\text{BAT}}</math> (<math>V_{\text{BRICK}}</math>) MEASUREMENT<sup>(10)</sup></b>						
$V_{\text{IN}}$	Input voltage range, BATn to VSS	FUNCTION_CONFIG[] = 0101xx00b	0		30	V
$V_{\text{RES}}$	Voltage resolution <sup>(11)</sup>	14 bits		~1.831		mV
$V_{\text{ACC}}$	Voltage accuracy	Total error $7.2\text{ V} \leq V_{\text{IN}} \leq 27\text{ V}$	-80	-30	20	mV
$C_{\text{IN}}$	Input capacitance	Converting		1		pF
$R_{\text{IN}}$	Effective input resistance	Converting		50		k $\Omega$
$E_{\text{N}}$	Noise				1.5	mV <sub>RMS</sub>
<b>GPAI MEASUREMENT<sup>(12)</sup></b>						
$V_{\text{IN}}$	Input voltage range, <sup>(13)</sup> GPAI+ to GPAI-		0		2.5	V
$V_{\text{RES}}$	Voltage resolution <sup>(14)</sup>	14 bits		~153		$\mu\text{V}$
$V_{\text{ACC}}$	Voltage accuracy, $V_{\text{IN}} = \text{GPAI+} - \text{GPAI-}$	$0.25\text{ V} \leq V_{\text{IN}} \leq 2.5\text{ V}$ $V_{\text{IN}} = 1.25\text{ V}, T_A = 25^\circ\text{C}$	-7	$\pm 2$	7	mV
$C_{\text{IN}}$	Input capacitance	Converting		40		pF
$R_{\text{IN}}$	Effective input resistance	Converting		50		k $\Omega$
$E_{\text{N}}$	Noise				150	$\mu\text{V}_{\text{RMS}}$
<b>TSn MEASUREMENT<sup>(15)</sup></b>						
$V_{\text{IN}}$	Input voltage range, <sup>(16)</sup> TSn+ to TSn-		0		2.5	V
$V_{\text{RES}}$	Voltage resolution <sup>(17)</sup>	14 bits, REG50 = 5 V, (Resolution $\approx V_{\text{REG50}} / 2^{15}$ )		~153		$\mu\text{V}$
$V_{\text{ACC}}$	Ratio accuracy, % of input <sup>(17)</sup>	$45\text{ mV} \leq V_{\text{IN}} < 250\text{ mV}$ $250\text{ mV} \leq V_{\text{IN}} \leq 2.4\text{ V}$	-3.5%	$\pm 1\%$	+3.5%	
$C_{\text{IN}}$	Input capacitance	Converting		40		pF
$R_{\text{IN}}$	Effective input resistance	Converting		50		k $\Omega$
$E_{\text{N}}$	Noise				150	$\mu\text{V}_{\text{RMS}}$
<b>THERMAL SHUTDOWN</b>						
$T_{\text{SD}}$	Shutdown threshold	$V_{\text{BAT}} = 22\text{ V}$	125	142	156	$^\circ\text{C}$
$T_{\text{HYS}}$	Recovery hysteresis			8	25	$^\circ\text{C}$
<b>UNDERVOLTAGE LOCKOUT (UVLO) and POWER-ON RESET (POR)</b>						
$V_{\text{UVLO}}$	Negative-going threshold		5		5.6	V
$V_{\text{UVLO\_HSY}}$	Hysteresis		250	375	500	mV
$\text{UVLO}_{\text{DELAY}}$	Delay to locked-out condition	$V \leq V_{\text{UVLO}} \text{ MIN}$		15		$\mu\text{s}$
$V_{\text{POR}}$	Negative-going threshold		4		5	V
$V_{\text{POR\_HSY}}$	Hysteresis		250	500	750	mV
$\text{POR}_{\text{DELAY}}$	Delay to disabled condition	$V \leq V_{\text{POR}} \text{ MIN}$		15		$\mu\text{s}$
$t_{\text{RST}}$	Reset delay time	$V \geq V_{\text{POR}} + V_{\text{POR\_HSY}}$	40	56	70	ms
$V_{\text{DELTA\_RISE}}$	Voltage delta between trip points	$V_{\text{UVLO}} - V_{\text{POR}}$ ( $V_{\text{BAT}}$ rising)	0.25	0.4	0.7	V
$V_{\text{DELTA\_FALL}}$	Voltage delta between trip points	$V_{\text{UVLO}} - V_{\text{POR}}$ ( $V_{\text{BAT}}$ falling)	0.4	0.52	0.7	V
<b>BATTERY PROTECTION THRESHOLDS</b>						

(10) FUNCTION\_CONFIG[] = 01xxxx00b for all test conditions

(11) See text for specific conversion formula.

(12) FUNCTION\_CONFIG[] = 0101xx00b for all test conditions

(13) 0 V may not lie within the range of measured values due to offset voltage limit and device calibration.

(14) See text for specific conversion formula.

(15) FUNCTION\_CONFIG[] = 01xxxx00b for all Test Conditions

(16) 0 V may not lie within the range of measured values due to offset voltage limit and device calibration.

(17) See text for specific conversion formula.

## Electrical Characteristics (接下页)

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{OVR}}$	OV detection threshold range <sup>(18)</sup>	$V_{\text{BAT}} = 12\text{ V}$ and $27\text{ V}$	2		5	V
$\Delta V_{\text{OVS}}$	OV detection threshold program step	$V_{\text{BAT}} = 12\text{ V}$ and $27\text{ V}$		50		mV
$V_{\text{OVH}}$	OV detection hysteresis	$V_{\text{BAT}} = 12\text{ V}$ and $27\text{ V}$		50		mV
$V_{\text{OVA1}}$	OV detection threshold accuracy	$3.3 \leq V_{\text{OV\_SET}} \leq 4.5$	-50	0	50	mV
$V_{\text{OVA2}}$	OV detection threshold accuracy	$V_{\text{OV\_SET}} < 3.3$ or $V_{\text{OV\_SET}} > 4.5$	-70	0	70	mV
$V_{\text{UVR}}$	UV detection threshold range <sup>(18)</sup>	$V_{\text{BAT}} = 22\text{ V}$	700		3300	mV
$\Delta V_{\text{UVS}}$	UV detection threshold program step	$V_{\text{BAT}} = 22\text{ V}$		100		mV
$V_{\text{UVH}}$	UV detection hysteresis	$V_{\text{BAT}} = 22\text{ V}$		100		mV
$V_{\text{UVA}}$	UV detection threshold accuracy		-100	0	100	mV
$V_{\text{OTR}}$	OT detection threshold range <sup>(19)</sup>	$V_{\text{REG50}} = 5\text{ V}$	1		2	V
$\Delta V_{\text{OTS}}$	OT detection threshold program step <sup>(19)</sup>			See <sup>(20)</sup>		V
$V_{\text{OTA}}$	OT detection threshold accuracy <sup>(19)</sup>	$T = 40^\circ\text{C}$ to $90^\circ\text{C}$	-0.015	0.01	0.05	V
$\Delta V_{\text{OTH}}$	OT reset hysteresis <sup>(21)</sup>	$T = 40^\circ\text{C}$ to $90^\circ\text{C}$	8%	12%	15%	
<b>BATTERY PROTECTION DELAY TIMES</b>						
$t_{\text{OV}}$	OV detection delay-time range		0		3200	ms
$\Delta t_{\text{OV}}$	OV detection delay-time step	COVT [ $\mu\text{s}$ ] = 0		100		$\mu\text{s}$
		COVT [ms] = 1		100		ms
$t_{\text{UV}}$	UV detection delay-time range		0		3200	ms
$\Delta t_{\text{UV}}$	UV detection delay-time step	CUVT[7] ( $\mu\text{s}$ ) = 0		100		$\mu\text{s}$
		CUVT[7] (ms) = 1		100		ms
$t_{\text{OT}}$	OT detection delay-time range		0		2550	ms
$\Delta t_{\text{OT}}$	OT detection delay-time step			10		ms
$t_{\text{acr}}$	OV, UV, and OT detection delay-time accuracy <sup>(22)</sup>	CUVT, (COVT) $\geq 500\ \mu\text{s}$	-12%	0%	10%	
$t_{\text{(DETECT)}}$	Protection comparator detection time	$V_{\text{OT}}$ or $V_{\text{OV}}$ or $V_{\text{UV}}$ threshold exceeded by $10\text{ mV}$			100	$\mu\text{s}$
<b>OTP EPROM PROGRAMMING CHARACTERISTICS</b>						
$V_{\text{PROG}}$	Programming voltage	$V_{\text{BAT}} \geq 22\text{ V}$	6.75	7	7.25	V
$t_{\text{PROG}}$	Programming time				50	ms
$I_{\text{PROG}}$	Programming current			10	20	mA

(18) COV and CUV thresholds must be set such that  $\text{COV} - \text{CUV} \geq 300\text{ mV}$

(19) Using recommended components. Consult 表 2 in text for voltage levels used.

(20) See 表 2 for trip points.

(21) Hysteresis measured to trip point voltage.

(22) Under double or multiple fault conditions (of a single type), the second or greater fault may have its delay time shortened by up to the step time for the fault. For example, the second and subsequent COV faults occurring within the delay time period for the first fault may have their delay time shortened by up to  $100\ \mu\text{s}$ .

## 6.6 Timing Requirements: AC SPI Data Interface

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{\text{BAT}} = 22\text{ V}$ , Min/Max values stated where  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  and  $V_{\text{BAT}} = 7.2\text{ V}$  to  $27\text{ V}$  (unless otherwise noted) See [Figure 1](#).

		MIN	NOM	MAX	UNIT	
$f_{\text{SCLK}}$	SCLK frequency <sup>(1)</sup>	10	250	1000	kHz	
SCLK <sub>DC</sub>	SCLK_H duty cycle, $t_{\text{(HIGH)}} / t_{\text{(SCLK)}}$ or $t_{\text{(LOW)}} / t_{\text{(SCLK)}}$	40%		60%		
$t_{\text{CS,LEAD}}$	CS_H lead time, CS_H low to clock	50	SCLK/2		ns	
$t_{\text{CS,LAG}}$	CS_H lag time. Last clock to CS_H high	10	SCLK/2		ns	
$t_{\text{CS,DLY}}$	CS_H high to CS_H low (inter-packet delay requirement)	3			$\mu\text{s}$	
$t_{\text{ACC}}$	CS_H access time <sup>(2)</sup> : CS_H low to SDO_H data out		125	250	ns	
$t_{\text{DIS}}$	CS_H disable time <sup>(2)</sup> : CS_H high to SDO_H high impedance		2.5	2.7	$\mu\text{s}$	
$t_{\text{SU,SDI}}$	SDI_H input-data setup time	15			ns	
$t_{\text{HD,SDI}}$	SDI_H input-data hold time	10			ns	
$t_{\text{VALID,SDO}}$	SDO_H output-data valid time SCLK_H edge to SDO_H valid		$C_L \leq 20\text{ pF}$	75	110	ns

- (1) Maximum SCLK frequency is limited by the number of bq76PL536A-Q1 devices in the vertical stack. The maximum listed here may not be realizable in systems due to delays and limits imposed by other components including wiring, connectors, PCB material and routing, and so forth. See text for details.
- (2) Time listed is for single device.

## 6.7 Vertical Communications Bus

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{BAT} = 22\text{ V}$  (unless otherwise noted)

			MIN	NOM <sup>(1)</sup>	MAX	UNIT
$t_{HV\_SCLK}$	Propagation delay, SCLK_H to SCLK_N	HOST = 0		40		ns
$t_{VB\_SCLK}$	Propagation delay, SCLK_S to SCLK_N	HOST = 1		30		ns
$t_{HV\_CS}$	Propagation delay, CS_H to CS_N	HOST = 0		40		ns
$t_{VB\_CS}$	Propagation delay, CS_S to CS_N	HOST = 1		30		ns
$t_{HV\_SDI}$	Propagation delay, SDI_H to SDI_N	HOST = 0		40		ns
$t_{VB\_SDI}$	Propagation delay, SDI_S to SDI_N	HOST = 1		30		ns
$t_{HV\_CONV}$	Propagation delay, CONV_H to CONV_N	HOST = 0		100		ns
$t_{VB\_CONV}$	Propagation delay, CONV_S to CONV_N	HOST = 1		30		ns
$t_{HV\_SDO}$	Propagation delay, SDO_N to SDO_H	HOST = 0		10		ns
$t_{VB\_SDO}$	Propagation delay, SDO_N to SDO_S	HOST = 1		40		ns
$t_{HV\_DRDY}$	Propagation delay, DRDY_N to DRDY_H	HOST = 0		60		ns
$t_{VB\_DRDY}$	Propagation delay, DRDY_N to DRDY_S	HOST = 1		40		ns
$t_{HV\_FAULT}$	Propagation delay, FAULT_N to FAULT_H	HOST = 0		55		ns
$t_{VB\_FAULT}$	Propagation delay, FAULT_N to FAULT_S	HOST = 1		30		ns
$t_{HV\_ALERT}$	Propagation delay, ALERT_N to ALERT_H	HOST = 0		65		ns
$t_{VB\_ALERT}$	Propagation delay, ALERT_N to ALERT_S	HOST = 1		30		ns

(1) Nominal values are quoted in place of MIN/MAX for design guidance only. Actual propagation delay depends heavily on wiring and capacitance in the signal path. These parameters are not tested in production due to these dependencies on system design considerations.

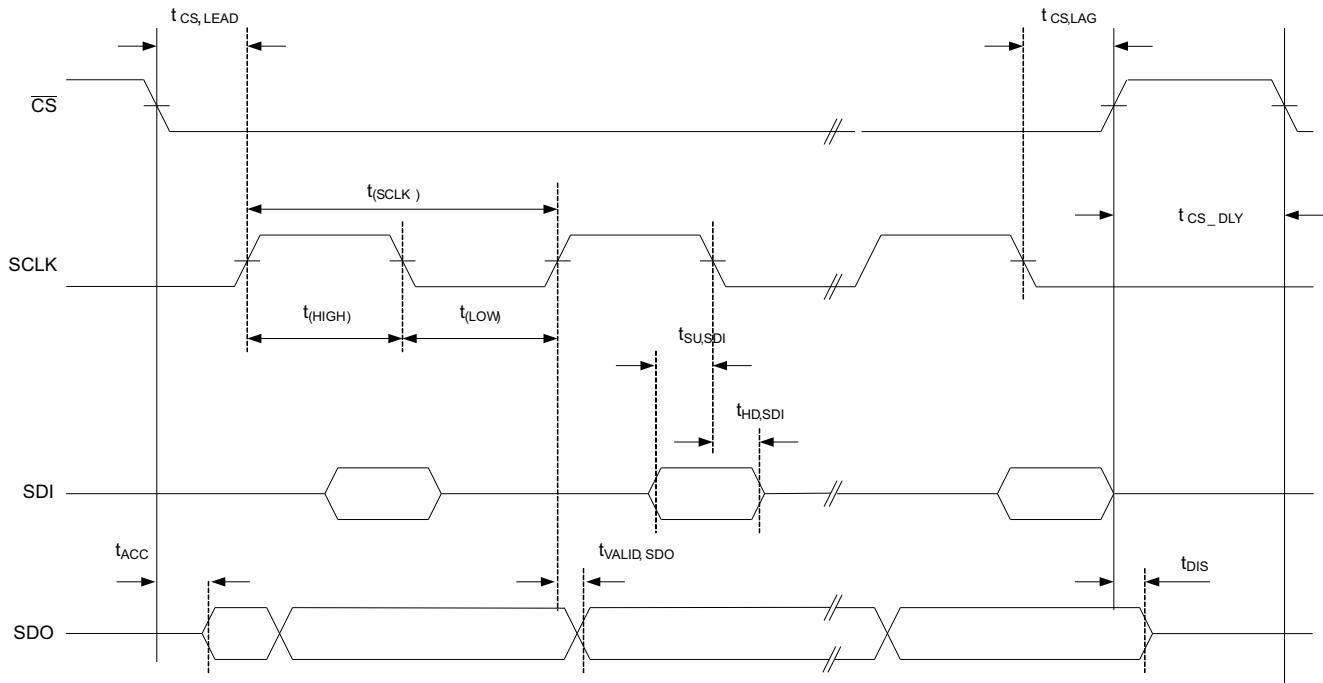


图 1. SPI Host Interface Timing

## 6.8 Typical Characteristics

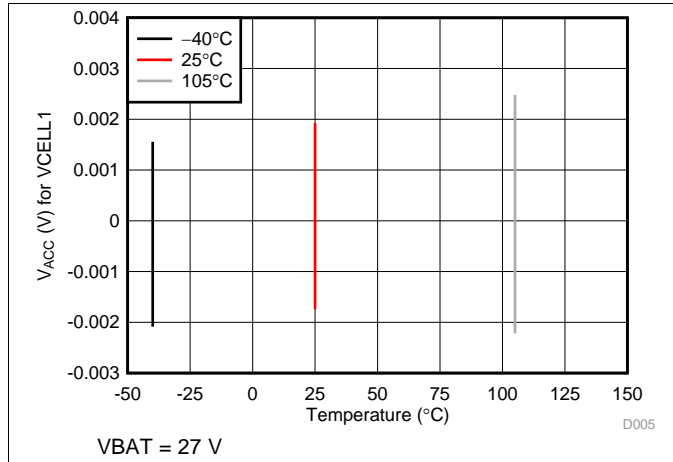


图 2. Total Channel Accuracy (V) for VCELL1

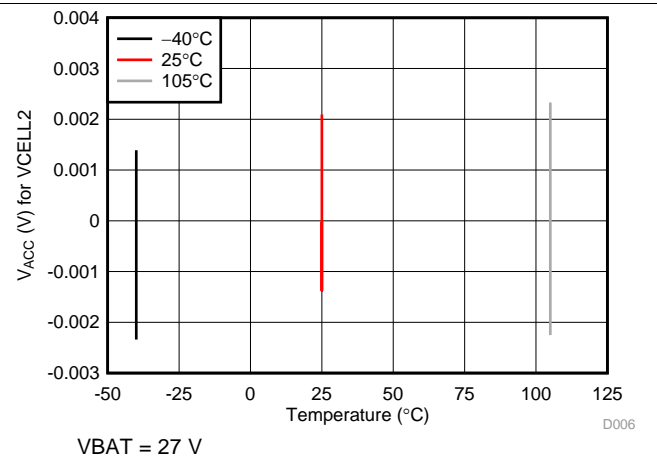


图 3. Total Channel Accuracy (V) for VCELL2

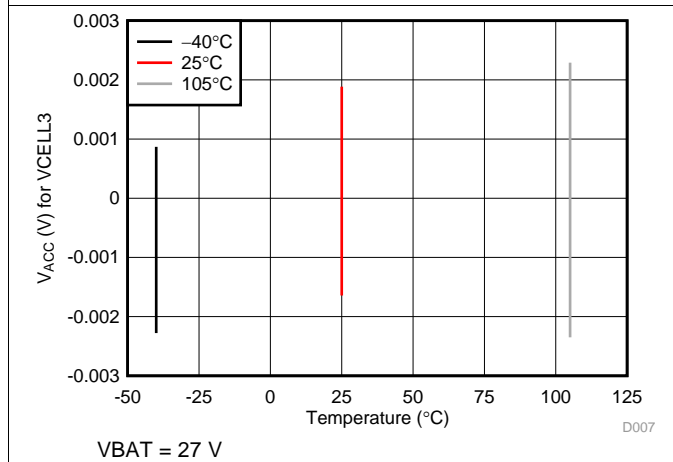


图 4. Total Channel Accuracy (V) for VCELL3

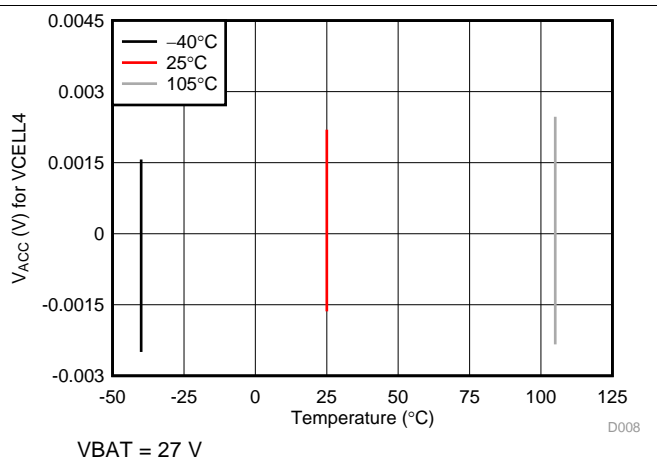


图 5. Total Channel Accuracy (V) for VCELL4

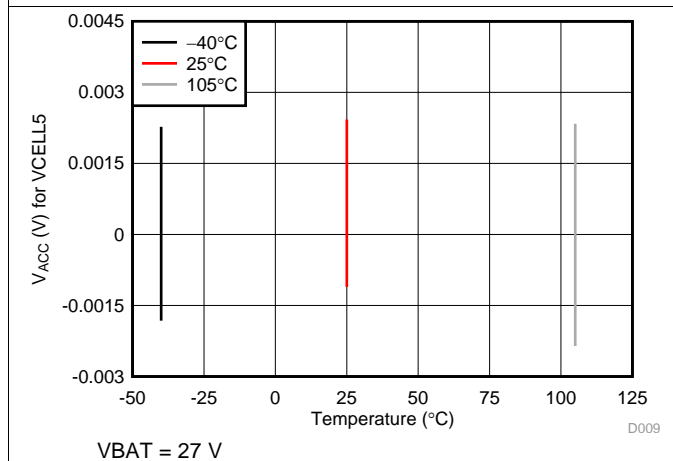


图 6. Total Channel Accuracy (V) for VCELL5

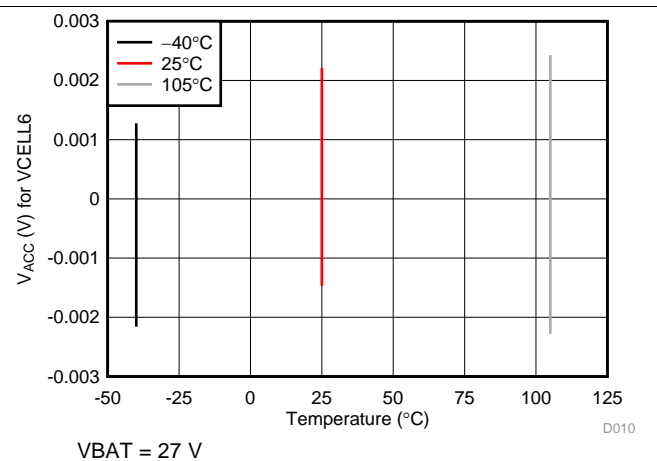
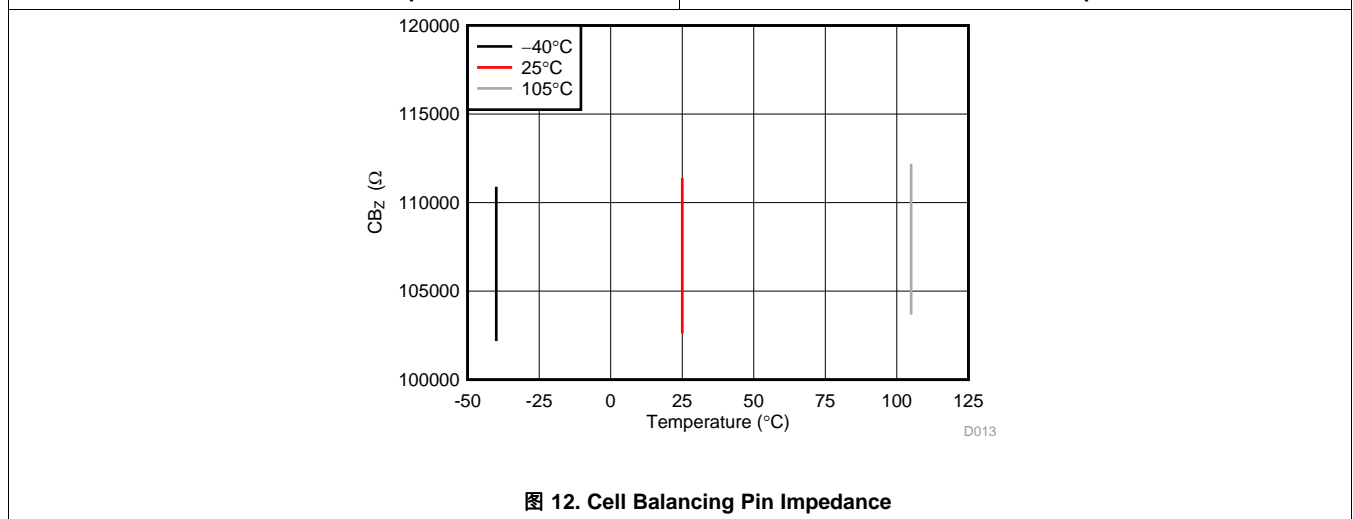
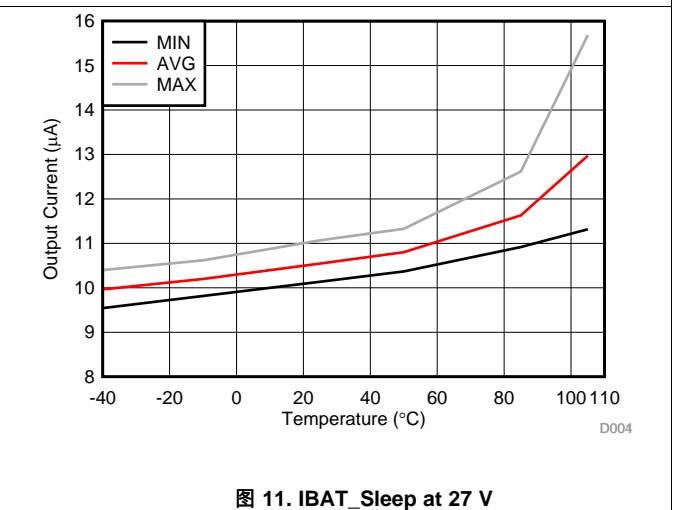
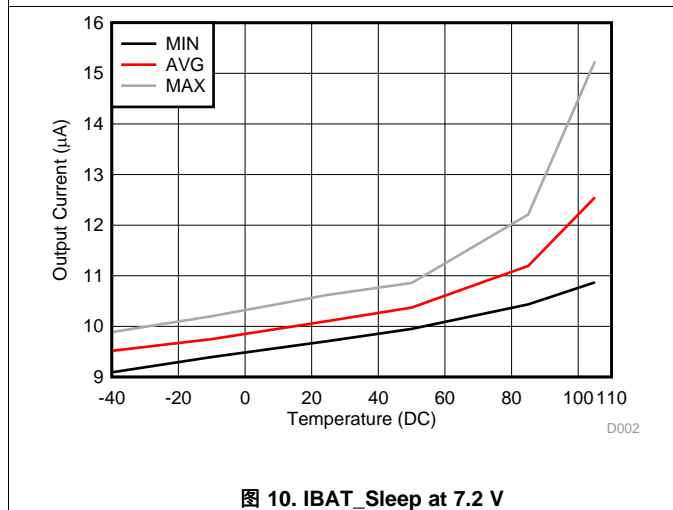
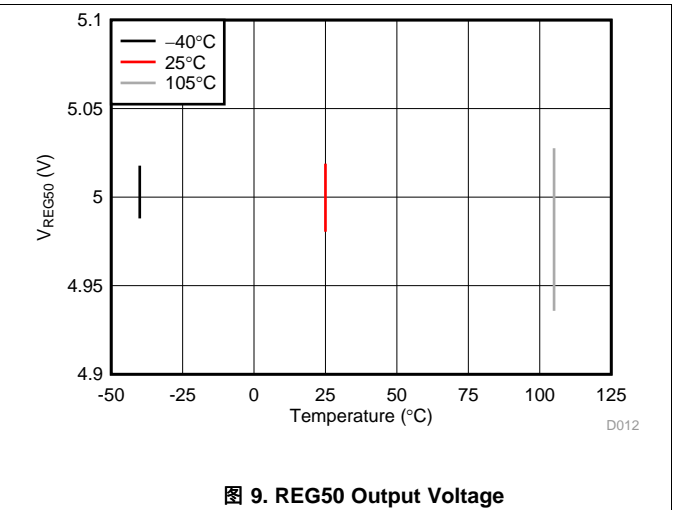
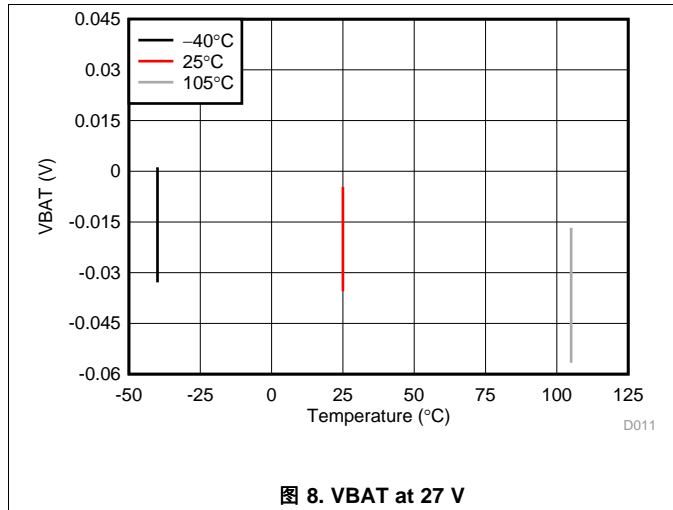


图 7. Total Channel Accuracy (V) for VCELL6

Typical Characteristics (接下页)



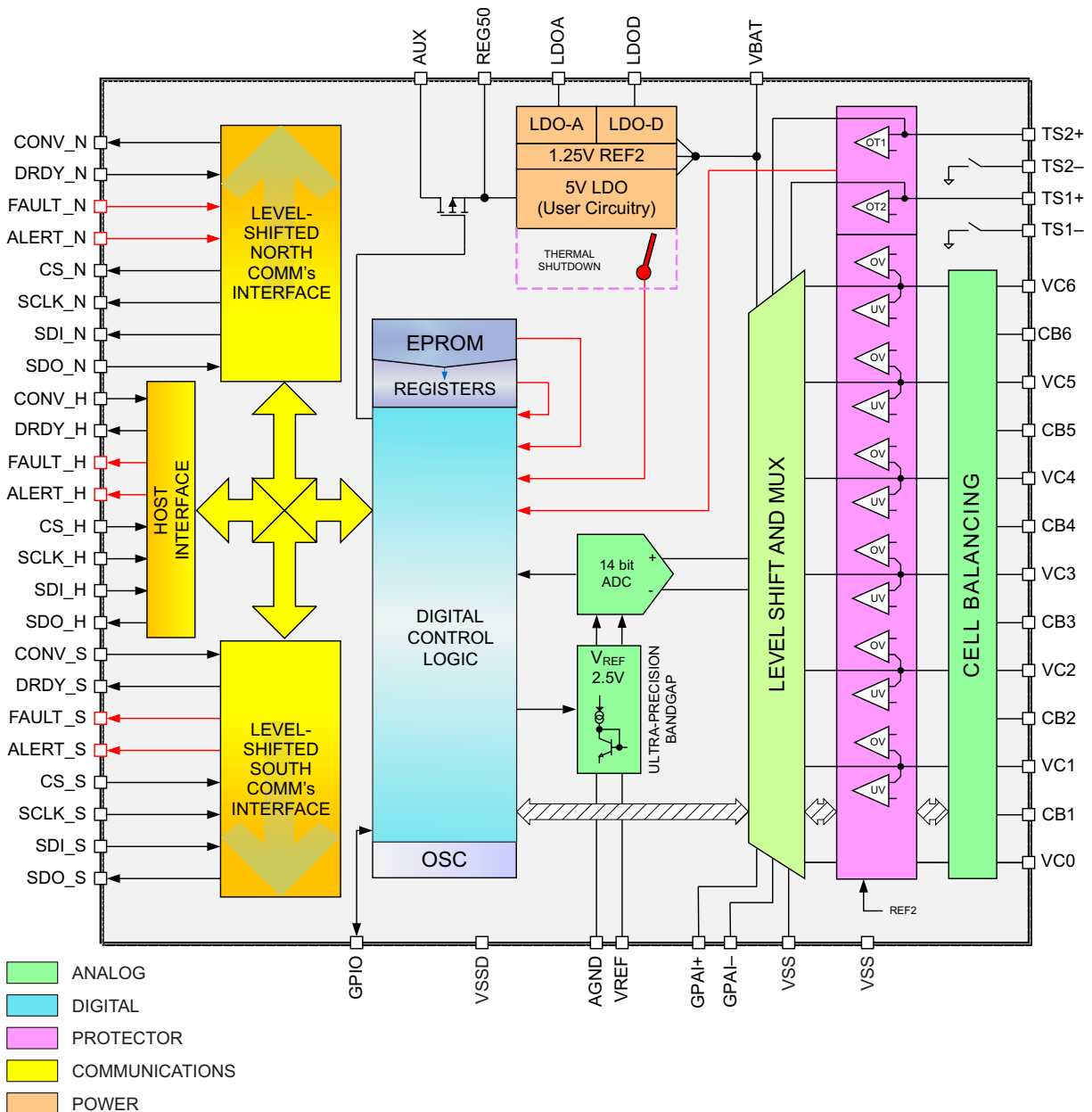
## 7 Detailed Description

### 7.1 Overview

The bq76PL536A-Q1 is a 3-to-6 series Lithium-ion battery monitor, secondary protector and analog front end (AFE) that can be stacked vertically to monitor up to 192 cells without the need for additional isolation components between ICs.

This device incorporates a precision analog-to-digital converter (ADC); independent cell voltage and temperature protection; cell balancing, and precision 5-V regulator to power user circuitry. The bq76PL536A-Q1 additionally provides full (secondary) protection for overvoltage, undervoltage, and overtemperature conditions.

### 7.2 Functional Block Diagram





## 7.3 Feature Description

### 7.3.1 Analog-to-Digital Conversion (ADC)

#### 7.3.1.1 General Features

The integrated 14-bit (unsigned) high-speed successive approximation register (SAR) analog-to-digital converter uses an integrated band-gap reference voltage ( $V_{REF}$ ) for the cell and brick measurements. The ADC has a front-end multiplexer for nine inputs – six cells, two temperature sensors, and one general-purpose analog input (GPAI). The GPAI input can further be multiplexed to measure the *brick* voltage between the BATx pin and VSS or the voltage between the GPAI+ and GPAI– pins.

The ADC and reference are factory trimmed to compensate for gain, offset, and temperature-induced errors for all inputs. The measurement result is not allowed to roll over due to offset error at the top and bottom of the range. For example, a reading near zero does not underflow to 0x03ff due to offset error and vice-versa.

The converter returns 14 valid unsigned magnitude bits in the following format:

<00xxxxxx xxxxxxxx>

Each word is returned in big-endian format in a register pair consisting of two adjacent 8-bit registers. The MSB of the word is located in the lower-address register of the pair, that is, data for cell 1 is returned in registers 0x03 and 0x04 as 00xxxxxx xxxxxxxxb.

#### 7.3.1.2 3-to-6 Series Cell Configuration

When fewer than 6 cells are used, the most-positive cell voltage of the series string should be connected to the BAT1/BAT2 pins, through the RC input network shown in the *Typical Application* section. Unused VCx inputs should be connected to the next VCx input down until an input connected to a cell is reached – that is, in a four cell stack, VC6 connects to VC5, which connects to VC4 (图 13).

The internal multiplexer control can be set to scan only the inputs which are connected to cells, thereby speeding up conversions slightly. The multiplexer is controlled by the ADC\_CONTROL[CN2:0] bits.

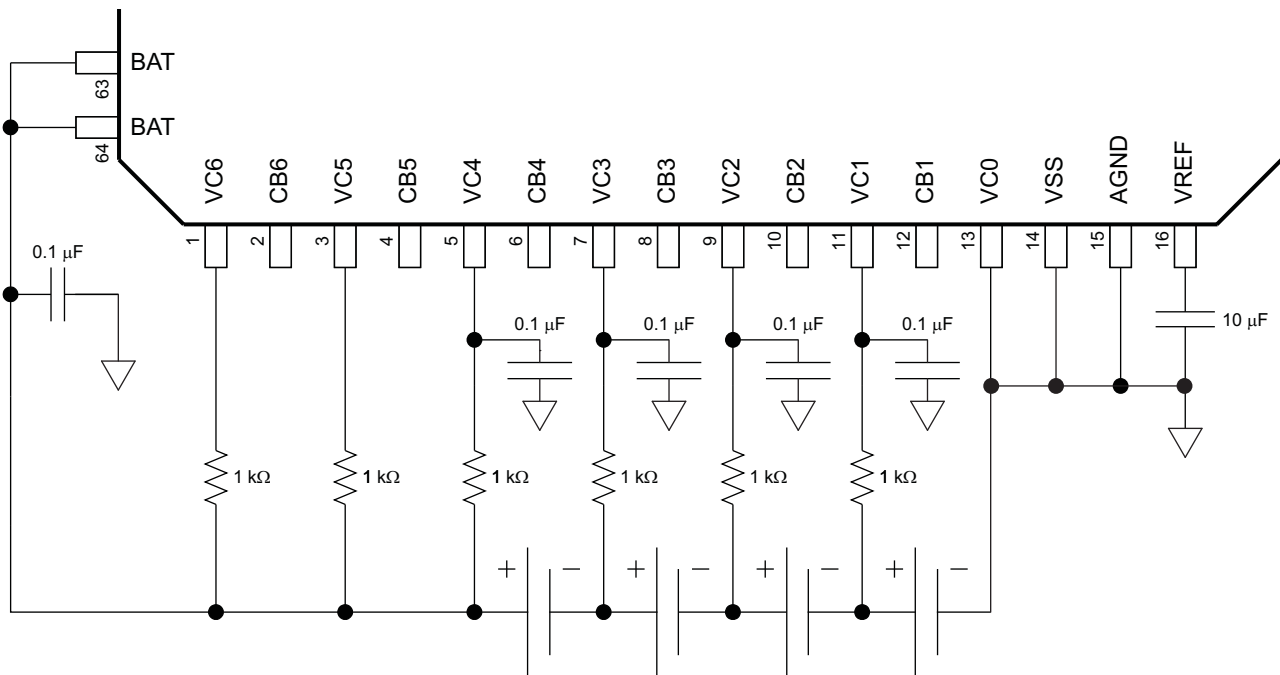


图 13. Connecting < 6 Cells (4 Shown)

## Feature Description (接下页)

### 7.3.1.3 Cell Voltage Measurements

Use the following formula (all values are in decimal) to convert the returned cell measurement value to a dc voltage (in mV).

$$\text{mV} = (\text{REG}_{\text{MSB}} \times 256 + \text{REG}_{\text{LSB}}) \times 6250 / 16383 \quad (1)$$

Example:

Cell\_1 == 3.35 V (3350 mV);  
 After conversion, REG\_03 == 0x22; REG\_04 == 0x4d  
 $0x22 \times 0x100 + 0x4d = 0x224d$  (8781.)  
 $8781 \times 6250 / 16,383 = 3349.89 \text{ mV} \approx 3.35 \text{ V}$

### 7.3.1.4 GPAl or $V_{\text{BAT}}$ Measurements

The bq76PL536A-Q1 features a differential input to the ADC from two external pins, GPAl+ and GPAl-. The ADC GPAl result register can be configured (via the FUNCTION\_CONFIG[GPAl\_SRC]) to provide a measurement of the voltage on these two pins, or of the *brick* voltage present between the BATx pins and VC0.

In the bq76PL536A-Q1 device, the  $V_{\text{BAT}}$  measurement is taken from the BATx pin to the VC0 pin, and is a separate input to the ADC mux. Because this is a separate input to the ADC, certain common system faults, such as a broken cell wire, can be easily detected using the bq76PL536A-Q1 and simple firmware techniques.

The GPAl measurement can be configured to use one of two references via FUNCTION\_CONFIG[GPAl\_REF]. Either the internal bandgap ( $V_{\text{REF}}$ ) or REG50 can be selected. When REG50 is selected, the ADC returns a ratio of the voltage at the inputs and REG50, removing the need for compensation of the REG50 voltage accuracy or drift when used as a source to excite the sensor. When the device is configured to measure  $V_{\text{BAT}}$  (FUNCTION\_CONFIG[GPAl\_SRC] = 1), the device selects VREF automatically and ignores the FUNCTION\_CONFIG[GPAl\_REF] setting.

#### 7.3.1.4.1 Converting GPAl Result to Voltage

To convert the returned GPAl measurement value to a voltage using the internal band-gap reference (FUNCTION\_CONFIG[GPAl\_REF] = 1), the following formula is used.

$$\text{mV} = (\text{REG}_{\text{MSB}} \times 256 + \text{REG}_{\text{LSB}}) \times 2500 / 16,383$$

- FUNCTION\_CONFIG[] = 0100 xxxxb (2)

Example:

The voltage connected to the GPAl inputs == 1.25 V;  
 After conversion, REG\_01 == 0x20; REG\_02 == 0x00  
 $0x20 \times 0x100 + 0x00 = 0x2000$  (8192.)  
 $8192 \times 2500 / 16,383 = 1250 \text{ mV}$

#### 7.3.1.4.2 Converting VBAT Result to Voltage

To convert the returned  $V_{\text{BAT}}$  measurement value to a voltage, the following formula is used.

$$V = (\text{REG}_{\text{MSB}} \times 256 + \text{REG}_{\text{LSB}}) \times 33.333 / 2^{14} \quad (33.333 \approx 6.25 / 0.1875)$$

- FUNCTION\_CONFIG[] = 0101 xxxxb (3)

Example:

The sum of the series cells connected to VC6–VC0 == 20.295 V;  
 After conversion, REG\_01 == 0x26; REG\_02 == 0xf7  
 $0x26 \times 0x100 + 0xf7 = 0x26f7$  (9975.)  
 $9975 \times 33.333 / 16,383 = 20.295 \text{ V}$

## Feature Description (接下页)

### 7.3.1.5 Temperature Measurement

The bq76PL536A-Q1 can measure the voltage TS1+, TS1– and TS2+, TS2– differential inputs using the ADC. An external thermistor/resistor divider network typically drives these inputs. The TSn inputs use the REG50 output divided down and internally connected as the ADC reference during conversions. This produces a ratiometric result and eliminates the need for compensation or correction of the REG50 voltage drift when used to drive the temperature sensors. The REG50 reference allows an approximate 2.5-V full-scale input at the TSn inputs. The final reading is limited between 0 and 16,383, corresponding to an external ratio of 0 to 0.5.

Two control bits are required for the ADC to convert the TSn input voltages successfully. ADC\_CONTROL[TSn] is set to cause the ADC to convert the TSn channel on the next requested conversion cycle. IO\_CONTROL[TSn] is set to cause the FET switch connecting the TSn– input to VSS to close, completing the circuit of the voltage divider. The IO\_CONTROL[] bits should only be set as needed to conserve power; at high temperatures, thermistor excitation current may be relatively high.

#### 7.3.1.5.1 External Temperature Sensor Support (TS1+, TS1–, TS2+, and TS2–)

The device is intended for use with a nominal 10 kΩ at 25°C NTC external thermistor (AT103 equivalent) such as the Panasonic ERT-J1VG103FA, a 1% device. A suitable external resistor-capacitor network should be connected to position the response of the thermistor within the range of interest. This is typically  $R_T = 1.47\text{ k}\Omega$  and  $R_B = 1.82\text{ k}\Omega$  (1%) as shown in 图 14. A parallel bypass capacitor in the range 1 nF to 47 nF placed across the thermistor should be added to reduce noise coupled into the measurement system. The response time delay created by this network should be considered when enabling the respective TS input prior to conversion and setting the OT delay timer. See 图 14 for details.

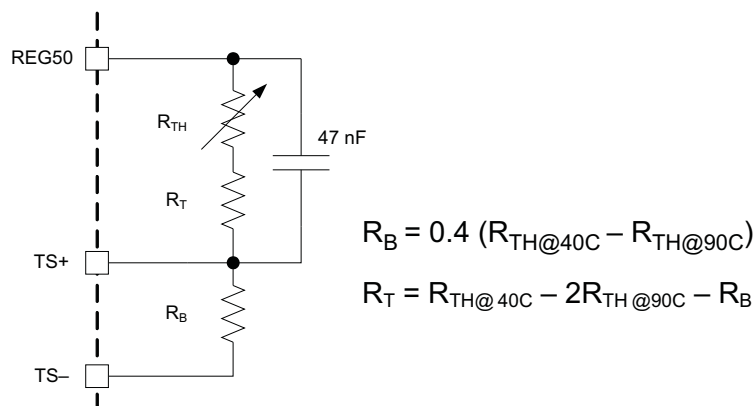


图 14. Thermistor Connection

#### 7.3.1.5.2 Converting TSn Result to Voltage (Ratio)

To convert the returned TSn measurement value to a ratio,  $R_{TS} = V_{TS} \cdot \text{REG50}$ , the following formulas are used. The setting FUNCTION\_CONFIG[] = 0100 xxxxb is assumed. Note that the offset and gain correction are slightly different for each channel.

$$\text{ADC behavior: COUNT} = (V_{\text{TSn}} / \text{REG50} \times \text{scalar}) - \text{OFFSET} \quad (4)$$

$$\text{TS1: } R_{\text{TS1}} = ((\text{TEMPERATURE1\_H} \times 256 + \text{TEMPERATURE1\_L}) + 2) / 33,046 \quad (5)$$

$$\text{TS2: } R_{\text{TS2}} = ((\text{TEMPERATURE2\_H} \times 256 + \text{TEMPERATURE2\_L}) + 9) / 33,068 \quad (6)$$

Example:

The voltage connected to the TS1 inputs (TS1+ – TS1–) == 0.661 V;  $V_{\text{REG50}} \approx 5\text{ V}$  nominal

After conversion,  $\text{REG}_{\text{MSB}} == 0x11$ ;  $\text{REG}_{\text{LSB}} == 0x16$

$\text{ACTUAL\_COUNT} = 0x11 \times 0x100 + 0x16 = 0x1116$  (4374.)

$(4374 + 2) / 33,046 = 0.1324$  (ratio of TSn inputs to REG50)

$0.1324 \times \text{REG50} = 0.662\text{ V}$

## Feature Description (接下页)

### 7.3.1.6 ADC Band-Gap Voltage Reference

The ADC and protection subsystems use separate and independent internal voltage references. The ADC band gap ( $V_{REF}$ ) is nominally 2.5 V. The reference is temperature-compensated and stable.

The internal reference is brought out to the VREF pin for bypassing. A high quality 10- $\mu$ F capacitor should be connected between the VREF and AGND pins, in very close physical proximity to the device pins, using short track lengths to minimize the effects of track inductance on signal quality. The AGND pin should be connected to VSS. Device VSS connections should be brought to a single point close to the IC to minimize layout-induced errors. The device tab should also be connected to this point, and is a convenient common VSS location. The internal VREF should not be used externally to the device by user circuits.

### 7.3.1.7 Conversion Control

#### 7.3.1.7.1 Convert Start

Two methods are available to start a conversion cycle. The CONV\_H pin may be asserted, or firmware may set the CONVERT\_CTRL[CONV] bit.

##### 7.3.1.7.1.1 Hardware Start

A single interface pin (CONV\_H) is used for conversion-start control by the host. A conversion cycle is started by a hardware signal when CONV\_H is transitioned low-to-high by the host. The host should hold this state until the conversion cycle is complete to avoid erroneous edges causing a conversion start when the present conversion is not complete. The signal is simultaneously sent to the higher device in the stack by the assertion of the CONV\_N signal. The bq76PL536A-Q1 automatically sequences through the series of measurements enabled via the ADC\_CONTROL[] register after a convert-start signal is received from either the register bit or the hardware pin.

If the CONV\_H pin is not used in the design, this pin must be maintained in a default low state (approximately 0 V) to allow use of the ADC\_CONVERT[CONV] bit to trigger ADC conversions. If the CONV pin is kept high, the ADC\_CONVERT[CONV] bit does not function, and device current consumption is increased by the signaling current, approximately 900  $\mu$ A. If the CONV\_H pin is not used by the user's design, the pin may be left floating; the internal current sink to VSS maintains proper bias.

##### 7.3.1.7.1.2 Firmware Start

The CONVERT\_CTRL[CONV] bit is also used to initiate a conversion by writing a 1 to the bit, which automatically resets at the end of a conversion cycle. The bit may only be written to 1; the IC always resets the bit to 0. The BROADCAST form of packet is recommended to start all device conversions simultaneously.

---

#### 注

For the designer: The external CONV\_H (CONV\_S) pin must be held in the de-asserted (=0) state to allow the CONV register bit to initiate conversions. An internal pulldown is provided on the pin to maintain this state.

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## Feature Description (接下页)

### 7.3.1.7.2 Data Ready

The bq76PL536A-Q1 signals that data is ready when the last conversion data has been stored to the associated data result register by asserting the DRDY\_S pin (DRDY\_H if HOST = 0) if the DRDY\_N pin is also asserted (图 15). DRDY\_S (DRDY\_H) signals are cleared on the next conversion start.

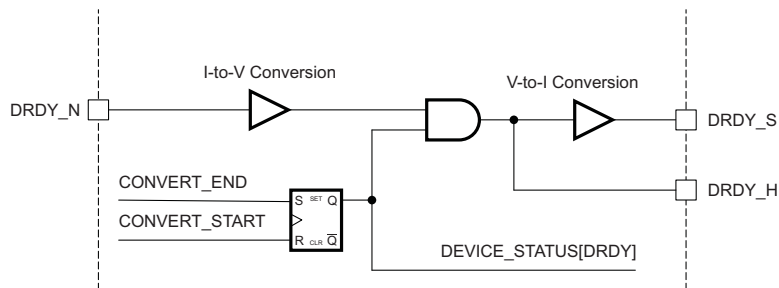


图 15. Data-Ready Logic

### 7.3.1.7.3 ADC Channel Selection

The ADC\_CONTROL register can be configured as follows:

表 1. ADC\_CONTROL Register Configuration

MEASUREMENT	ADC_CONTROL
VCELL1	CELL_SEL = 0x00
VCELL1, VCELL2	CELL_SEL = 0x01
VCELL1, VCELL2, VCELL3	CELL_SEL = 0x02
VCELL1, VCELL2, VCELL3, VCELL4	CELL_SEL = 0x03
VCELL1, VCELL2, VCELL3, VCELL4, VCELL5	CELL_SEL = 0x04
VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6	CELL_SEL = 0x05
External thermistor input 1	TS1 = 1
External thermistor input 2	TS2 = 1
General-purpose analog input	GPAI = 1

### 7.3.1.7.4 Conversion Time Control

The ADC conversion time is fixed at approximately 6  $\mu$ s per converted channel, plus 6  $\mu$ s overhead at the start of the conversion. Total conversion time ( $\mu$ s) is approximately  $6 \times \text{num\_channels} + 6$ .

### 7.3.1.7.5 Automatic Versus Manual Control

The ADC\_CONTROL[ADC\_ON] bit controls powering up the ADC section and the main bandgap reference. If the bit is set to 1, the internal circuits are powered on, and current consumption by the part increases. Conversions begin immediately on command. The host CPU should wait >500  $\mu$ s before initiating the qfirst conversion after setting this bit.

If the ADC\_ON bit is false, an additional 500  $\mu$ s is required to stabilize the reference before conversions begin.

If the sampling interval (time between conversions) used is less than approximately 10 ms, manual mode should be selected to avoid shifting the voltage reference, leading to inaccuracy in the measurements.

### 7.3.1.8 Secondary Protection

The bq76PL536A-Q1 integrates dedicated overvoltage and undervoltage fault detection for each cell and two overtemperature fault-detection inputs for each device. The protection circuits use a separate band-gap reference from the ADC system and operate independently. The protector also uses separate I/O pins from the main communications bus, and therefore is capable of signaling faults in hardware without intervention from the host CPU.

### 7.3.1.8.1 Protector Functionality

When a fault state is detected, the respective fault flag in the FAULT\_STATUS[] or ALERT\_STATUS[] registers is set. All flags in the FAULT and ALERT registers are then ORed into the DEVICE\_STATUS[] FAULT and ALERT bits. The FAULT and ALERT bits in DEVICE\_STATUS[] in turn cause the hardware FAULT\_S or ALERT\_S pin to be set. The bits in DEVICE\_STATUS[] and the hardware pins are latched until reset by the host via SPI command, ensuring that the host CPU does not miss an event.

A separate timer is provided for each fault source (cell overvoltage, cell undervoltage, overtemperature) to prevent false alarms. Each timer is programmable from 100  $\mu$ s to more than 3 s. The timers may also be disabled, which causes fault conditions to be sensed immediately and not latched.

The clearing of the FAULT or ALERT flag (and pin) occurs when the respective flag is written to a 1, which also restarts the respective fault timer. This also clears the FAULT\_S (\_H) or ALERT\_S (\_H) pin. If the actual fault remains present, the FAULT (ALERT) pin is again asserted at the expiration of the timer. This cycle repeats until the cause of the fault is removed.

On exit from the SLEEP state, the COV, CUV, and OT fault comparators are disabled for approximately 200  $\mu$ s to allow internal circuitry to stabilize and prevent false error condition detection.

#### 7.3.1.8.1.1 Using the Protector Functions With 3–5 Cells

The OV/UV condition can be ignored for unused channels by setting the FUNCTION\_CONFIG[CNx] bits to the maximum number of cells connected to the device. If fewer than 6 cells are configured, the corresponding OV/UV faults are ignored. For example, if the FUNCTION\_CONFIG[] bits are set to xxxx 1000, then the OV/UV comparators are disabled for cells 5 and 6. Correct setting of this register prevents spurious false alarms.

### 7.3.1.9 Cell Overvoltage Fault Detection (COV)

When the voltage across a cell exceeds the programmed COV threshold for a period of time greater than set in the COV timer (COVT), the COV\_FAULT[] flag for that cell is set (图 16). The bits in COV\_FAULT[] are then ORed into the FAULT[COV] flag, which is then ORed into the DEVICE\_STATUS[FAULT] flag, which causes the FAULT\_S (\_H) pin also to be asserted. The COV flag is latched unless COVT is programmed to 0, in which case the flag follows the fault condition. Care should be taken when using this setting to avoid *chatter* of the fault status. To reset the FAULT flag, first remove the source of the fault (for example, the overvoltage condition) and then write a 1 to FAULT[COV], followed by a 0 to FAULT[COV]. See (图 16) for details.

The voltage trip point is set in the CONFIG\_COV register. Set points are spaced every 50 mV. Hysteresis is provided to avoid chatter of the fault sensing. The filter delay time is set in the CONFIG\_COVT[] register to prevent false alarms. A start-up deglitch circuit is applied to the timers to prevent false triggering. The deglitch time is 0–50  $\mu$ s, and introduces a small error in the timing for short times. For both COVT and CUVT, this can cause an error greater than the 10% maximum specified for delays < 500  $\mu$ s.

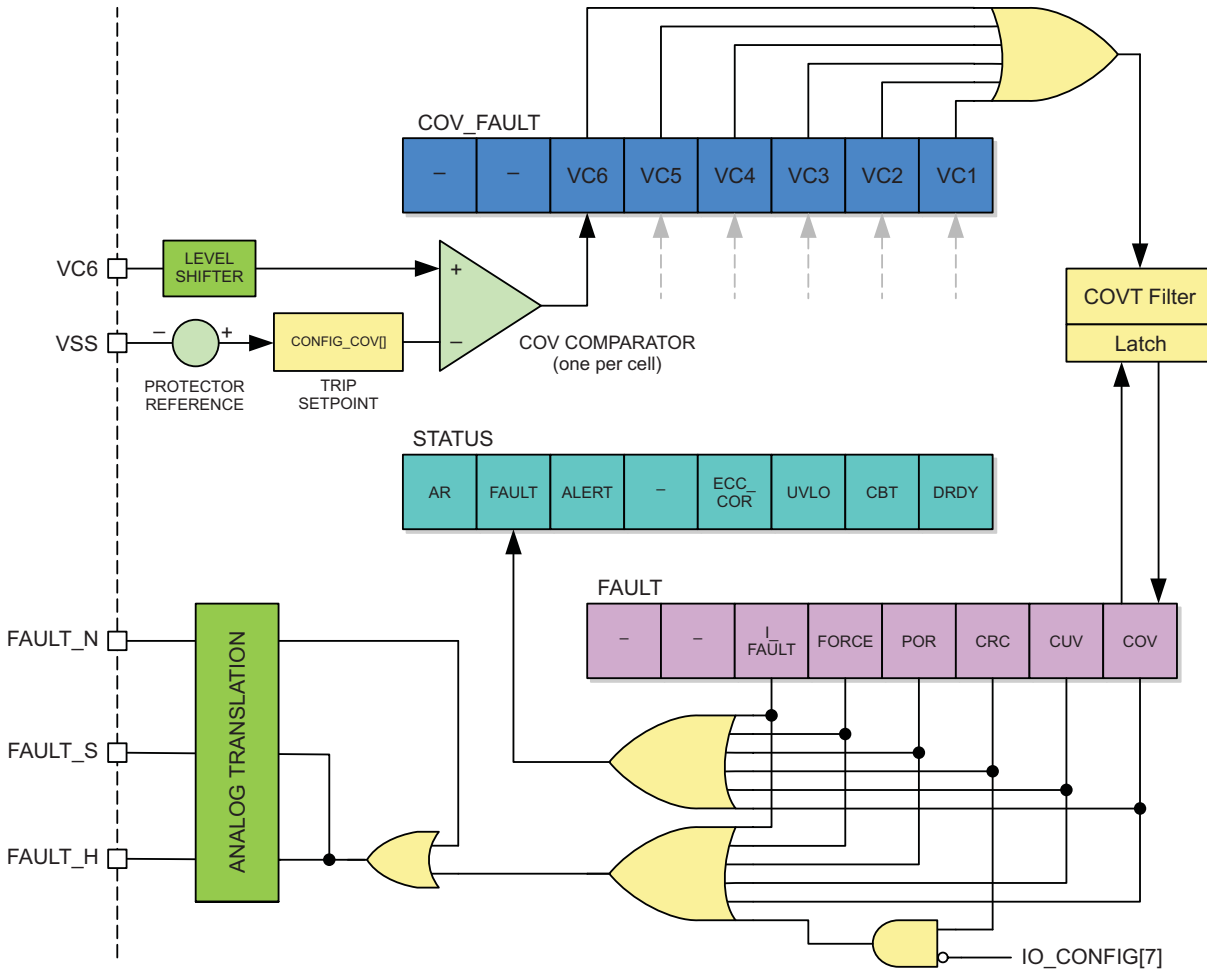


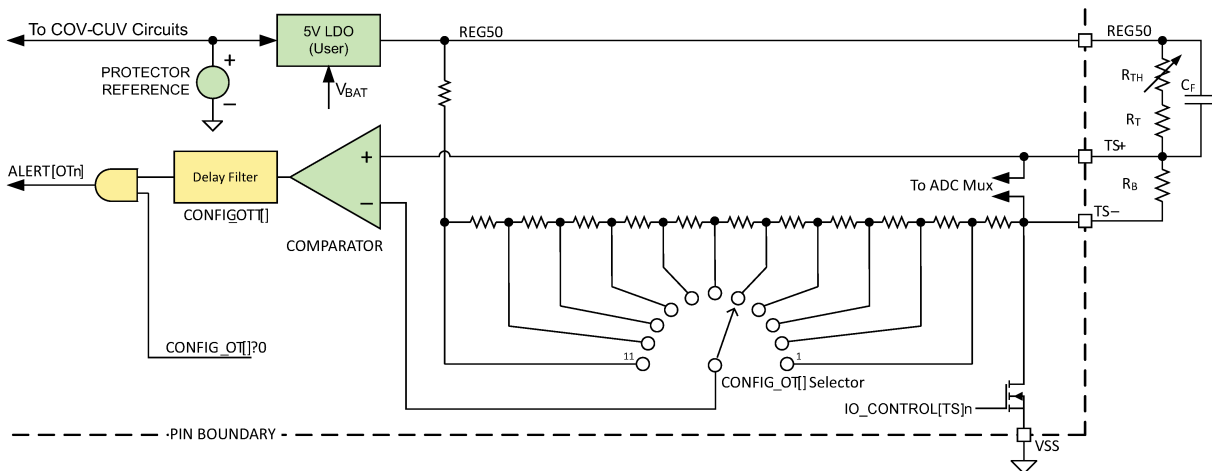
图 16. COV FAULT Simplified Logic Tree

### 7.3.1.10 Cell Undervoltage Fault Detection (CUV)

Cell undervoltage detection operates in a similar manner to the COV protection. When the voltage across a cell falls below the programmed CUV threshold (CONFIG\_CUV[]) for a period of time greater than CUVT (CONFIG\_CUVT[]), the CUV\_FAULT[] flag for that cell is set. The bits in CUV\_FAULT[] are then ORed into the FAULT[CUV] flag, which is then ORed into the DEVICE\_STATUS[FAULT] flag, which causes the FAULT\_S (\_H) pin also to be asserted. The CUV flag is latched unless CUVT is programmed to 0, in which case the flag follows the fault condition. Care should be taken when using this setting to avoid *chatter* of the fault status. To reset the FAULT flag, first remove the source of the fault (for example, the overvoltage condition) and then write a 1 to FAULT[CUV], followed by a 0 to FAULT[CUV].

### 7.3.1.11 Overtemperature Detection

When the temperature input TS1 or TS2 exceeds the programmed OT1 or OT2 threshold (CONFIG\_OT[]) for a period of time greater than OTT (CONFIG\_OTT[]) the ALERT\_STATUS[OT1, OT2] flag is set (图 17). The ALERT[] flags are then ORed into the DEVICE\_STATUS[ALERT] flag, and the ALERT\_S (\_H) pin is also asserted. The OT flag is latched unless OTT is programmed to 0, in which case the flag follows the fault condition. Care should be taken when using this setting to avoid *chatter* of the fault status. To reset the FAULT flag, first remove the source of the alert (for example, the overtemperature condition) and then write a 1 to ALERT[OTn], followed by a 0 to FAULT[OTn].


**图 17. Simplified Overtemperature Detection Schematic**

As shown in [图 17](#), the OT thresholds are detectable in 11 steps representing approximately 5°C divisions when a thermistor and gain/offset setting resistors are chosen using the formula in the [External Temperature Sensor Support \(TS1+, TS1– and TS2+, TS2–\)](#) section. A *DISABLED* setting is also available. This results in an adjustment range from approximately 40°C to 90°C, but the range center can be moved by modifying the  $R_T$  value. The steps are spaced in a non-linear fashion to correspond to typical thermistor response curves. Typical accuracy of a few degrees C or better can be achieved (with no additional calibration requirements) by careful selection of the thermistor and resistors.

Each input sensor can be adjusted independently via separate registers `CONFIG_OT1[]` and `CONFIG_OT2[]`. The two temperature set points share a common filter delay set in the `CONFIG_OTT[]` register. A setting of 0 in the `CONFIG_OTT[]` register causes the fault sensing to be both instantaneous and not latched. All other settings provide a latched ALERT state.

#### 7.3.1.11.1 Ratiometric Sensing

The OT protector circuits use ratiometric inputs to sense fault conditions. The REG50 output is applied internally to the divider, which forms the reference voltages used by the comparator circuit. The REG50 output is also used externally as the excitation source for the temperature sensor. This allows the REG50 output to vary over time or temperature (within data-sheet limits) and have virtually no effect on the correct operation of the circuit. Any change seen by the sensor is also seen by the divider, and therefore, changes proportionally. Although representing the trip set points as voltages is valid, if you assume that REG50 is at exactly 5 V, in practice this is not the case. In [表 2](#), the correct ratios  $[R_B / (R_B + R_T + R_{TH})]$  are shown, along with the equivalent voltage points when REG50 is assumed to be 5 V.



**表 2. Overtemperature Trip Set Points**

OT THRESHOLDS					
CONFIG_OT	T <sub>NOM</sub> °C <sup>(1)</sup>	V <sub>TS</sub> RATIO SET	V <sub>TS</sub> RATIO CLEAR	V <sub>SET</sub> <sup>(2)</sup>	V <sub>CLEAR</sub> <sup>(2)</sup>
0	Disabled	Disabled	Disabled	Disabled	Disabled
1	40	0.2000	0.1766	1.000	0.883
2	45	0.2244	0.2000	1.122	1.000
3	50	0.2488	0.2270	1.244	1.135
4	55	0.2712	0.2498	1.356	1.249
5	60	0.2956	0.2750	1.478	1.375
6	65	0.3156	0.2956	1.578	1.478
7	70	0.3356	0.3162	1.678	1.581
8	75	0.3556	0.3368	1.778	1.684
9	80	0.3712	0.3528	1.856	1.764
10	85	0.3866	0.3688	1.933	1.844
11	90	0.4000	0.3824	2.000	1.912

(1) T<sub>NOM</sub> depends on thermistor selection

(2) Assumes REG50 = 5.000 V

#### 7.3.1.11.2 Thermistor Power

To minimize power consumption, the thermistors are not powered ON by default. Two bits are provided in IO\_CONTROL[] to control powering the thermistors, TS1 and TS2. The TS<sub>n</sub>– input is only connected to VSS when the corresponding bit is set. The user firmware must set these bits to 1 to enable both temperature measurement and the secondary protector functions. When the thermistor functions are not in use, the bits may be programmed to 0 to remove current through the thermistor circuits.

#### 7.3.1.11.3 Thermistor Input Conditioning

A filter capacitor is recommended to minimize noise in to the ADC and protector. The designer should insure that the filter capacitor has sufficient time to charge before reading the thermistors. The CONFIG\_OTT[] value should also be set to > 5t, the time delay introduced by the RC network comprising C<sub>F</sub>, R<sub>TH</sub>, R<sub>T</sub>, and R<sub>B</sub>, to avoid false triggering of the PROTECTOR function and ALERT signal when the TS1 and/or TS2 bits are set to 1 and the inputs enabled.

On exit from the SLEEP state, the OT fault comparators are disabled for approximately 200 μs to allow internal circuitry to stabilize and prevent false error-condition detection.

#### 7.3.1.12 Fault and Alert Behavior

When the FAULT\_N pin is asserted by the next higher bq76PL536A-Q1 in the stack, then the FAULT\_S is also asserted, thereby passing the signal down the array of stacked devices if they are present. FAULT\_N should always be connected to the FAULT\_S of the next higher device in the stack. If no higher device exists, it should be tied to V<sub>BAT</sub> of this bq76PL536A-Q1, either directly or via a pull-up resistor from approximately 10 kΩ to 1 MΩ. The FAULT\_x pins are active-high and current flows when asserted. The ALERT\_x pins behave in a similar manner. If the FAULT\_N pin of the base device (HSEL = 0) becomes asserted, it asserts its FAULT\_H signal to the host microcontroller. This signal chain may be used to create an interrupt to the CPU or drive other compatible logic or I/O directly. See 表 3 for further details.

**表 3. Fault Detection Summary**

FAULT	DETECTION	SIGNALING			
		PIN		DEVICE_STATUS BIT SET	X_STATUS BIT SET
		HSEL = 1	HSEL = 0		
EPROM double bit error	ECC logic fault detected	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[I_FAULT]
FORCE	User set FORCE bit	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[FORCE]
POR	Power-on reset occurred	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[POR]
CRC <sup>(1)</sup>	CRC fail on received packet	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[CRC]
CUV	$V_{Cx} < V_{UV}$ for $t_{UV}$	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[CUV]
COV	$V_{Cx} > V_{OV}$ for $t_{OV}$	FAULT_S	FAULT_H	FAULT	FAULT_STATUS[COV]
AR	Address $\neq$ (0x01 → 0x3e)	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[AR]
Protected-register parity error	Parity not even in protected register	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[PARITY]
EPROM single-bit error	ECC logic fault detected and corrected	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[ECC_COR]
FORCE	User set FORCE bit	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[FORCE]
Thermal shutdown	Die temperature $\geq$ TSD <sub>THRESHOLD</sub>	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[TSD]
SLEEP	IC exited SLEEP mode	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[SLEEP]
OT2	$V_{TS2} > V_{OT}$ for $t_{OT}$	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[OT2]
OT1	$V_{TS1} > V_{OT}$ for $t_{OT}$	ALERT_S	ALERT_H	ALERT	ALERT_STATUS[OT1]

(1) The CRC fault may be prevented from setting the FAULT pin by setting IO\_CONFIG[7] = 1. The FAULT\_STATUS[CRC] bit is still set when CRC error is detected, but the FAULT pin remains de-asserted.

#### 7.3.1.12.1 Fault Recovery Procedure

When any error flag in DEVICE\_STATUS[], FAULT\_STATUS[], or ALERT\_STATUS[] is set and latched, the state can only be cleared by host communication via SPI. Writing to the respective FAULT\_STATUS or ALERT\_STATUS register bit with a 1 clears the latch for that bit. The exceptions are the two FORCE bits, which are cleared by writing a 0 to the bit.

The FAULT\_STATUS[] and ALERT\_STATUS[] register bits are read-only, with the exception of the FORCE bit, which may be directly written to either a 1 or 0.

#### 7.3.1.13 Secondary Protector Built-In Self-Test Features

The secondary protector functions have built-in test for verifying the connections through the signal chain of ICs in the stack back to the host CPU. This verifies the wiring, connections, and signal path through the ICs by forcing a current through the signal path.

To implement this feature, host firmware should set the FAULT[FORCE] or ALERT[FORCE] bit in the top-most device in the stack. The device asserts the associated pin on the South interface, and it propagates down the stack, back to the base device. The base device in turn asserts the FAULT\_H (ALERT\_H) pin to the host, allowing the host to check for the received signal and thereby verify correct operation.

### 7.3.2 Cell Balancing

The bq76PL536A-Q1 has six dedicated outputs (CB1...CB6) that can be used to control external N-FETs as part of a cell balancing system. The implementation of appropriate algorithms is controlled by the system host. The CB\_CTRL[CBAL1–6] bits control the state of each of the outputs. The outputs are copied from the bit state of the CB\_CTRL register, that is, a 1 in this register activates the external balance FET by placing a high on the associated pin.

The CBx pins switch between approximately the positive and negative voltages of the cell across which the external FET is connected. This allows the use of a small, low-cost N-FET in series with a power resistor to provide cell balancing.

### 7.3.2.1 Cell Balance Control Safety Timer

The CBx outputs are cleared when the internal safety timer expires. The internal safety timer (CB\_TIME) value is programmed in units of seconds or minutes (range set by CB\_CTRL bit 7) with an accuracy of  $\pm 10\%$ .

The timer begins when any CB\_CTRL bit changes from 0 to 1. The timer is reset if all CB\_CTRL bits are modified by the host from 1 to 0, or by expiration of the timing period. The timing begins counting the programmed period from start **each time** the CB\_CTRL[] register is programmed from a zero to a non-zero value in the lower six bits. In the example, if the CB\_TIME[] is set for 30 s, then one or more bits are set in the CB\_CTRL[] register to balance the corresponding cells; then after 10 s, the user firmware sets CB\_CTRL[] to 0x00, takes a measurement, and then reprograms CB\_CTRL[] with the same or new bit pattern and the timer begins counting 30 s again before expiring and disabling balancing. This restart occurs each time the CB\_CTRL bits are set to a non-zero value. If this is done at a greater rate than the balancing period for which timer CB\_TIME[] is set, balancing is effectively never disabled – until the timer is either allowed to expire without changing the CB\_CTRL[] register to a non-zero value, or the CB\_CTRL[] register is set to zero by the user firmware. If the CB\_CTRL[] register is not manipulated from zero to non-zero while the timer is running, the timer expires as expected. Alterations of the value from a non-zero to a different non-zero value *do not* restart the timer (such as, from 0x02 to 0x03, and so forth).

While the timer is running, the host may set or reset any bit in the CB\_CTRL[] register at any time, and the CBx output follows the bit.

The host may re-program the timer at any time. The timer must always be programmed to allow the CBx outputs to be asserted. While the timer is non-zero, the CB\_CTRL[] settings are reflected at the outputs.

During periods when the timer is actively running (not expired), then DEVICE\_STATUS[CBT] is set.

### 7.3.3 Other Features and Functions

#### 7.3.3.1 Internal Voltage Regulators

The bq76PL536A-Q1 derives power from the BAT pin using several internal low dropout (LDO) voltage regulators. There are separate LDOs for internal analog circuits (5 V at LDOA), digital circuits (5 V at LDOD1 and LDOD2), and external, user circuits (5 V at REG50). The BAT pin should be connected to the most-positive cell input from cell 3, 4, 5, or 6, depending on the number of cells connected. Locate filter capacitors as close to the IC as possible. The internal LDOs and internal  $V_{REF}$  should not be used to power external circuitry, with the exception that LDODx should be used to source power to any external pull-up resistors.

##### 7.3.3.1.1 Internal 5-V Analog Supply

The internal analog supply should be bypassed at the LDOA pin with a good quality, low-ESR, 2.2- $\mu$ F ceramic capacitor.

##### 7.3.3.1.2 Internal 5-V Digital Supply

The internal digital supply should be bypassed at the LDOD1(2) pin with a good-quality, low-ESR, 2.2- $\mu$ F ceramic capacitor. The two pins are connected internally and provided to enhance single-pin failure-mode fault tolerance. They should also be connected together externally.

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**注**

For the Designer: Because the LDODx inputs are pulled to approximately 7 V during programming, programming time **MUST** be < 50 ms.

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##### 7.3.3.1.3 Low-Dropout Regulator (REG50)

The bq76PL536A-Q1 has a low-dropout (LDO) regulator provided to power the thermistors and other external circuitry. The input for this regulator is  $V_{BAT}$ . The output of REG50 is typically 5 V. A minimum 2.2- $\mu$ F capacitor is required for stable operation. The output is internally current-limited. The output is reduced to near zero if excess current is drawn, causing die temperatures to rise to unacceptable levels.

The 2.2- $\mu$ F output capacitor is required whether REG50 is used in the design or not.

REG50 is disabled in SLEEP mode, and may be turned off under thermal-shutdown conditions, and therefore should not be used as a pull-up source for terminating device pins where required.

### 7.3.3.1.4 Auxiliary Power Output (AUX)

The bq76PL536A-Q1 provides an approximately 1-mA auxiliary power output that is controlled via IO\_CONTROL[AUX]. This output is taken directly from REG50. The current drawn from this pin must be included in the REG50 current-limit budget by the designer.

### 7.3.3.2 Undervoltage Lockout and Power-On Reset

The device incorporates two comparators to detect low  $V_{BAT}$  conditions. The first detects low voltage where some device digital operations are still available. The second, (POR) detects a voltage below which device operation is **not** ensured.

#### 7.3.3.2.1 UVLO

When the UVLO threshold voltage is sensed for a period  $\geq UVLO_{DELAY}$ , the device is no longer able to make accurate analog measurements and conversions. The ADC, cell-balancing and fault-detection circuitry are disabled. The digital circuitry, including host CPU and vertical communications between ICs, is fully functional. Register contents are preserved with the exception that CB\_CTRL is set to 0, and the UVLO bit is set in DEVICE\_STATUS[.].

#### 7.3.3.2.2 Power-On Reset (POR)

When the POR voltage threshold or lower is sensed for a period  $\geq UVLO_{DELAY}$ , the device is no longer able to function reliably. The device is disabled, including all fault-detection circuitry, host SPI communications, vertical communications, and so forth.

After the voltage rises above the hysteresis limit longer than the delay time, the device exits the reset state, with all registers set to default conditions. The FAULT\_STATUS[POR] bit is set and latched until reset by the host. The device no longer has a valid address (DEVICE\_ADDRESS[AR] = 0, ADDRESS\_CONTROL[] = 0). The device should be reprogrammed with a valid address, and any registers re-written if non-default values are desired.

#### 7.3.3.2.3 Reset Command

The bq76PL536A-Q1 can also be reset by writing the reset code (0xa5) to the RESET register. All devices respond to a broadcast RESET command regardless of their current assigned address. The result is identical to a POR with the exception that the normal POR period is reduced to several hundred microseconds.

### 7.3.3.3 Thermal Shutdown (TSD)

The bq76PL536A-Q1 contains an integrated thermal shutdown circuit whose sensor is located near the REG50 LDO and has a threshold of  $T_{SD}$ . When triggered, the REG50 regulator reduces its output voltage to zero, and the ADC is turned off to conserve power. The thermal shutdown circuit has a built-in hysteresis that delays recovery until the die has cooled slightly. When the thermal shutdown is active, the DEVICE\_STATUS[TSD] bit is set. The IO\_CONTROL[SLEEP] and ALERT[SLEEP] bits also become set to reduce power consumption.

#### **CAUTION**

The secondary protector settings are DISABLED in the TSD state.

Temperature measurement and monitoring do not function due to loss of power if the thermistors are powered from the REG50 or AUX pins and TSD occurs. Protection-dependent schemes implemented by the designer which depend on the REG50 voltage also may not function as a result of loss of the REG50 output.

### 7.3.3.4 GPIO

The bq76PL536A-Q1 includes a general-purpose input/output pin controlled by the IO\_CONTROL[GPIO\_OUT] bit. The state of this bit is reflected on the pin. To use the pin as an input, program GPIO\_OUT to a 1, and then read the IO\_CONTROL[GPIO\_IN] bit. A pull-up (10 k $\Omega$ –1 M $\Omega$ , typ.) is required on this pin if used as an input. *If the pull-up is not included in the design, system firmware must program a 0 in IO\_CONTROL[GPIO\_OUT] to prevent excess current draw from the floating input. Use of a pull-up is recommended in all designs to prevent an unintentional increase in current draw.*

### 7.3.4 Communications

#### 7.3.4.1 SPI Communications – Device to Host

Device-to-host (D2H) mode is provided on the SPI interface pins for connection to a local host microcontroller, logic, and so forth. D2H communications operate in voltage mode as a standard SPI interface for ease of connection to the outside world from the bq76PL536A-Q1 device. Standard TTL-compatible logic levels are presented. All relevant SPI timing and performance parameters are met by this interface.

The host interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. The SPI clock is normally low; data changes on rising edges, and is sampled on the falling edge. All transfers are MSB-first.

The pins of the base IC (only) in a stack should have the SCLK\_H and SDI\_H pins terminated with pull-ups to minimize current draw of the part if the host ever enters a state where the pins are not driven, that is, held in the high-impedance state by the host. In non-base devices, the \_H pins are forced to be all outputs driven low when the HSEL pin is high. In non-base devices, all \_H pins should remain unconnected.

The CS\_H has a pull-up resistor of approximately 100 kΩ. SDO\_H is a 3-state output and is terminated with a weak pull-up.

#### 注

For the Designer: When  $V_{BAT}$  is at or below the UVLO trip point voltage, the internal LDO which supplies the xxxx\_H host SPI communications pins (VLODx) begins to fall out of regulation. The output high voltage on the xxxx\_H pins falls off with the LDO voltage in an approximately linear manner until at the POR voltage trip point it is reduced to approximately 3.5 V. This action is not tested in production.

#### 7.3.4.2 Device-to-Device Vertical Bus (VBUS) Interface

Device-to-device (D2D) communications makes use of a unique, current-mode interface which provides common-mode voltage isolation between successive bq76PL536A-Q1s. This *vertical bus* (VBUS) is found on the \_N and corresponding \_S pins. It provides high-speed I/O for both the SPI bus and the direct I/O pins CONV and DRDY. The current-mode interface minimizes the effects of wiring capacitance on the interface speed.

The \_S (south-facing) pins connect to the next-lower device (operating at a lower potential) in the stack of bq76PL536A-Q1s. The \_N (North facing) pins connect to the next-higher device. The pins cannot be swapped; \_S always points South, and \_N always point North. The \_S and \_N pins are interconnected to the pin with the same name, but opposite suffix. All pins operate within the voltages present at the BAT and VSS pins.

#### WARNING

**Use caution; these pins may be several hundred volts above system ground, depending on their position in the stack.**

#### 注

For the Designer: North (\_N) pins of the top, most-positive device in the stack should be connected to the BAT1(2) pins of the device for correct operation of the string. South (\_S) pins of the lowest, most-negative device in the stack should be connected to VSS of the device.

The number of devices in the vertical stack and other factors limit the maximum SCLK frequency. Each device imposes an approximately 30-ns delay on the round trip communications speed, that is, from SCLK rising (an input to all devices) to the SDO pin transitioning requires approximately 30 ns per device. The designer must add to this the delay caused by the PCB trace (in turn determined by the material and layout), any connectors in series with the connection, and any other wiring or cabling between devices in the system. To maximize speed, these other system components should be carefully selected to minimize delays and other detrimental effects on signal quality. Wiring and connectors should receive special attention to their transmission line characteristics.

Other factors, which should be considered, are clock duty cycle, clock jitter, temperature effects on clock and system components, user-selected drive level for the level-shift interface, and desired design margin.

The VBUS SPI interface is placed in a low-power mode when CS\_H is not asserted on the base device.

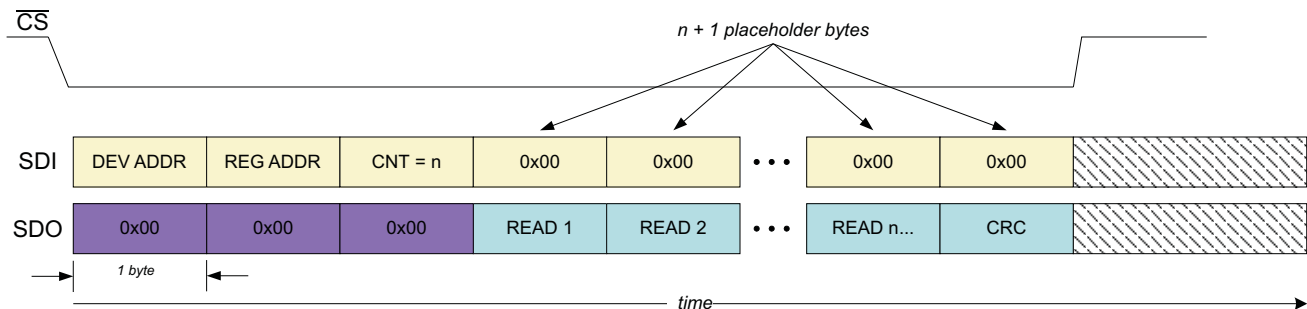
The CS\_N/S pins are asserted by a logic high on the vertical interface bus (logically inverted from CS\_H). This creates a default VBUS CS condition of logic low, reducing current consumption to a minimum.

To reduce power consumption of the SPI interface to a minimum, the SCLK\_H and SDI\_H should be maintained at a logic low (de-asserted) while CS\_H is asserted (low). Most SPI buses are operated this way by microcontrollers. The VBUS versions of these signals are not inverted from the host interface. The device also de-asserts by default the SDO\_N/S pins to minimize power consumption.

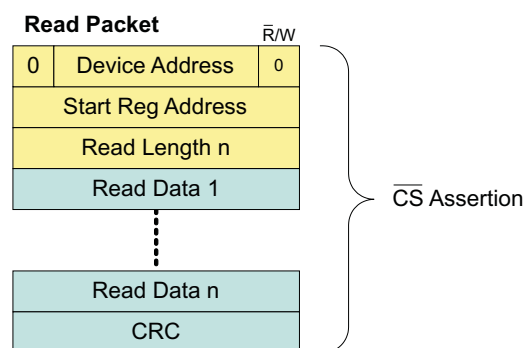
### 7.3.4.3 Packet Formats

#### 7.3.4.3.1 Data Read Packet

When the bq76PL536A-Q1 is selected (CS\_S [CS\_H for first device] is active and the bq76PL536A-Q1 has been addressed) and read request has been initiated, then the data is transmitted on the SDO\_S pin to the SDO\_N pin of the next device down the stack. This continues to the first device in the stack, where the data in from the SDO\_N pin is transmitted to the host via the SDO\_H pin. The device supplying the read data generates a CRC as the last byte sent. See [图 18](#) and [图 19](#) for additional information.



**图 18. READ Packet Format**



**图 19. READ Packet Detail**

#### 7.3.4.3.2 Data Write Packet

When the bq76PL536A-Q1 is selected (CS\_S is active and the bq76PL536A-Q1 has been addressed) and a write request has been initiated, the bq76PL536A-Q1 receives data through the SDI\_S pin, which is connected to the SDO\_N of the lower device. For the first device in the stack, the data is input to the SDI\_H pin from the host, and transmitted up the stack on the SDI\_S pin to the SDI\_N pin of the next higher device. If enabled, the device checks the CRC, which it expects as the last byte sent. If the CRC is valid, no action is taken. If the CRC is invalid or missing, the device asserts the ALERT\_S signal to the next lower device, which ripples down the stack to the ALERT\_H pin on the lowest device. The host should then take action to clear the condition. See [图 20](#) and [图 21](#) for details.

Unused or undefined register bits should be written as zeroes.

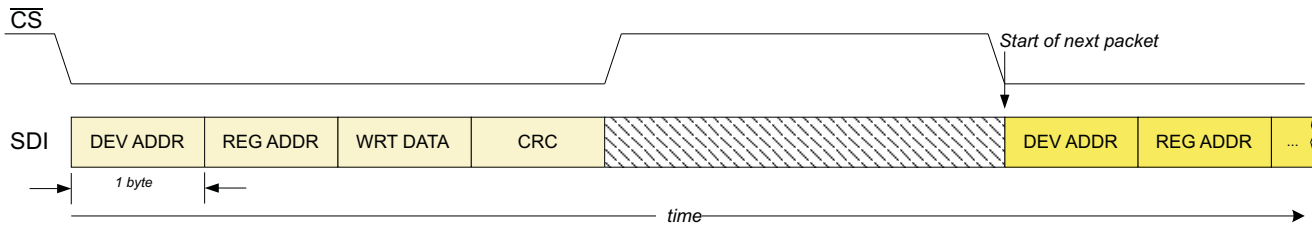


图 20. WRITE Packet Format

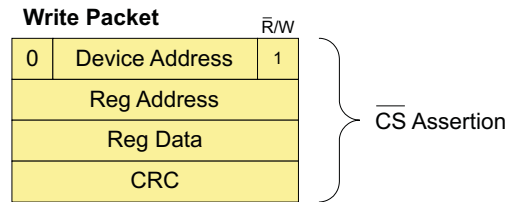


图 21. WRITE Packet Detail

#### 7.3.4.3.3 Broadcast Writes

The bq76PL536A-Q1 supports broadcasting single register writes to all devices. A write to device address 0x3f is recognized by all devices on the bus with a valid address, and permits efficient simultaneous configuration of all registers in the stack of devices. This also permits synchronizing all ADC conversions by a firmware command sent to the CONVERT\_CTRL[] register as an alternative to using the CONV and DRDY pins.

#### 7.3.4.3.4 Communications Packet Structure

The bq76PL536A-Q1 has two primary communication modes via the SPI interface. These two modes enable single-byte read / write and multiple data reads. All writes are single-byte; the logical address is shifted one bit left, and the LSB = 1 for writing.

All transactions are in the form of packets comprising:

表 4. Communication Packet Order

BYTE	DESCRIPTION
#1	6-bit bq76PL536A-Q1 slave address + R/W bit 0b0xxx xxxW
#2	Starting data-register offset
#3	Number of data bytes to be read (n) (omitted for writes)
#4 to 3+n	Data bytes
#4+n	CRC (omit if IO_CONFIG[CRC_DIS] = 1)

### 7.3.4.3.5 CRC Algorithm

The cyclic redundancy check (CRC) is a CRC-8 error-checking byte, calculated on all the message bytes (including addresses). It is identical in structure to the SMBus 2.0 packet error check (PEC), and is also known as the ATM-8 CRC. The CRC is appended to the message for all SPI packets by the device that supplied the data as the last byte in the packet (when `IO_CONTROL[CRC] == 1`).

Each bus transaction requires a CRC calculation by both the transmitter and receiver within each packet. The CRC is calculated in a way that conforms to the polynomial,  $C(x) = x^8 + x^2 + x^1 + 1$  and must be calculated in the order of the bits as received, MSB first. The CRC calculation includes all bytes in the transmission, including address, command, and data. When reading data from the device, the CRC is based on the `ADDRESS + FIRST_REGISTER + LENGTH + returned_device_data[n]`. The stuff-bytes used to clock out the data from the IC are not used as part of the calculation, although if the value `0x00` is used, the 0s have no effect on the CRC.

CRC verification is performed by the receiver when the `CS_x` line goes false, indicating the end of a packet. If the CRC verification fails, the message is ignored (discarded), the CRC failure flag is set in the `FAULT_STATUS[CRC]` register, and the `FAULT` line becomes asserted and latched until the error is read and cleared by the host.

The CRC bit returned in the `FAULT_STATUS[]` register reflects the last packet received, not the CRC condition of the packet reading the `FAULT_STATUS` contents. CRC errors should be handled at a high priority by the host controller, before writing to additional registers.

### 7.3.4.3.6 Data Packet Usage Examples

The bq76PL536A-Q1 can be enabled via the host to read just the specific voltage data which would require a total of 2 written bytes (chip address and R/W [#1] + first (starting) register offset [#2]) + `LENGTH` [#3] and 13 <null> stuff bytes (12 [n] data bytes + CRC).

The data packet can be expanded periodically to accommodate temperature and GPAI readings as well as device status as needed by changing the `REGISTER_FIRST` offset and `LENGTH` values.

### 7.3.4.4 Device Addressing

Each individual device, in the series stack, requires an address to allow communication with it. Each bq76PL536A-Q1 has a `CS_S` and `CS_N` that are used in assigning addresses. Once addresses have been assigned, the normal operation of the `CS_N/S` lines is asserted (logic high) during communications, and the appropriate bq76PL536A-Q1 in the stack responds according to the address transmitted as part of the packet (图 22).

When the bq76PL536A-Q1 is reset, the `DEVICE_STATUS[AR]` (address request) flag is cleared, the address register is set to `0x00`, and `ALERT_S` is set and passed down the stack. In this state, where `address = 0x00`, the `CS_N` signal is forced to a de-asserted state (`CS` is not passed north when an `address = 0`). In this manner, after a reset the host is assured that a response at `address 0x00` is from the first physical device in the stack. After address assignment of the current device, the host is assured that the next response at `address 0x00` is from the next physical device in the stack.

Once a valid address is assigned to the device, the `CS_N` signal responds normally, and follows the `CS_H` or `CS_S` signal, propagating to the next device in the stack. Valid addresses are in the range `0x01` through `0x3e`. `0x00` is reserved for device discovery after reset. `0x3f` is reserved as a broadcast address for all devices.

#### 注

For the Designer: Broadcast messages are only received by devices with a valid address, and the next higher device. Any device with an address of `0x00` blocks messages to devices above it. A broadcast message may not be received by all devices in a stack in situations where some devices do not have a valid address.

Once the address is written, the `ADDRESS_CONTROL[AR]` bit is set which is copied to the `DEVICE_STATUS[AR]` and also `ALERT_S` if `ALERT_N` is also de-asserted. This allows the `CS_N` pin to follow (asserted) the `CS_S` pin assertions. The process of addressing can now be repeated as device 'n' has a new address and device n+1 has the default address of `0x00`, and can be changed to its *correct* address in the stack.



If a device loses its address through a POR or it is replaced, then this device will be the highest logical device in the stack able to be addressed (0x00), as its CS\_N will be disabled and the addressing process is required for this and higher devices.

All devices:  
ADDRESS = 0x?? (unknown)  
expected = # devices in stack

Note: validated = one more than  
devices found at this point

Assign unique address (n) to  
this device @address 0x00

Validation test: Read same  
device for unique address (n)  
just assigned

Validate device was  
successfully found and  
addressed

This loop finds one *new*  
device per iteration

(Implied: n == look\_for here)

This loop resets all addressed  
devices, then looks for all  
previously found+1 devices  
again. Corrects any  
addressing faults in the stack

(Implied: n == expected here)

All devices found?

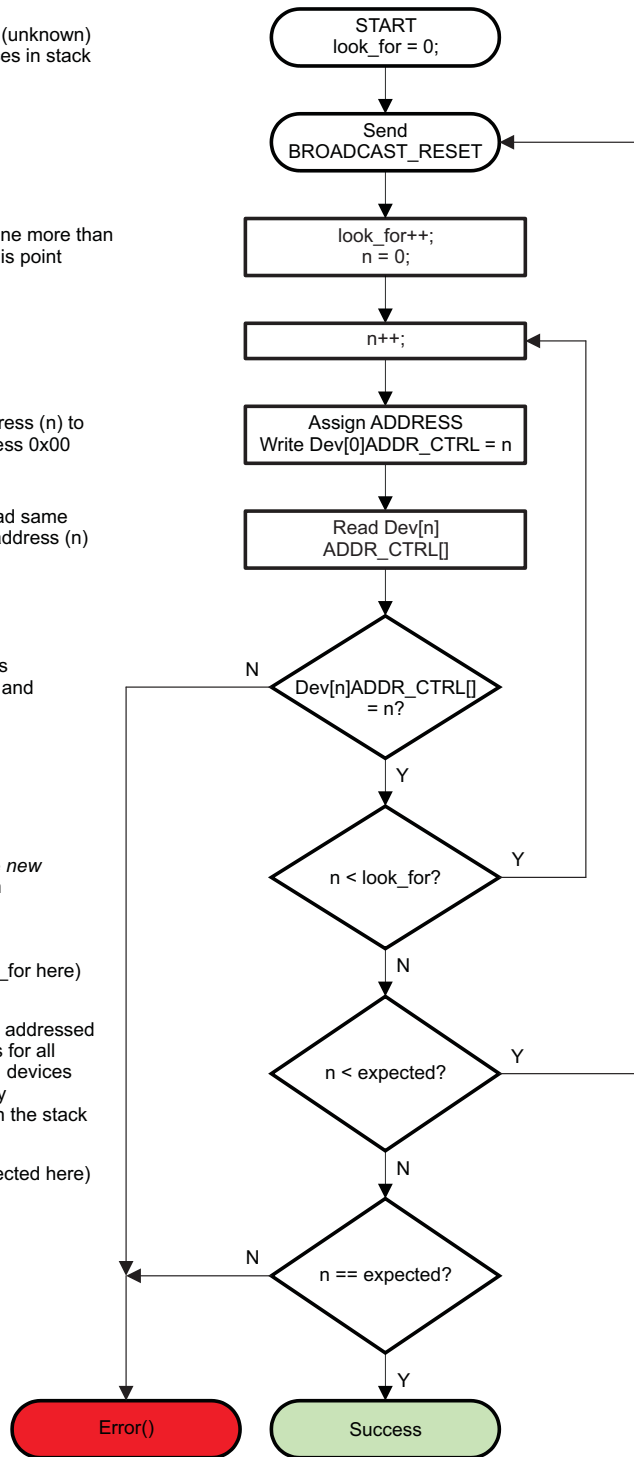


图 22. Address Discovery and Assignment Algorithm

## 7.4 Device Functional Modes

### 7.4.1 SLEEP Functionality

The bq76PL536A-Q1 provides the host a mechanism to put the part into a low-power sleep state by setting the IO\_CONTROL[SLEEP] bit. When this bit is set/reset, the following actions occur as stated in the following paragraphs.

#### 7.4.1.1 SLEEP State Entry (Bit Set)

If a conversion is in progress, the device waits for it to complete, then sets DRDY true (high).

The device sets the ALERT\_STATUS[SLEEP] bit, which in turn causes the ALERT pin to be asserted.

The device gates off all other sources of FAULT or ALERT *except* ALERT[SLEEP]. The existing state of the FAULT and ALERT registers is preserved. The host should service and reset the ALERT generated by the SLEEP bit being set to minimize SLEEP state current draw by writing a 1 to ALERT[SLEEP] followed by a 0 to ALERT[SLEEP]. The ALERT North-South signal chain can draw up to approximately 1 mA of current when active, so this ALERT source should be cleared prior to the host entering the SLEEP state of its own. This signaling is provided to notify the host that the unmonitored/unprotected state is being entered.

The REG50 LDO is shut down and the output is allowed to float. The ADC, its reference, and clocks are disabled. The COV, CUV, and OT circuits are disabled, and their band-gap reference shut off.

#### CAUTION

The SLEEP State effectively removes protection and monitoring from the cells; the designer should take the necessary design steps and verifications to ensure the cells cannot be put into an unsafe condition by other parts of the system or usage characteristics.

IO\_CONTROL[TS1:TS2] bits are not modified. The host must also set these bits to zero to minimize current draw of the thermistors themselves.

SPI communications are preserved; all registers may be read or written.

#### 7.4.1.2 SLEEP State Exit (Bit Reset)

VREG50 operation is restored.

COV, CUV, OT circuits are re-enabled.

The ADC circuitry returns to its former state. Note that there is a warm-up delay associated with the ADC enable, the same delay as specified for enabling from a cold start.

The FAULT and ALERT registers are restored to their pre-SLEEP state. If a FAULT or ALERT condition was present prior to SLEEP, the FAULT or ALERT pin is immediately asserted.

IO\_CONTROL[TS1:TS2] should be set by the host if the OT function or temperature measurement functions are desired.

## 7.5 Programming

### 7.5.1 Programming the EPROM Configuration Registers

The bq76PL536A-Q1 has a block of OTP-EPROM that is used for configuring the operation of the bq76PL536A-Q1. Programming of the EPROM should take place during pack/system manufacturing. A 7-V ( $V_{PP}$ ) pulse is required on the PROG pin. The part uses an internal window comparator to check the voltage, and times the internal pulse delivered to the EPROM array.

## Programming (接下页)

The user first writes the desired values to all of the equivalent Group3 protected register addresses. The desired data is written to the appropriate address by first applying 7 V to the LDOD1(2) pins. Programming then performed by writing to the EE\_EN register (address 0x3f) with data 0x91. After a time period > 1500  $\mu$ s, the 7 V is removed. Nominally, the voltage pulse should be applied for approximately 2–3 ms. Applying the voltage for an extended period of time may lead to device damage. The write is self-timed internally after receipt of the command. The following flow chart (图 23) illustrates the procedure for programming.

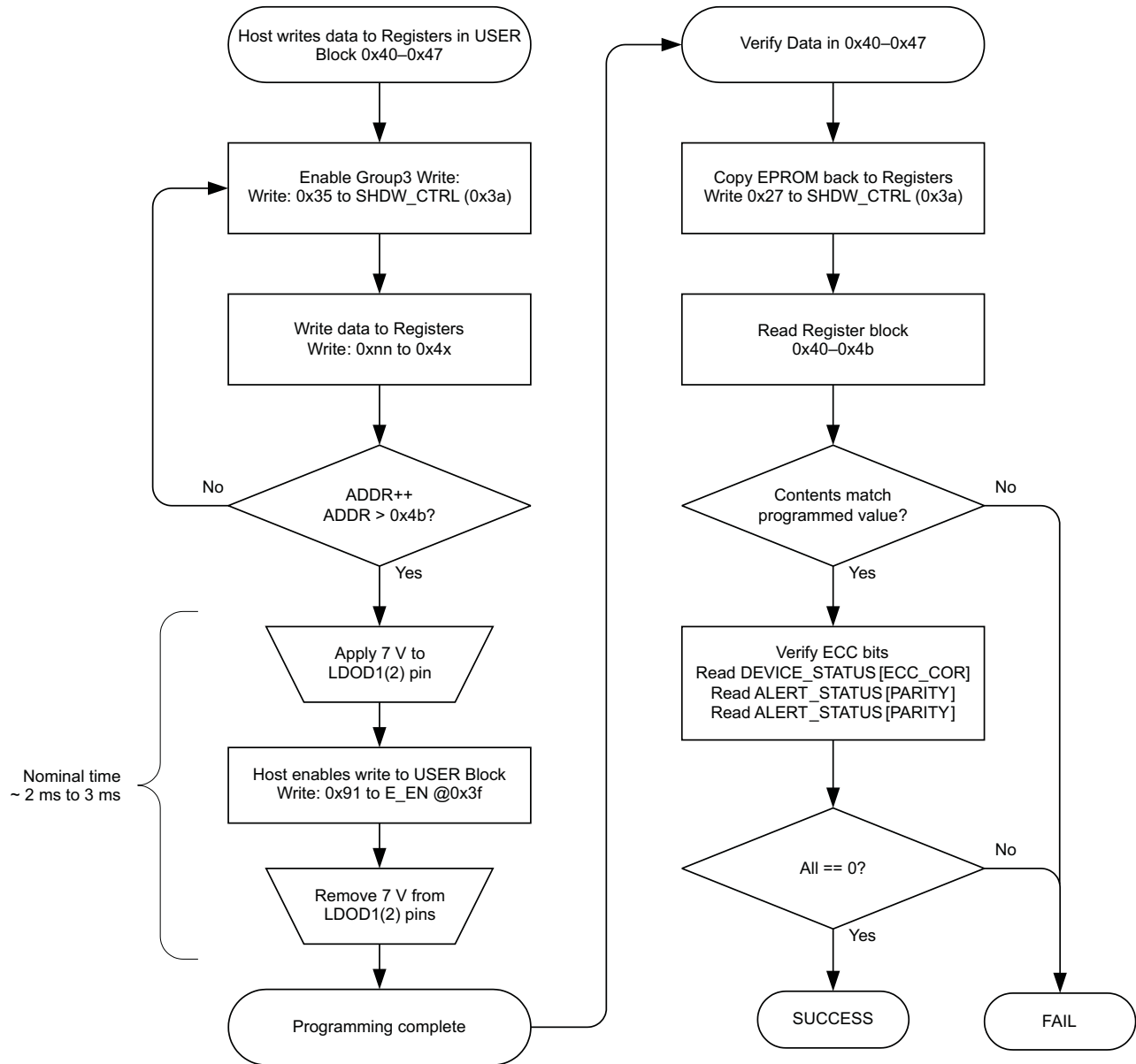


图 23. EPROM Programming

## 7.6 Register Maps

### 7.6.1 I/O Register Details

The bq76PL536A-Q1 has 48 addressable I/O registers. These registers provide status, control, and configuration information for the battery protection system. Reserved registers return 0x00. Unused registers should not be written to; the results are undefined. Unused or undefined bits should be written as zeroes, and will always read back as zeroes. Several types of registers are provided, details are in the following sections and tables.

### 7.6.2 Register Types

#### 7.6.2.1 Read-Only (Group 1)

These registers contain the results of conversions, or device status information set by internal logic. The contents are re-initialized by a device reset as a result of either POR or the RESET command. Contents of the register are changed by either a conversion command, or when there is an internal state change (that is, a fault condition is sensed).

#### 7.6.2.2 Read / Write (Group 2)

The Read/Write register group modifies the operations or behavior of the device, or indicates detailed status in the ALERT\_STATUS[] and FAULT\_STATUS[] registers (图 24). The contents are re-initialized by a device reset as a result of either POR or the RESET command. Contents of the register are changed either by a conversion command, or when there is an internal state change (that is, a fault condition is sensed).

Contents may also be changed by a write from the host CPU to the register. Writes may only modify a single register at a time. If CRCs are enabled, the write packet is buffered until the CRC is checked for correctness. Packets with bad CRCs are discarded without writing the value to the register, after setting the FAULT\_STATUS[CRC] flag.

Unused or undefined bits in any register should be written as zeroes, and will always read back as zeroes.

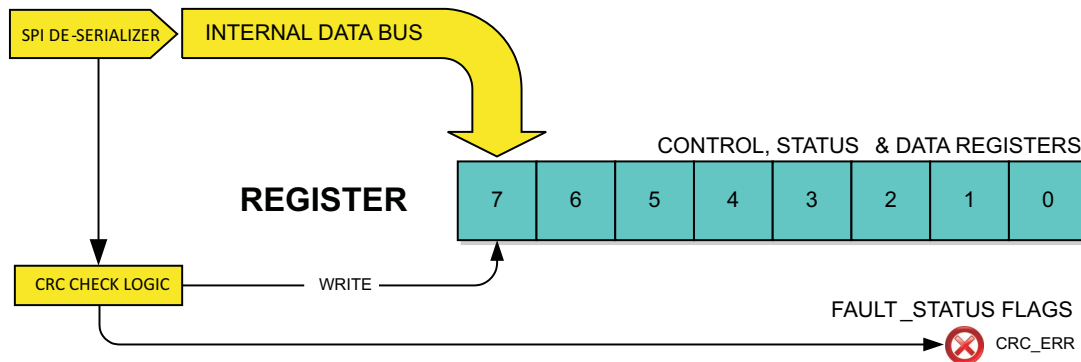


图 24. Register Group2 Architecture

#### 7.6.2.3 Read / Write, Initialized From EPROM (Group3)

These registers control the device configuration and functionality. The contents of the registers are initialized from EPROM-stored constants as a result of POR, RESET command, or the RELOAD\_SHADOW command. This feature ensures that the secondary protector portion of the device (COV, CUV, OT) is fully functional after any reset, without host CPU involvement. See 图 25 for a simplified view.

These registers may only be modified by using a special, sequential-write sequence to guard against accidental changes. The value loaded from EPROM at reset (or by command) may be temporarily overwritten by using the special write sequence. The temporary value is overwritten to the programmed EPROM initialization value by the next reset or command to reload. To write to a these protected registers, first write 0x35 to SHDW\_CONTROL[], immediately followed by the write to the desired register. Any intervening write cancels the special sequence.

To re-initialize the entire set of Group3 registers to the EPROM defaults, write the value 0x27 to SHDW\_CONTROL[].

## Register Maps (接下页)

These registers are protected further against corruption by a ninth parity bit that is automatically updated when the register is written using even parity. If the contents of the register ever become corrupted, the bad parity causes the ALERT\_STATUS[PARITY] bit to become set, alerting the host CPU of the problem.

The EPROM-stored constants are programmed by writing the values to the register(s), then applying the programming voltage to the LDODx pins, then issuing the EPROM\_WRITE command to register E\_EN[]. All Group3 registers are programmed simultaneously, and this operation can only be performed once to the one-time-programmable (OTP) memory cells. The process is not reversible.

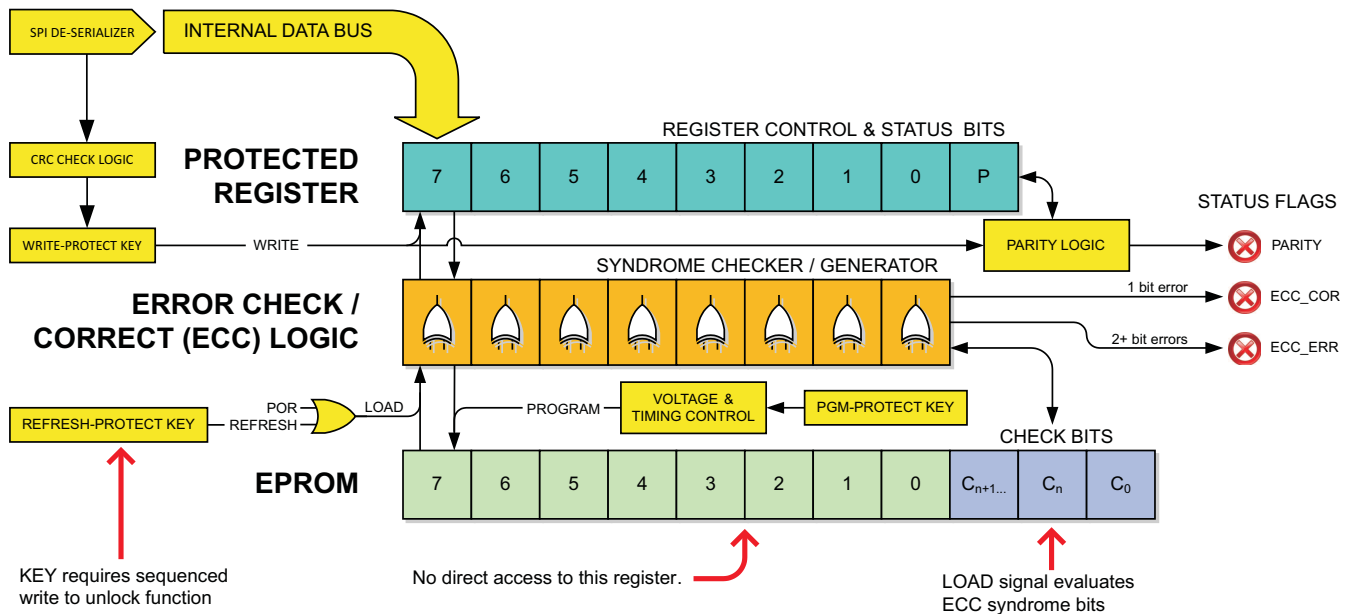


图 25. Protected Register Group3 Architecture, Simplified View

### 7.6.2.4 Error Checking and Correcting (ECC) EPROM

The EPROM used to initialize this group is also protected by error-check-and-correct (ECC) logic. The ECC bits provide a highly reliable storage solution in the presence of external disturbances. This feature cannot be disabled by user action. Implementation is fully self-contained and automatic and requires no special computations or provisioning by the user.

When the Group3 contents are permanently written to EPROM, an additional array of hidden ECC-OTP cells is also automatically programmed. The ECC logic implements a Hamming code that automatically corrects all single-bit errors in the EPROM array, and senses additional multi-bit errors. If any corrections are made, the DEVICE\_STATUS[ECC\_COR] flag bit is set. If any multi-bit errors are sensed, the ALERT\_STATUS[ECC\_ERR] flag is set. The corrective action or detection is performed anytime the contents of EPROM are loaded into the registers – POR, RESET, or by REFRESH command. *Note: The ECC\_COR and ECC\_ERR bits may glitch during OTP-EPROM writes; this is normal. If this occurs, reset the tripped bit; it should remain cleared.*

When a double-bit (uncorrectable) error is found, DEVICE\_STATUS[ALERT] is set, the ALERT\_S (ALERT\_H for bottom stack device) line is activated, and the ALERT\_STATUS[] register returns the ECC\_ERR and/or I\_FAULT bit = 1(true). *The device may return erroneous measurement data, and/or fail to detect COV, CUV, or OT faults in this state.*

EPROM bits are shipped from the factory set to 0 and must be programmed to the 1 state, as required.

**Register Maps (接下页)**
**表 5. Data and Control Register Descriptions**

NAME	ADDR	GROUP	ACCESS <sup>(1)</sup>	RESET	DESCRIPTION
DEVICE_STATUS	0x00	1	R	0	Status register
GPAI	0x01, 0x02	1	R	0	GPAI measurement data
VCELL1	0x03, 0x04	1	R	0	Cell 1 voltage data
VCELL2	0x05, 0x06	1	R	0	Cell 2 voltage data
VCELL3	0x07, 0x08	1	R	0	Cell 3 voltage data
VCELL4	0x09, 0x0a	1	R	0	Cell 4 voltage data
VCELL5	0x0b, 0x0c	1	R	0	Cell 5 voltage data
VCELL6	0x0d, 0x0e	1	R	0	Cell 6 voltage data
TEMPERATURE1	0x0f, 0x10	1	R	0	TS1+ to TS1– differential voltage data
TEMPERATURE2	0x11, 0x12	1	R	0	TS2+ to TS2– differential voltage data
RSVD	0x13–0x1f	—	—	—	Reserved for future use
ALERT_STATUS	0x20	2	R/W	0x80	Indicates source of ALERT signal
FAULT_STATUS	0x21	2	R/W	0x08	Indicates source of FAULT signal
COV_FAULT	0x22	1	R	0	Indicates cell in OV fault state
CUV_FAULT	0x23	1	R	0	Indicates cell in UV fault state
PRESULT_A	0x24	1	R	0	Parity result of Group3 protected registers (A)
PRESULT_B	0x25	1	R	0	Parity result of Group3 protected registers (B)
RSVD	0x26–0x2f	—	—	—	Reserved for future use
ADC_CONTROL	0x30	2	R/W	0	ADC measurement control
IO_CONTROL	0x31	2	R/W	0	I/O pin control
CB_CTRL	0x32	2	R/W	0	Controls the state of the cell-balancing outputs CBx
CB_TIME	0x33	2	R/W	0	Configures the CB control FETs maximum on time
ADC_CONVERT	0x34	2	R/W	0	ADC conversion start
RSVD	0x35–0x39	—	—	—	Reserved for future use
SHDW_CTRL	0x3a	2	R/W	0	Controls WRITE access to Group3 registers
ADDRESS_CONTROL	0x3b	2	R/W	0	Address register
RESET	0x3c	2	W	0	RESET control register
TEST_SELECT	0x3d	2	R/W	0	Test mode selection register
RSVD	0x3e	—	—	—	Reserved for future use
E_EN	0x3f	2	R/W	0	EPROM programming mode enable
FUNCTION_CONFIG	0x40	3	R/W	EPROM	Default configuration of device
IO_CONFIG	0x41	3	R/W	EPROM	I/O pin configuration
CONFIG_COV	0x42	3	R/W	EPROM	Overvoltage set point
CONFIG_COVT	0x43	3	R/W	EPROM	Overvoltage time-delay filter
CONFIG_CUV	0x44	3	R/W	EPROM	Undervoltage set point
CONFIG_CUVT	0x45	3	R/W	EPROM	Undervoltage time-delay filter
CONFIG_OT	0x46	3	R/W	EPROM	Overtemperature set point
CONFIG_OTT	0x47	3	R/W	EPROM	Overtemperature time-delay filter
USER1	0x48	3	R	EPROM	User data register 1, not used by device
USER2	0x49	3	R	EPROM	User data register 2, not used by device
USER3	0x4a	3	R	EPROM	User data register 3, not used by device
USER4	0x4b	3	R	EPROM	User data register 4, not used by device
RSVD	0x4c–0xff	—	—	—	Reserved

(1) Key: R = Read; W = Write

### 7.6.3 Register Details

#### 7.6.3.1 DEVICE\_STATUS Register (0x00)

The STATUS register provides information about the current state of the bq76PL536A-Q1.

**图 26. DEVICE\_STATUS Register**

7	6	5	4	3	2	1	0
AR	FAULT	ALERT	—	ECC_COR	UVLO	CBT	DRDY

- [7] (ADDR\_RQST): This bit is written to indicate that the ADDR[0]...[5] bits have been written to the correct address. This bit is a copy of in the ADDRESS\_CONTROL[AR] bit.
- 0 = Address has not been assigned
  - 1 = Address has been assigned
- [6] (FAULT): This bit indicates that this bq76PL536A-Q1 has detected a condition causing the FAULT signal to become asserted.
- 0 = No FAULT exists
  - 1 = A FAULT exists. Read FAULT\_STATUS[] to determine the cause.
- [5] (ALERT): This bit indicates that this bq76PL536A-Q1 has detected a condition causing the ALERT pin to become asserted.
- 0 = No FAULT exists
  - 1 = An ALERT exists. Read ALERT\_STATUS[] to determine the cause.
- [4] (not implemented)
- [3] (ECC\_COR): This bit indicates a one-bit error has been detected and corrected in the EPROM.
- 0 = No errors are detected in the EPROM
  - 1 = A one-bit (single bit) error has been detected and corrected by on-chip logic.
- [2] (UVLO): This bit indicates the device VBAT has fallen below the undervoltage lockout trip point. Some device operations are not valid in this condition.
- 0 = Normal operation
  - 1 = UVLO trip point reached, device operation is **not** ensured.
- [1] (CBT): This bit indicates the cell balance timer is running.
- 0 = The cell balance timer is has not started or has expired.
  - 1 = The cell balance timer is running.
- [0] (DRDY): This bit indicates the data is ready to read (no conversions active).
- 0 = There are conversion(s) running.
  - 1 = There are no conversion(s) running.

### 7.6.3.2 GPAI (0x01, 0x02) Register

The GPAI register reports the ADC measurement of GPAI+/GPAI– in units of LSBs.

Bits 15–8 are returned at address 0x01, bits 7–0 at address 0x02.

**图 27. GPAI (0x01, 0x02) Register**

15	14	13	12	11	10	9	8
GPAI[15]	GPAI [14]	GPAI [13]	GPAI [12]	GPAI [11]	GPAI [10]	GPAI [9]	GPAI [8]
7	6	5	4	3	2	1	0
GPAI [7]	GPAI [6]	GPAI [5]	GPAI [4]	GPAI [3]	GPAI [2]	GPAI [1]	GPAI [0]

### 7.6.3.3 VCELLn Register (0x03...0x0e)

The VCELLn registers report the converted data for cell n, where n = 1 to 6.

Bits 15–8 are returned at odd addresses (for example, 0x03), bits 7–0 at even addresses (for example, 0x04).

**图 28. VCELLn Register**

15	14	13	12	11	10	9	8
VCELLn[15]	VCELLn[14]	VCELLn[13]	VCELLn[12]	VCELLn[11]	VCELLn[10]	VCELLn[9]	VCELLn[8]
7	6	5	4	3	2	1	0
VCELLn[7]	VCELLn[6]	VCELLn[5]	VCELLn[4]	VCELLn[3]	VCELLn[2]	VCELLn[1]	VCELLn[0]

### 7.6.3.4 TEMPERATURE1 Register (0x0f, 0x10)

The TEMPERATURE1 register reports the converted data for TS1+ to TS1–.

Bits 15–8 are returned at odd addresses (for example, 0x0f), bits 7–0 at even addresses (for example, 0x10).

**图 29. TEMPERATURE1 Register**

15	14	13	12	11	10	9	8
TEMP1[15]	TEMP1[14]	TEMP1[13]	TEMP1[12]	TEMP1[11]	TEMP1[10]	TEMP1[9]	TEMP1[8]
7	6	5	4	3	2	1	0
TEMP1[7]	TEMP1[6]	TEMP1[5]	TEMP1[4]	TEMP1[3]	TEMP1[2]	TEMP1[1]	TEMP1[0]

### 7.6.3.5 TEMPERATURE2 Register (0x11, 0x12)

The TEMPERATURE2 register reports the converted data for TS2+ to TS2–.

Bits 15–8 are returned at odd addresses (for example, 0x11), bits 7–0 at even addresses (for example, 0x12).

**图 30. TEMPERATURE2 Register**

15	14	13	12	11	10	9	8
TEMP2[15]	TEMP2[14]	TEMP2[13]	TEMP2[12]	TEMP2[11]	TEMP2[10]	TEMP2[9]	TEMP2[8]
7	6	5	4	3	2	1	0
TEMP2[7]	TEMP2[6]	TEMP2[5]	TEMP2[4]	TEMP2[3]	TEMP2[2]	TEMP2[1]	TEMP2[0]



### 7.6.3.6 ALERT\_STATUS Register (0x20)

The ALERT\_STATUS register provides information about the source of the ALERT signal. The host must clear each alert flag by writing a 1 to the bit that is set. The exception is bit 4, which may be written 1 or 0 as needed to implement self-test of the IC stack and wiring.

**图 31. ALERT\_STATUS Register**

7	6	5	4	3	2	1	0
AR	PARITY	ECC_ERR	FORCE	TSD	SLEEP	OT2	OT1

- [7] (AR): This bit indicates that the ADDR[0]...[5] bits have been written to a valid address. This bit is an inverted copy of the ADDRESS\_CONTROL[AR] bit. It is not cleared until an address has been programmed in ADDRESS\_CONTROL and a 1 followed by a 0 (two writes) is written to the bit.
- 0 = Address has been assigned.
  - 1 = Address has not been assigned (default at RESET).
- [6] (PARITY): This bit is used to validate the contents of the protected Group3 registers.
- 0 = Group3 protected register(s) contents are valid.
  - 1 = Group3 protected register(s) contents are invalid. Group3 registers should be refreshed from OTP or directly written from the host.
- [5] (ECC\_ERR): This bit is used to validate the OTP register blocks.
- 0 = No double-bit errors (a corrected one-bit error may/may not exist)
  - 1 = An uncorrectable error has been detected in the OTP-EPROM register bank. OTP-EPROM register(s) are not valid.
- [4] (FORCE): This bit asserts the ALERT signal. It can be used to verify correct operation and connectivity of the ALERT as a part of system self-test.
- 0 = De-assert ALERT (default)
  - 1 = Assert the ALERT signal.
- [3] (TSD): This bit indicates thermal shutdown is active.
- 0 = Thermal shutdown is inactive (default).
  - 1 = Die temperature has exceeded  $T_{SD}$ .
- [2] (SLEEP): This bit indicates SLEEP mode was activated. This bit is only set when SLEEP is first activated; no continuous ALERT or SLEEP status is indicated after the host resets the bit, even if the IO\_CONTROL[SLEEP] bit remains true. (See IO\_CONTROL[] register for details.)
- 0 = Normal operation
  - 1 = SLEEP mode was activated.
- [1] (OT2): This bit indicates an overtemperature fault has been detected via TS2.
- 0 = Temperature is lower than or equal to the  $V_{OT2}$  (or input disabled by IO\_CONTROL[TS2] = 0).
  - 1 = Temperature is higher than  $V_{OT2}$ .
- [0] (OT1): This bit indicates an overtemperature fault has been detected via TS1.
- 0 = Temperature is lower than or equal to the  $V_{OT1}$  (or input disabled by IO\_CONTROL[TS1] = 0).
  - 1 = Temperature is higher than  $V_{OT1}$ .

### 7.6.3.7 FAULT\_STATUS Register (0x21)

The FAULT\_STATUS register provides information about the source of the FAULT signal, see [Error Checking and Correcting \(ECC\) EPROM](#) for more information. The host must clear each fault flag by writing a 1 to the bit that is set. The exception is bit 4, which may be written 1 or 0 as needed to implement self-test of the IC stack and wiring.

**图 32. FAULT\_STATUS Register**

7	6	5	4	3	2	1	0
—	—	I_FAULT	FORCE	POR	CRC	CUV	COV

- [7] Not implemented.
- [6] Not implemented.
- [5] (I\_FAULT): The device has failed an internal register consistency check. Measurement data and protection function status may not be accurate and should not be used.
- 0 = No internal register consistency check fault exists.
  - 1 = The internal consistency check has failed self-test. The host should attempt to reset the devices, see the *RESET* section. If the fault persists, the failure should be considered uncorrectable.
- [4] (FORCE): This bit asserts the FAULT signal. It can be used to verify correct operation and connectivity of the FAULT line as a part of system self-test.
- 0 = De-assert FAULT (default)
  - 1 = Assert the FAULT signal.
- [3] (POR): This bit indicates a power-on reset (POR) has occurred.
- 0 = No POR has occurred since this bit was last cleared by the host.
  - 1 = A POR has occurred. This notifies the host that default values have been loaded to Group1 and Group2 registers and OTP contents have been copied to Group3 registers.
- [2] (CRC): This bit indicates a garbled packet reception by the device.
- 0 = Normal errors
  - 1 = A CRC error was detected in the last packet received.
- [1] (CUV): This bit indicates that this bq76PL536A-Q1 has detected a cell undervoltage (CUV) condition. Examine CUV\_FAULT[] to determine which cell caused the ALERT.
- 0 = All cells are above the CUV threshold (default).
  - 1 = One or more cells are below the CUV threshold.
- [0] (COV): This bit indicates that this bq76PL536A-Q1 has detected a cell overvoltage (COV) condition. Examine COV\_FAULT[] to determine which cell caused the FAULT.
- 0 = All cells are below the COV threshold (default).
  - 1 = One or more cells are above the COV threshold.

**7.6.3.8 COV\_FAULT Register (0x22)**
**图 33. COV\_FAULT Register**

7	6	5	4	3	2	1	0
—	—	OV[6]	OV[5]	OV[4]	OV[3]	OV[2]	OV[1]

[0..5] (OV[1]..[6]): These bits indicate which cell caused the DEVICE\_STATUS[COV] flag to be set.

0 = Cell[n] does not have an overvoltage fault (default).

1 = Cell[n] does have an overvoltage fault.

**7.6.3.9 CUV\_FAULT Register (0x23)**
**图 34. CUV\_FAULT Register**

7	6	5	4	3	2	1	0
—	—	UV[6]	UV[5]	UV[4]	UV[3]	UV[2]	UV[1]

b0..5 (UV[1]..[6]): These bits indicate which cell caused the DEVICE\_STATUS[CUV] flag to be set.

0 = Cell[n] does not have an undervoltage fault (default).

1 = Cell[n] does have an undervoltage fault.

**7.6.3.10 PARITY\_H Register (0x24) [PRESULT\_A (R/O)]**

The PRESULT\_A register holds the parity result bits for the first eight Group3 protected registers.

**图 35. PARITY\_H Register (0x24) [PRESULT\_A (R/O)]**

7	6	5	4	3	2	1	0
OTT	OTV	CUVT	CUVV	COVT	COVV	IO	FUNC

**7.6.3.11 PARITY\_H Register (0x25) [PRESULT\_B (R/O)]**

The PRESULT\_B register holds the parity result bits for the second eight Group3 protected registers.

**图 36. PARITY\_H Register (0x25) [PRESULT\_B (R/O)]**

7	6	5	4	3	2	1	0
0	0	0	0	USER4	USER3	USER2	USER1

### 7.6.3.12 ADC\_CONTROL Register (0x30)

The ADC\_CONTROL register controls some features of the bq76PL536A-Q1.

**图 37. ADC\_CONTROL Register**

7	6	5	4	3	2	1	0
—	ADC_ON	TS2	TS1	GPAI	CELL_SEL[2]	CELL_SEL[1]	CELL_SEL[0]

[7] *Not implemented. Must be written as 0.*

[6] (ADC\_ON): This bit forces the ADC subsystem ON. This has the effect of eliminating internal start-up and settling delays, but increases current consumption.

0 = Auto mode. ADC subsystem is OFF until a conversion is requested. The ADC is turned on, a wait is applied to allow the reference to stabilize. Automatically returns to OFF state at end of requested conversion. Note that there is a start-up delay associated with turning the ADC to the ON state in this mode.

1 = ADC subsystem is ON, regardless of conversion state. Power consumption is increased.

**Table 6. Temperature sensor Inputs**

TS[1]	TS[0]	MEASURE T
0	0	None (default)
0	1	TS1
1	0	TS2
1	1	Both

[3] (GPAI): This bit enables and disables the GPAI input to be measured on the next conversion-sequence start.

0 = GPAI is not selected for measurement.

1 = GPAI is selected for measurement.

[2–0] (CELL\_SEL): These three bits select the series cells for voltage measurement translation on the next conversion sequence start.

**Table 7. Series Cells for Voltage Measurement Translation**

CELL_SEL[2]	CELL_SEL[1]	CELL_SEL[0]	SELECTED CELL
0	0	0	Cell 1 only
0	0	1	Cells 1-2
0	1	0	Cells 1-2-3
0	1	1	Cells 1-2-3-4
1	0	0	Cells 1-2-3-4-5
1	0	1	Cells 1-2-3-4-5-6
Other			Cell 1 only

### 7.6.3.13 IO\_CONTROL Register (0x31)

The IO\_CONTROL register controls some features of the bq76PL536A-Q1 external I/O pins.

**图 38. IO\_CONTROL Register**

7	6	5	4	3	2	1	0
AUX	GIPI_OUT	GPIO_IN	0	0	SLEEP	TS2	TS1

- [7] (AUX): Controls the state of the AUX output pin, which is internally connected to REG50.  
0= Open  
1= Connected to REG50
- [6] (GPIO\_OUT): Controls the state of the open-drain GPIO output pin; the pin should be programmed to 1 to use the GPIO pin as an input.  
0= Output low  
1= Open-drain
- [5] (GPIO\_IN): Represents the input state of GPIO pin when used as an input.  
0= GPIO input is low.  
1= GPIO input is high.
- [4] *Not implemented. Must be written as 0.*
- [3] *Not implemented. Must be written as 0.*
- [2] (SLEEP): Places the device in a low quiescent-current state. All CUV, COV, and OT comparators are disabled. A 1-ms delay to stabilize the reference voltage is required to exit SLEEP mode and return to active COV, CUV monitoring.  
0= ACTIVE mode  
1= SLEEP mode
- [1..0] (TSx): Controls the connection of the TS1:TS2 inputs to the ADC VSS connection point. When set, the TSx(–) input is connected to VSS. These bits should be set to 0 to reduce the current draw of the system.  
0= Not connected  
1= Connected

### 7.6.3.14 CB\_CTRL Register (0x32)

The CB\_CTRL register determines the internal cell-balance output state.

**图 39. CB\_CTRL Register**

7	6	5	4	3	2	1	0
—	—	CBAL[6]	CBAL[5]	CBAL[4]	CBAL[3]	CBAL[2]	CBAL[1]

CB\_CTRL b(n = 5 to 0) (CBAL(n + 1)): This bit determines if the CB(n) output is high or low.

- 0 = CB[n] output is low (default).  
1 = CB[n] output is high (active).

### 7.6.3.15 CB\_TIME Register (0x33)

The CB\_TIME register sets the maximum high (active) time for the cell balance outputs from 0 seconds to 63 minutes. When set to 0, no balancing can occur – balancing is effectively disabled.

**图 40. CB\_TIME Register**

7	6	5	4	3	2	1	0
CBT[7]	—	CBT[5]	CBT[4]	CBT[3]	CBT[2]	CBT[1]	CBT[0]

- [7] Controls minutes/seconds counting resolution.  
 0 = Seconds (default)  
 1 = Minutes

- [5..0] Sets the time duration as scaled by CBT.7

### 7.6.3.16 ADC\_CONVERT Register (0x34)

The CONVERT\_CTRL register is used to start conversions.

**图 41. ADC\_CONVERT Register**

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	CONV

- [0] (CONV): This bit starts a conversion, using the settings programmed into the ADC\_CONTROL[] register. It provides a programmatic method of initiating conversions.  
 0 = No conversion (default)  
 1 = Initiate conversion. This bit is reset automatically after conversion is complete.

### 7.6.3.17 SHDW\_CTRL Register (0x3a)

The SHDW\_CTRL register controls writing to Group3 protected registers. Default at RESET = 0x00.

The value 0x35 must be written to this register to allow writing to Group3 protected registers in the range 0x40–0x4f. The register always returns 0x00 on read. The register is reset to 0x00 after any successful write, including a write to non-Group3 registers. A read operation does not reset this register.

Writing the value 0x27 results in all Group3 protected registers being refreshed from OTP programmed values. The register is reset to 0x00 after the REFRESH is complete.

**图 42. SHDW\_CTRL Register**

7	6	5	4	3	2	1	0
SHDW[7]	SHDW[6]	SHDW[5]	SHDW[4]	SHDW[3]	SHDW[2]	SHDW[1]	SHDW[0]

### 7.6.3.18 ADDRESS\_CONTROL Register (0x3b)

The ADDRESS\_CONTROL register allows the host to assign an address to the bq76PL536A-Q1 for communication. The default for this register is 0x00 at RESET.

**图 43. ADDRESS\_CONTROL Register**

7	6	5	4	3	2	1	0
AR	0	ADDR[5]	ADDR[4]	ADDR[3]	ADDR[2]	ADDR[1]	ADDR[0]

[7] (ADDR\_RQST): This bit is written to indicate that the ADDR[0]...[5] bits have been written to the correct address. This bit is reflected in the DEVICE\_STATUS[AR] bit

0 = Address has not been assigned (default at RESET).

1 = Address has been assigned.

[5..0] (ADDR): These bits set the device address for SPI communication. This provides to a range of addresses from 0x00 to 0x3f. Address 0x3f is reserved for broadcast messages to all connected **and** addressed 76PL536 devices. The default for these 6 bits is 0x00 at RESET.

### 7.6.3.19 RESET Register (0x3c)

The RESET register allows the host to reset the bq76PL536A-Q1 directly.

Writing 0xa5 causes the device to RESET. Other values are ignored.

**图 44. RESET Register**

7	6	5	4	3	2	1	0
RST[7]	RST[6]	RST[5]	RST[4]	RST[3]	RST[2]	RST[1]	RST[0]

### 7.6.3.20 TEST\_SELECT Register (0x3d)

The TEST\_SELECT places the SPI port in a special mode useful for debug.

TSEL (b7–b0) is used to place the SPI\_H interface pins in a mode to support test/debug of a string of bq76PL536A-Q1 devices. 0 = normal operating mode.

When the sequence 0xa4, 0x25 ("JR") is written on subsequent write cycles, the device enters a special TEST mode useful for stack debugging. Writes to other registers between the required sequence bytes results in the partial sequence being voided; the entire sequence must be written again. POR, RESET, or writing a 0x00 to this register location exits this mode.

In this state, SPI pin SCLK and SDI become outputs and are enabled, and reflect the state of the SCLK\_S, SDI\_S pins of the device. SDO remains an output. This allows observation of bus traffic mid-string. The lowest device in the string should **not** be set to operate in this mode.

**CAUTION**

The user is cautioned to condition the connection to a mid- or top-string device with suitable isolation circuitry to prevent injury or damage to connected devices. Programming the most-negative device on the stack in this mode prevents further communications with the stack until POR, and may result in device destruction; this condition should be avoided.

**图 45. TEST\_SELECT Register**

7	6	5	4	3	2	1	0
TSEL[7]	TSEL[6]	TSEL[5]	TSEL[4]	TSEL[3]	TSEL[2]	TSEL[1]	TSEL[0]

### 7.6.3.21 E\_EN Register (0x3f)

The E\_EN register controls the access to the programming of the integrated OTP EPROM.

This register should be written the value 0x91 to permit writing the USER block of EPROM. Values other than 0x00 and 0x91 are reserved and may result in undefined operation. The next read or write of any type to the device resets (closes) the write window. If a Group3 protected write occurs, the window is closed after the write.

**图 46. E\_EN Register**

7	6	5	4	3	2	1	0
E_EN[7]	E_EN [6]	E_EN [5]	E_EN [4]	E_EN [3]	E_EN [2]	E_EN [1]	E_EN [0]

### 7.6.3.22 FUNCTION\_CONFIG Register (0x40)

The FUNCTION\_CONFIG sets the default configuration for special features of the device.

**图 47. FUNCTION\_CONFIG Register**

7	6	5	4	3	2	1	0
0	0	GPAI_REF	GPAI_SRC	CN[1]	CN[0]	—	0

- [7..6] (0) Reserved
- [5] (GPAI\_REF): This bit sets the reference for the GPAI ADC measurement.  
 0 = Internal ADC bandgap reference  
 1 =  $V_{REG50}$  (ratiometric)
- [4] (GPAI\_SRC): This bit controls multiplexing of the GPAI register and determines whether the ADC mux is connected to the external GPAI inputs, or internally to the BAT1 pin. The register results are scaled automatically to match the input.  
 0 = External GPAI inputs are converted to result in GPAI register 0x01–02.  
 1 = BAT pin to VSS voltage is measured and reported in the GPAI register.
- [3..2] (CN[1..0]): These two bits configure the number of series cells used. If fewer than 6 cells are configured, the corresponding OV/UV faults are ignored. For example, if the CN[x] bits are set to 10b (2), then the OV/UV comparators are ignored for cells 5 and 6. Refer to [表 8](#).

**表 8. Series Cells**

CN[1]	CN[0]	SERIES CELLS
0	0	6 (DEFAULT)
0	1	5
1	0	4
1	1	3



### 7.6.3.23 IO\_CONFIG Register (0x41)

The IO\_CONFIG sets the default configuration for miscellaneous I/O features of the device.

**图 48. IO\_CONFIG Register**

7	6	5	4	3	2	1	0
CRCNOFLT	—	—	—	—	—	—	CRC_DIS

- [7] (CRCNOFLT): This bit enables and disables detected CRC errors asserting the FAULT pin.
- 0 = CRC errors cause the FAULT[CRC] bit to be set and the FAULT pin to assert. The FAULT[CRC] bit must be reset as described in the text.
  - 1 = CRC errors cause the FAULT[CRC] bit to be set and the FAULT pin is not asserted. The FAULT[CRC] bit must be reset as described in the text.
- [0] (CRC\_DIS): This bit enables and disables the automatic generation of the CRC for the SPI communication packet. The packet size is determined by the host as part of the read request protocol. The CRC is checked at the de-assertion of the CS pin. TI recommends that this bit be changed using the broadcast address (0x3f), so that all devices in a battery stack use the same protocol.
- 0 = A CRC is expected, and generated as the last byte of the packet.
  - 1 = A CRC is not used in communications.

### 7.6.3.24 CONFIG\_COV Register (0x42)

The CONFIG\_COV register determines cell-overvoltage threshold voltage.

**图 49. CONFIG\_COV Register**

7	6	5	4	3	2	1	0
DISABLE	—	COV[5]	COV[4]	COV[3]	COV[2]	COV[1]	COV[0]

- [7] (DISABLE): Disables the overvoltage function when set
- 0 = Overvoltage function enabled
  - 1 = Overvoltage function disabled
- [5..0] (COV[5]...[0]): Configuration bits with corresponding voltage threshold
- 0x00 = 2 V; each binary increment adds 50 mV until 0x3c = 5 V.

### 7.6.3.25 CONFIG\_COVT Register (0x43)

The CONFIG\_COVT register determines cell-overvoltage detection delay time.

**图 50. CONFIG\_COVT Register**

7	6	5	4	3	2	1	0
μs/ms	—	—	COVD[4]	COVD[3]	COVD[2]	COVD[1]	COVD[0]

- [7] (μs/ms): Determines the units of the delay time, microseconds or milliseconds
- 0 = Microseconds
  - 1 = Milliseconds
- [4..0] COVD: 0x01 = 100; each binary increment adds 100 until 0x1f = 3100
- Note: When this register is programmed to 0x00, the delay becomes 0s AND the COV state is NOT latched in the COV\_FAULT[] register. In this operating mode, the overvoltage state for a cell is virtually instantaneous in the COV\_FAULT[] register. This mode may cause system firmware to miss a dangerous cell overvoltage condition.*

### 7.6.3.26 CONFIG\_UV Register (0x44)

The CUV register determines cell-undervoltage threshold voltage.

图 51. CONFIG\_UV Register

7	6	5	4	3	2	1	0
DISABLE	—	—	CUV[4]	CUV[3]	CUV[2]	CUV[1]	CUV[0]

[7] (DISABLE): Disables the undervoltage function when set  
 0 = Undervoltage function enabled  
 1 = Undervoltage function disabled

[5..0] (CUV[4]...[0]): Configuration bits with corresponding voltage threshold  
 0x00 = 0.7 V; each binary increment adds 100 mV until 0x1a = 3.3 V.

### 7.6.3.27 CONFIG\_CUVT Register (0x45)

The CONFIG\_CUVT register determines cell-overflow detection delay time.

图 52. CONFIG\_CUVT Register

7	6	5	4	3	2	1	0
μs/ms	—	—	CUVD[4]	CUVD[3]	CUVD[2]	CUVD[1]	CUVD[0]

[7] (μs/ms): Determines the units of the delay time, microseconds or milliseconds  
 0 = Microseconds  
 1 = Milliseconds

[4..0] CUVD: 0x01 = 100; each binary increment adds 100 until 0x1f = 3100.

*Note: When this register is programmed to 0x00, the delay becomes 0 s AND the CUV state is NOT latched in the CUV\_FAULT[] register. In this operating mode, the overvoltage state for a cell is virtually instantaneous in the CUV\_FAULT[] register. This mode may cause system firmware to miss a dangerous cell undervoltage condition.*

### 7.6.3.28 CONFIG\_OT Register (0x46)

The CONFIG\_OT register holds the configuration of the overtemperature thresholds for the two TS inputs.

For each respective nibble (OT1 or OT2), the value 0x0 disables this function. Other settings program a trip threshold. See the [Ratiometric Sensing](#) section for details of setting this register. Values above 0x0b are illegal and should not be used.

图 53. CONFIG\_OT Register

7	6	5	4	3	2	1	0
OT2[3]	OT2[2]	OT2[1]	OT2[0]	OT1[3]	OT1[2]	OT1[1]	OT1[0]

### 7.6.3.29 CONFIG\_OTT Register (0x47)

The CONFIG\_OTT register determines cell overtemperature detection delay time.

0x01 = 10 ms; each binary increment adds 10 ms until 0xff = 2.55 seconds.

**图 54. CONFIG\_OTT Register**

7	6	5	4	3	2	1	0
COTD[7]	COTD[6]	COTD[5]	COTD[4]	COTD[3]	COTD[2]	COTD[1]	COTD[0]

*Note: When this register is programmed to 0x00, the delay becomes 0 s AND the OT state is NOT latched in the ALERT\_STATUS[] register. In this operating mode, the overtemperature state for a TSn input is virtually instantaneous in the register. This mode may cause system firmware to miss a dangerous overtemperature condition.*

### 7.6.3.30 USERx Register (0x48–0x4b) (USER1–4)

The four USER registers can be used to store user data. The part does not use these registers for any internal function. They are provided as convenient storage for user S/N, date of manufacture, and so forth.

**图 55. USERx Register**

7	6	5	4	3	2	1	0
USER[7]	USER[6]	USER[5]	USER[4]	USER[3]	USER[2]	USER[1]	USER[0]

## 8 Application and Implementation

---

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 8.1 Application Information

The bq76PL536A-Q1 is a series cell Lithium-Ion battery monitor and secondary protector for Electric Vehicles (EV), Hybrid Electric Vehicles (HEV), Uninterruptible Power Systems (UPS), E-Bike/Scooter, Large-Format Battery Systems, and so forth.

To allow for optimal performance in the end application, special consideration must be taken to ensure minimization of measurement error through proper printed circuit board (PCB) layout.

#### 8.1.1 Anti-Aliasing Filter

An anti-aliasing filter is required for each VCn input VC6–VC1, consisting of a 1-k $\Omega$ , 1% series resistor and 100-nF capacitor. Good-quality components should be used. A 1% resistor is recommended, because the resistor creates a small error by forming a voltage divider with the input impedance of the part. The part is factory-trimmed to compensate for the error introduced by the filter.

#### 8.1.2 Host SPI Interface Pin States

The CS\_H pin is active-low. The host asserts the pin to a logic zero to initiate communications. The CS pin should remain low until the end of the current packet. When the CS\_H pin is asserted, the SPI receiver and interface of the device are reset and resynchronized. This action ensures that a slave device that has lost synchronization during a previous transmission or as the result of noise on the bus does not remain permanently hung. CS\_H must be driven false (high) between packets; see [Timing Requirements: AC SPI Data Interface](#), for timing details.

8.2 Typical Application

Full-size reference schematics are available from TI on request.

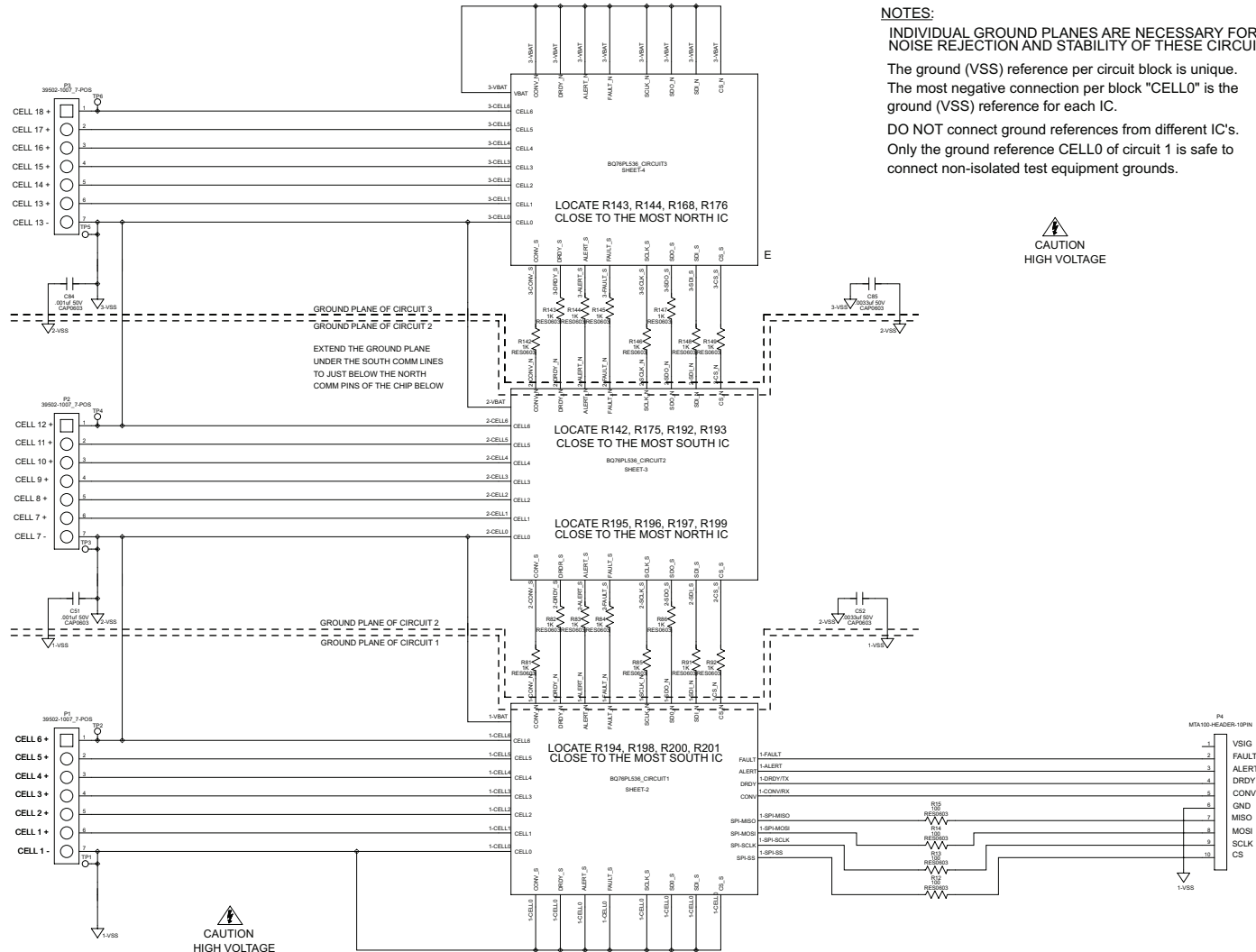


图 56. Schematic (Page 1 of 4)

S001

Typical Application (接下页)

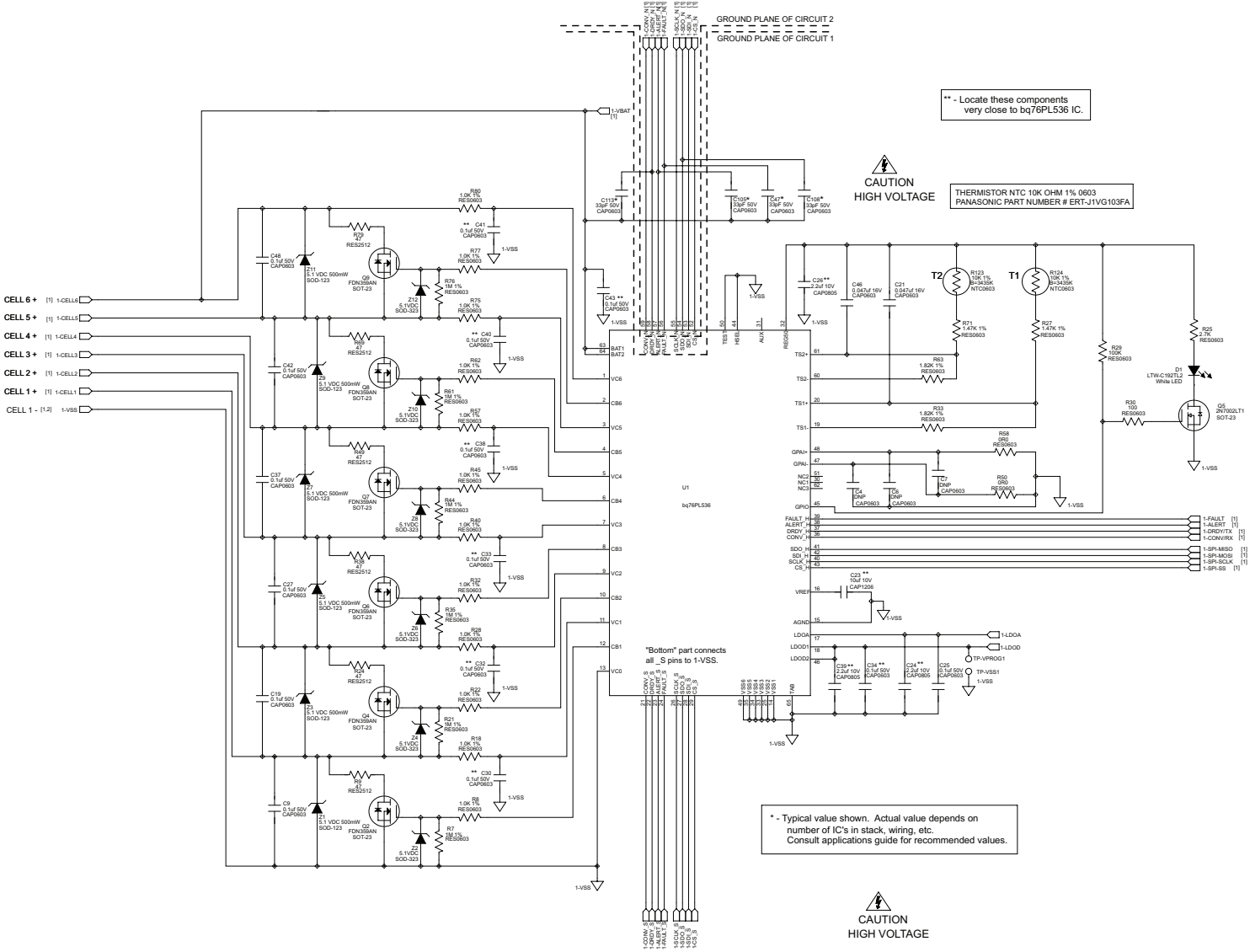


图 57. Schematic (Page 2 of 4)

Typical Application (接下页)

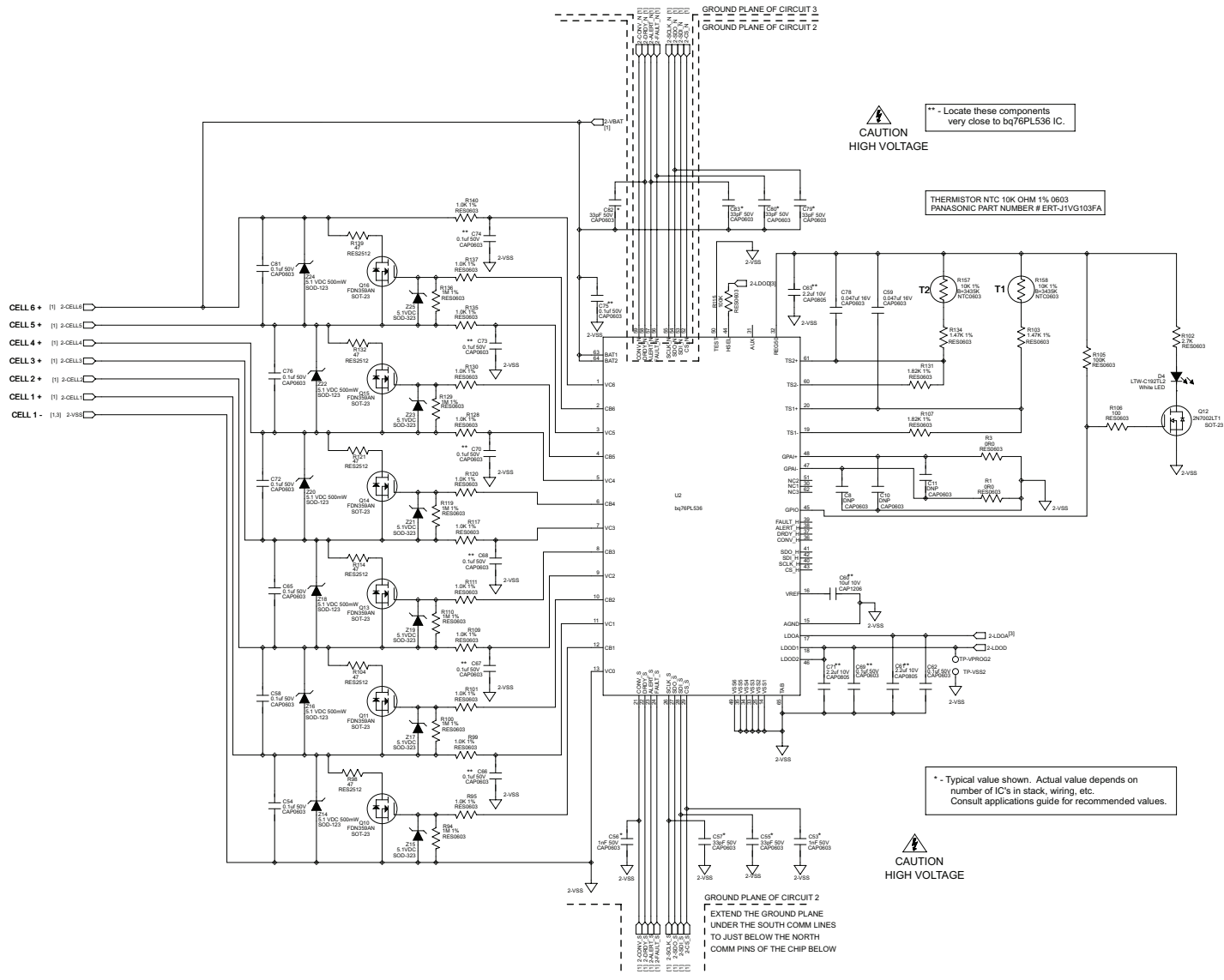


图 58. Schematic (Page 3 of 4)

Typical Application (接下页)

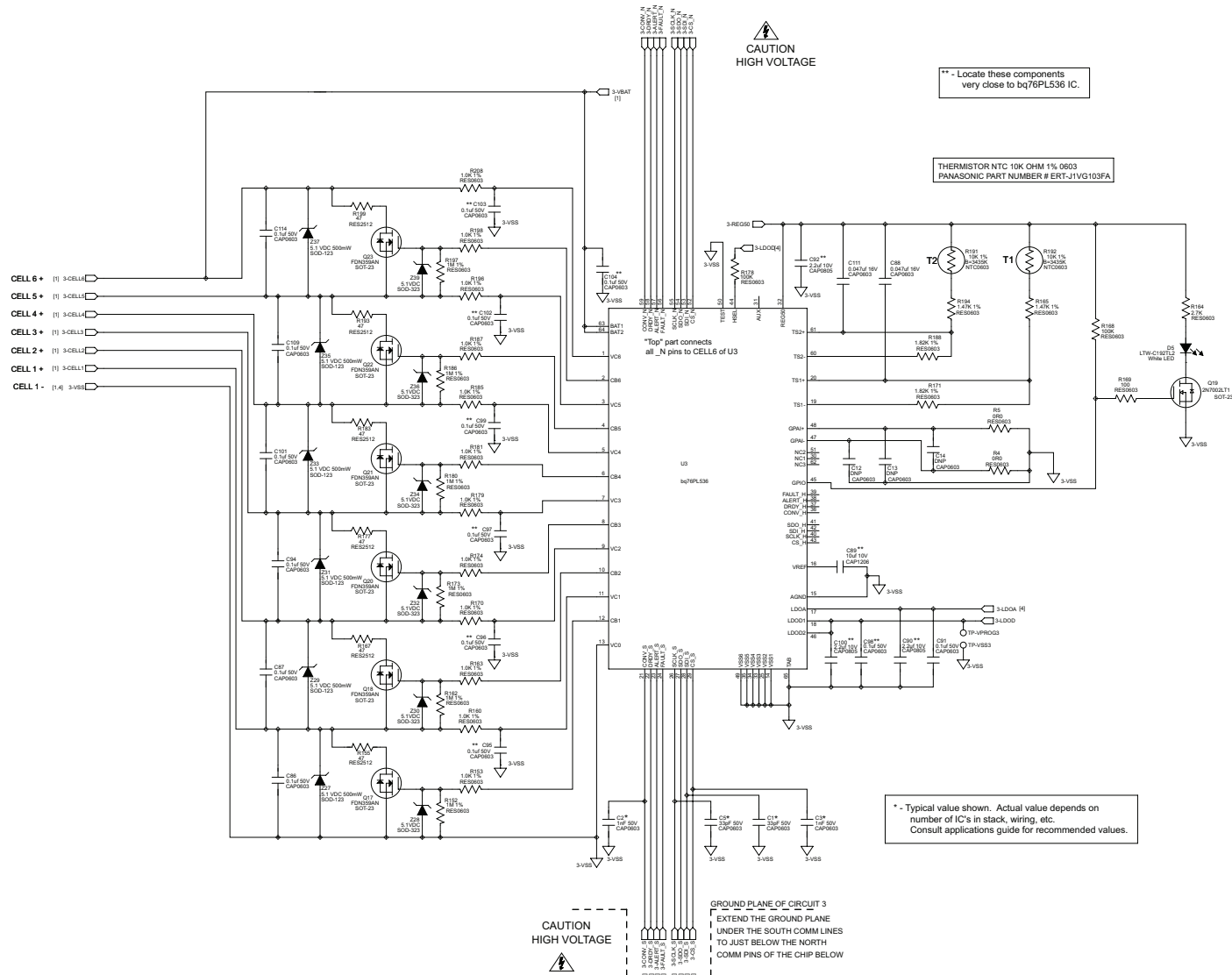


图 59. Schematic (Page 4 of 4)



## 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 9.

**表 9. Design Parameters**

PARAMETER	DESCRIPTION	EXAMPLE VALUE	UNIT
C <sub>EMI</sub>	EMI Capacitor	3300	pF
C <sub>FILT</sub>	Filter Capacitor	0.1	μF
C <sub>IN</sub>	Input Capacitor	0.1	μF
C <sub>REGOUT</sub>	REGOUT Capacitor	2.2 (minimum)	μF
C <sub>VDDA_1</sub>	Internal analog 5-V LDO bypass connection 1	2.2	μF
C <sub>VDDA_2</sub>	Internal analog 5-V LDO bypass connection 2	0.2	μF
C <sub>VDD_D_1</sub>	Capacitor for internal digital 5-V LDO bypass connection 1	2.2	μF
C <sub>VDD_D_2</sub>	Capacitor for internal digital 5-V LDO bypass connection 2	0.2	μF
C <sub>VREF</sub>	VREF Capacitor	10	μF
L <sub>EMI</sub>	EMI Ferrite Resistor	500	Ω
R <sub>BAL</sub>	Balance Resistor	47	Ω
R <sub>IN</sub>	Input Resistor	1	kΩ
R <sub>PULL1</sub> -R <sub>PULL3</sub>	Pullup Resistors for digital open-drain I/O	10	kΩ
R <sub>PULL4</sub> -R <sub>PULL5</sub>	Pullup Resistors for general-purpose (differential) analog input (GPAI), connect to VSS if unused		kΩ

## 8.2.2 Detailed Design Procedure

Use the following for the procedure for the recommended front-end circuit:

- Select the RC filter closest to the cell for filter requirements. Additional poles can be added with a differential capacitor to get very low  $f_c$ .
- ADC is calibrated to use  $R_{IN} = 1\text{ k}\Omega$  and  $C_{IN} = 0.1\text{ }\mu\text{F}$ .
- Select Zener diode for lowest possible reverse leakage.
- A balance FET gate-protection diode is required (available internally).
- Select the capacitors for LDO Filters according to 表 9.
  - LDO1 and LDO2 require a 2.2-μF ceramic capacitor for stability. These pins are tied together internally. Tie LDO1 to LDOD2 externally.
- For pullup supply, the following information applies:
  - REG50 turns off in SLEEP mode
  - Use LDOD for pullups in normal use
  - Use REG50 for programming EEPROM (LDOD will see 7 V)
  - Connect GPAI+ and GPA– to VSS if unused
- Select low impedance and polarized connectors. Numbered or colored connectors are also good options.
- Select the input Zener TVS so that it clamps below 5.6 Vdc, with low-leakage current, and must be able to handle transient surge energy
- Select capacitors based on temperature and environment with voltages well above the operating voltage
- Select balancing MOSFETs according to the following:
  - Low turn on threshold voltage (must turn on with the lowest cell voltage)
  - Drain-to-source voltage and gate-to-source voltage
  - Power dissipation
  - Current based on selected bleed resistor value
- Select the Bleed Resistor according to the following:
  - Value based on desired current
  - Wattage to handle the current and temperature rise such as  $4.2\text{ V} \times 47 = 0.089\text{ A} \therefore 0.37\text{ W}$

### 8.2.3 Application Curves

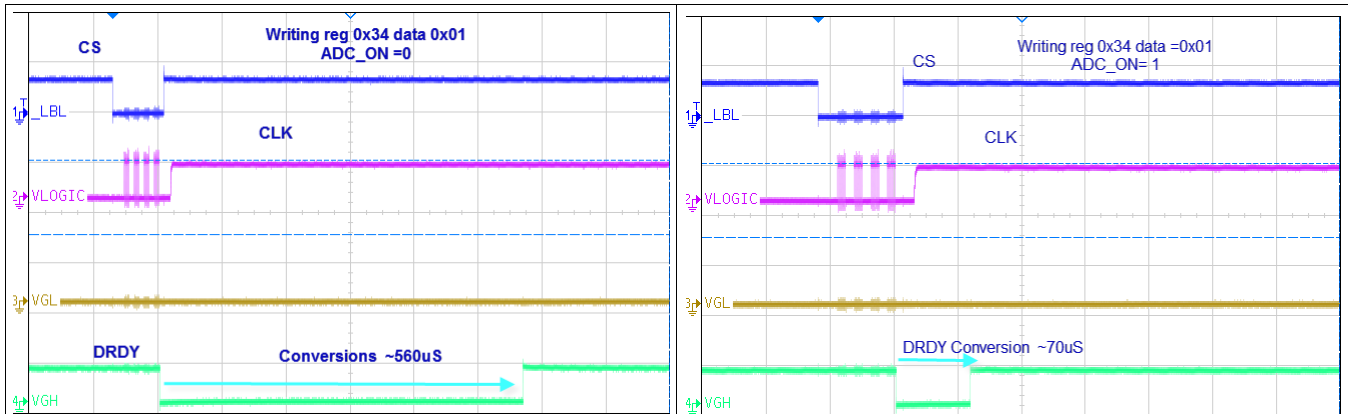


图 60. Firmware Conversion with ADC\_ON = 0

图 61. Firmware Conversion with ADC\_ON = 1

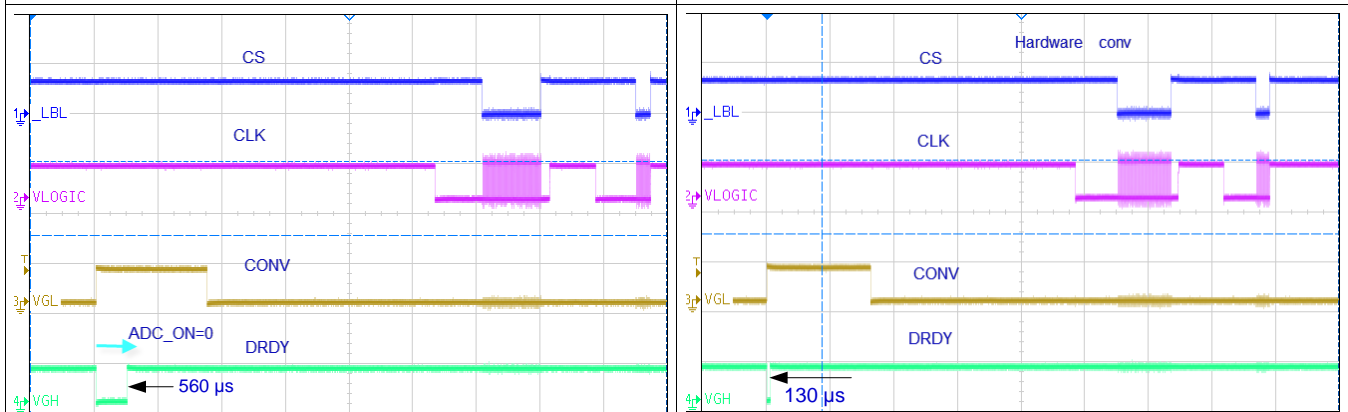


图 62. Hardware Conversion with ADC\_ON = 0

图 63. Hardware Conversion with ADC\_ON = 1

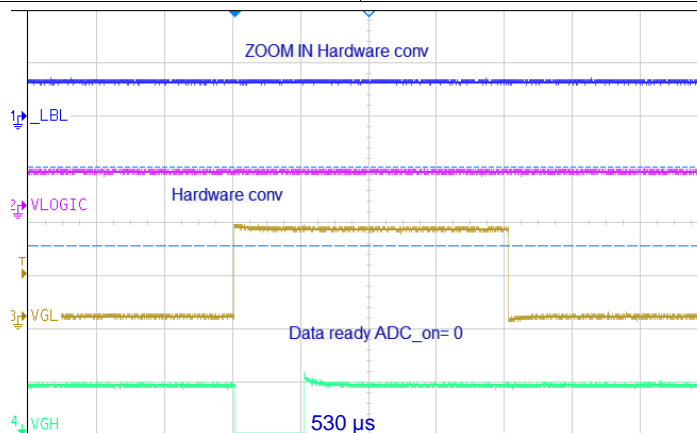


图 64. ZOOM IN Hardware Conversion

## 9 Power Supply Recommendations

### 9.1 Power Supply Decoupling

The LDOA, LDOD1, LDOD2 and REG50 pins all require a 2.2- $\mu$ F ceramic capacitor to be placed as closely as possible to the respective pins to optimize stability. bq76PL536A-Q1 requires a power supply with between 7.2 V to 27 V inputs. When fewer than six cells are used, see [Figure 13](#) for details.

bq76PL536A-Q1 requires a power supply between 7.2 V to 27 V inputs. When fewer than 6 cells are used, see [Figure 13](#) for details.

## 10 Layout

### 10.1 Layout Guidelines

For typical applications, the following guidelines and practices should be followed closely:

- VREF and AGND pins require a high-quality 10- $\mu$ F capacitor be connected between them, in very close physical proximity to the device pins, using short track lengths to minimize the effects of track inductance on signal quality.
  - The AGND pin should be connected to VSS. Device VSS connections should be brought to a single point close to the IC to minimize layout-induced errors. The device tab should also be connected to this point, and is a convenient common VSS location. The internal VREF should not be used externally to the device by user circuits.
- The internal analog supply should be bypassed at the LDOA pin with a good-quality, low-ESR, 2.2- $\mu$ F ceramic capacitor.

---

#### 注

Because the LDODx inputs are pulled to approximately 7 V during programming, programming time MUST be < 50 ms.

---

- The bq76PL536A-Q1 has a low-dropout (LDO) regulator provided to power the thermistors and other external circuitry. The input for this regulator is VBAT. The output of REG50 is typically 5 V. A minimum 2.2- $\mu$ F capacitor is required for stable operation. The output is internally current-limited and is reduced to near zero, if excess current is drawn, causing die temperatures to rise to unacceptable levels. The 2.2- $\mu$ F output capacitor is required whether REG50 is used in the design or not. REG50 is disabled in SLEEP mode, may be turned off under thermal-shutdown conditions, and therefore should not be used as a pull-up source for terminating device pins where required.
- The bq76PL536A-Q1 includes a general-purpose input/output pin controlled by the IO\_CONTROL[GPIO\_OUT] bit. The state of this bit is reflected on the pin. To use the pin as an input, program GPIO\_OUT to a 1, and then read the IO\_CONTROL[GPIO\_IN] bit. A pull-up (10 k $\Omega$ –1 M $\Omega$ , typical) is required on this pin if used as an input. If the pull-up is not included in the design, system firmware must program a 0 in IO\_CONTROL[GPIO\_OUT] to prevent excess current draw from the floating input. Use of a pull-up is recommended in all designs to prevent an unintentional increase in current draw.
- Device-to-device (D2D) communications makes use of a unique, current-mode interface which provides common-mode voltage isolation between successive bq76PL536A-Q1s. This vertical bus (VBUS) is found on the \_N and corresponding \_S pins. It provides high-speed I/O for both the SPI bus and the direct I/O pins CONV and DRDY. The current-mode interface minimizes the effects of wiring capacitance on the interface speed. The \_S (south-facing) pins connect to the next-lower device (operating at a lower potential) in the stack of bq76PL536A-Q1s. The \_N (North facing) pins connect to the next-higher device. The pins cannot be swapped; \_S always points South, and \_N always point North. The \_S and \_N pins are interconnected to the pin with the same name, but opposite suffix.
  - All pins operate within the voltages present at the BAT and VSS pins.
  - The maximum SCLK frequency is limited by the number of devices in the vertical stack and other factors. Each device imposes an approximately 30-ns delay on the round trip communications speed; that is, from SCLK rise time (an input to all devices) to the SDO pin transition time requires approximately 30 ns per device. The designer must add to this the delay caused by the PCB trace (in turn determined by the material and layout), any connectors in series with the connection, and any other wiring or cabling

## Layout Guidelines (接下页)

between devices in the system.

- When designing the layout, several considerations need to be taken into account.
  - First, in a stacked system, individual ground planes are necessary for proper noise rejection and stability of the circuits.
  - Second, the ground (VSS) reference per circuit block is unique. The most negative connection, per block “CELL0”, is the ground (VSS) reference for each IC. Do not connect ground references from different ICs. Only the ground reference CELL0, of the most southerly IC, is safe to connect non-isolated test equipment grounds.

### CAUTION

Be careful as the BAT and VSS pins may be several hundred volts above system ground, depending on their position in the stack.

### 注

North (\_N) pins of the top, most-positive device in the stack, should be connected to the BAT1(2) pins of the device for correct operation of the string. South (\_S) pins of the lowest, most-negative device in the stack, should be connected to VSS of the device.

The PowerPAD™ package is a thermally enhanced standard-size IC package designed to eliminate the use of bulky heat sinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures. See 图 65.

The PowerPAD™ package is designed so that the lead frame die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low-thermal resistance ( $R_{\theta JC}$ ) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heat sink. In addition, through the use of thermal bias, the thermal pad can be directly connected to a ground plane or special heat sink structure designed into the PCB.

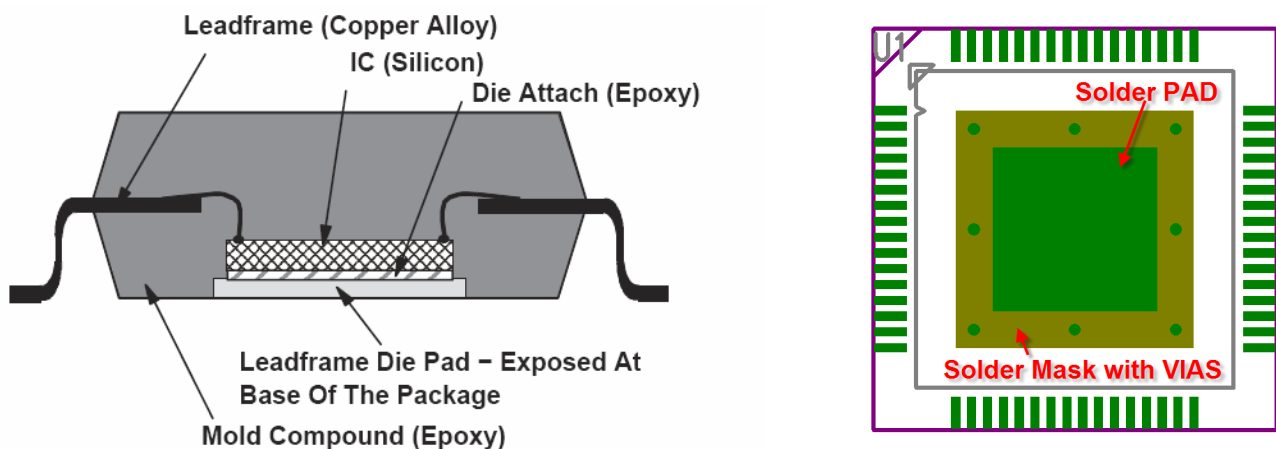


图 65. Section View of PowerPAD™ Package and Top View of Solder Mask and Pad

## 10.2 Layout Example

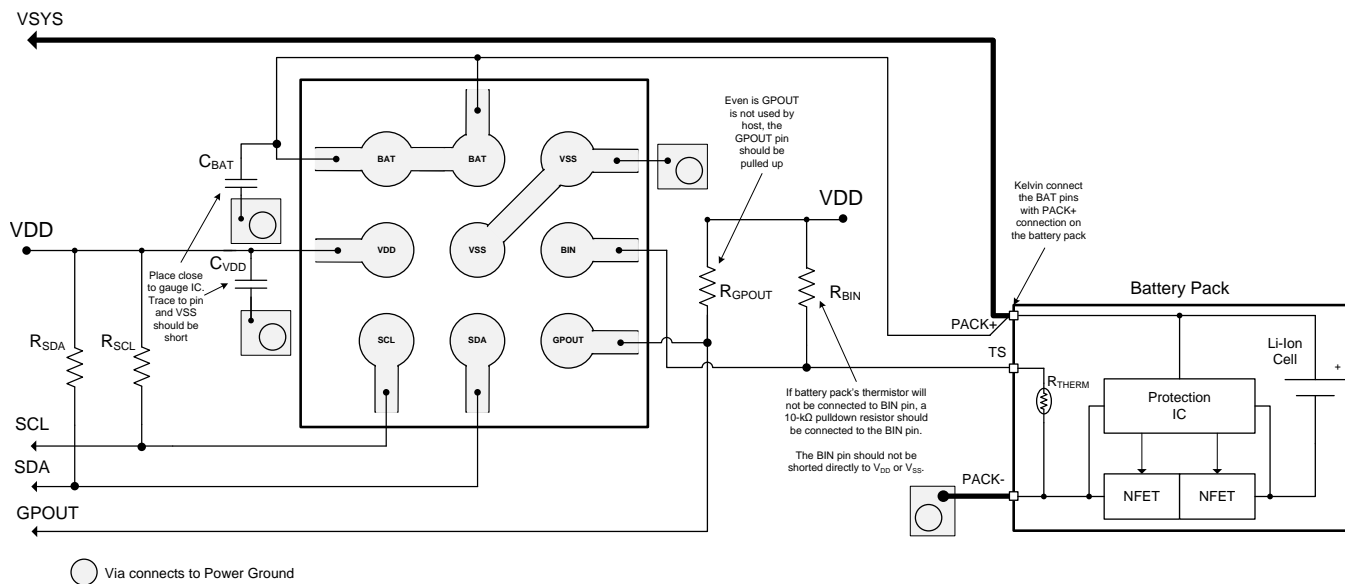


图 66. Layout

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ76PL536APAPR	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	BQ76PL536A	<a href="#">Samples</a>
BQ76PL536APAPT	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	BQ76PL536A	<a href="#">Samples</a>
BQ76PL536ATPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	76PL536AQ1	<a href="#">Samples</a>
BQ76PL536ATPAPTQ1	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	76PL536AQ1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ76PL536APAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
BQ76PL536ATPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ76PL536APAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0
BQ76PL536ATPAPRQ1	HTQFP	PAP	64	1000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

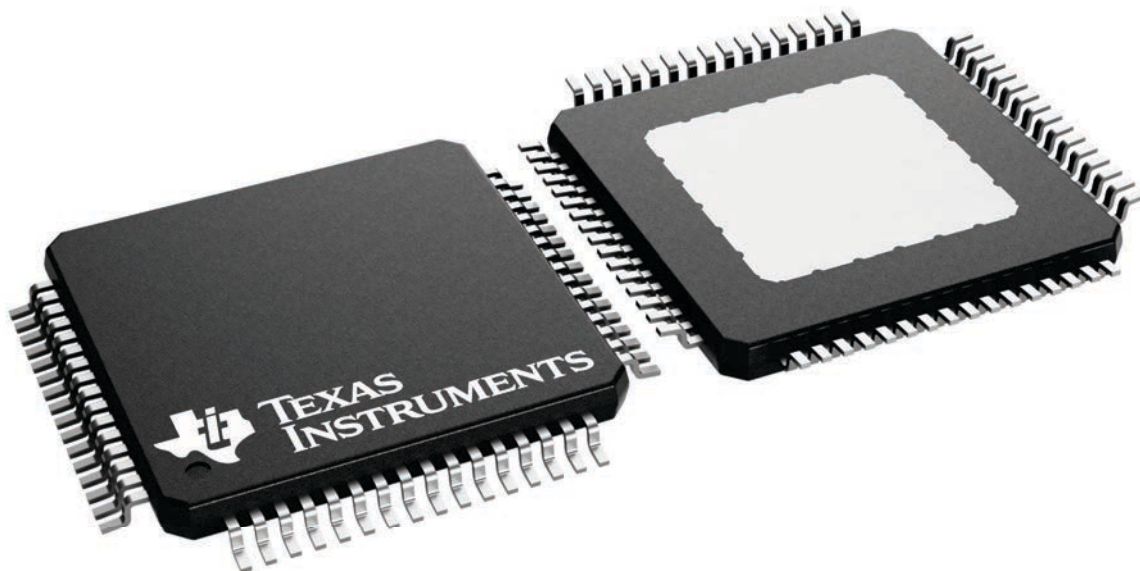
**PAP 64**

**HTQFP - 1.2 mm max height**

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



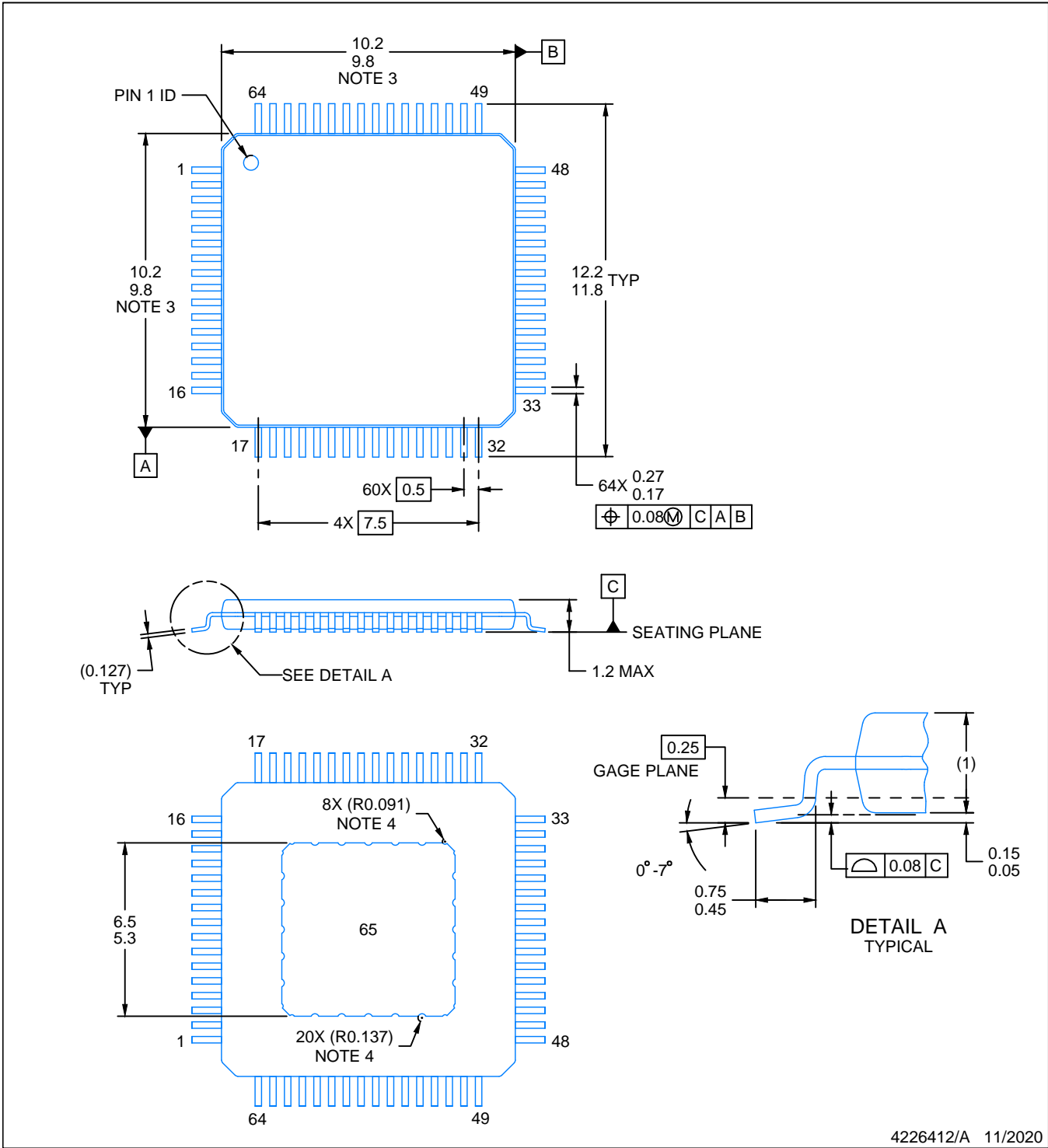
4226442/A

# PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4226412/A 11/2020

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

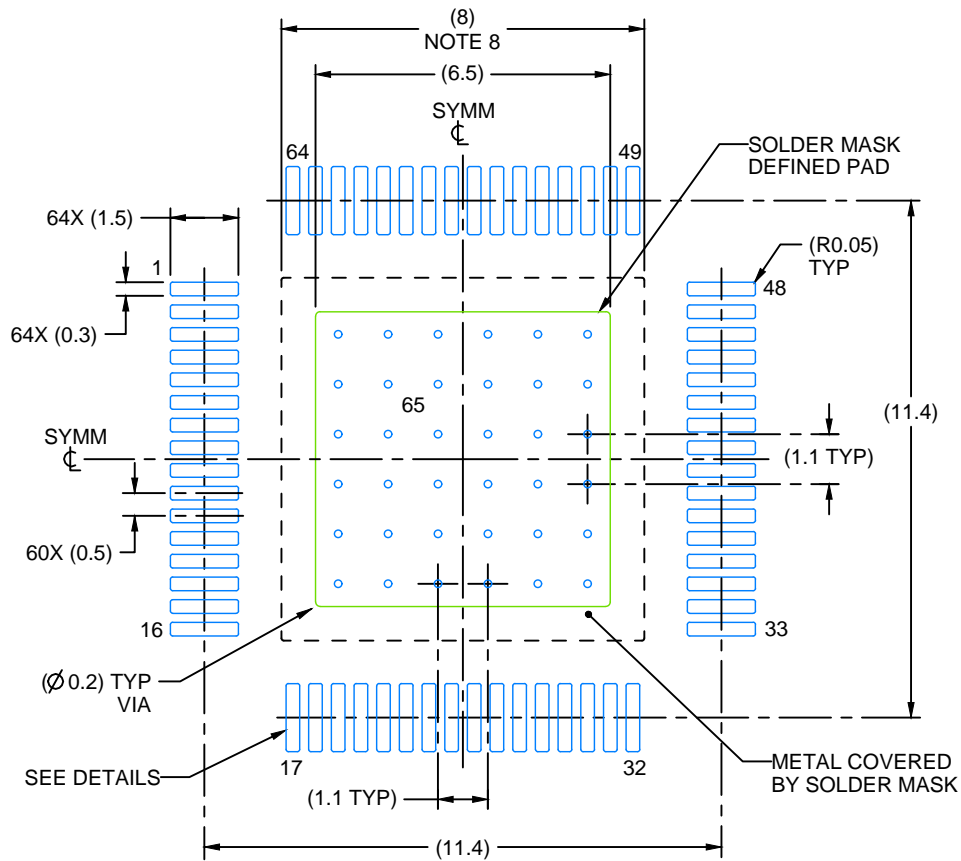
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

# EXAMPLE BOARD LAYOUT

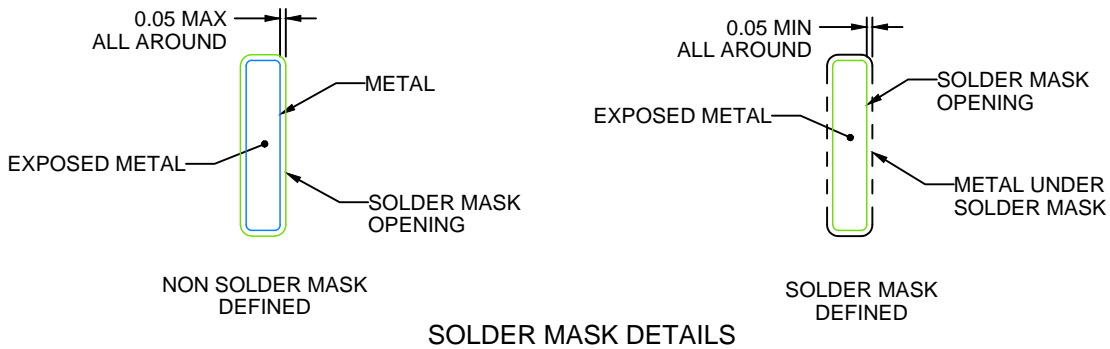
PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

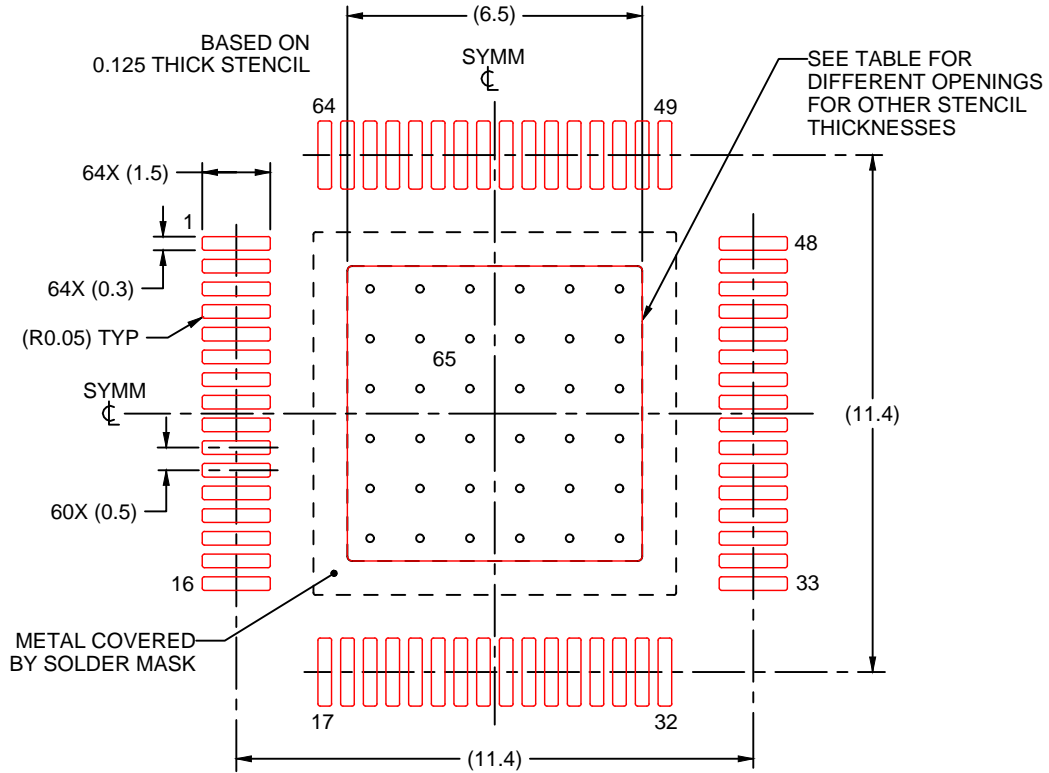
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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