BC856B, BC857B, BC858A

General Purpose Transistors

PNP Silicon

These transistors are designed for general purpose amplifier applications. They are housed in the SC−70/SOT−323 which is designed for low power surface mount applications.

Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage BC856 BC857 BC858	V_{CEO}	 −65 −45 −30	V
Collector-Base Voltage BC856 BC857 BC858	V_{CBO}	 −80 −50 −30	V
Emitter−Base Voltage	V_{EBO}	−5.0	V
Collector Current − Continuous	I_C	−100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	883	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−5 = 1.0 x 0.75 x 0.062 in.

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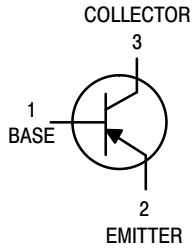
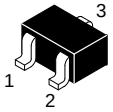
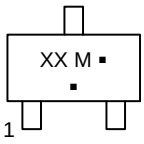




SC−70/SOT−323
CASE 419
STYLE 3

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Emitter Breakdown Voltage (I_C = −10 mA)	BC856 BC857 BC858	$V_{(BR)CEO}$	−65 −45 −30	− − −	− − −	V
Collector−Emitter Breakdown Voltage (I_C = −10 μA, V_{EB} = 0)	BC856 BC857 BC858	$V_{(BR)CES}$	−80 −50 −30	− − −	− − −	V
Collector−Base Breakdown Voltage (I_C = −10 μA)	BC856 BC857 BC858	$V_{(BR)CBO}$	−80 −50 −30	− − −	− − −	V
Emitter−Base Breakdown Voltage (I_E = −1.0 μA)	BC856 BC857 BC858	$V_{(BR)EBO}$	−5.0 −5.0 −5.0	− − −	− − −	V
Collector Cutoff Current (V_{CB} = −30 V) (V_{CB} = −30 V, T_A = 150°C)		I_{CBO}	− −	− −	−15 −4.0	nA μA
ON CHARACTERISTICS						
DC Current Gain (I_C = −10 μA, V_{CE} = −5.0 V) (I_C = −2.0 mA, V_{CE} = −5.0 V)	BC856A, BC585A BC856B, BC857B, BC858B BC857C BC856A, BC858A BC856B, BC857B, BC858B BC857C	h_{FE}	− − − 125 220 420	90 150 270 180 290 520	− − − 250 475 800	−
Collector−Emitter Saturation Voltage (I_C = −10 mA, I_B = −0.5 mA) (I_C = −100 mA, I_B = −5.0 mA)		$V_{CE(sat)}$	 − −	 − −	 −0.3 −0.65	V
Base−Emitter Saturation Voltage (I_C = −10 mA, I_B = −0.5 mA) (I_C = −100 mA, I_B = −5.0 mA)		$V_{BE(sat)}$	 − −	 −0.7 −0.9	 − −	V
Base−Emitter On Voltage (I_C = −2.0 mA, V_{CE} = −5.0 V) (I_C = −10 mA, V_{CE} = −5.0 V)		$V_{BE(on)}$	 −0.6 −	 − −	 −0.75 −0.82	V
SMALL−SIGNAL CHARACTERISTICS						
Current−Gain − Bandwidth Product (I_C = −10 mA, V_{CE} = −5.0 Vdc, f = 100 MHz)		f_T	100	−	−	MHz
Output Capacitance (V_{CB} = −10 V, f = 1.0 MHz)		C_{ob}	−	−	4.5	pF
Noise Figure (I_C = −0.2 mA, V_{CE} = −5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)		NF	−	−	10	dB

BC857/BC858

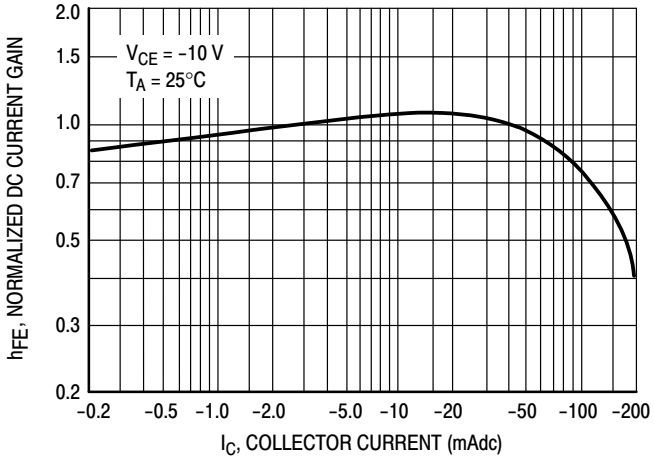


Figure 1. Normalized DC Current Gain

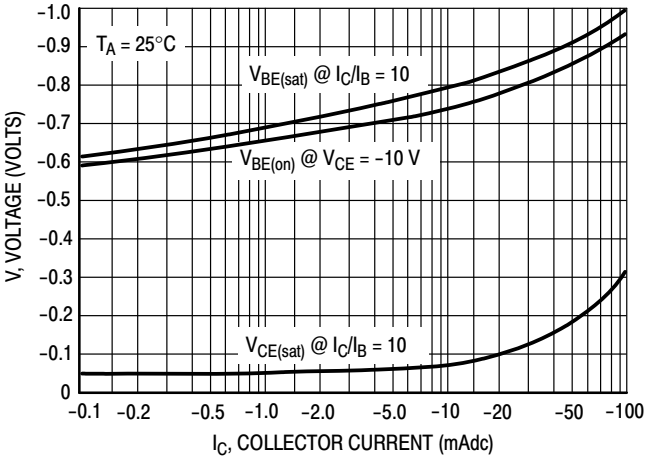


Figure 2. “Saturation” and “On” Voltages

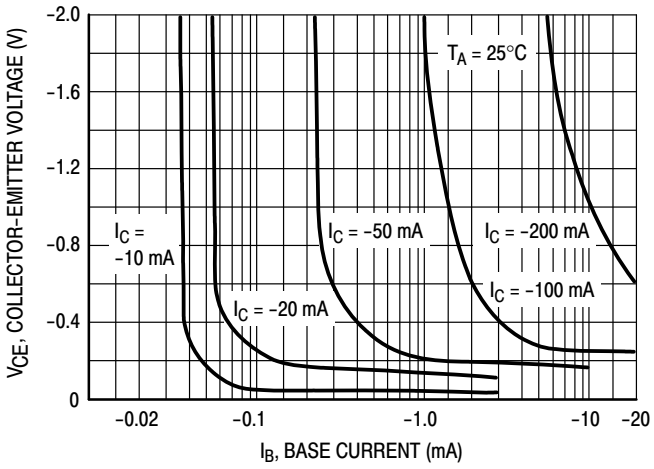


Figure 3. Collector Saturation Region

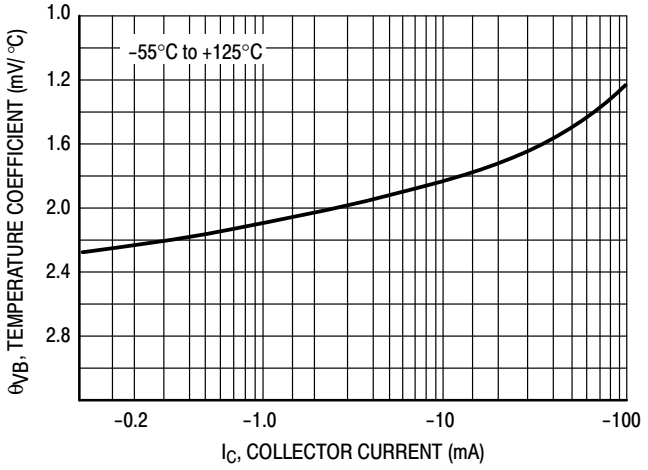


Figure 4. Base−Emitter Temperature Coefficient

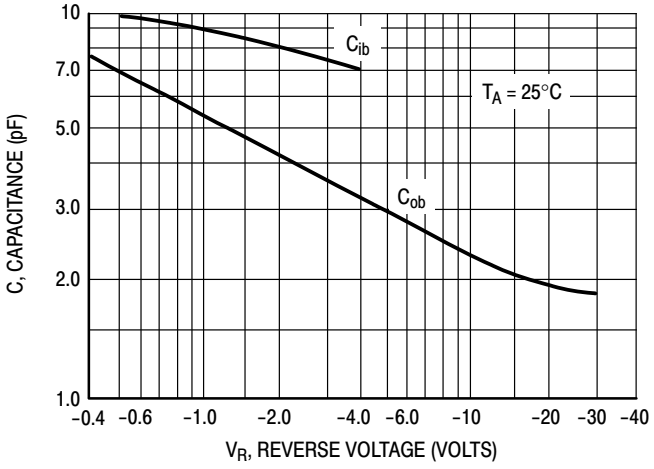


Figure 5. Capacitances

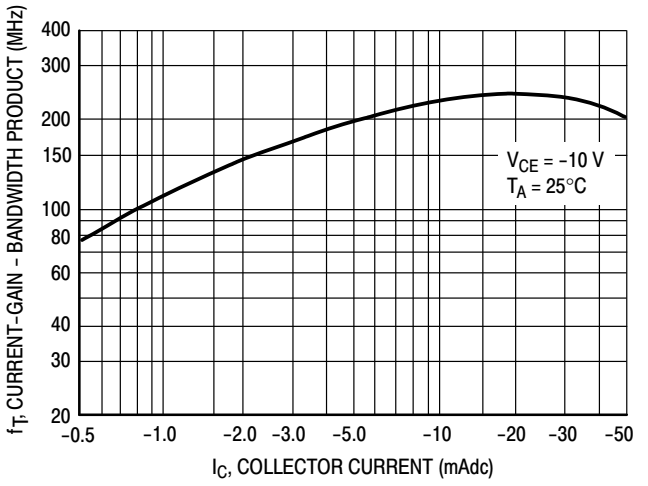


Figure 6. Current−Gain − Bandwidth Product

BC856

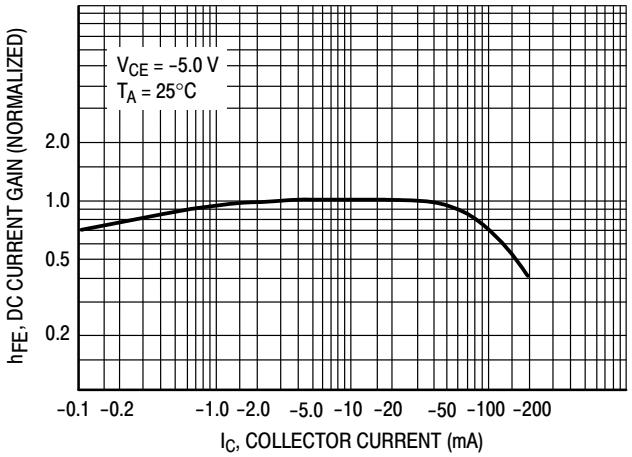


Figure 7. DC Current Gain

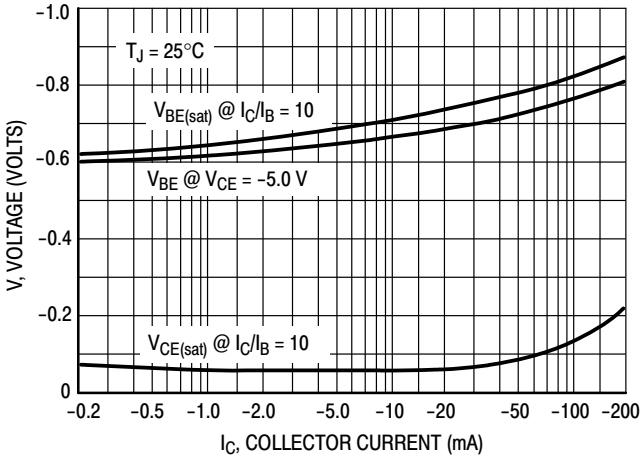


Figure 8. “On” Voltage

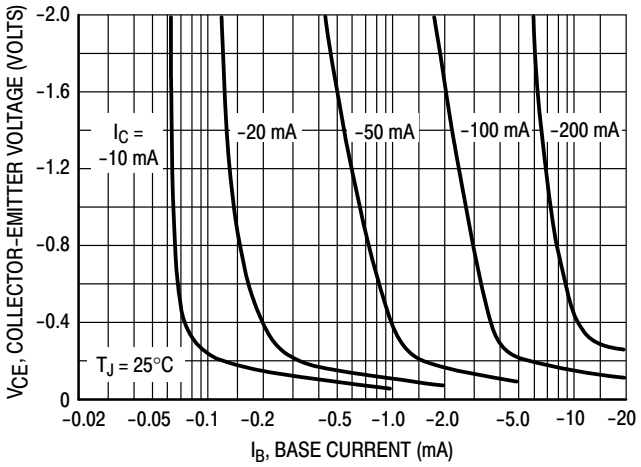


Figure 9. Collector Saturation Region

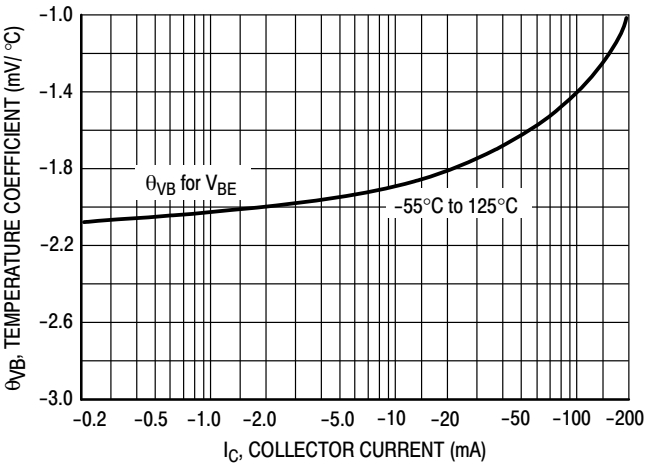


Figure 10. Base−Emitter Temperature Coefficient

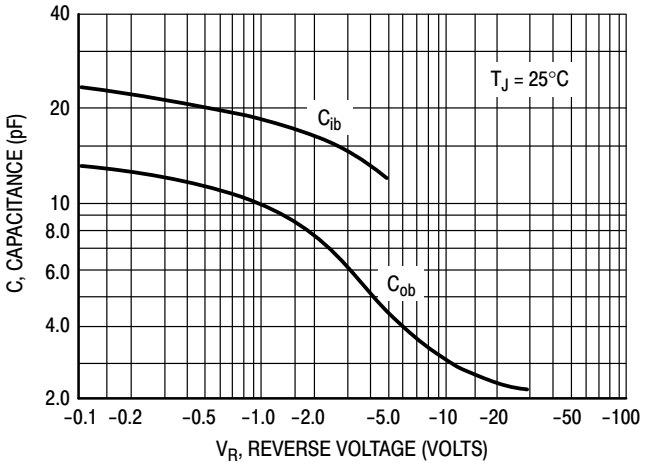


Figure 11. Capacitance

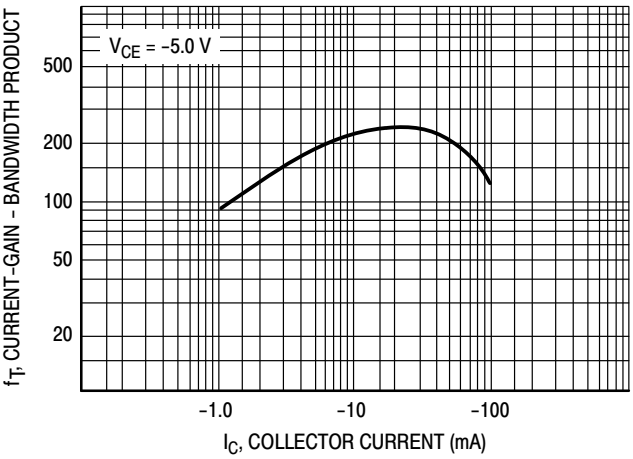


Figure 12. Current−Gain − Bandwidth Product

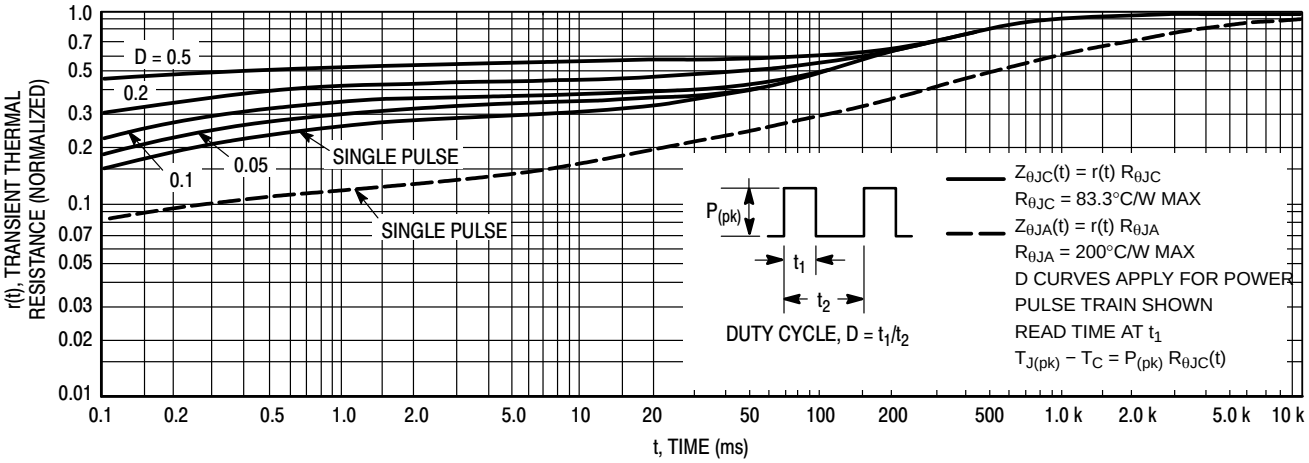


Figure 13. Thermal Response

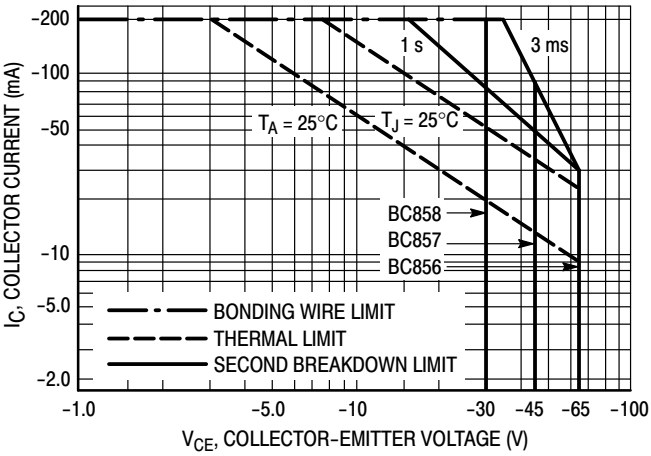


Figure 14. Active Region Safe Operating Area

The safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 14 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
BC856BWT1G	3B	SC−70/SOT−323 (Pb−Free)	3,000 / Tape & Reel
SBC856BWT1G*			
BC857BWT1G	3F	SC−70/SOT−323 (Pb−Free)	3,000 / Tape & Reel
SBC857BWT1G*			
BC857CWT1G	3G	SC−70/SOT−323 (Pb−Free)	3,000 / Tape & Reel
NSVBC857CWT1G*			
BC858AWT1G	3J	SC−70/SOT−323 (Pb−Free)	3,000 / Tape & Reel
BC858BWT1G	3K	SC−70/SOT−323 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

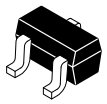
*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

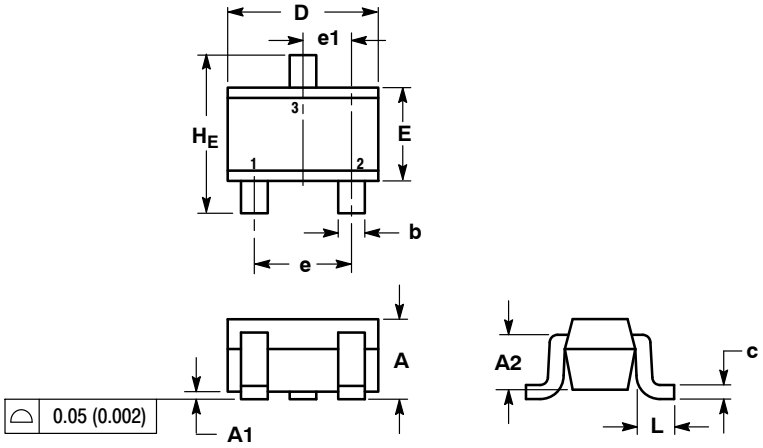
ON Semiconductor®

SC−70 (SOT−323)
CASE 419−04
ISSUE N

DATE 11 NOV 2008



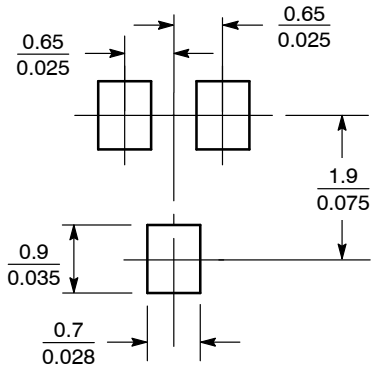
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

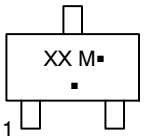
SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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