

MC14017B

Decade Counter

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature (8-Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

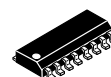
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



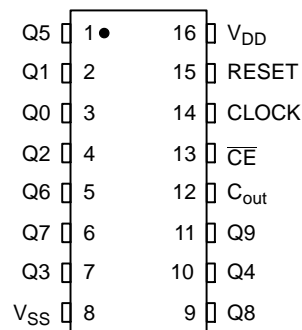
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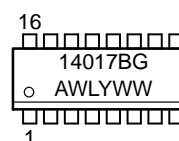


SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

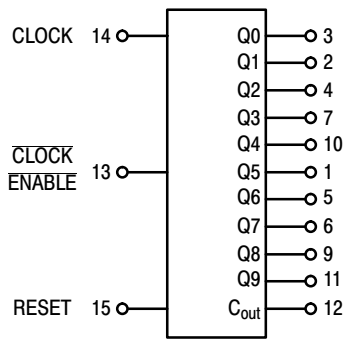
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FUNCTIONAL TRUTH TABLE (Positive Logic)

| Clock | Clock Enable | Reset | Decode Output=n |
|-------|--------------|-------|-----------------|
| 0 | X | 0 | n |
| X | 1 | 0 | n |
| X | X | 1 | Q0 |
| ↗ | 0 | 0 | n+1 |
| ↘ | X | 0 | n |
| X | ↗ | 0 | n |
| 1 | ↘ | 0 | n+1 |

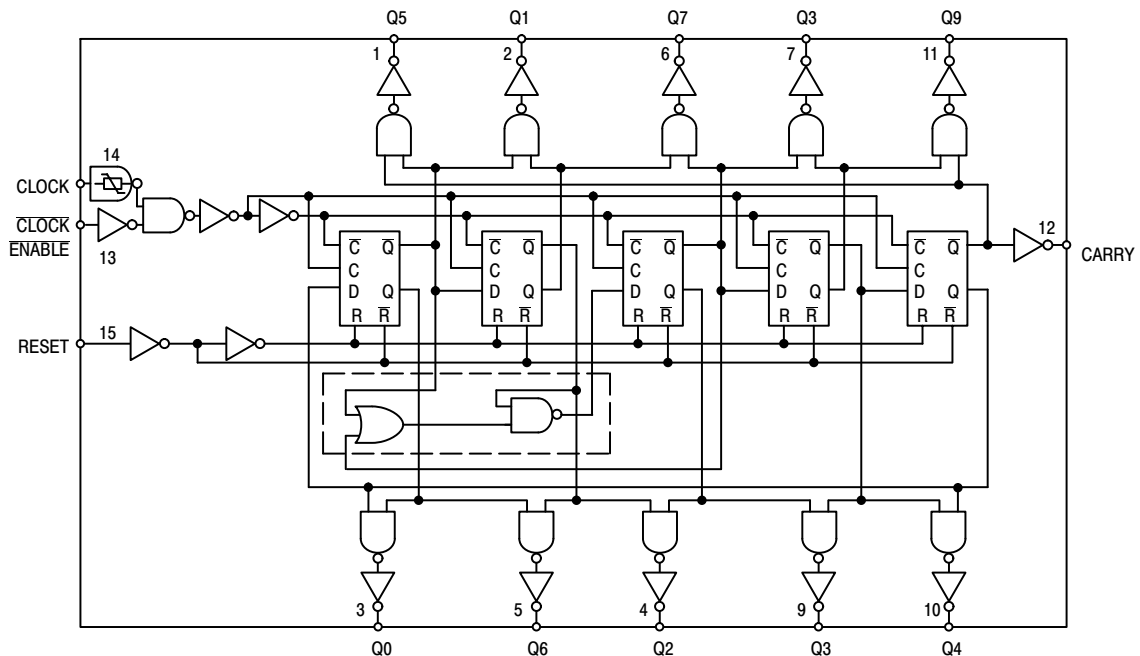
X = Don't Care. If n < 5 Carry = "1",
Otherwise = "0".

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit | |
|---|---|------------------------|--|-------|-------|-----------------|------|-------|-------|------|---|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level V _{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc | |
| | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | | |
| | "1" Level V _{in} = 0 or V _{DD} | V _{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | | - |
| | | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | | - |
| | | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | | - |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level V _{IL} | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | Vdc | |
| | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | | |
| | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | | |
| | "1" Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc) | V _{IH} | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | | - |
| | | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | | - |
| | | | 15 | 11 | - | 11 | 8.25 | - | 11 | | - |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source I _{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc | |
| | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | | |
| | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | | |
| | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | | |
| | Sink I _{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | | |
| | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | | |
| 15 | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | - | | | |
| Input Current | I _{in} | 15 | - | ±0.1 | - | ±0.00001 | ±0.1 | - | ±1.0 | μAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | μAdc | |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (0.27 μA/kHz) f + I _{DD} | | | | | | | μAdc | |
| | | 10 | I _T = (0.55 μA/kHz) f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (0.83 μA/kHz) f + I _{DD} | | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.0011.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (Note 6) | Max | Unit |
|---|--------------------------|-----------------|-------------------|-------------------|--------------------|------|
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{TLH} , t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Reset to Decode Output t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | – – – | 500 230 175 | 1000 460 350 | ns |
| Propagation Delay Time Clock to C_{out} t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | – – – | 400 175 125 | 800 350 250 | ns |
| Propagation Delay Time Clock to Decode Output t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | – – – | 500 230 175 | 1000 460 350 | ns |
| Turn-Off Delay Time Reset to C_{out} $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$ | t_{PLH} | 5.0 10 15 | – – – | 400 175 125 | 800 350 250 | ns |
| Clock Pulse Width | $t_{w(H)}$ | 5.0 10 15 | 250 100 75 | 125 50 35 | – – – | ns |
| Clock Frequency | f_{cl} | 5.0 10 15 | – – – | 5.0 12 16 | 2.0 5.0 6.7 | MHz |
| Reset Pulse Width | $t_{w(H)}$ | 5.0 10 15 | 500 250 190 | 250 125 95 | – – – | ns |
| Reset Removal Time | t_{rem} | 5.0 10 15 | 750 275 210 | 375 135 105 | – – – | ns |
| Clock Input Rise and Fall Time | t_{TLH} , t_{THL} | 5.0 10 15 | No Limit | | | – |
| Clock Enable Setup Time | t_{su} | 5.0 10 15 | 350 150 115 | 175 75 52 | – – – | ns |
| Clock Enable Removal Time | t_{rem} | 5.0 10 15 | 420 200 140 | 260 100 70 | – – – | ns |

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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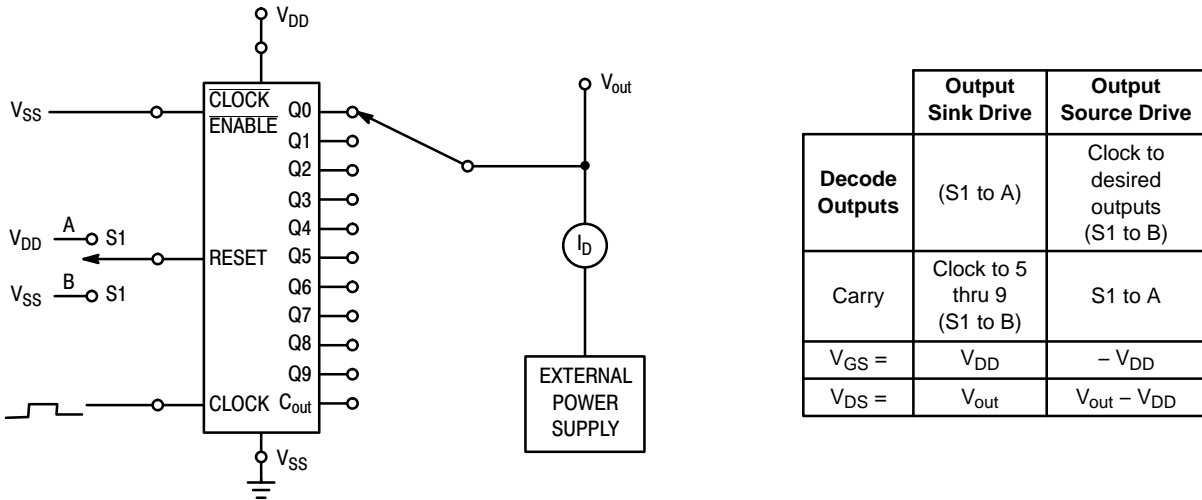


Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

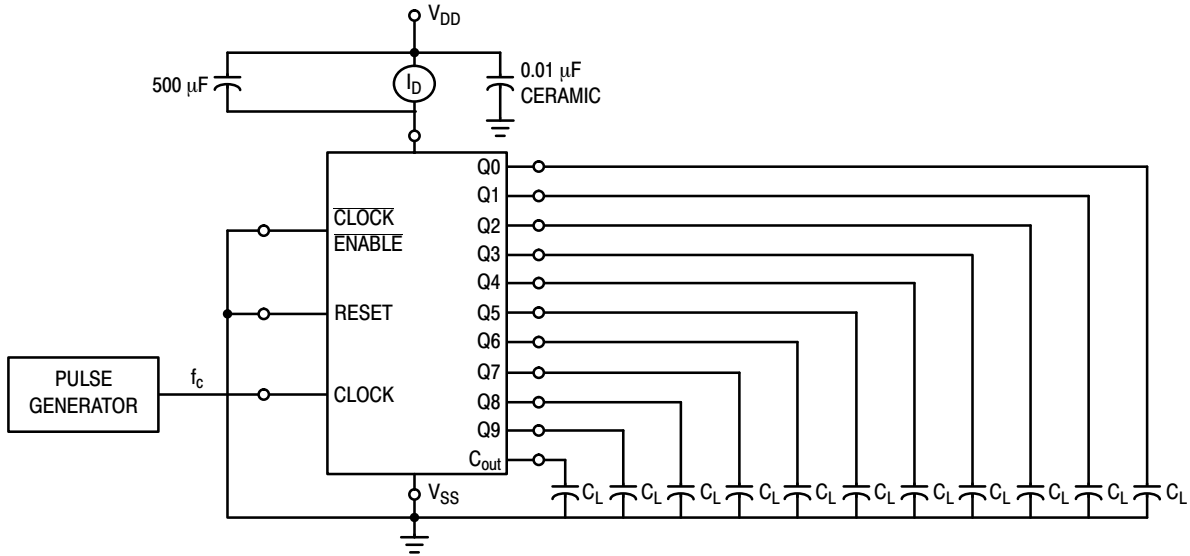


Figure 2. Typical Power Dissipation Test Circuit

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APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

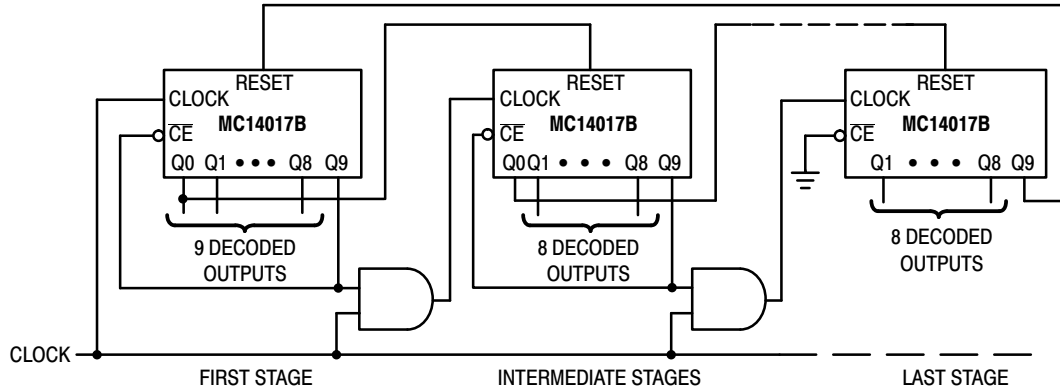


Figure 3. Counter Expansion

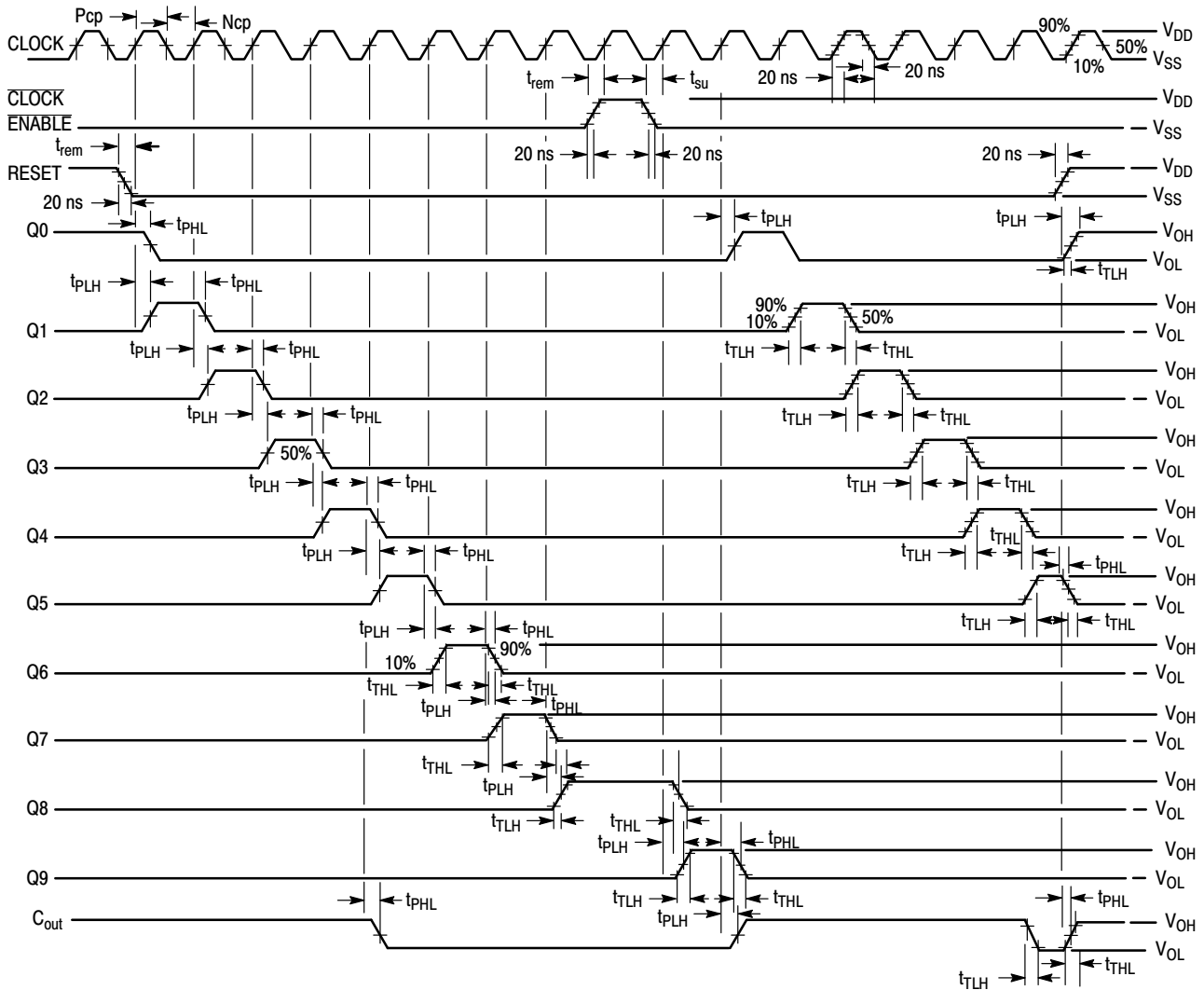


Figure 4. AC Measurement Definition and Functional Waveforms

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ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|----------------------|--------------------------|
| MC14017BDG | SOIC-16 (Pb-Free) | 48 Units / Rail |
| NLV14017BDG* | SOIC-16 (Pb-Free) | 48 Units / Rail |
| MC14017BDR2G | SOIC-16 (Pb-Free) | 2500 Units / Tape & Reel |
| NLV14017BDR2G* | SOIC-16 (Pb-Free) | 2500 Units / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p> | |

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

| | | |
|-------------------------|--------------------|---|
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