TPS2378 IEEE 802.3at PoE 高功率 PD 接口

1 特性

- 带有状态标志的 IEEE 802.3at 2 类硬件分类
- 适配器优先级输入
- 直流 (DC)/DC 转换器启用
- 稳健耐用的 100V、0.5Ω 热插拔金属氧化物半导体场效应晶体管 (MOSFET)
- 工作电流高达 850mA
- 1A（典型值）工作电流限值
- 15kV 和 8kV 系统级静电放电 (ESD) 能力
- PowerPAD™HSOP 封装

2 应用

- IEEE 802.3at 兼容器件
- 视频和网络语音 (VoIP) 电话
- 多频带访问点
- 监控摄像机
- 微微基站
- 强制型、四对、高功率设备（SLVA625）

3 说明

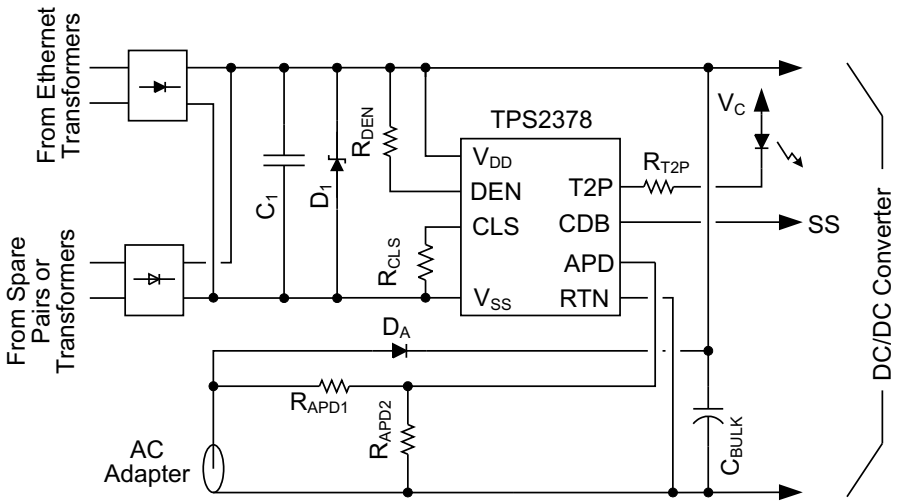
这款 8 引脚集成电路包含 实现 IEEE802.3at 2 类受电设备 (PD) 所需的全部功能。该控制器的内部开关电阻低至 0.5Ω，并且采用耐热增强型 PowerPAD 封装，因此能够长时间在高达 0.85A 的电流下运行。TPS2378 具有 一个辅助电源检测 (APD) 输入，可优先连接外部电源适配器。该器件还 具有 100V 导通晶体管、140mA 浪涌电流限制、2 类指示、自动重试故障保护以及开漏电源正常状态输出。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS2378	HSOP (8)	4.89mm × 3.90mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型应用电路



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (November 2012) to Revision C — **Page**

- 已添加 *ESD 额定值表，特性 描述* 部分，*器件功能模式，应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Deleted *Detailed Pin Description* section. ... 15
- Deleted *CBD Pin Interface* section ... 22
- Deleted APD Pin Divider Network, R_{APD1}, R_{APD2} section ... 22

Changes from Revision A (March 2012) to Revision B — **Page**

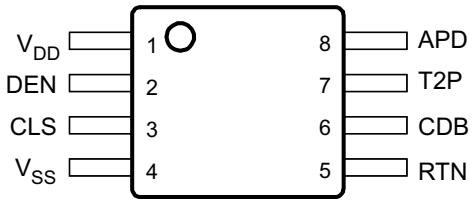
- 已增加应用：强制型、四对、高功率设备 (SLVA625) ... 1
- Added Note 1 to the ELECTRICAL CHARACTERISTICS table ... 6
- Added section: Forced, Four-Pair, High Power PoE ... 13
- Changed Table 2, From: POWER ≤ 12.95W To: POWER ≤ 13W, From: POWER > 12.95W To POWER > 13W, and PD INPUT POWER (max) From: 12.95 W To 13W ... 14
- Changed Table 2, PSE Output Power for 802.3at (Type 2) From: 36W to 30W ... 14
- Changed text in the Detection section From: "(ΔV / ΔI) between 23.75 kΩ and 26.25 kΩ at the PI." To: "(ΔV / ΔI) between 23.7 kΩ and 26.3 kΩ at the PI." ... 16
- Added text to the Startup and Converter Operation section: "Additional loading applied between V_{VDD} and V_{RTN} during the inrush state may prevent successful PD and subsequent converter start up." ... 17
- Changed text in the Detection Resistor, R_{DEN} section From: "R_{DEN} between 23.75 kΩ and 26.25 kΩ, or 25 kΩ ± 5%. " To: "R_{DEN} between 23.7 kΩ and 26.3 kΩ, or 25 kΩ ± 5%." ... 22

Changes from Original (March 2012) to Revision A — **Page**

- Changed the Inrush termination MAX value From: 100% To: 99% ... 5

5 Pin Configuration and Functions

DDA Package
8-Pin HSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	I	Connect to positive PoE input power rail. Bypass with 0.1 µF to V_{SS}.
DEN	2	I/O	Connect 24.9 kΩ to V_{DD} for detection. Pull to V_{SS} disable pass MOSFET.
CLS	3	O	Connect resistor from CLS to V_{SS} to program classification current.
V_{SS}	4	—	Connect to negative power rail derived from PoE source.
RTN	5	—	Drain of PoE pass MOSFET.
CDB	6	O	Active low, open-drain converter disable output, referenced to RTN.
T2P	7	O	Active low indicates type 2 PSE connected or APD active.
APD	8	I	Raise 1.5 V above RTN to disable pass MOSFET and force T2P active.
Pad	—	—	The PowerPad™ must be connected to V_{SS}. A large fill area is required to assist in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended T_J range; voltages with respect to V_{VSS} (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{DD}, DEN	–0.3	100	V
	RTN(2)	–0.6	100	
	CLS(3)	–0.3	6.5	
	APD to RTN	–0.3	19	
	[CDB, T2P] to RTN	–0.3	100	
Sinking current	RTN(4)	Internally limited		mA
	CDB, T2P		5	
	DEN		1	
Sourcing current	CLS		65	mA
T_{JMAX}	Maximum junction temperature	Internally limited		°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) With $I_{(RTN)} = 0$
(3) Do not apply voltages to these pins
(4) SOA limited to RTN = 80 V at 1.2 A.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	
	IEC 61000-4-2 contact discharge(3)	8000	
	IEC 61000-4-2 air-gap discharge(3)	15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Discharges applied to circuit of Figure 24 between RJ-45, adapter, and output voltage rails

6.3 Recommended Operating Conditions

over operating free-air temperature range and voltages with respect to V_{SS} (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	RTN, VDD	0		57	V
	APD to RTN	0		18	
	CDB, T2P to RTN	0		57	
Sinking current	RTN			0.85	A
	CDB, T2P			2	mA
Resistance	CLS(1)	60			Ω
Junction temperature		–40		125	°C

(1) Voltage should not be externally applied to this pin.

6.4 Thermal Information

THERMAL METRIC(1)		TPS2378 DDA (HSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

40 V ≤ V_{VDD} ≤ 57 V, R_{DEN} = 24.9 kΩ, V_{CDB}, V_{CLS}, and V_{T2P} open; V_{APD} = V_{RTN}; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION (DEN)						
	Bias current	DEN open, V_{VDD} = 10.1 V, Measure I_{SUPPLY}(VDD, RTN, DEN), Not in mark	3	4.8	12	µA
	Detection current	Measure I_{SUPPLY}(VDD, RTN, DEN), V_{DD} = 1.4 V	53.8	56.5	58.3	µA
		Measure I_{SUPPLY}(VDD, RTN, DEN), V_{DD} = 10.1 V, Not in mark	395	410	417	
V_{PD_DIS}	Disable threshold	DEN falling	3	3.7	5	V
	Hysteresis		50	113	200	mV
AUXILIARY POWER DETECTION (APD)						
V_{APDEN}	Voltage threshold	V_{APD} rising, measure to V_{RTN}	1.4	1.5	1.6	V
V_{APDH}	Voltage threshold	Hysteresis, measure to V_{RTN}	0.27	0.3	0.33	
	Sinking current	$V_{(APD–RTN)}$ = 5 V, measure I_{APD}	1	1.73	3	µA
CLASSIFICATION (CLS)						
I_{CLS}	Classification current	13 V ≤ V_{VDD} ≤ 21 V, Measure IV_{DD} + I_{DEN} + I_{RTN}				mA
		R_{CLS} = 1270 Ω	1.8	2.17	2.6	
		R_{CLS} = 243 Ω	9.9	10.6	11.2	
		R_{CLS} = 137 Ω	17.6	18.6	19.4	
		R_{CLS} = 90.9 Ω	26.5	27.9	29.3	
		R_{CLS} = 63.4 Ω	38	39.9	42	
V_{CL_ON}	Class lower threshold	V_{VDD} rising, I_{CLS} ↑	11.9	12.5	13	V
V_{CL_H}	Class lower threshold	Hysteresis	1.4	1.6	1.7	
V_{CU_ON}	Class upper threshold	V_{VDD} rising, I_{CLS}↓	21	22	23	V
V_{CU_H}	Class upper threshold	Hysteresis	0.5	0.78	0.9	
V_{MSR}	Mark reset threshold	V_{VDD} falling	3	3.9	5	V
	Mark state resistance	2-point measurement at 5 V and 10.1 V	6	10	12	kΩ
	Leakage current	V_{VDD} = 57 V, V_{CLS} = 0 V, measure I_{CLS}			1	µA
PASS DEVICE (RTN)						
$r_{DS(on)}$	On resistance		0.2	0.42	0.75	Ω
	Input bias current	V_{VDD} = V_{RTN} = 30 V, measure I_{RTN}			30	µA
	Current limit	V_{RTN} =1.5 V	0.85	1	1.2	A
	Inrush current limit	V_{RTN} = 2 V, V_{VDD}: 20 V → 48 V	100	140	180	mA
	Inrush termination	Percentage of inrush current	80%	90%	99%	
	Foldback threshold	V_{RTN} rising	11	12.3	13.6	V

Electrical Characteristics (continued)

40 V ≤ V_{VDD} ≤ 57 V, R_{DEN} = 24.9 kΩ, V_{CDB}, V_{CLS}, and V_{T2P} open; V_{APD} = V_{RTN}; –40°C ≤ T_J ≤ 125°C. Positive currents are into pins. Typical values are at 25°C. All voltages are with respect to V_{VSS} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Foldback deglitch time	V_{RTN} rising to when current limit changes to inrush current limit	500	800	1500	µs
CONVERTER DISABLE (CDB)						
	Output low voltage	Measure V_{CDB} – V_{RTN}, I_{CDB} = 2 mA, V_{RTN} = 2 V, V_{DD}: 20 V → 48 V		0.27	0.5	V
	Leakage current	V_{CDB} = 57 V, V_{RTN} = 0 V			10	µA
TYPE 2 PSE INDICATION (T2P)						
V_{T2P}	Output low voltage	I_{T2P} = 2 mA, after 2-event classification and inrush is complete, V_{RTN} = 0 V		0.26	0.6	V
	Leakage current	V_{T2P} = 57 V, V_{RTN} = 0 V			10	µA
UVLO						
V_{UVLO_R}	UVLO rising threshold	V_{VDD} rising	36.3	38.1	40	V
	UVLO falling threshold	V_{VDD} falling	30.5	32	33.6	
V_{UVLO_H}	UVLO hysteresis			6.1		V
THERMAL SHUTDOWN						
	Shutdown	T_J↑	135	145		°C
	Hysteresis (1)			20		°C
BIAS CURRENT						
	Operating current	40 V ≤ V_{VDD} ≤ 57 V		285	500	µA

(1) Parameters provided for reference only, and do not constitute part of TI published specifications for purposes of TI product warranty.

6.6 Typical Characteristics

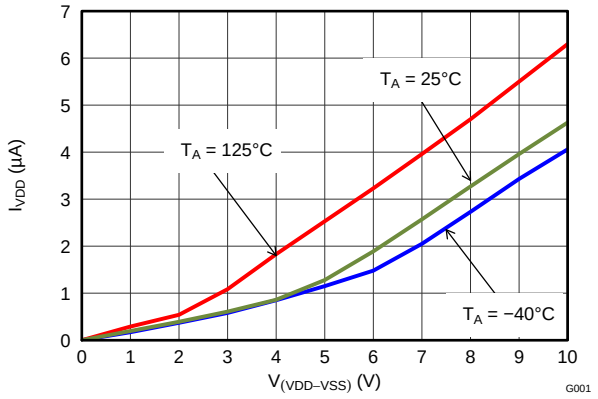


Figure 1. Detection Bias Current vs PoE Voltage

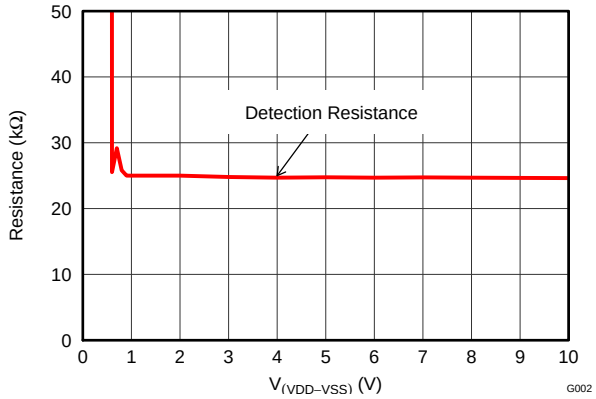


Figure 2. Detection Resistance vs PoE Voltage

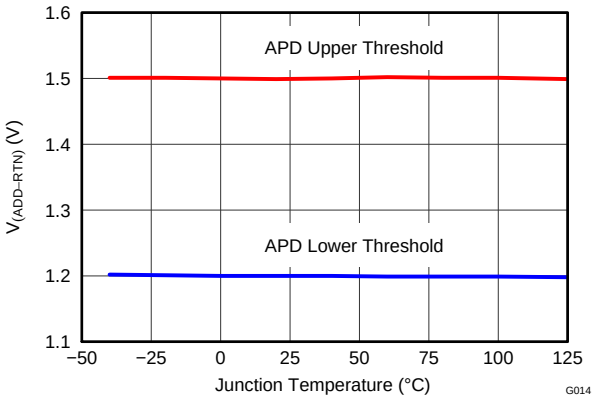


Figure 3. APD Threshold Voltage vs Temperature

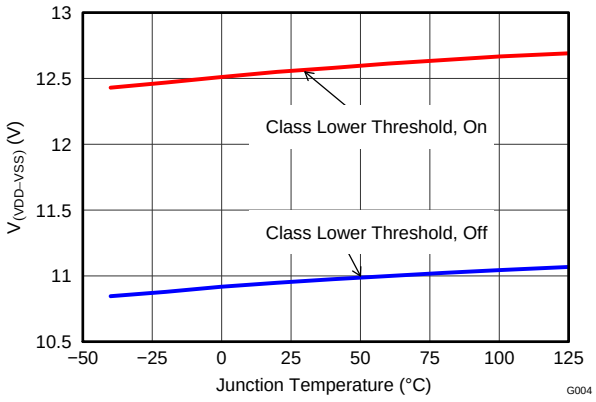


Figure 4. Classification Lower Threshold vs Temperature

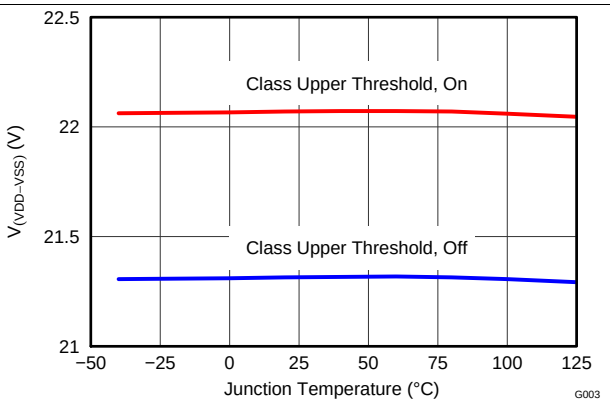


Figure 5. Classification Upper Threshold vs Temperature

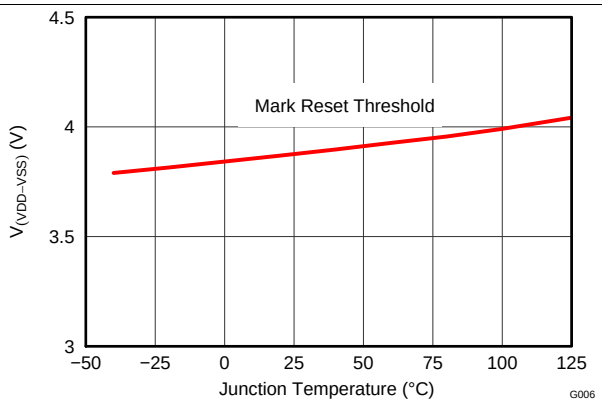


Figure 6. Mark Reset Threshold vs Temperature

Typical Characteristics (continued)

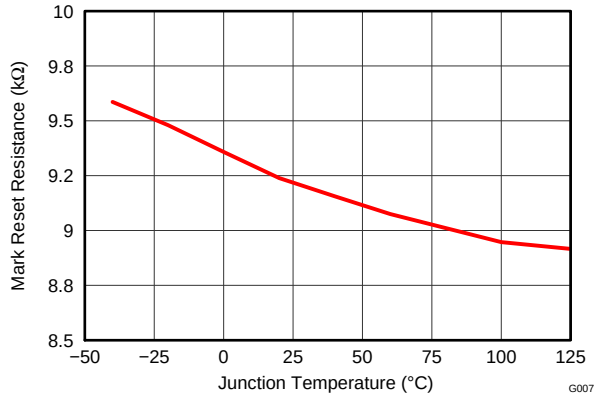


Figure 7. Mark Resistance vs PoE Voltage

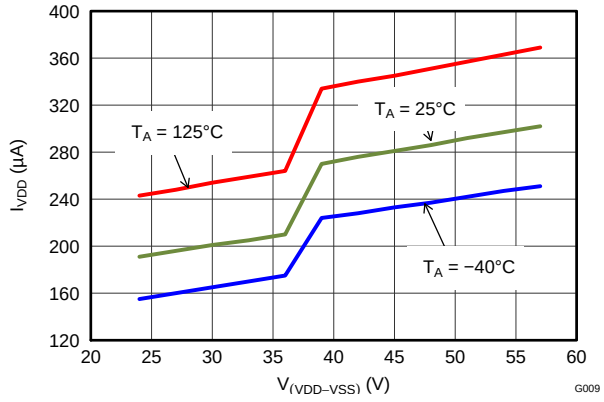


Figure 8. I_{VDD} Bias Current vs Voltage

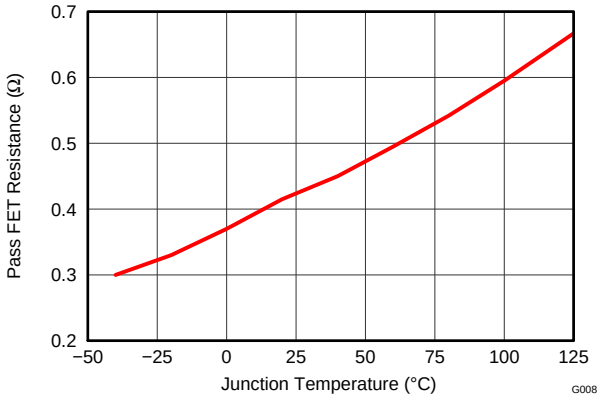


Figure 9. Pass FET Resistance vs Temperature

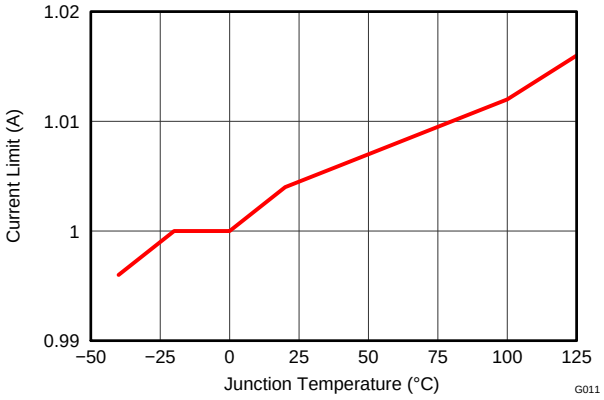


Figure 10. PoE Current Limit vs Temperature

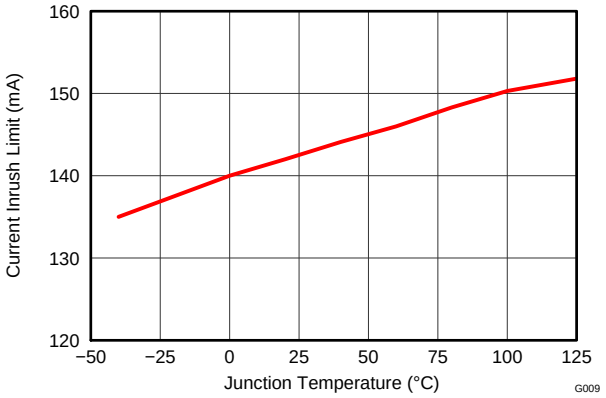


Figure 11. PoE Inrush Current Limit vs Temperature

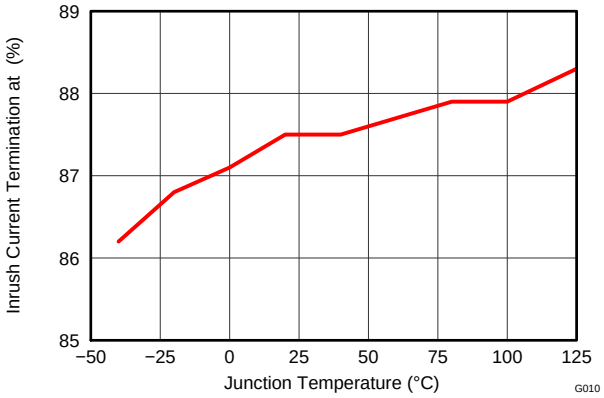


Figure 12. Inrush Termination Threshold vs Temperature

Typical Characteristics (continued)

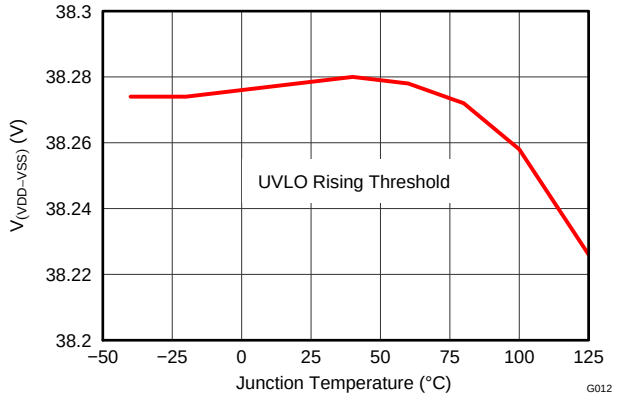


Figure 13. UVLO Rising Threshold vs Temperature

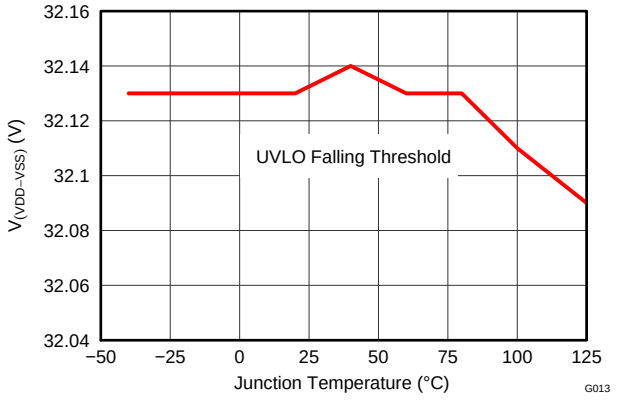


Figure 14. UVLO Falling Threshold vs Temperature

7 Detailed Description

7.1 Overview

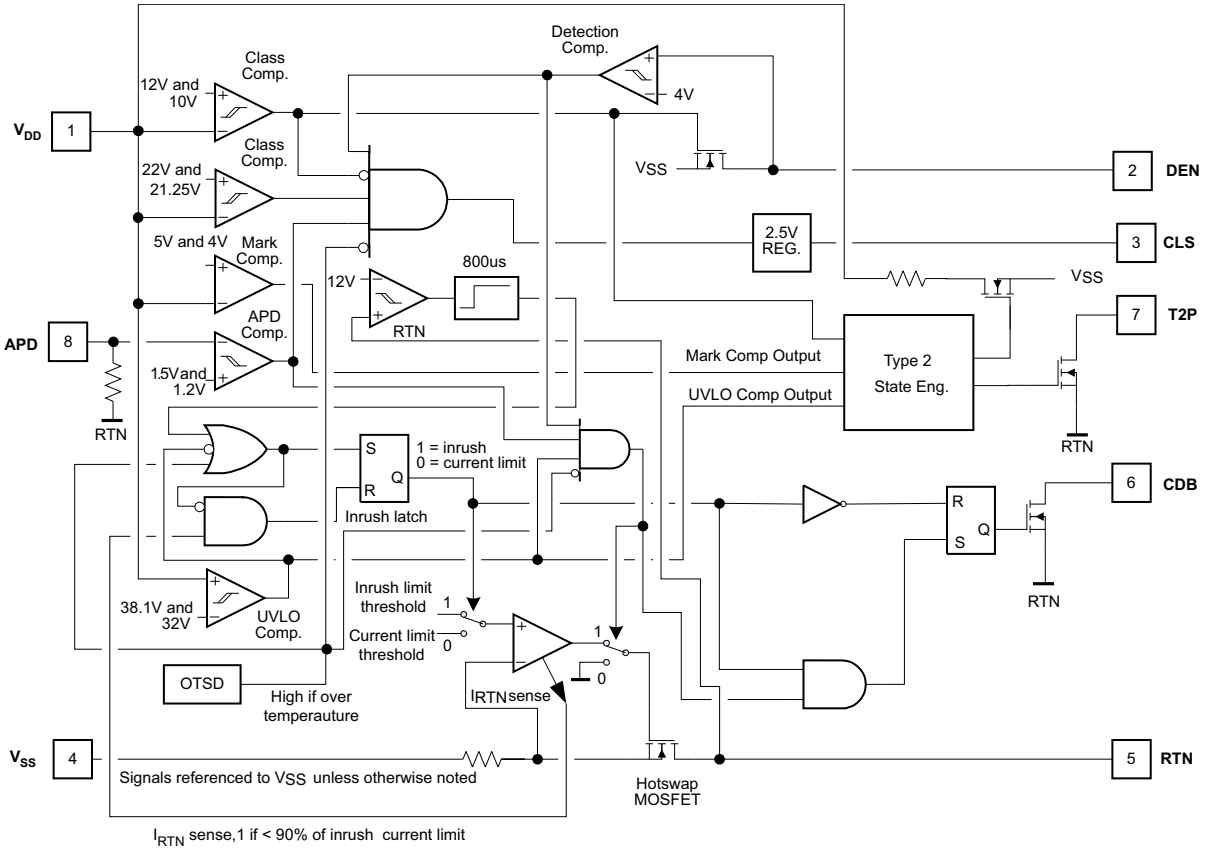
The TPS2378 device is an 8-pin integrated circuit that contains all of the features needed to implement an IEEE802.3at type-2 powered device (PD) such as Detection, Classification, Type 2 Hardware Classification, and 140-mA inrush current limit during start-up.

The TPS2378 integrates a low 0.5-Ω internal switch to allow for up to 0.85 A of continuous current through the PD during normal operation.

The TPS2378 features an auxiliary power detect (APD) input, providing priority for an external power adapter.

The TPS2378 contains several protection features such as thermal shutdown, current limit foldback, and a robust 100-V internal switch.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 APD Auxiliary Power Detect

The APD pin is used in applications that may draw power either from the Ethernet cable or from an auxiliary power source. A voltage of more than about 1.5 V on the APD pin relative to RTN turns off the internal pass MOSFET, disables the CLS output, and enables the T2P output, giving adapter source priority over the PoE. A resistor divider (R_{APD1}–R_{APD2} in Figure 24) provides system-level ESD protection for the APD pin, discharges leakage from the blocking diode (D_A in Figure 24) and provides input voltage supervision to ensure that switch-over to the auxiliary voltage source does not occur at excessively low voltages. If not used, connect APD to RTN.

Feature Description (continued)

7.3.2 CDB Converter Disable Bar Pin Interface

CDB is an active low output that is pulled to RTN when the device is in inrush current limiting. It remains in a high impedance state at all other times. This pin is an open-drain output, and it may require a pullup resistor or other interface to the downstream load. CDB may be left open if it is not used.

The CDB pin can be used to inhibit downstream converter start-up by keeping the soft start pin low. Figure 15 shows an example where CDB connects to the SS pin of a UCC2897A DC-DC controller. Because CDB is an open drain output, it will not affect the soft start capacitor charge time when it deasserts. Another common use of the CDB pin is to enable a converter with an active-high enable input. In this case, CDB may require a pullup resistor to either VDD, or to a bias supply, depending on the requirements of the controller enable pin.

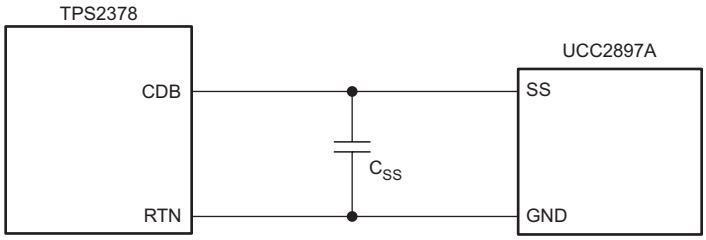


Figure 15. CDB Interface

7.3.3 CLS Classification

An external resistor (RCLS in Figure 24) connected between the CLS pin and VSS provides a classification signature to the PSE. The controller places a voltage of approximately 2.5 V across the external resistor whenever the voltage differential between VDD and VSS lies from about 10.9 V to 22 V. The current drawn by this resistor, combined with the internal current drain of the controller and any leakage through the internal pass MOSFET, creates the classification current. Table 1 lists the external resistor values required for each of the PD power ranges defined by IEEE802.3at. The maximum average power drawn by the PD, plus the power supplied to the downstream load, should not exceed the maximum power indicated in Table 1. Holding APD high disables the classification signature.

High-power PSEs may perform two classification cycles if Class 4 is presented on the first cycle.

Table 1. Class Resistor Selection

CLASS	MINIMUM POWER AT PD (W)	MAXIMUM POWER AT PD (W)	RESISTOR (Ω)
0	0.44	12.95	1270
1	0.44	3.84	243
2	3.84	6.49	137
3	6.49	12.95	90.9
4	12.95	25.5	63.4

7.3.4 DEN Detection and Enable

DEN pin implements two separate functions. A resistor (R_{DEN} in Figure 24) connected between V_{DD} and DEN generates a detection signature whenever the voltage differential between V_{DD} and V_{SS} lies from approximately 1.4 to 10.9 V. Beyond this range, the controller disconnects this resistor to save power. The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} from 23.75 kΩ to 26.25 kΩ, or 25 kΩ ± 5%. TI recommends a resistor of 24.9 kΩ ± 1% for R_{DEN}.

If the resistance connected between V_{DD} and DEN is divided into two roughly equal portions, then the application circuit can disable the PD by grounding the tap point between the two resistances. This action simultaneously spoils the detection signature and thereby signals the PSE that the PD no longer requires power.

7.3.5 Internal Pass MOSFET

RTN pin provides the negative power return path for the load. Once V_{DD} exceeds the UVLO threshold, the internal pass MOSFET pulls RTN to VSS. Inrush limiting prevents the RTN current from exceeding about 140 mA until the bulk capacitance (C_{BULK} in Figure 24) is fully charged. Inrush ends when the RTN current drops below about 125 mA. The RTN current is subsequently limited to about 1 A. The CDB pulls low to signal the downstream load that the bulk capacitance is fully charged. If RTN ever exceeds about 12 V for longer than 800 μs, then the TPS2378 returns to inrush limiting.

7.3.6 T2P Type-2 PSE Indicator

The TPS2378 pulls T2P to RTN whenever type-2 hardware classification has been observed or the APD pin is pulled high. The T2P output will return to a high-impedance state if the part enters thermal shutdown, the pass MOSFET enters inrush limiting, or if a type-2 PSE was not detected and the voltage on APD drops below its threshold. The circuitry that watches for type-2 hardware classification latches its result when the V_{DD}-to-V_{SS} voltage differential rises above the upper classification threshold. This circuit resets when the V_{DD}-to-V_{SS} voltage differential drops below the mark threshold. The T2P pin can be left unconnected if it is not used.

The T2P pin is an active-low, open-drain output, which indicates that a high power source is available. An optocoupler can interface the T2P pin to circuitry on the secondary side of the converter. A high-gain optocoupler and a high-impedance (for example, CMOS) receiver are recommended. Design of the T2P optocoupler interface can be accomplished as follows:

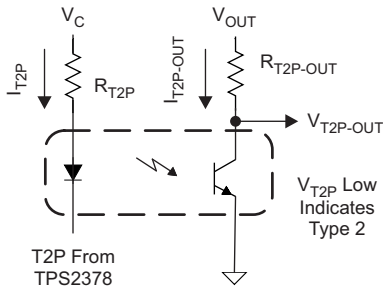


Figure 16. T2P Interface

1. As shown in Figure 16, let V_C = 12 V, V_{OUT} = 5 V, $R_{T2P–OUT}$ = 10 kΩ, V_{T2P} = 260 mV, V_{T2P} = 400 mV.

$$I_{T2P–OUT} = \frac{V_{OUT} - V_{T2P–OUT}}{R_{T2P–OUT}} = \frac{5 - 0.4}{10000} = 0.46\text{mA} \quad (1)$$

2. The optocoupler current transfer ratio, CTR, is needed to determine RT2P. A device with a minimum CTR of 100% at 1 mA LED bias current, IT2P, is selected. In practice, CTR will vary with temperature, LED bias current, and aging, These variations may require some iteration using the CTR-versus-IDIODE curve on the optocoupler data sheet.
   (a) The approximate forward voltage of the optocoupler diode, VFWLED, is 1.1 V from the data sheet.
   (b) Use Equation 2.

$$I_{T2P\text{-}MIN} = \frac{I_{T2P\text{-}OUT}}{CTR} = \frac{0.46\text{mA}}{1.00} = 0.46\text{mA}, \text{ Select } I_{T2P} = 1\text{mA}$$

$$R_{T2P} = \frac{V_C - V_{T2P} - V_{FWLED}}{I_{T2P}} = \frac{12\text{ V} - 0.26\text{ V} - 1.1\text{ V}}{1\text{mA}} = 10.6\text{k}\Omega \quad (2)$$

   (c) Select a 10.7-kΩ resistor.

7.3.7 VDD Supply Voltage

VDD pin connects to the positive side of the input supply. It provides operating power to the PD controller and allows monitoring of the input line voltage.

7.3.8 VSS

VSS pin is the input supply negative rail that serves as a local ground. The PowerPAD must be connected to this pin to ensure proper operation.

7.3.9 PowerPAD

The PowerPAD is internally connected to V_{SS}. It should be tied to a large V_{SS} copper area on the PCB to provide a low resistance thermal path to the circuit board. TI recommends maintaining a clearance of 0.025" between V_{SS} and high-voltage signals such as V_{DD}.

7.3.10 Forced, Four-Pair, High Power PoE

TPS2378 can be arranged in a dual fashion to support high power, four pair operation at 51 W at the input RJ45 connector. Additional information is available in the *Dual TPS2378 PD for 51 W High Power-Four Pair PoE* (SLVA625) application report.

7.4 Device Functional Modes

7.4.1 PoE Overview

The following text is intended as an aid in understanding the operation of the TPS2378 but not as a substitute for the IEEE 802.3at standard. The IEEE 802.3at standard is an update to IEEE 802.3-2008 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2008 is referred to as a type 1 device, and devices with high power and enhanced classification will be referred to as type 2 devices. Standards change and should always be referenced when making design decisions.

The IEEE 802.3at standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE may inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 2 PSEs are required to do type 1 hardware classification plus a (new) data-layer classification, or an enhanced type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A type 2 PD must do type 2 hardware classification as well as DLL classification. The PD may return the default, 13-W current-encoded class, or one of four other choices. DLL classification occurs after power-on and the Ethernet data link has been established.

Once started, the PD must present a maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 17 shows the operational states as a function of PD input voltage. The upper half is for IEEE 802.3-2008, and the lower half shows specific differences for IEEE 802.3at. The dashed lines in the lower half indicate these are the same (for example, Detect and Class) for both.

Device Functional Modes (continued)

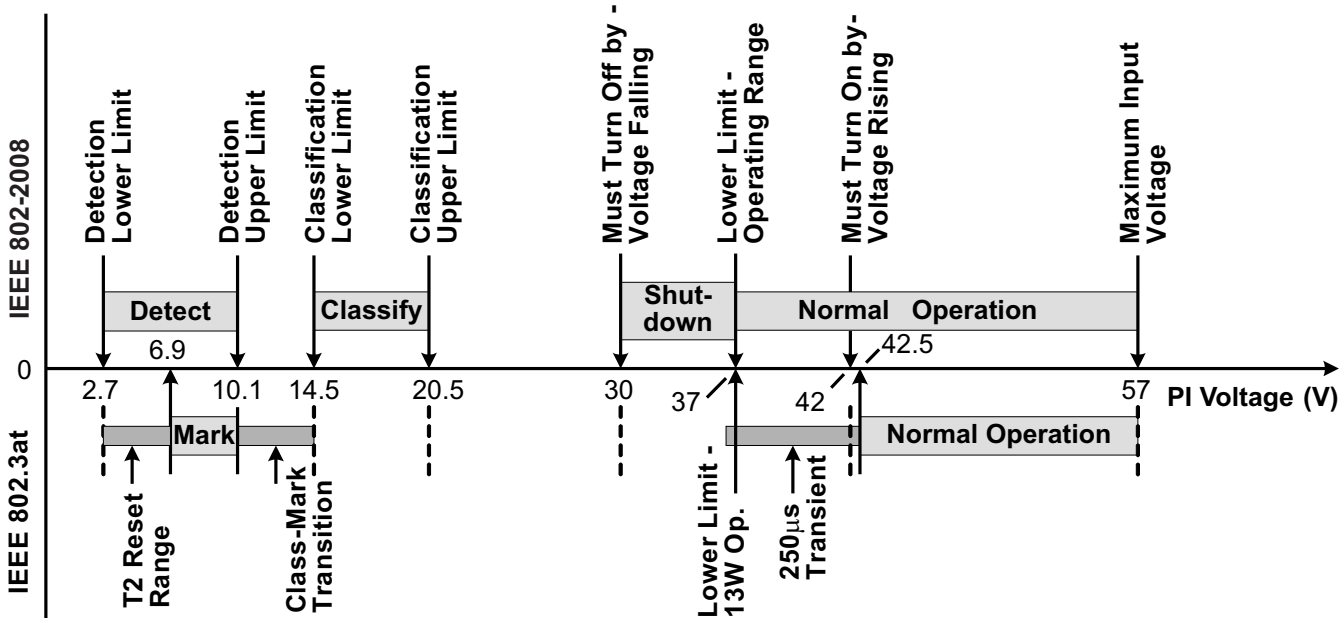


Figure 17. Threshold Voltages

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2008 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at type 2 cabling power loss allotments and voltage drops have been adjusted for 12.5-Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG 24 conductors). Table 2 shows key operational limits broken out for the two revisions of the standard.

Table 2. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (MAX)	PSE OUTPUT POWER (MIN)	PSE STATIC OUTPUT VOLTAGE (MIN)	PD INPUT POWER (MAX)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 13 W	POWER > 13 W
IEEE802.3at-2008 802.3at (Type 1)	20 Ω	15.4 W	44 V	13 W	37 V – 57 V	N/A
802.3at (Type 2)	12.5 Ω	30 W	50 V	25.5 W	37 V – 57 V	42.5 V – 57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1–2 and 3–6 for 10baseT or 100baseT), or between the two spare pairs (4–5 and 7–8). Power application to the same pin combinations in 1000baseT systems is recognized in IEEE 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS2378 specifications.

A compliant type 2 PD has power management requirements not present with a type 1 PD. These requirements include the following:

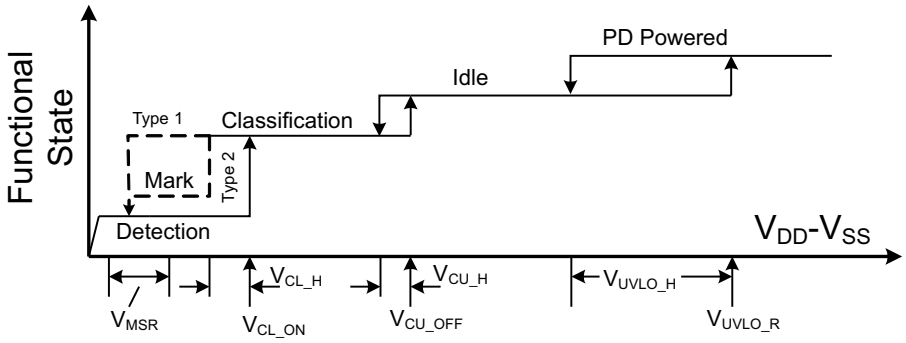
1. Must interpret type 2 hardware classification.
2. Must present hardware class 4.
3. Must implement DLL negotiation.
4. Must behave like a type 1 PD during inrush and start-up.
5. Must not draw more than 13 W for 80 ms after the PSE applies operating voltage (power up).

6. Must not draw more than 13 W if it has not received a type 2 hardware classification or received permission through DLL.
7. Must meet various operating and transient templates.
8. Optionally monitor for the presence or absence of an adapter (assume high power).

As a result of these requirements, the PD must be able to dynamically control its loading, and monitor T2P for changes. In cases where the design needs to know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

7.4.2 Threshold Voltages

The TPS2378 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 18 relates the parameters in Electrical Characteristics to the PoE states. The mode labeled Idle between Classification and Operation implies that the DEN, CLS, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the new type 2 hardware class state machine.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 18. Threshold Voltages

7.4.3 PoE Start-up Sequence

The waveforms of Figure 19 demonstrate detection, classification, and start-up from a PSE with type 2 hardware classification. The key waveforms shown are $V_{(VDD-VSS)}$, $V_{(RTN-VSS)}$, and IPI. IEEE 802.3at requires a minimum of two detection levels, two class and mark cycles, and start-up from the second mark event. V_{RTN} to V_{SS} falls as the TPS2378 charges C_{BULK} following application of full voltage. In Figure 19, deassertion of the CDB signal is delayed and used to enable load current as seen in the I_{PI} waveform.

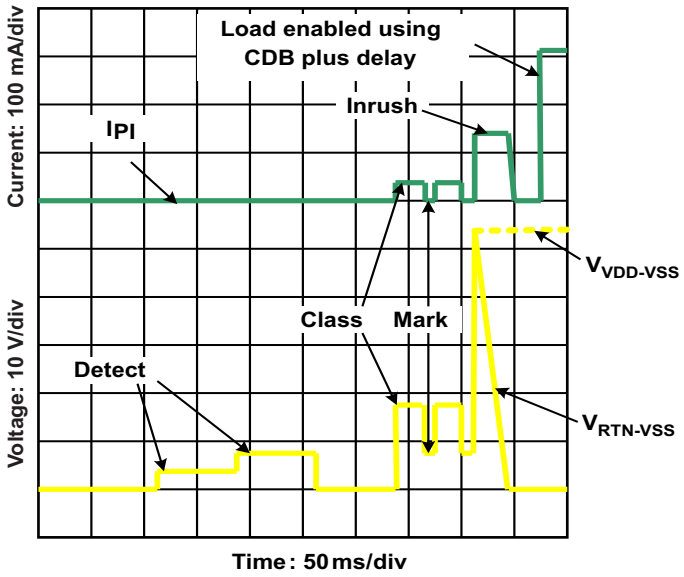


Figure 19. Start-up

7.4.4 Detection

The TPS2378 pulls DEN to V_{SS} whenever $V_{(VDD-VSS)}$ is below the lower classification threshold. When the input voltage rises above V_{CL_ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 kΩ (±1%), presents the correct signature. It may be a small, low-power resistor because it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance ($\Delta V / \Delta I$) from 23.7 kΩ to 26.3 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of Ω at the low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially compensated by the TPS2378 effective resistance during detection.

The type 2 hardware classification protocol of IEEE 802.3at specifies that a type 2 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as a mark event (see Figure 19). After the first mark event, the TPS2378 will present a signature less than 12 kΩ until it has experienced a $V_{(VDD-VSS)}$ voltage below the mark reset threshold (V_{MSR}). This is explained more fully under *Hardware Classification*.

7.4.5 Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2 hardware classification permits high power PSEs and PDs to determine whether the connected device can support high-power operation. A type 2 PD presents class 4 in hardware to indicate that it is a high-power device. A type 1 PSE will treat a class 4 device like a class 0 device, allotting 13 W if it chooses to power the PD. A PD that receives a 2-event class understands that it is powered from a high-power PSE and it may draw up to 25.5 W immediately after the 80-ms start-up period completes. A type 2 PD that does not receive a 2-event hardware classification may choose to not start, or must start in a 13-W condition and request more power through the DLL after start-up. The standard requires a type 2 PD to indicate that it is underpowered if this occurs. Start-up of a high-power PD under 13 W implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated class power, which may be the hardware class or a lower DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit; however, the average power requirement always applies.

The TPS2378 implements two-event classification. Selecting an R_{CLS} of 63.4 Ω provides a valid type 2 signature. TPS2378 may be used as a compatible type 1 device simply by programming class 0–3 per Table 1. DLL communication is implemented by the Ethernet communication system in the PD and is not implemented by the TPS2378.

The TPS2378 disables classification above V_{CU_ON} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limiting or when APD or $\overline{DEN}$ is active. The CLS output is inherently current-limited, but should not be shorted to V_{SS} for long periods of time.

Figure 20 shows how classification works for the TPS2378. Transition from state-to-state occurs when comparator thresholds are crossed (see Figure 17 and Figure 18). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2-event classification follows the (heavy lined) path towards the bottom, ending up with a latched type 2 decode along the lower branch that is highlighted. This state results in a low T2P during normal operation. Once the valid path to type 2 PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

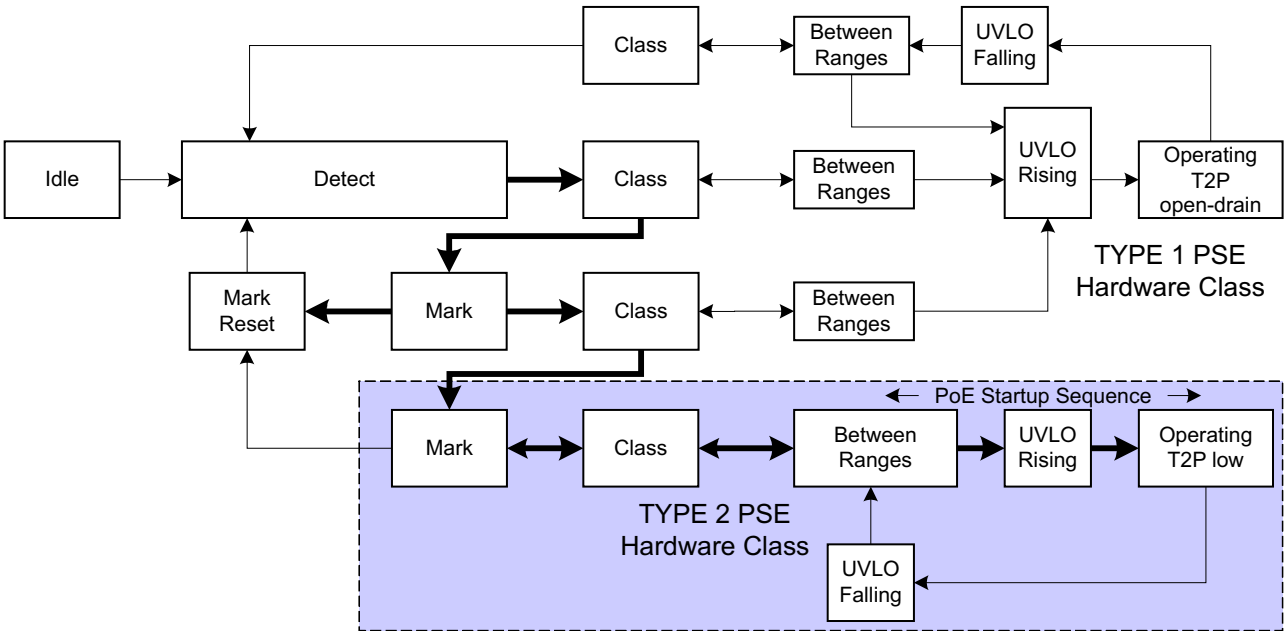


Figure 20. Two-Event Class Internal States

7.4.6 Inrush and Start-up

IEEE 802.3at has a start-up current and time limitation, providing type 2 PSE compatibility for type 1 PDs. A type 2 PSE limits output current to from 400 mA to 450 mA for up to 75 ms after power up (applying 48 V to the PI) to mirror type 1 PSE functionality. The type 2 PSE will support higher output current after 75 ms. The TPS2378 implements a 140-mA inrush current, which is compatible with all PSE types. A high-power PD must limit its converter start-up peak current. The operational current cannot exceed 400 mA for a period of 80 ms or longer. This requirement implicitly requires some form of powering down sections of the application circuits.

7.4.7 Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum dc current of 10 mA (or a 10-mA pulsed current for at least 75 ms every 325 ms) and an AC impedance lower than 26.3 kΩ in parallel with 0.05 µF. The AC impedance is usually accomplished by the minimum operating C_{BULK} requirement of 5 µF. When either APD or DEN is used to force the hotswap switch off, the DC MPS will not be met. A PSE that monitors the DC MPS will remove power from the PD when this occurs. A PSE that monitors only the ac MPS may remove power from the PD.

7.4.8 Start-up and Converter Operation

The internal PoE UVLO (Undervoltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{BULK} while the PD is unpowered. Thus $V_{(VDD-RTN)}$ will be a small voltage just after full voltage is applied to the PD, as seen in Figure 19. The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO_R}, approximately 38 V) with RTN high, the TPS2378 enables the hotswap MOSFET with a approximately 140 mA (inrush) current limit as seen in Figure 21. The CDB pin is active while C_{BULK} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}. Additional loading applied between V_{VDD} and V_{RTN} during the inrush state may prevent successful PD and subsequent converter start up. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (approximately 1000 mA) and CDB is deassert to allow downstream converter circuitry to start. In Figure 21, T2P is active when a type 2 PSE is plugged in.

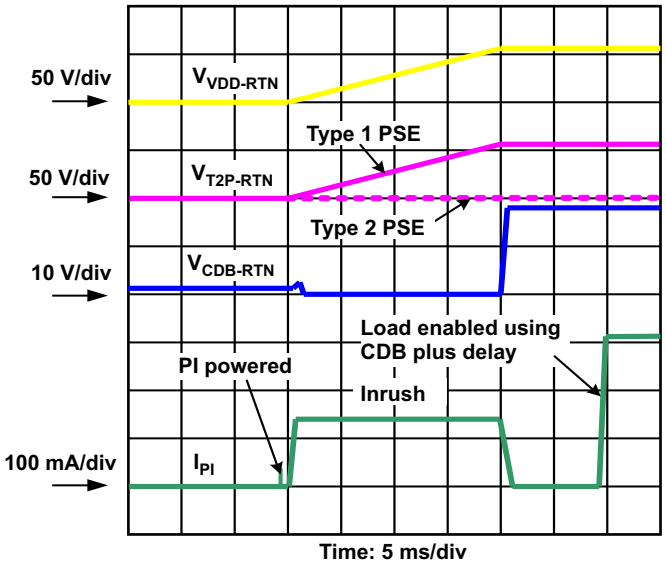


Figure 21. Power Up and Start

7.4.9 PD Hotswap Operation

IEEE 802.3at has taken a new approach to PSE output limiting. A type 2 PSE must meet an output current vs time template with specified minimum and maximum sourcing boundaries. The peak output current may be as high as 50 A for 10 µs or 1.75 A for 75 ms. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2008.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with $V_{(RTN-VSS)}$ rising as a result. If $V_{(RTN-VSS)}$ rises above approximately 12 V for longer than approximately 800 µs, the current limit reverts to the inrush value. The 800-µs deglitch feature prevents momentary transients from causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 22 shows an example of the RTN current profile during V_{DD} to RTN short circuit. The hotswap MOSFET goes into current limit, causing the RTN voltage to increase. Once V_{RTN} exceeds 12 V, I_{RTN}, which was clamped to the current limit drops to the level of inrush current limit after 800 µs. The inrush current limit is reestablished when $V_{(VDD-VSS)}$ drops below UVLO.

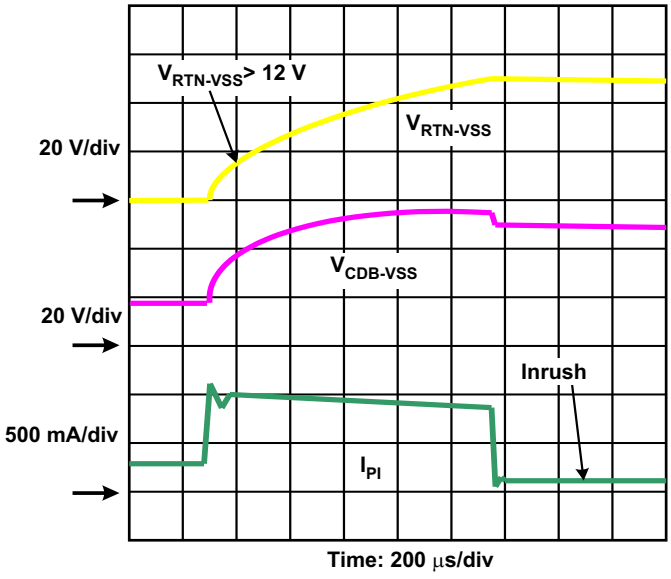


Figure 22. Response to PD Output Short Circuit

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like start-up or operation into a V_{DD}-to-RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The hotswap MOSFET will be re-enabled with the inrush current limit when exiting from an overtemperature event. Pulling DEN to VSS during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with option three ORing per Figure 23 to achieve adapter priority.

The hotswap switch will be forced off under the following conditions:

1. V_{APD} above V_{APDEN} (approximately 1.5 V),
2. $V_{(DEN\ –VSS)} < V_{PD-DIS}$ when $V_{(VDD-VSS)}$ is in the operational range,
3. PD is over-temperature, or
4. $V_{(DEN\ –VSS)}$ < PoE UVLO falling threshold (approximately 32 V).

7.4.10 Start-up and Power Management, CDB and T2P

CDB (converter disable) is an active-low pin that indicates when the internal hotswap MOSFET is in inrush limiting. CDB deasserts when inrush is over and can be used to enable a downstream converter to start up. Common interfaces to the converter controller include the soft start or enable pins.

T2P (type 2 PSE) is an active-low multifunction pin that indicates if

[(PSE = Type_2) or (1.5 V < V_{APD})] and (pd current limit ≠ Inrush).

The APD term allows the PD to operate from an adapter at high-power if a type 2 PSE is not present, assuming the adapter has sufficient capacity. Applications must monitor the state of T2P to detect power source transitions. Transitions could occur when a local power supply is added or dropped, or when a PSE is enabled on the far end. The PD may be required to adjust the load appropriately. The usage of T2P is demonstrated in Figure 24.

In order for a type 2 PD to operate at less than 13 W for the first 80 ms after power application, the various delays must be estimated and used by the application controller to meet the requirement. The bootup time of many application processors may be long enough to eliminate the need for any timing.

7.4.11 Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS2378 supports forced operation from either of the power sources. Figure 23 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS2378 PoE input, option 2 applies power between the TPS2378 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. Many of the basic ORing configurations and much of the discussion contained in the application note *Advanced Adapter ORing Solutions* using the TPS23753 (SLVA306), apply to the TPS2378 incorporating a DC/DC converter.

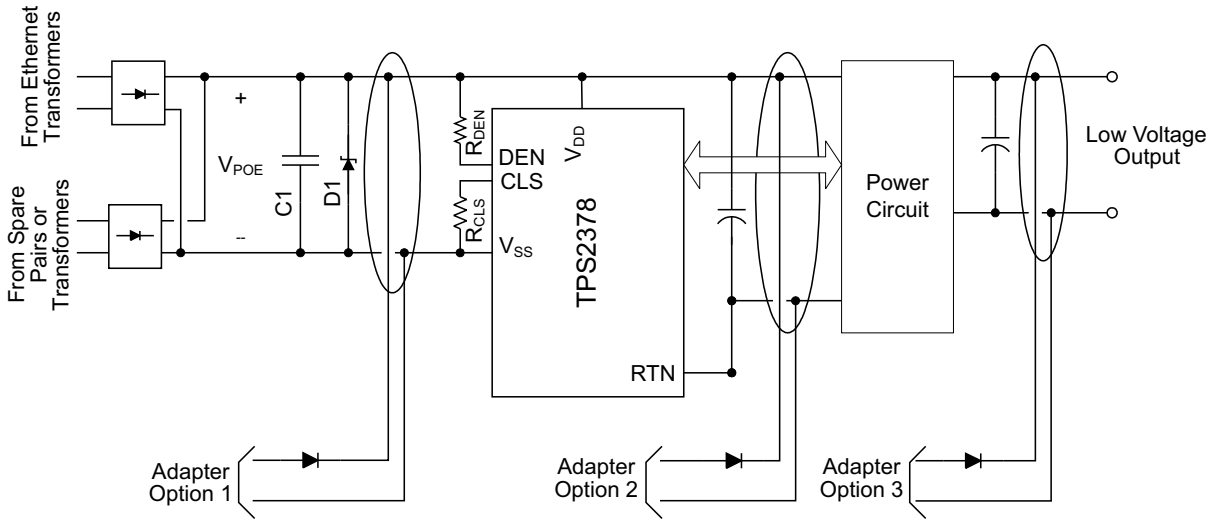


Figure 23. Oring Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, or damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

7.4.12 Using DEN to Disable PoE

The DEN pin may be used to turn the PoE hotswap switch off by pulling it to V_{SS} while in the operational state, or to prevent detection when in the idle state. A low voltage on DEN forces the hotswap MOSFET off during normal operation. Additional information is available in the *Advanced Adapter ORing Solutions* using the TPS23753 (SLVA306) application report.

7.4.13 ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult, if not impossible, for many of the combinations. However, the TPS2378 offers several built-in features that simplify some combinations.

Several examples demonstrate the limitations inherent in ORing solutions. Diode ORing a 48-V adapter with PoE (option 1) presents the problem that either source may have the higher voltage. A blocking switch would be required to assure that one source dominates. A second example combines a 12-V adapter with PoE using option 2. The converter draws approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from PoE power to adapter may demand more current than can be supplied by the PSE. The converter must be turned off while the C_{BULK} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example involves the loss of the MPS when running from the adapter, causing the PSE to remove power from the PD. If AC power is then lost, the PD will stop operating until the PSE detects and powers the PD.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS2378 has the flexibility to be implemented in IEEE802.3at and Universal Power Over Ethernet (UPOE) PDs. Therefore, it can be used in a wide range applications such as video and VoIP telephones, multiband access points, security cameras, and pico-base stations.

8.2 Typical Application

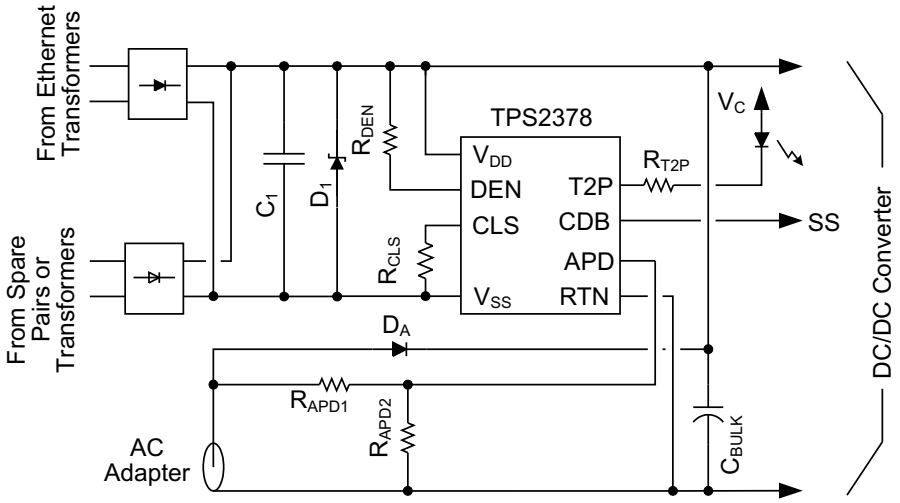


Figure 24. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters in Table 3.

Table 3. Design Parameters

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
POWER INTERFACE				
Input voltage	Applied to the power pins of connectors J1 or J3 (adapter)	0	57	V
Operating voltage	After start-up	30	57	V
Input UVLO	Rising input voltage at device terminals	—	40	V
	Falling input voltage	30.5	—	
Detection voltage	At device terminals	1.4	10.1	V
Classification voltage	At device terminals	11.9	23	V
Classification current	Class 4	38	42	mA
Inrush current limit		100	180	mA
Operating curent-limit		850	1200	mA

8.2.2 Detailed Design Requirements

8.2.2.1 Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges will reduce the power dissipation in these devices by about 30%. There are, however, some things to consider when using them. The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100-kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. To compensate, use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges.

Schottky diode leakage currents and lower dynamic resistances can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DEN} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients than PN junction diodes. After exposure to ESD, Schottky diodes may become shorted or leak. Take care to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

As a general recommendation, use 1 A or 2 A, 100 V rated discrete or bridge diodes for the input rectifiers.

8.2.2.2 Protection, D_1

A TVS, D_1, across the rectified PoE voltage per Figure 24 must be used. TI recommends a SMAJ58A, or equivalent, is recommended for general indoor applications. If an adapter is connected from V_{DD} to RTN, as in ORing option 2 above, then voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

8.2.2.3 Capacitor, C_1

The IEEE 802.3at standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 μF to 0.12 μF. Typically a 0.1 μF, 100 V, 10% ceramic capacitor is used.

8.2.2.4 Detection Resistor, R_{DEN}

The IEEE 802.3at standard specifies a detection signature resistance, R_{DEN} between 23.7 kΩ and 26.3 kΩ, or 25 kΩ ± 5%. A resistor of 24.9 kΩ ± 1% is recommended for R_{DEN}.

8.2.2.5 Classification Resistor, R_{CLS}

Connect a resistor from CLS to V_{SS} to program the classification current according to the IEEE 802.3at standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to Table 1.

Choose class 4 and R_{CLS} = 63.4 Ω.

8.2.2.6 APD Pin Divider Network RAPD1, RAPD2

For an adapter voltage threshold to switch from PoE to adapter at 37 V, choose 10 kΩ for RAPD2.

$$\frac{V_{Adapter}\ R_{APD2}}{R_{APD1} + R_{APD2}} = 1.5\ V \tag{3}$$

$$\frac{37\ V \times 10\ k}{10\ k + R_{APD1}} = 1.5\ V \tag{4}$$

Solving for RAPD1:

$$RAPD1 = 237\ k\Omega \tag{5}$$

8.2.3 Application Curves

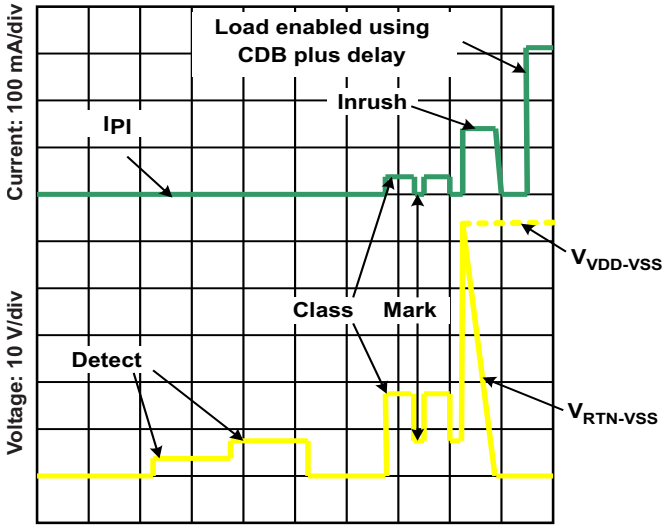


Figure 25. Start-up

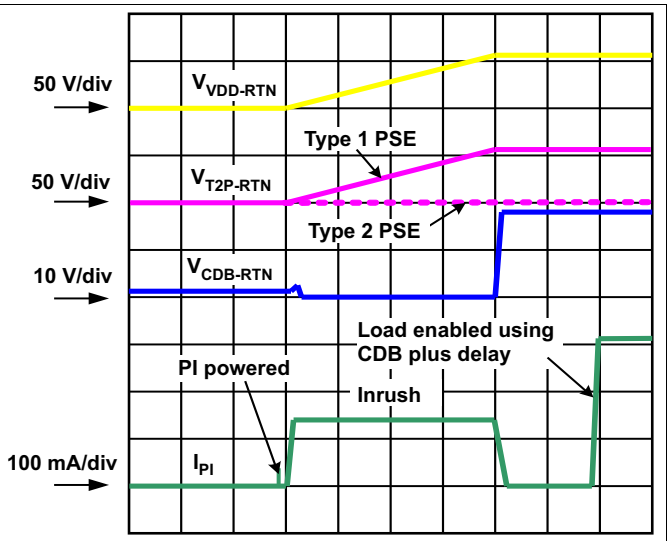


Figure 26. Power Up and Start

9 Power Supply Recommendations

The TPS2378 device will typically be followed by a power supply such as an isolated flyback or active clamp forward converter or a non-isolated buck converter. The input voltage of the converter should be capable of operating within the IEEE802.3at recommended input voltage as shown in Table 2.

10 Layout

10.1 Layout Guidelines

The layout of the PoE front end should follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1-μF capacitor, and TPS2378.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS2378 should be located over split, local ground planes referenced to VSS for the PoE input and to RTN for the switched output.
- Large copper fills and traces should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.

10.2 Layout Example

Figure 27 and Figure 28 show the top and bottom layer and assemblies of the TPS2378EVM-105 as a reference for optimum parts placement. A detailed PCB layout can be found in the user's guide of the TPS2378EVM-105 (SLVU682).

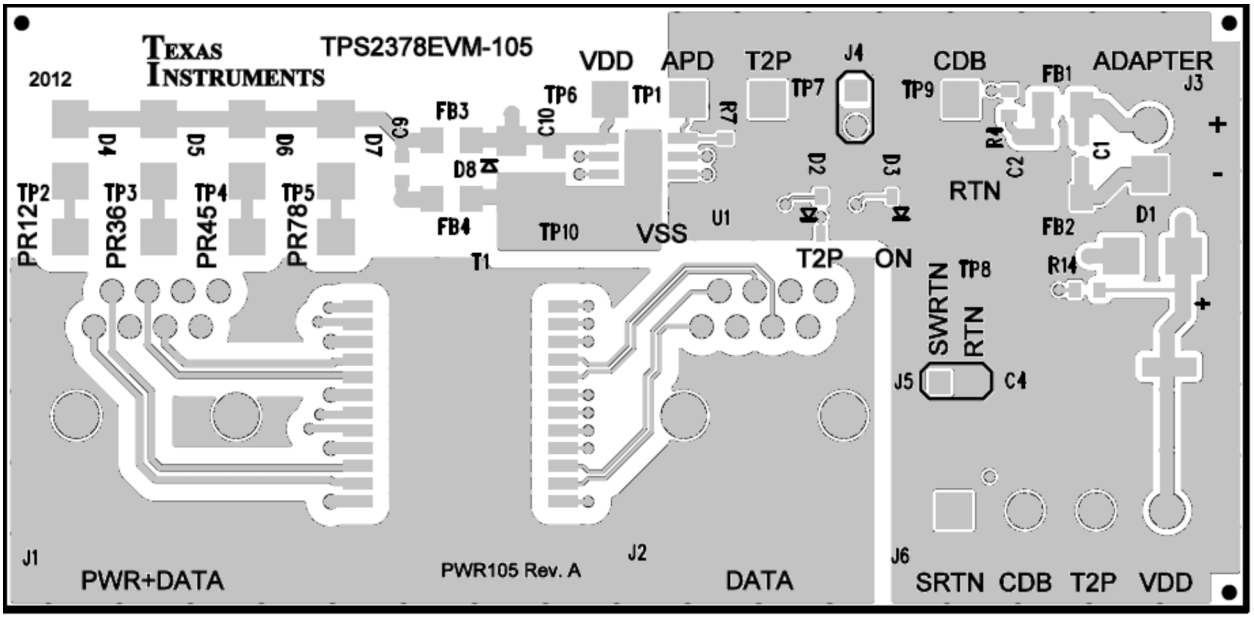


Figure 27. Top Side

Layout Example (continued)

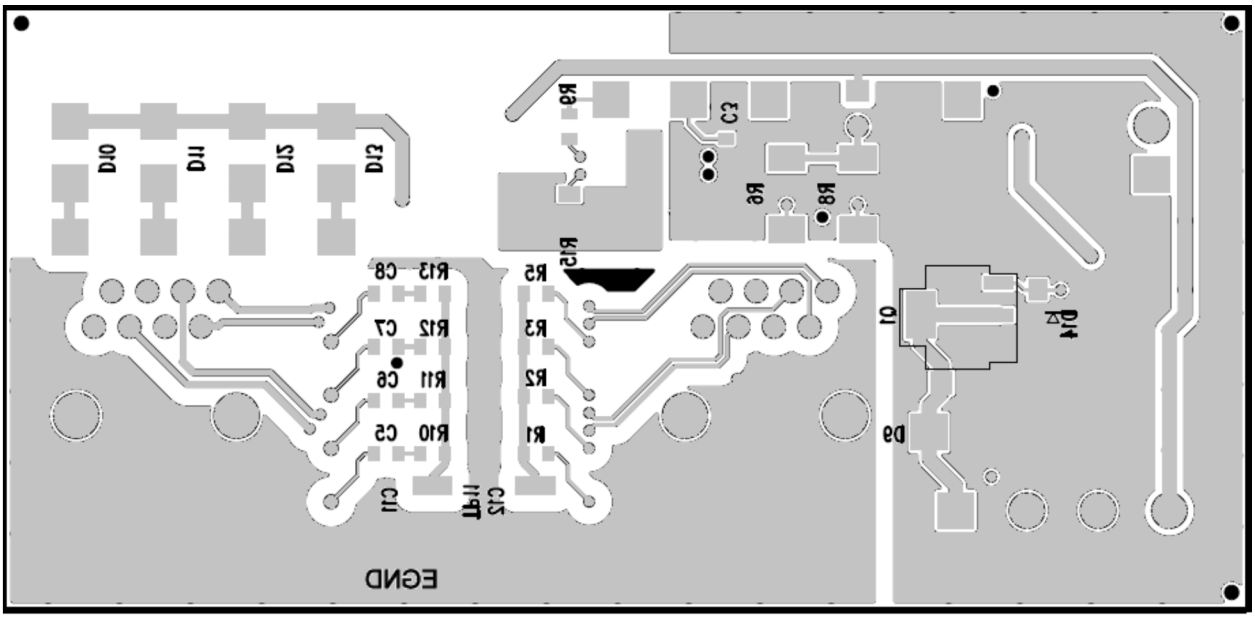


Figure 28. Bottom Side

10.3 EMI Containment

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives).
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods).
- Use 4 layer PCB if economically feasible (for better grounding).
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup).
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane.
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground).
- Use of ferrite beads on input (allow for possible use of beads or 0 ohm resistors).
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line).
- Possible use of common-mode inductors.
- Possible use of integrated RJ-45 jacks (shielded with internal transformer and Bob Smith terminations).
- End-product enclosure considerations (shielding).

10.4 Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS2378 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS2378 device to experience an OTSD event if it is excessively heated by a nearby device.

10.5 ESD

ESD requirements for a unit that incorporates the TPS2378 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS2378.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- *《采用 TPS23753 的高级适配器 ORing 解决方案》*，SLVA306

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2378DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	2378	Samples
TPS2378DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	2378	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

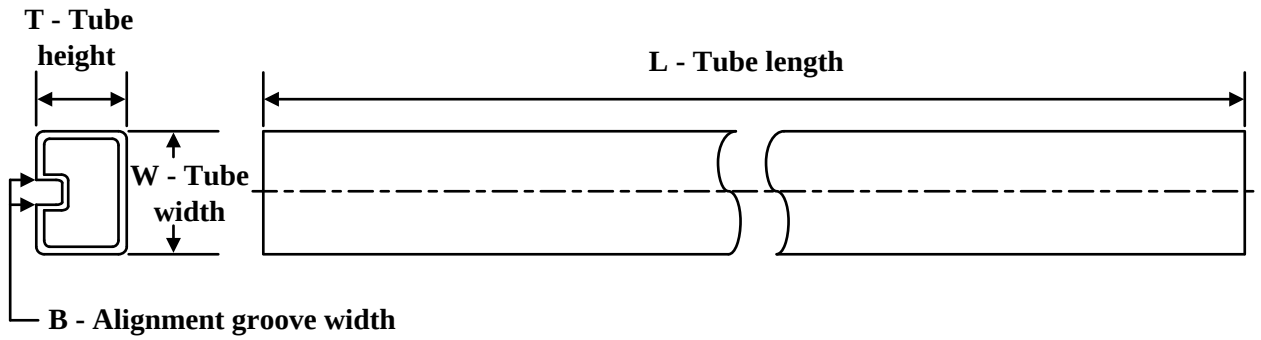
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE

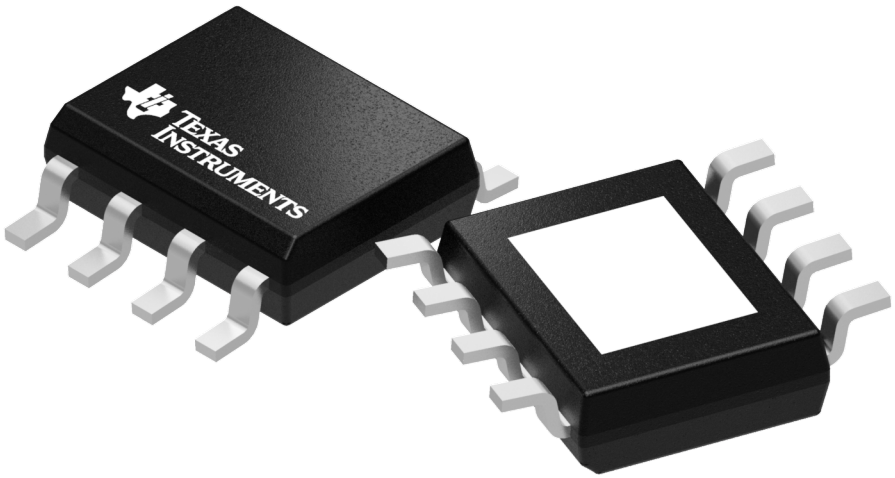


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2378DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS2378DDA	DDA	HSOIC	8	75	507	8	3940	4.32

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



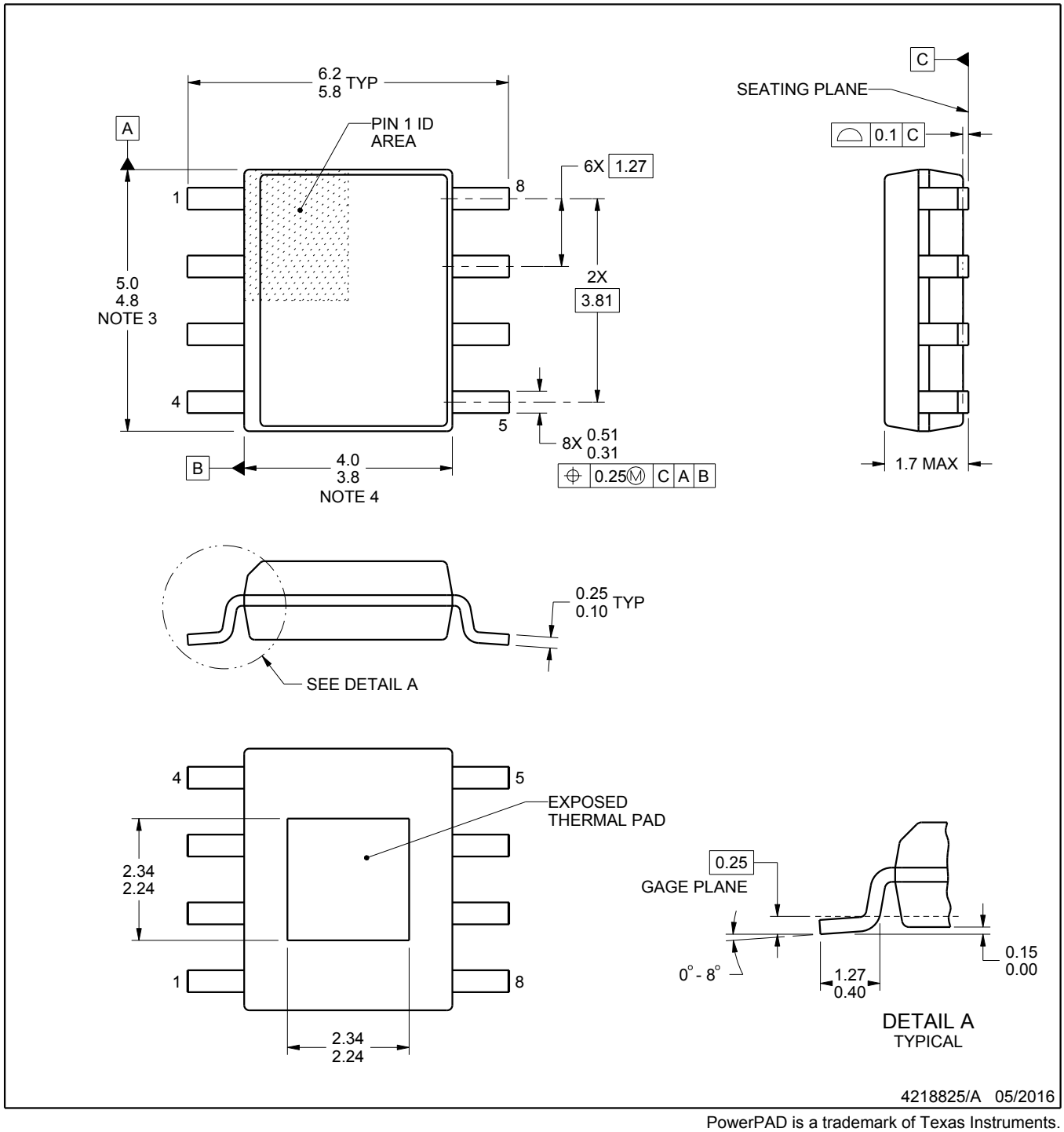
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



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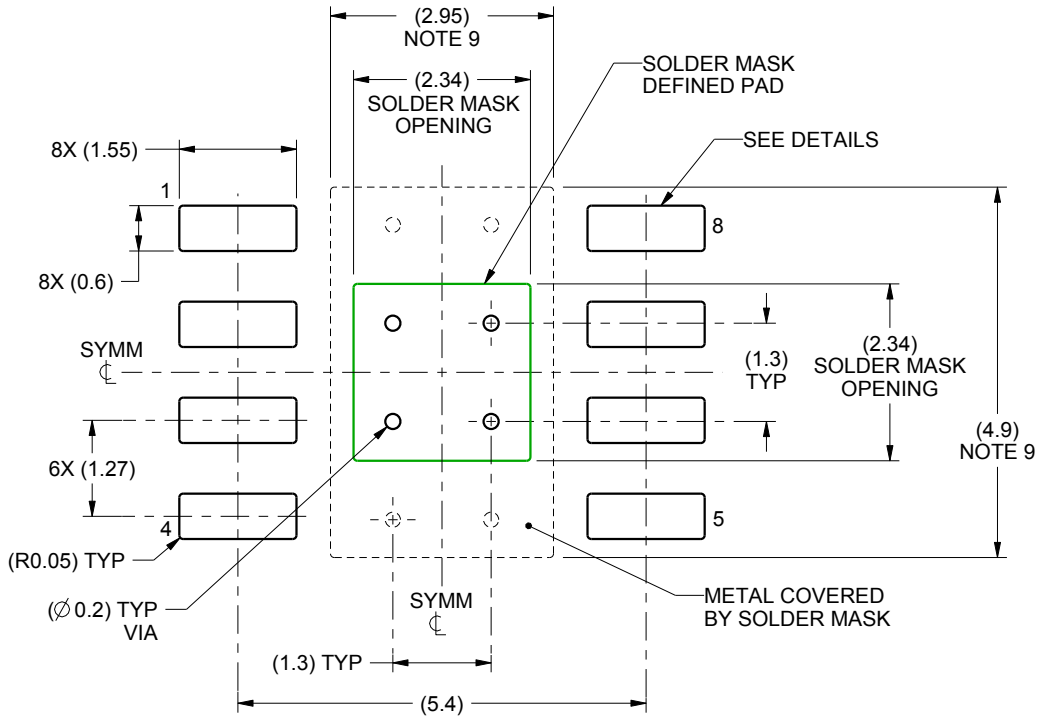
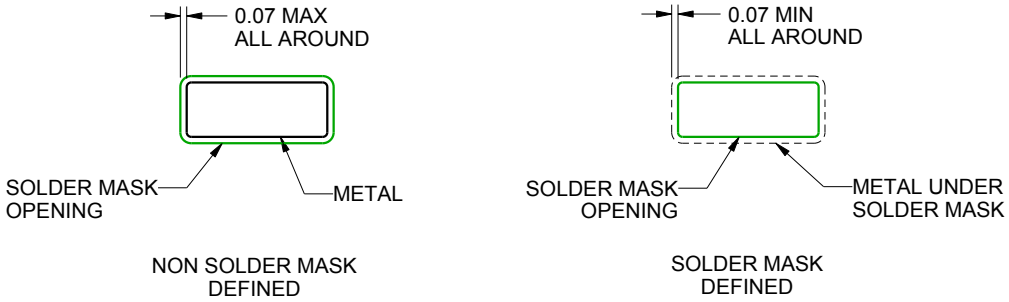
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

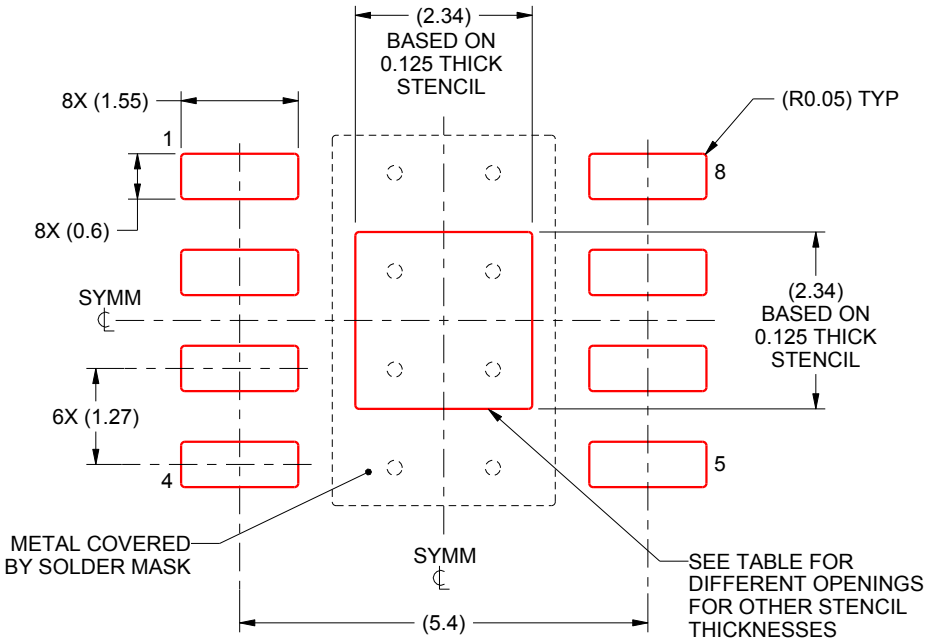


SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

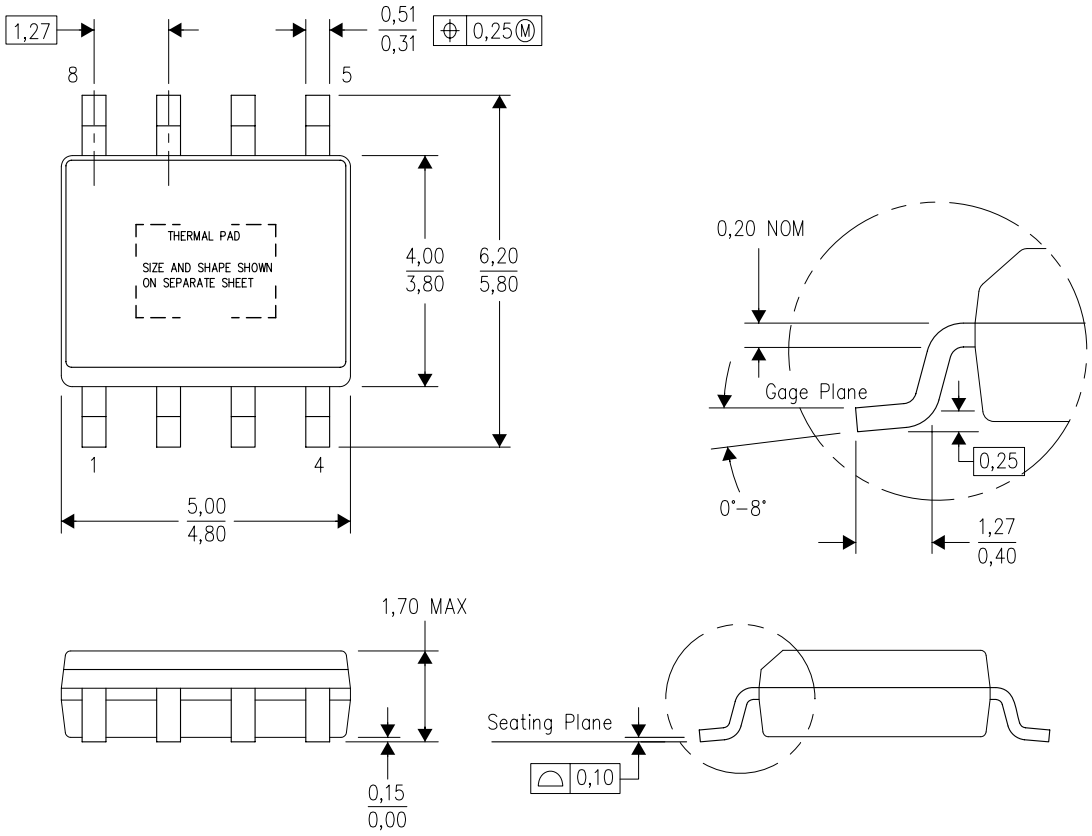
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

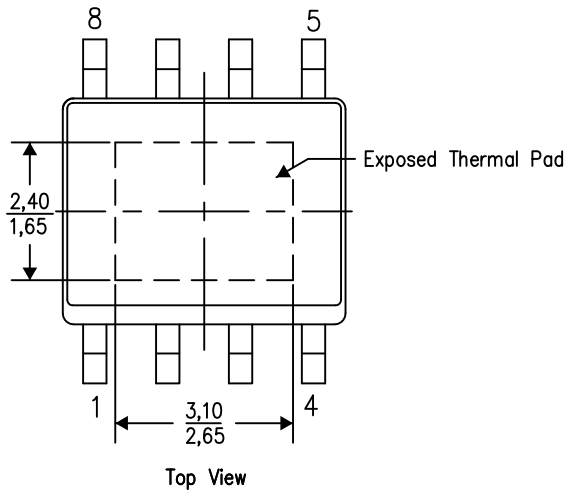
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

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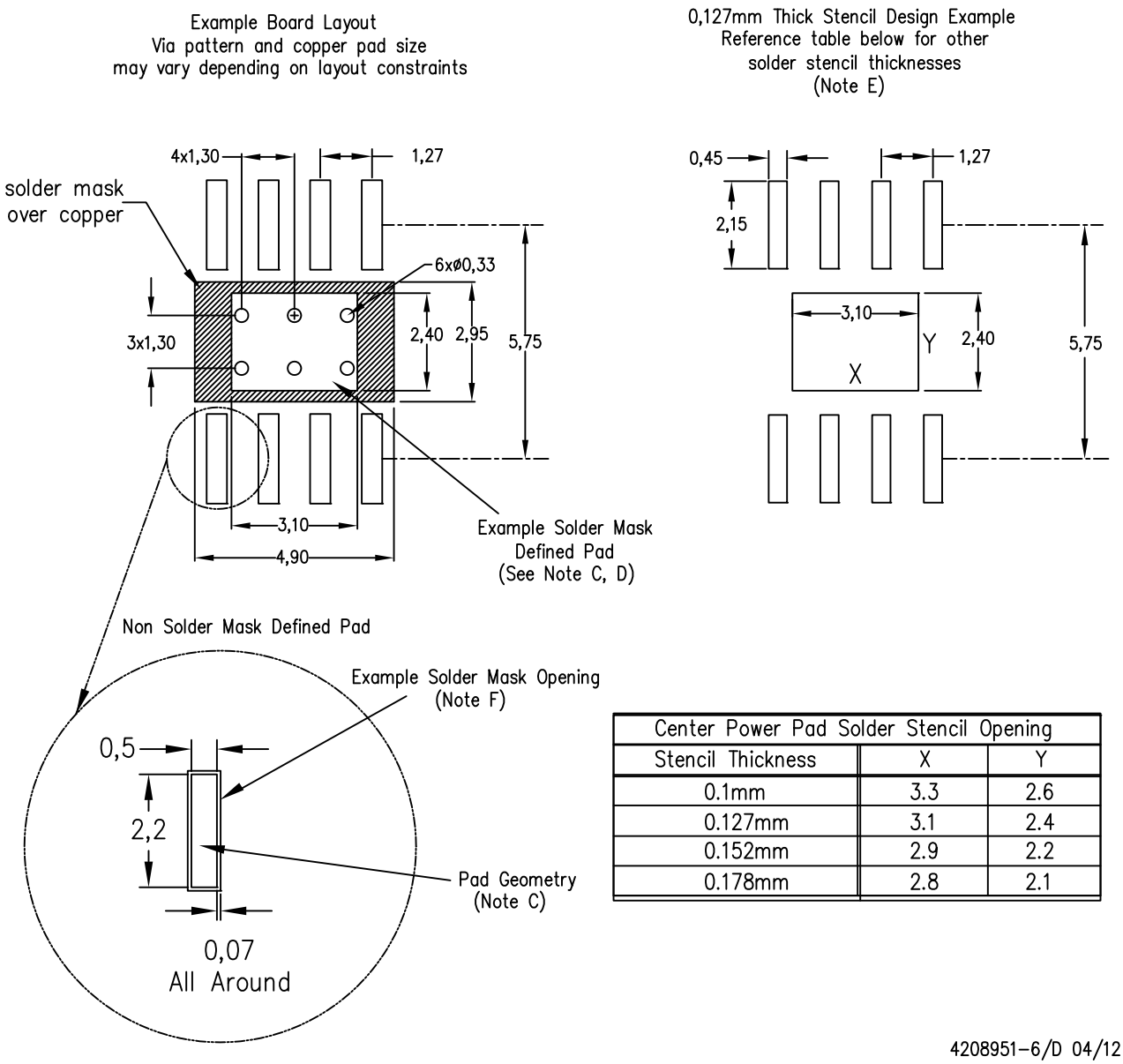
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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