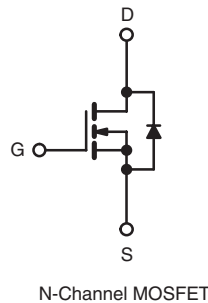
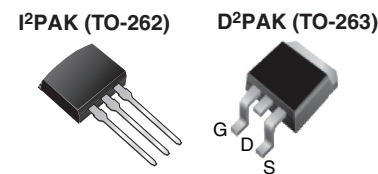


## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V	1.2
$Q_g$ (Max.) (nC)	60	
$Q_{gs}$ (nC)	8.3	
$Q_{gd}$ (nC)	30	
Configuration	Single	

### FEATURES

- Surface Mount (IRFBC40S/SiHFBC40S)
- Low-Profile Through-Hole (IRFBC40L, SiHFBC40L)
- Available in Tape and Reel (IRFBC20S, SiHFBC20S)
- Dynamic  $dV/dt$  Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead (Pb)-free Available



### DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D<sup>2</sup>PAK is a surface mount power package capable of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application. The through-hole version (IRFBC40L/SiHFBC40L) is available for low-profile applications.

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free	IRFBC40SPbF SiHFBC40S-E3	IRFBC40STRLPbF <sup>a</sup> SiHFBC40STL-E3 <sup>a</sup>	IRFBC40LPbF SiHFBC40L-E3
SnPb	IRFBC40S SiHFBC40S	IRFBC40STRL <sup>a</sup> SiHFBC40STL <sup>a</sup>	IRFBC40L SiHFBC40L

#### Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage <sup>e</sup>	$V_{DS}$	600	V
Gate-Source Voltage <sup>e</sup>	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25$ °C	6.2
		$T_C = 100$ °C	3.9
Pulsed Drain Current <sup>a,e</sup>		$I_{DM}$	25
Linear Derating Factor			1.0
Single Pulse Avalanche Energy <sup>b,e</sup>		$E_{AS}$	570
Repetitive Avalanche Current <sup>a</sup>		$I_{AR}$	6.2
Repetitive Avalanche Energy <sup>a</sup>		$E_{AR}$	13
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	130
	$T_A = 25$ °C		3.1
Peak Diode Recovery $dV/dt$ <sup>c,e</sup>		$dV/dt$	3.0

\* Pb containing terminations are not RoHS compliant, exemptions may apply

# IRFBC40S, IRFBC40L, SiHFBC40S, SiHFBC40L

Vishay Siliconix



ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted			
PARAMETER	SYMBOL	LIMIT	UNIT
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	

## Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ ; starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 27\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 6.2\text{ A}$  (see fig. 12).
- $I_{SD} \leq 6.2\text{ A}$ ,  $di/dt \leq 80\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.
- Uses IRFBC40/SiHFBC40 data and test conditions.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, steady-state) <sup>a</sup>	$R_{thJA}$	-	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{thJC}$	-	1.0	

## Note

- When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.70	-	$\text{V}/^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$   $I_D = 3.7\text{ A}^b$	-	-	1.2	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 100\text{ V}$ , $I_D = 3.7\text{ A}^b$	4.7	-	-	S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5 <sup>c</sup>	-	1300	-	pF
Output Capacitance	$C_{oss}$		-	160	-	
Reverse Transfer Capacitance	$C_{riss}$		-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$   $I_D = 6.2\text{ A}$ , $V_{DS} = 3600\text{ V}$ , see fig. 6 and 13 <sup>b, c</sup>	-	-	60	nC
Gate-Source Charge	$Q_{gs}$		-	-	8.3	
Gate-Drain Charge	$Q_{gd}$		-	-	30	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$ , $I_D = 6.2\text{ A}$ , $R_G = 9.1\text{ }\Omega$ , $R_D = 47\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b, c</sup>	-	13	-	ns
Rise Time	$t_r$		-	18	-	
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	
Fall Time	$t_f$		-	20	-	
Internal Source Inductance	$L_S$	Between lead, and center of die contact	-	7.5	-	nH

SPECIFICATIONS $T_J = 25^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6.2	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$		-	-	25	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}$ , $I_S = 6.2\text{ A}$ , $V_{GS} = 0\text{ V}^b$	-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25^\circ\text{C}$ , $I_F = 6.2\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}^b$	-	450	940	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	3.8	7.9	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )				

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c. Uses IRFBC40/SiHFBC40 data and test conditions.

**TYPICAL CHARACTERISTICS**  $25^\circ\text{C}$ , unless otherwise noted

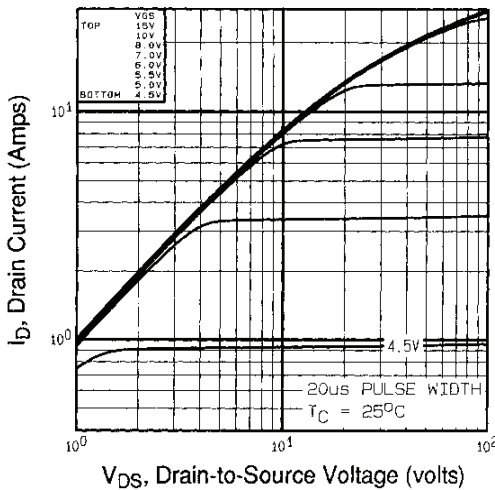


Fig. 1 - Typical Output Characteristics

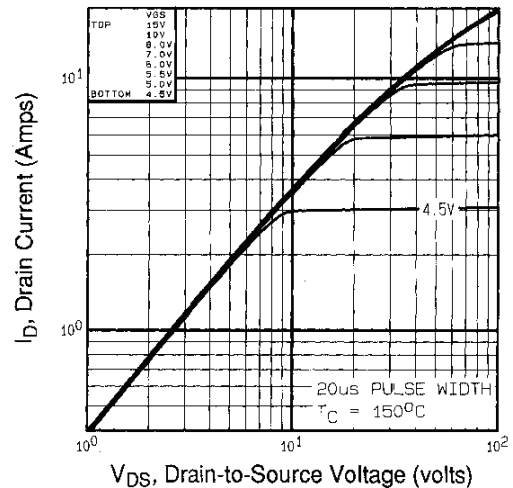


Fig. 2 - Typical Output Characteristics

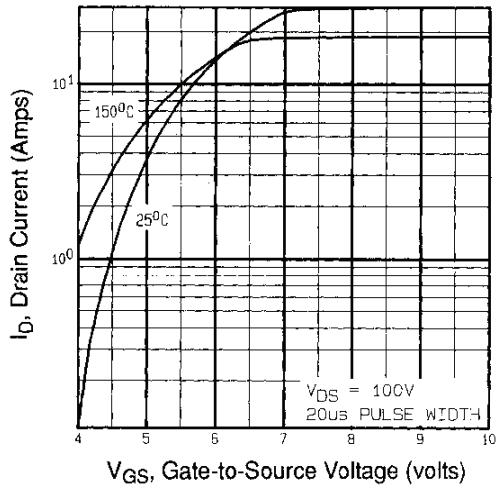


Fig. 3 - Typical Transfer Characteristics

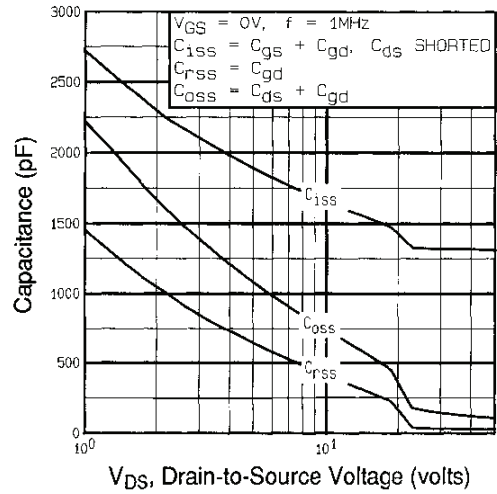


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

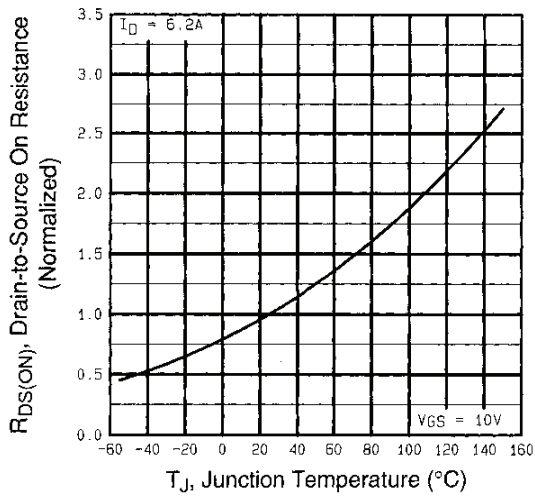


Fig. 4 - Normalized On-Resistance vs. Temperature

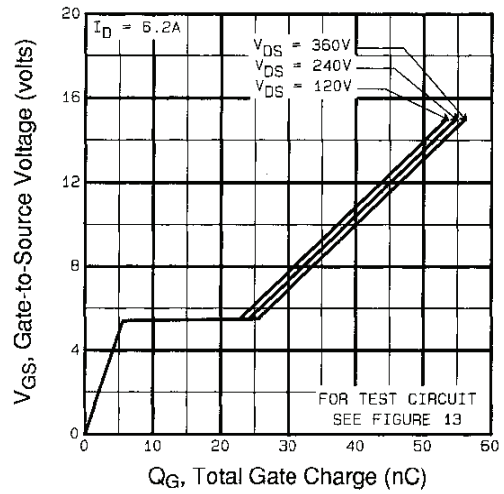


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

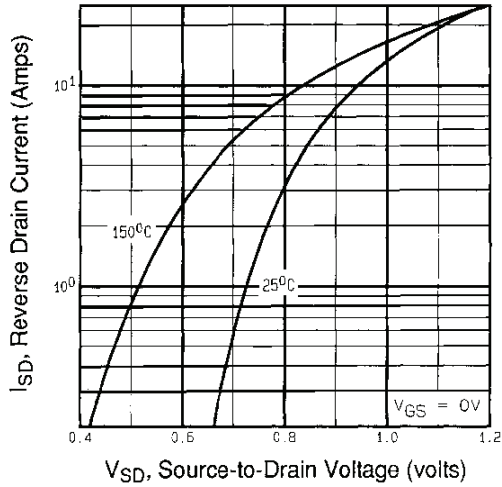


Fig. 7 - Typical Source-Drain Diode Forward Voltage

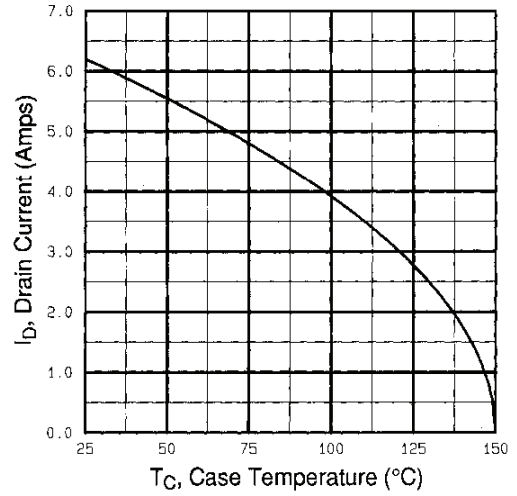


Fig. 9 - Maximum Drain Current vs. Case Temperature

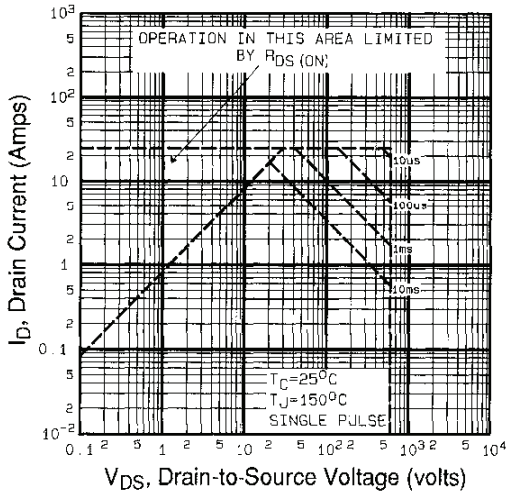


Fig. 8 - Maximum Safe Operating Area

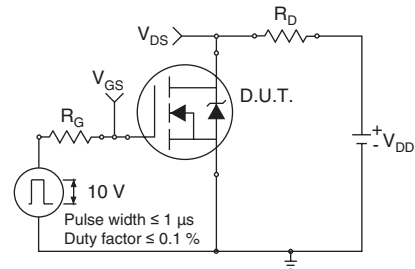


Fig. 10a - Switching Time Test Circuit

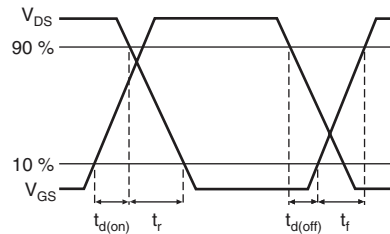


Fig. 10b - Switching Time Waveforms

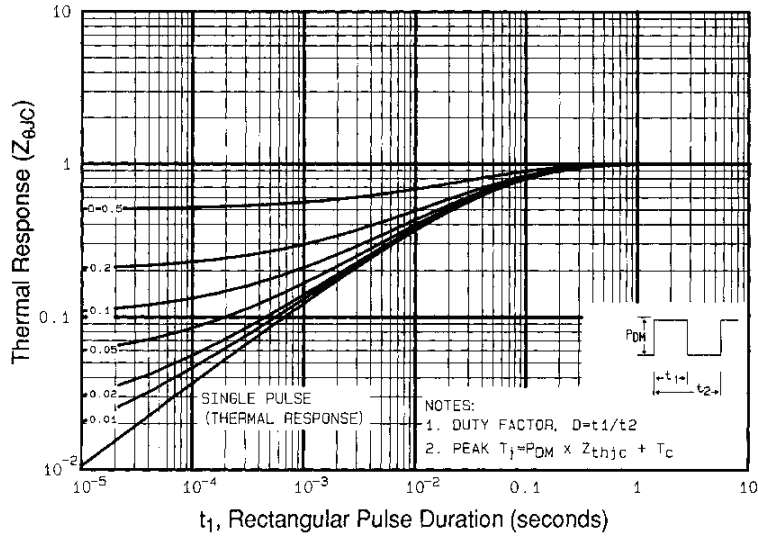


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

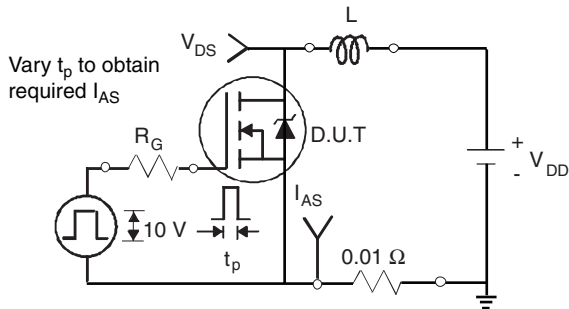


Fig. 12a - Unclamped Inductive Test Circuit

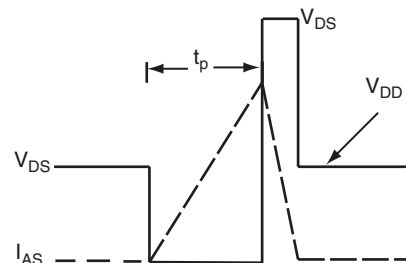


Fig. 12b - Unclamped Inductive Waveforms

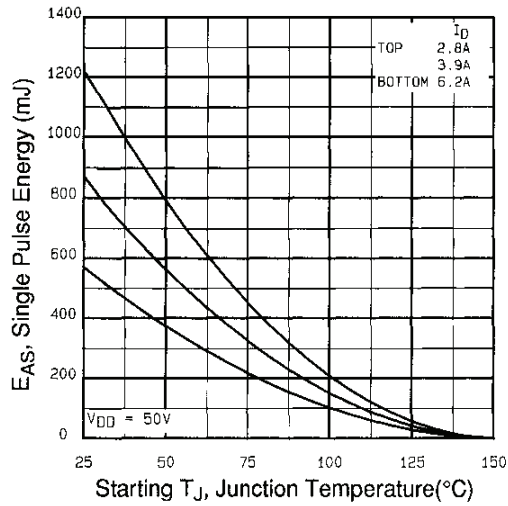


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

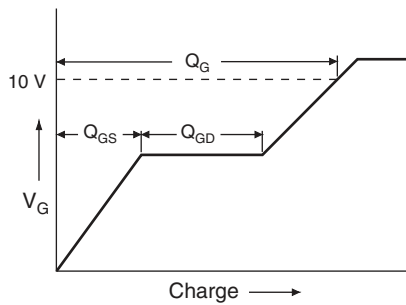


Fig. 13a - Basic Gate Charge Waveform

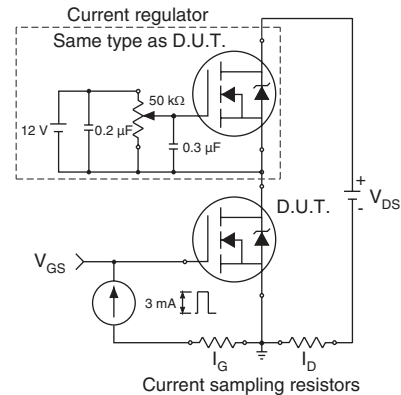
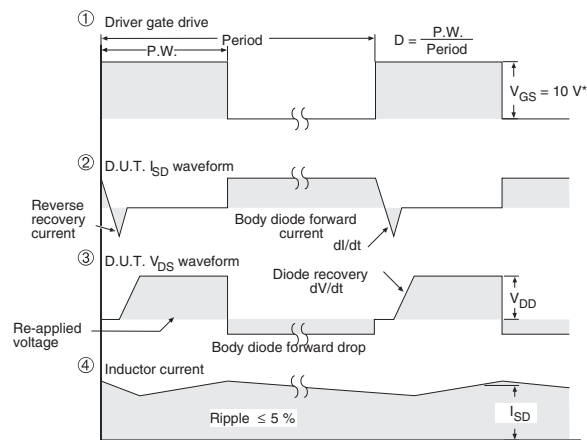
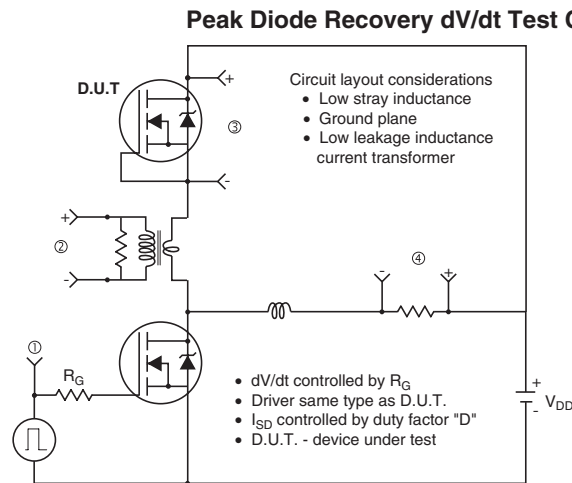


Fig. 13b - Gate Charge Test Circuit



\*  $V_{GS} = 5V$  for logic level devices

Fig. 14 - For N-Channel

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