

# STK57FU394A-E



ON Semiconductor®

www.onsemi.com

## Advanced Information PFC Converter + Inverter IPM for 3-phase Motor Drive

This IPM (Intelligent Power Module) includes the PFC, the output stage of a 3-phase inverter, pre-drive circuits, as well as protection circuits in one package.

### Features

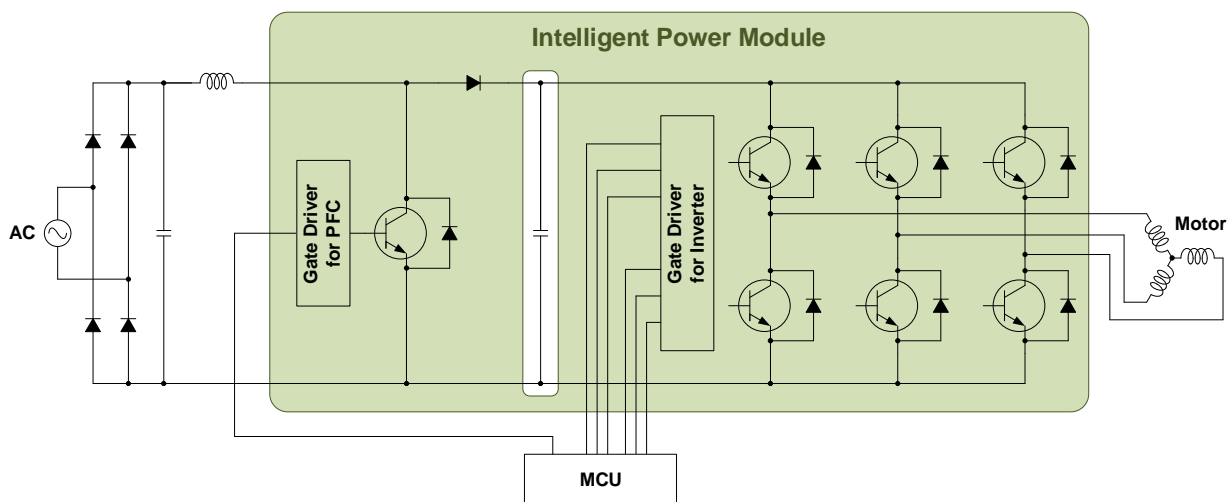
- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status outputs are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Under-voltage lockout for all channels
- Protective terminals including for over current protection each of Inverter section and PFC section are built in.
- Externally accessible embedded thermistor for substrate temperature measurement

### Certification

- UL1557 (File Number : E339285)

### Typical Applications

- Motor Control System
- Industrial/ General Control System
- HVAC



This document contains information on a new product. Specifications and information herein are subject to change without notice.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

# STK57FU394A-E

## BLOCK DIAGRAM

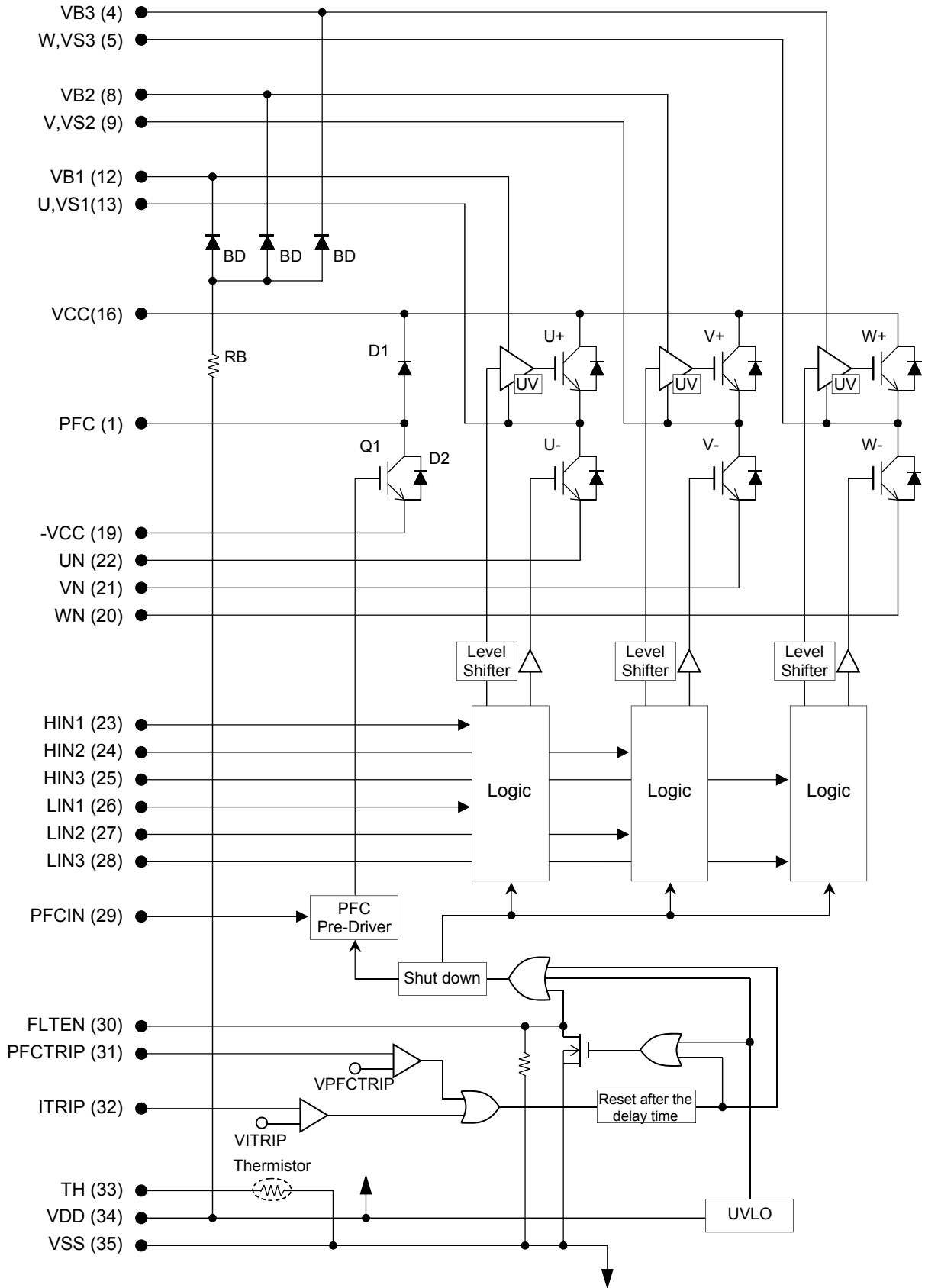


Figure 1. STK57FU394A-E Block diagram

# STK57FU394A-E

## APPLICATION CIRCUIT EXAMPLES

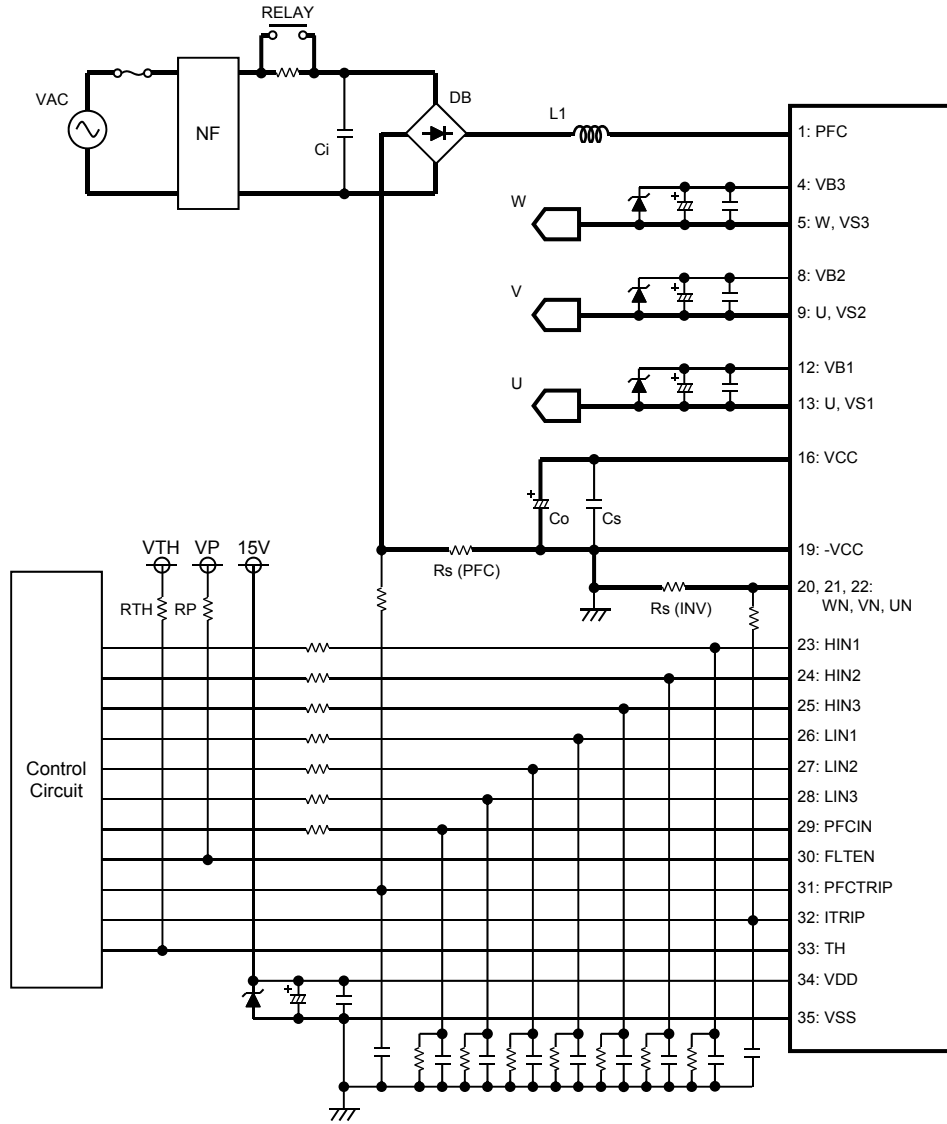


Figure 2. Motor drive application using STK57FU394A-E

## STK57FU394A-E

### PIN FUNCTION DISCRIPTION

Pin	Name	Description
1	PFC	Input the Rectified AC Voltage
2	-	Without pin
3	-	Without pin
4	VB3	High Side Floating Supply Voltage 3
5	W,VS3	Output 3 – High Side Floating Supply Offset Voltage
6	-	Without pin
7	-	Without pin
8	VB2	High Side Floating Supply Voltage 2
9	V,VS2	Output 2 – High Side Floating Supply Offset Voltage
10	-	Without pin
11	-	Without pin
12	VB1	High Side Floating Supply Voltage 1
13	U,VS1	Output 1 – High Side Floating Supply Offset Voltage
14	-	Without pin
15	-	Without pin
16	VCC	Positive PFC Output voltage / Positive Bus Input Voltage
17	-	Without pin
18	-	Without pin
19	-VCC	Negative PFC Output Voltage
20	WN	Low Side Emitter Connection – Phase W
21	VN	Low Side Emitter Connection – Phase V
22	UN	Low Side Emitter Connection – Phase U
23	HIN1	Logic Input High Side Gate Driver – Phase U
24	HIN2	Logic Input High Side Gate Driver – Phase V
25	HIN3	Logic Input High Side Gate Driver – Phase W
26	LIN1	Logic Input Low Side Gate Driver – Phase U
27	LIN2	Logic Input Low Side Gate Driver – Phase V
28	LIN3	Logic Input Low Side Gate Driver – Phase W
29	PFCIN	Logic Input PFC Gate Driver
30	FLTEN	Enable input / Fault output
31	PFCT RIP	Current protection pin for PFC
32	ITRIP	Current protection pin for Inverter
33	TH	Thermistor output
34	VDD	+15V Main Supply
35	VSS	Negative Main Supply

# STK57FU394A-E

## MAXIMUM RATINGS (Note 1)

### (1) PFC Section

Parameter		Symbol	Conditions	Ratings	Unit
IGBT (Q1)	Collector-emitter voltage	$V_{CE}$	PFC to $-V_{CC}$	600	V
	Repetitive peak collector current	ICP	P.W.=1ms	40	A
	Collector current	IC	$T_c=25^{\circ}C$	27	A
			$T_c=100^{\circ}C$	13	A
Power dissipation	PC		62	W	
FRD1 (D1)	Diode reverse voltage	VRM	PFC to $V_{CC}$	600	V
	Repetitive peak forward current	IFP1	P.W.=1ms	60	A
	Diode forward current	IF1		30	A
	Power dissipation	PD1		56	W
FRD2 (D2)	Repetitive peak forward current	IFP2	P.W.=1ms	11	A
	Diode forward current	IF2		5	A
	Power dissipation	PD2		10	W
Maximum AC input voltage		VAC	Single-phase Full-rectified	264	V
Maximum output voltage		$V_o$	Under the Application Circuit (VAC=200V)	450	V
Input AC current (steady state)		lin		15	Arms

### (2) Inverter Section

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	$V_{CC}$	$V_{CC}$ to UN, VN, WN surge < 500V (Note 2)	450	V
Collector-emitter voltage	$V_{CE}$	$V_{CC}$ to U, V, W or U, V, W to UM, VN, WN	600	V
Output current	Io	$V_{CC}$ , UN, VN, WN, U, V, W terminal current	$\pm 15$	A
		$V_{CC}$ , UN, VN, WN, U, V, W terminal current at $T_c=100^{\circ}C$	$\pm 8$	A
Output peak current	Iop	$V_{CC}$ , UN, VN, WN, U, V, W terminal current for a Pulse width of 1ms	$\pm 30$	A
Maximum loss	Pd	IGBT per channel	37	W

### (3) Control (Pre-driver) Section

Parameter	Symbol	Remarks	Ratings	Unit
Pre-driver supply voltage	VD1,2,3,4	VB1-VS1, VB2-VS2, VB3-VS3, $V_{DD}-V_{SS}$	-0.3 to 20	V
Input signal voltage	$V_{IN}$	HIN1, 2, 3, LIN1, 2, 3, PFCIN terminal	-0.3 to $V_{DD}$	V
FLTEN terminal voltage	VFLTEN	FLTEN terminal	-0.3 to $V_{DD}$	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	-0.3 to 10	V
PFCTRIP terminal voltage	VPFCTRIP	PFCTRIP terminal	-1.5 to 2.0	V

### (4) Total

Parameter	Symbol	Remarks	Ratings	Unit
Junction temperature	$T_j$	IGBT, FRD	150	$^{\circ}C$
Storage temperature	$T_{stg}$		-40 to +125	$^{\circ}C$
Operating Case temperature	$T_c$	IPM case temperature	-20 to +100	$^{\circ}C$
Tightening torque	MT	Case mounting screws (Note 3)	1.0	N-m
Withstand voltage	Vis	50Hz sine wave AC 1 minute (Note 4)	2000	VRM

- Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
- Surge voltage developed by the switching operation due to the wiring inductance between P and UN(VN, WN) terminal.
- Flatness of the heat-sink should be less than 0.15mm.
- Test conditions : AC2500V, 1s.

## STK57FU394A-E

### THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
PFC IGBT(Q1) Thermal Resistance, Junction-to-Case	$\theta_{j-c}(T)$	2.3	°C/W
PFC FRD(D1) Thermal Resistance, Junction-to-Case	$\theta_{j-c}(D)$	2.5	°C/W
Inverter Single IGBT Thermal Resistance, Junction-to-Case	$\theta_{j-c}(T)$	3.5	°C/W
Inverter Single FRD Thermal Resistance, Junction-to-Case	$\theta_{j-c}(D)$	6.0	°C/W

### RECOMMENDED OPERATING RANGES (Note 5)

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V <sub>CC</sub>	V <sub>CC</sub> to -V <sub>CC</sub> , UN, VN, WN	0	280	400	V
Pre-driver supply voltage	VD1,2,3	VB1 to U, VB2 to V, VB3 to W	12.5	15	17.5	V
	VD4	V <sub>DD</sub> to V <sub>SS</sub> (Note 6)	13.5	15	16.5	
ON-state input voltage	V <sub>IN(ON)</sub>	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3, PFCIN	2.5	-	5.0	V
OFF-state input voltage	V <sub>IN(OFF)</sub>		0	-	0.3	
PWM frequency(PFC part)	fP <sub>WMp</sub>		1	-	40	kHz
PWM frequency(Inverter part)	fP <sub>WMi</sub>		1	-	20	kHz
Dead time	DT	Upper/lower input signal downtime	1.5	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque	MT	'M3' type screw	0.6	-	0.9	N·m

5. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
6. Pre-driver power supply (VD4=15±1.5V) must be have the capacity of I<sub>o</sub>=20mA(DC), 0.5A(Peak).

# STK57FU394A-E

## ELECTRICAL CHARACTERICALS

Tc=25°C, VB1, VB2, VB3, VDD=15V unless otherwise noted. (Note 7, 8)

### (1) PFC Section

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Power output section							
Collector-emitter cut-off current	I <sub>CE</sub>	V <sub>CE</sub> =600V	Fig.1	-	-	0.1	mA
Reverse leakage current(FRD1)	I <sub>R</sub>	V <sub>R</sub> =600V		-	-	0.1	mA
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	I <sub>C</sub> =30A, T <sub>j</sub> =25°C	Fig.2	-	2.2	2.8	V
		I <sub>C</sub> =15A, T <sub>j</sub> =100°C		-	1.8	-	
Diode forward voltage(FRD1)	V <sub>F1</sub>	I <sub>F</sub> =30A, T <sub>j</sub> =25°C	Fig.3	-	1.8	2.4	V
		I <sub>F</sub> =15A, T <sub>j</sub> =100°C		-	1.3	-	
Diode forward voltage(FRD2)	V <sub>F2</sub>	I <sub>F</sub> =5A, T <sub>j</sub> =25°C		-	1.7	2.3	V
Switching characteristics							
Switching time	t <sub>ON</sub>	I <sub>o</sub> =30A, V <sub>CC</sub> =300V V <sub>D</sub> =15V, L=0.5mH, T <sub>c</sub> =25°C	Fig.6	0.1	0.4	0.9	μs
	t <sub>OFF</sub>			0.1	0.4	0.9	μs
Diode reverse recovery time	t <sub>rr</sub>	I <sub>o</sub> =15A, V <sub>CC</sub> =300V V <sub>D</sub> =15V, T <sub>c</sub> =100°C		-	80	-	ns

### (2) Inverter Section

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Power output section							
Collector-emitter cut-off current	I <sub>CE</sub>	V <sub>CE</sub> =600V	Fig.1	-	-	0.1	mA
Bootstrap diode reverse current	I <sub>R(BD)</sub>	V <sub>R(BD)</sub> =600V		-	-	0.1	mA
Collector-emitter saturation voltage	V <sub>CE(sat)</sub>	I <sub>C</sub> =15A, T <sub>j</sub> =25°C	Fig.2	-	2.0	2.6	V
		I <sub>C</sub> =8A, T <sub>j</sub> =100°C		-	1.7	-	
Diode forward voltage	V <sub>F</sub>	I <sub>F</sub> =15A, T <sub>j</sub> =25°C	Fig.3	-	2.1	2.7	V
		I <sub>F</sub> =8A, T <sub>j</sub> =100°C		-	1.7	-	
Switching characteristics							
Switching time	t <sub>ON</sub>	I <sub>o</sub> =15A Inductive load	Fig.6	0.1	0.5	1.0	μs
	t <sub>OFF</sub>			0.2	0.7	1.2	μs
Reverse bias safe operating area	RBSOA	I <sub>o</sub> =30A, V <sub>CE</sub> =450V		Full square			
Short circuit safe operating area	SCSOA	V <sub>CE</sub> =400V		4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U, V, W to UN, VN, WN		-50	-	50	V/ns

## STK57FU394A-E

### (3) Control (Pre-driver) Section

Parameter	Symbol	Conditions	Test circuit	min	typ	max	Unit
Pre-driver current consumption	ID	VD1, 2, 3=15V	Fig.4	-	0.08	0.4	mA
		VD4=15V		-	0.85	2.4	
High level input voltage	V <sub>INH</sub>	HIN1, 2, 3, LIN1, 2, 3, PFCIN to VSS	-	2.5	-	-	V
Low level input voltage	V <sub>INL</sub>		-	-	-	0.8	V
Logic1 input leakage current	I <sub>IN+</sub>	V <sub>IN</sub> =+3.3V	-	-	100	143	μA
Logic0 input leakage current	I <sub>IN-</sub>	V <sub>IN</sub> =0V	-	-	-	2	μA
FLTEN terminal input electric current	I <sub>oSD</sub>	FAULT:ON / VFLTEN=0.1V	-	-	2	-	mA
FAULT clearance delay time	FLTCLR	Fault output latch time	-	1	2	3	ms
FLTEN threshold	V <sub>EN+</sub>	VEN rising	-	-	-	2.5	V
	V <sub>EN-</sub>	VEN falling	-	0.8	-	-	V
ITRIP threshold voltage	V <sub>ITRIP</sub>	ITRIP to V <sub>SS</sub>	Fig.5	0.44	-	0.54	V
PFCTRIP threshold voltage	V <sub>PFCTRIP</sub>	PFCTRIP to V <sub>SS</sub>		-0.37	-	-0.25	V
ITRIP to shutdown propagation delay	t <sub>ITRIP</sub>			490	600	850	ns
PFCTRIP to shutdown propagation delay	t <sub>PFCTRIP</sub>			440	550	800	ns
ITRIP and PFCTRIP blanking time	t <sub>ITRIPBL</sub> t <sub>PFCTRIPBL</sub>			250	350	-	ns
VDD and VBS supply undervoltage protection reset	V <sub>DDUV+</sub> V <sub>BSUV+</sub>		-	10.5	11.1	11.7	V
VDD and VBS supply undervoltage protection set	V <sub>DDUV-</sub> V <sub>BSUV-</sub>		-	10.3	10.9	11.5	V
VDD and VBS supply undervoltage hysteresis	V <sub>CCUVH</sub> V <sub>BSUVH</sub>		-	0.14	0.2	-	V

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
8. Reference voltage is "VSS" terminal voltage unless otherwise specified.

#### Notes

1. The pre-drive power supply low voltage protection has approximately 200mV of hysteresis and operates as follows.
  - Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.
  - Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
2. When assembling the IPM on the heat sink the tightening torque range is 0.6Nm to 0.9Nm.
3. The pre-drive low voltage protection protects the device when the pre-drive supply voltage falls due to an operating malfunction.
4. When use the over-current protection with external shunt resistor, please set the current protection level to be equal to or less than the rating of output peak current.



# STK57FU394A-E

## The characteristic of Thermistor

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	$R_{25}$	$T_c=25^{\circ}\text{C}$	99	100	101	k $\Omega$
Resistance	$R_{100}$	$T_c=100^{\circ}\text{C}$	5.18	5.38	5.60	k $\Omega$
B-Constant(25-50°C)	B		4208	4250	4293	K
Temperature Range			-40		+125	$^{\circ}\text{C}$

■ This data shows the example of the application circuit, does not guarantee a design as the mass production set.

## TYPICAL CHARACTERISTICS

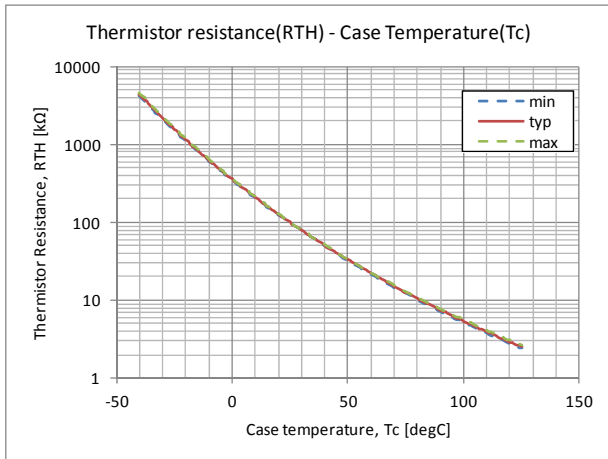


Figure 3. Thermistor resistance – Case temperature

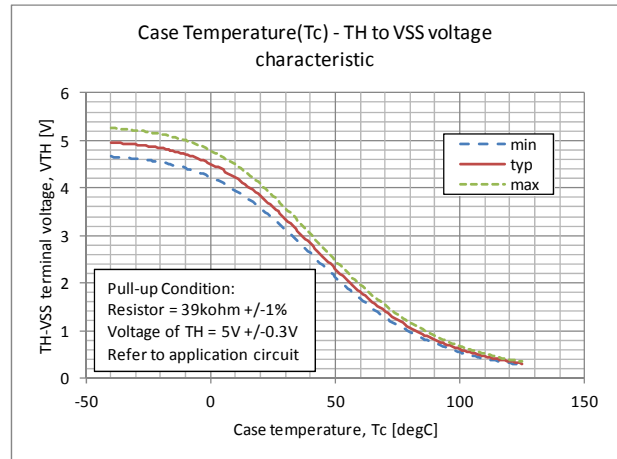


Figure 4. Thermistor voltage – Case temperature(Reference)

# STK57FU394A-E

## Timing Chart

### ■ UVLO(under Voltage Lockout) protection

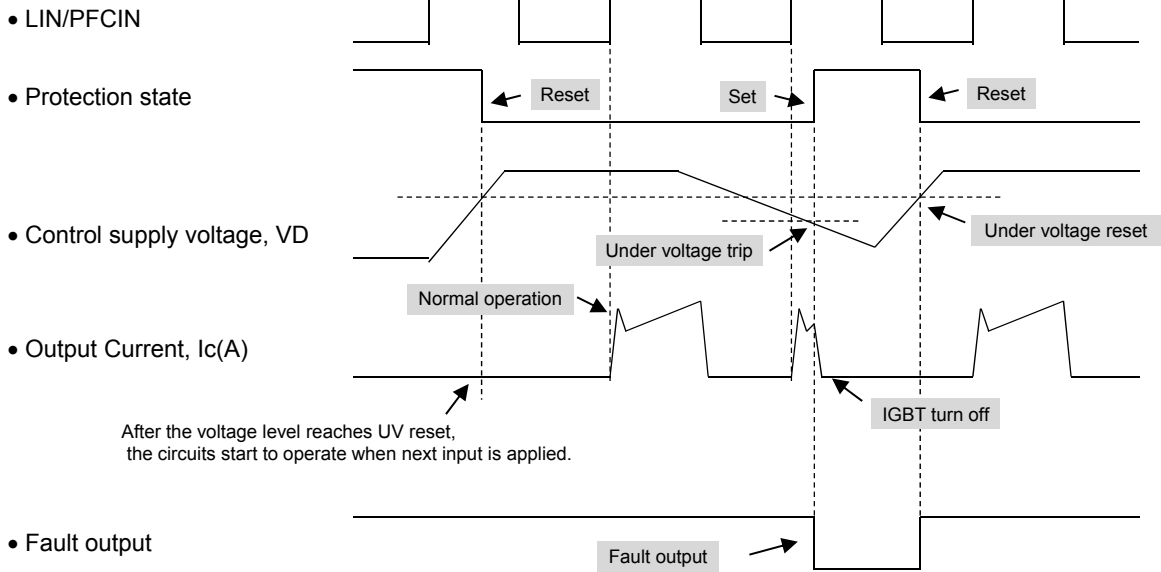


Figure 5. UVLO timing diagram

- \*1 : When  $V_{DD}$  decreases all gate output signals will go low and cut off all 6 IGBT outputs. When  $V_{DD}$  rises the operation will resume immediately.
- \*2 : When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.

### ■ Over current protection (ITRIP/PFCTRIP)

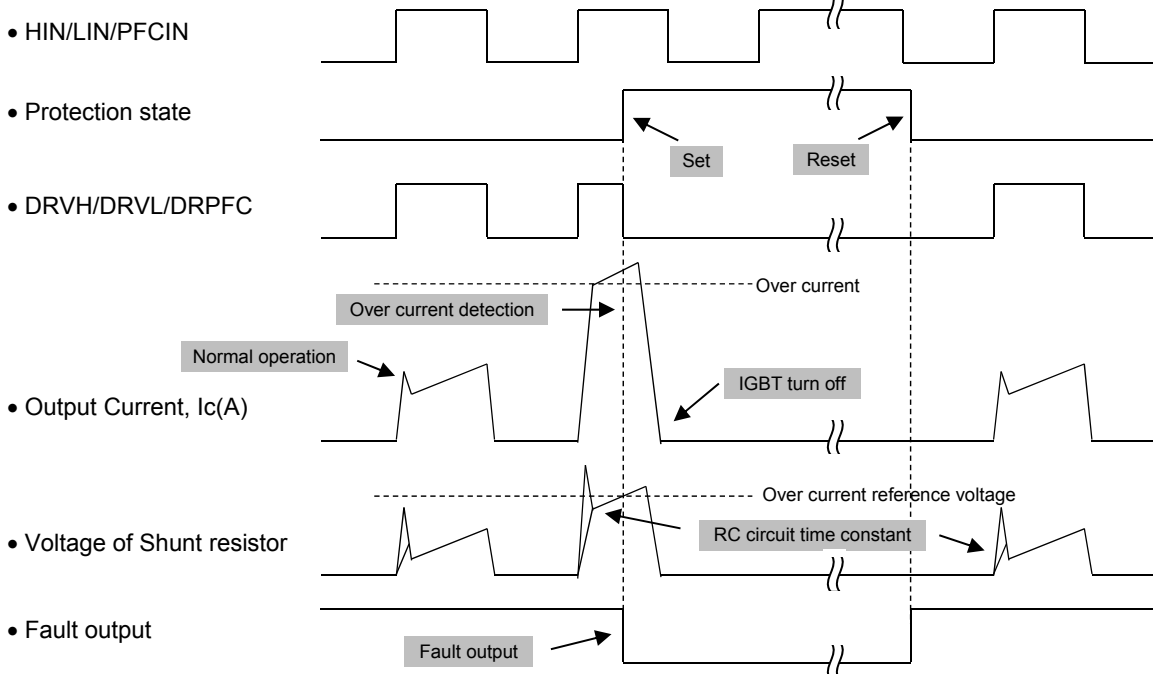


Figure 6. OCP timing diagram

- \*1 : When  $V_{ITRIP}$  exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

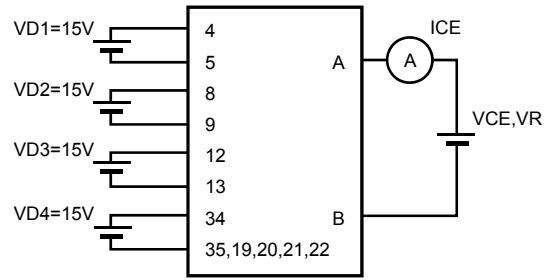
# STK57FU394A-E

## Test Circuit

### ■ ICES, IR(BD)

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19

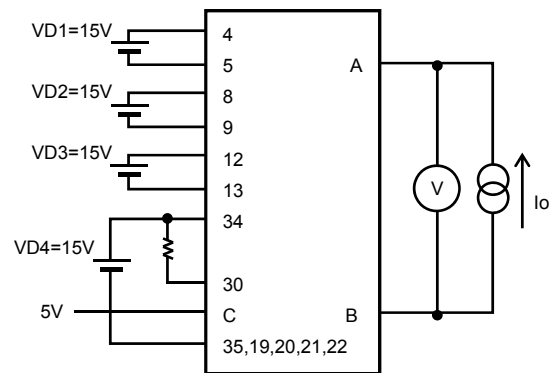
	U(BD)	V(BD)	W(BD)	D1
A	12	8	4	16
B	35	35	35	1



<Fig.1>

### ■ V<sub>CE(sat)</sub> (Test by pulse)

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19
C	23	24	25	26	27	28	29

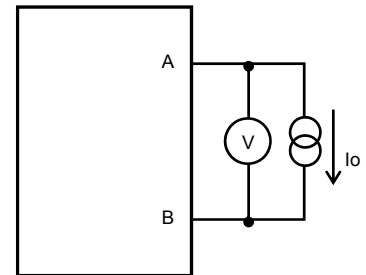


<Fig.2>

### ■ V<sub>F</sub> (Test by pulse)

	U+	V+	W+	U-	V-	W-
A	16	16	16	13	9	5
B	13	9	5	22	21	20

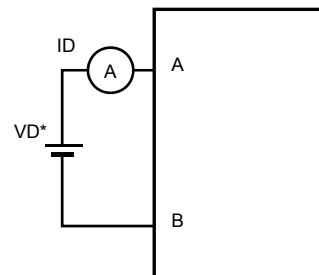
	U(BD)	V(BD)	W(BD)	D1	D2
A	12	8	4	16	1
B	34	34	34	1	19



<Fig.3>

### ■ I<sub>D</sub>

	VD1	VD2	VD3	VD4
A	12	8	4	34
B	13	9	5	35

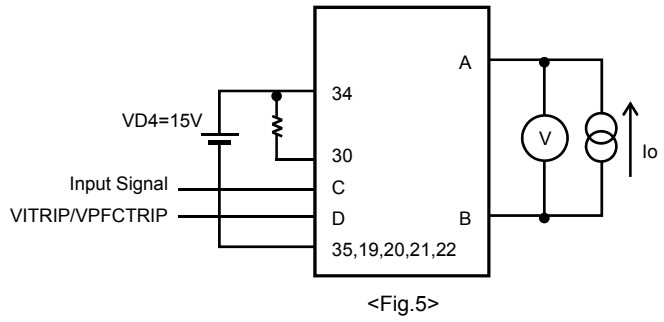
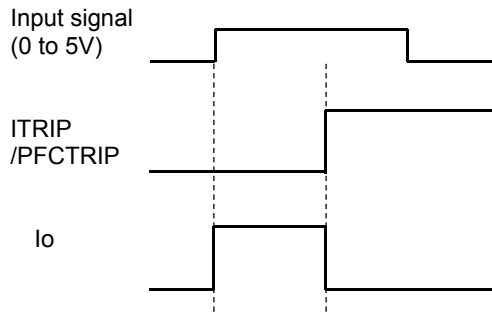


<Fig.4>

# STK57FU394A-E

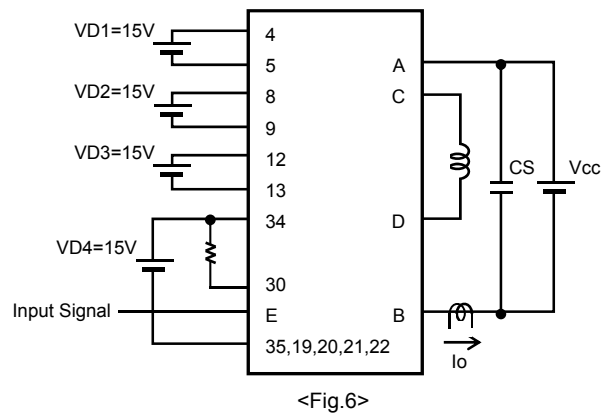
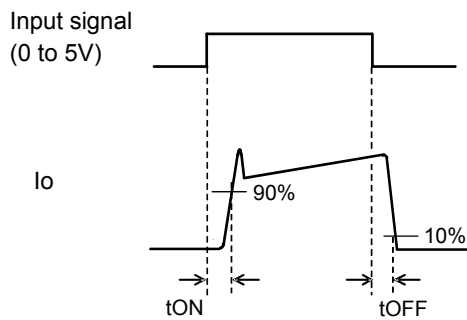
## ■ VITRIP, VPFCTRIP

	VITRIP(U-)	VPFCTRIP
A	13	1
B	22	19
C	26	29
D	32	31



## ■ Switching time

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	16	16	16	16
B	22	21	20	22	21	20	19
C	13	9	5	13	9	5	1
D	22	21	20	16	16	16	16
E	23	24	25	26	27	28	29



# STK57FU394A-E

## Usage Precaution

1. This IPM includes internal bootstrap circuit. By adding a bootstrap capacitor "CB", a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 $\mu$ F, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each high side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of "CS" is in the range of 0.1 to 10 $\mu$ F.
3. The "FLTEN" terminal is open Drain (It is operating as "FLTEN" when becoming Low). This terminal serves as the shut down function of the built-in pre-driver (When the terminal voltage is above 2.5V, normalcy works, and it is shut down when it is equal to or less than 0.8V). Please make pulling up outside so that "FLTEN" terminal voltages become more than 2.5V. When the pull up voltage (VP) is at 5V, pull up resistor (RP) connects above 6.8k $\Omega$ , and in case of VP=15V, RP connects above 20k $\Omega$ .
4. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between TH terminal and V<sub>SS</sub> terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used.
5. The pull-down resistor (:33k $\Omega$ (typ)) is connected with the inside of the signal input terminal, but please connect the pull-down resistor(about 2.2 to 3.3k $\Omega$ ) outside to decrease the influence of the noise by wiring etc.
6. As protection of IPM to the unusual current by a short circuit etc, it recommends installing shunt resistors and an over-current protection circuit outside. Moreover, for safety, installation of a fuse in V<sub>CC</sub> line, etc. is recommended.
7. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.
8. The "ITRIP" terminal and the "PFCTRIP" terminal are the input terminal of the built-in comparator. It can stop movement by inputting the voltage more than reference voltage. (At the time of movement, usually those terminals give it for the voltage less than reference voltage). Please use it as various protections such as the over-current protection (feedback from external shunt resistance). In addition, the protection movement is not done a latch of. After the protection movement end, It becomes the movement return state after 2ms (typ.). So, please do the protection movement detection of all input signals in OFF (LOW) promptly afterward.
9. When input pulse width is less than 1 $\mu$ s, an output may not react to the pulse. (Both ON signal and OFF signal)

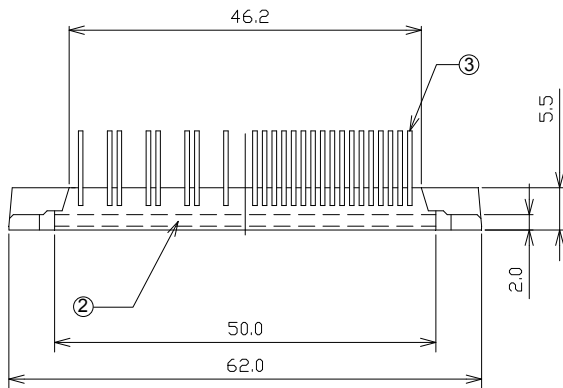
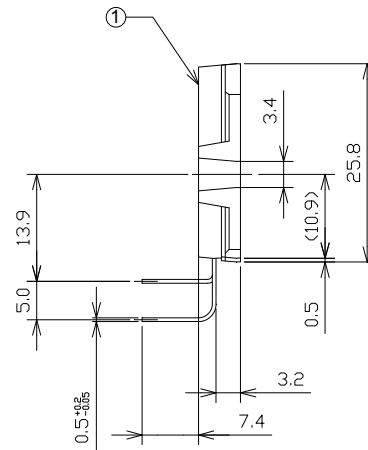
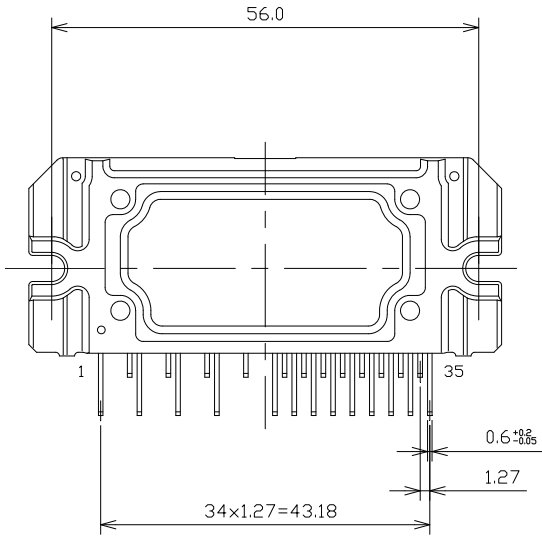
# STK57FU394A-E

## PACKAGE DIMENSIONS

unit : mm

The tolerances of length are +/- 0.5mm unless otherwise specified.

Missing Pin : 2, 3, 6, 7, 10, 11, 14, 15, 17, 18



- note1 : Mark of No.1 pin identification.  
 note2 : The form of a character in this drawing differs from that of IPM.  
 note3 : This indicates the Lot code.  
 The form of a character in this drawing differs from that of IPM.

No.	Part Name	Material	Treatment
①	Case	EPOXY	-
②	Substrate	IMST Substrate	-
③	Lead Frame	Cu	Sn

## STK57FU394A-E

### ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK57FU394A-E	SIP35 56x25.8 / SIP2A (Pb-Free)	8 / Tube

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.