

**IRLR8713PbF**  
**IRLU8713PbF**

**Applications**

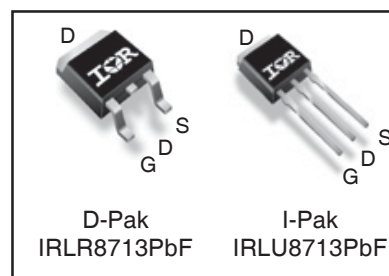
- High Frequency Synchronous Buck Converters for Computer Processor Power
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use

**Benefits**

- Very Low  $R_{DS(on)}$  at 4.5V  $V_{GS}$
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

HEXFET® Power MOSFET

<b><math>V_{DSS}</math></b>	<b><math>R_{DS(on)}</math> max</b>	<b>Qg</b>
<b>25V</b>	<b>4.8m<math>\Omega</math></b>	<b>17.4nC</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	25	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	100 <sup>④</sup>	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	72 <sup>④</sup>	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	410	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation <sup>⑤</sup>	81	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation <sup>⑤</sup>	40	
	Linear Derating Factor	0.54	W/ $^\circ\text{C}$
$T_J$	Operating Junction and	-55 to + 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑥</sup>	—	1.86	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) <sup>⑥⑥</sup>	—	50	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑥</sup>	—	110	

Notes <sup>①</sup> through <sup>⑥</sup> are on page 10

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

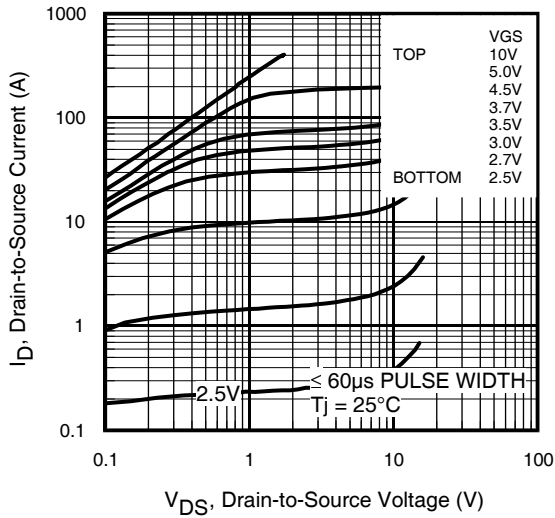
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	25	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	16	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	3.8	4.8	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 21A ③
		—	5.0	6.3		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.35	1.85	2.35	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-7.0	—	mV/°C	
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1.0	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V
		—	—	150		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
g <sub>fs</sub>	Forward Transconductance	79	—	—	S	V <sub>DS</sub> = 13V, I <sub>D</sub> = 17A
Q <sub>g</sub>	Total Gate Charge	—	17.4	26	nC	V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 17A See Fig.16
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	4.0	—		
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	2.2	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	5.8	—		
Q <sub>godr</sub>	Gate Charge Overdrive	—	5.4	—		
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	8.0	—	nC	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V
Q <sub>oss</sub>	Output Charge	—	8.6	—		
R <sub>G</sub>	Gate Resistance	—	0.9	1.6	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	14	—	ns	V <sub>DD</sub> = 13V, V <sub>GS</sub> = 4.5V ③ I <sub>D</sub> = 17A Clamped Inductive Load
t <sub>r</sub>	Rise Time	—	24	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	12	—		
t <sub>f</sub>	Fall Time	—	5.9	—		
C <sub>iss</sub>	Input Capacitance	—	2240	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 13V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	580	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	270	—		

## Avalanche Characteristics

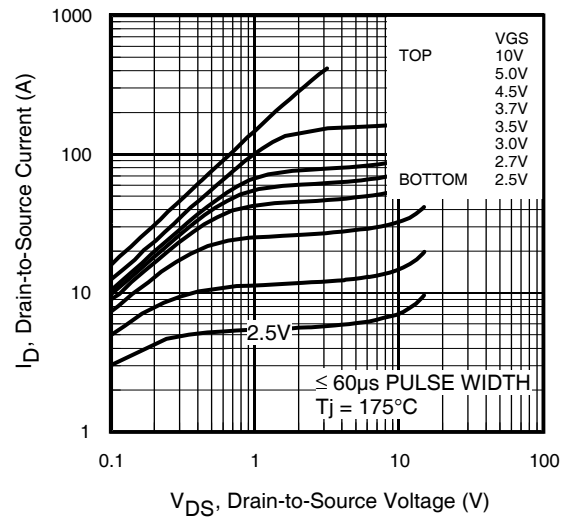
	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	190	mJ
I <sub>AR</sub>	Avalanche Current ①	—	17	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	—	8.1	mJ

## Diode Characteristics

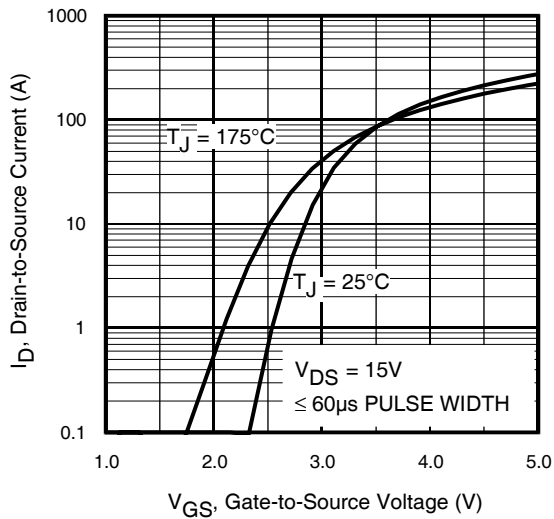
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	100 ④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	410		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 17A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	16	24	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 17A, V <sub>DD</sub> = 13V
Q <sub>rr</sub>	Reverse Recovery Charge	—	15	23	nC	di/dt = 300A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



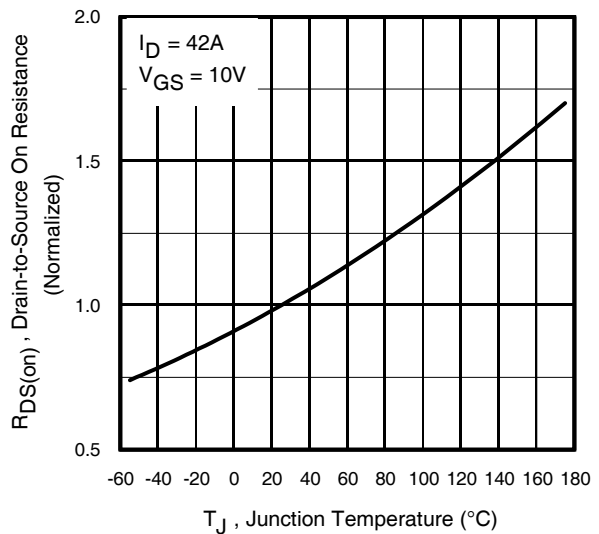
**Fig 1.** Typical Output Characteristics



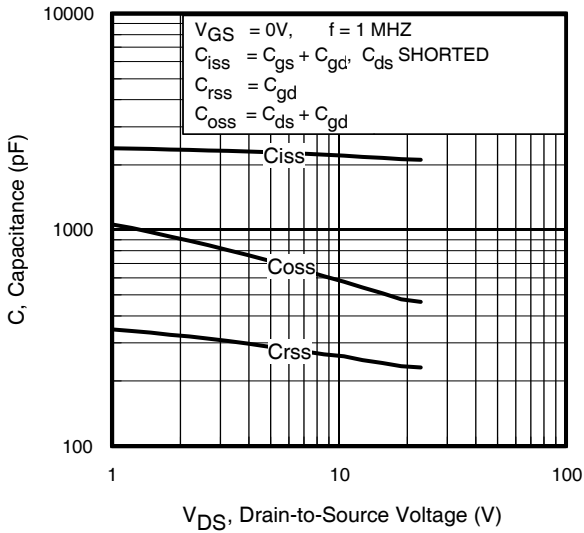
**Fig 2.** Typical Output Characteristics



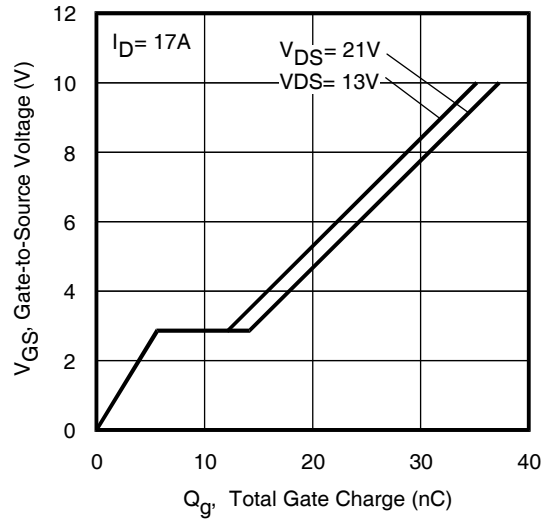
**Fig 3.** Typical Transfer Characteristics



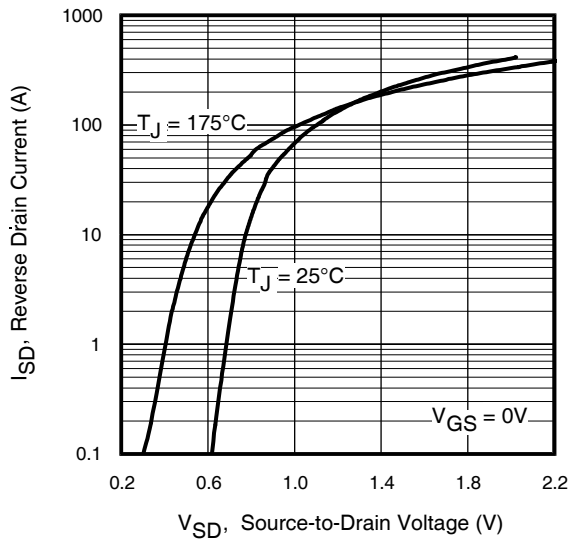
**Fig 4.** Normalized On-Resistance Vs. Temperature



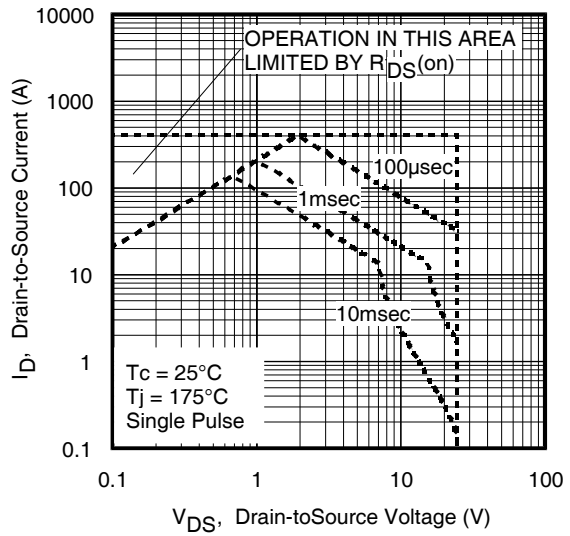
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



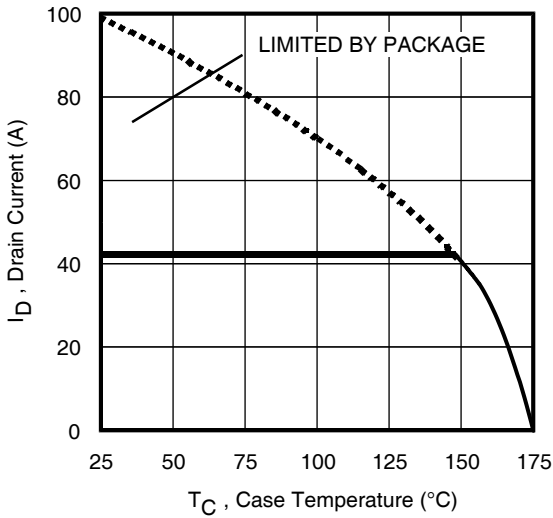
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



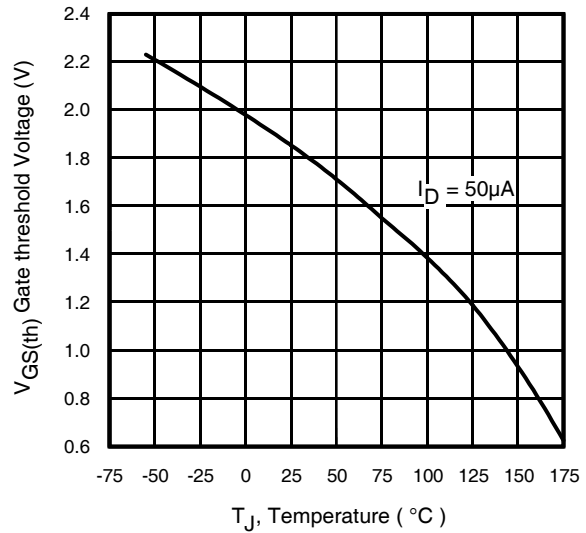
**Fig 7.** Typical Source-Drain Diode Forward Voltage



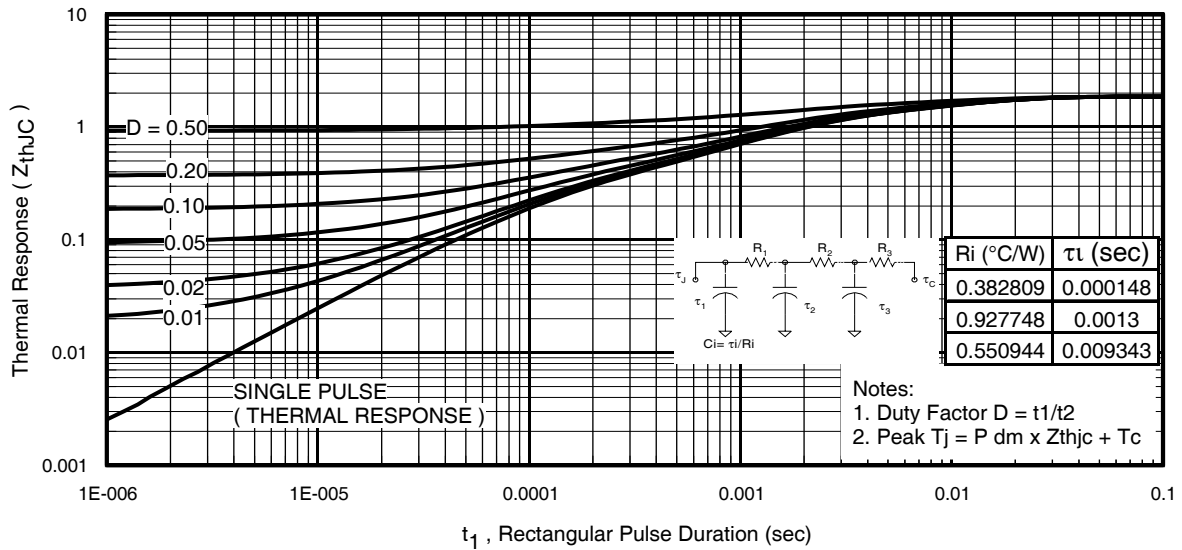
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature



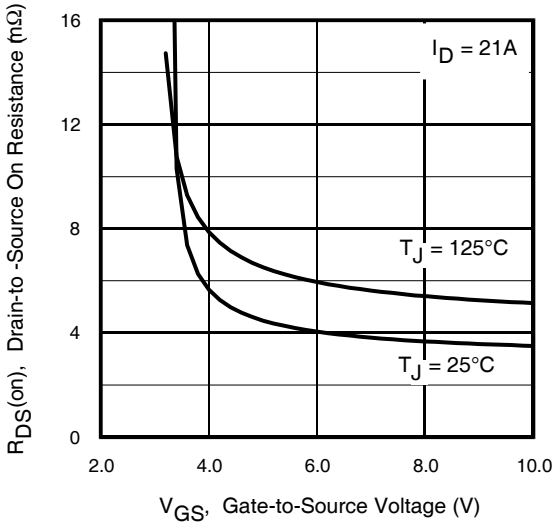
**Fig 10.** Threshold Voltage Vs. Temperature



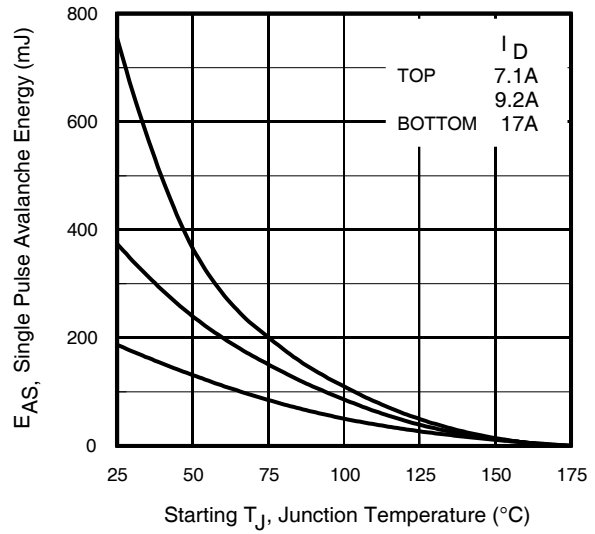
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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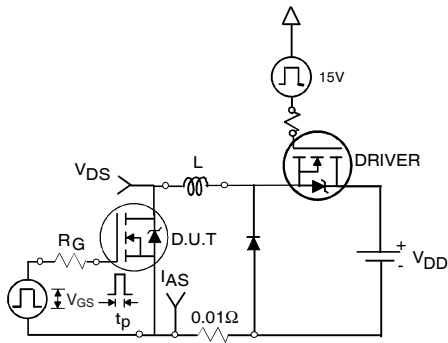
International  
**IR** Rectifier



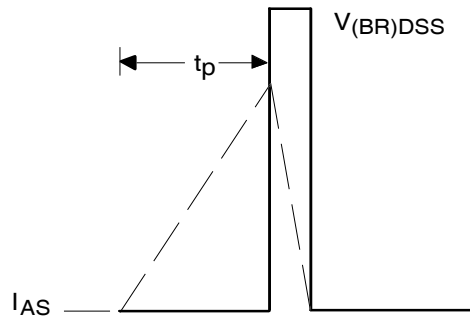
**Fig 12.** On-Resistance vs. Gate Voltage



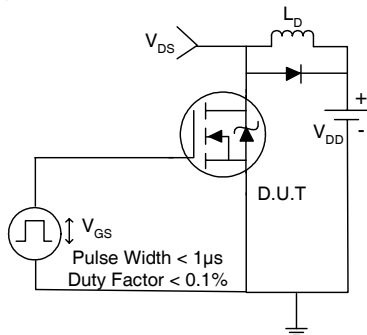
**Fig 13.** Maximum Avalanche Energy vs. Drain Current



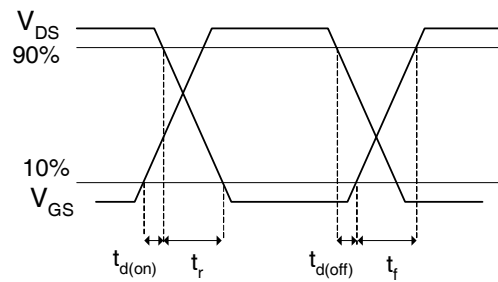
**Fig 14a.** Unclamped Inductive Test Circuit



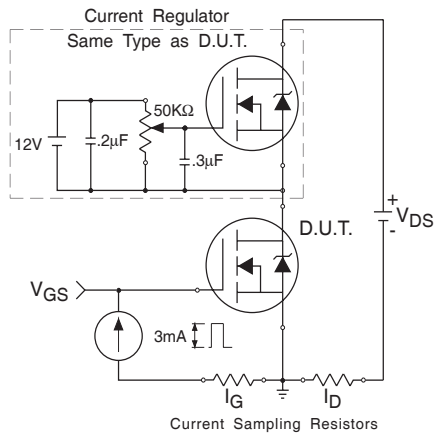
**Fig 14b.** Unclamped Inductive Waveforms



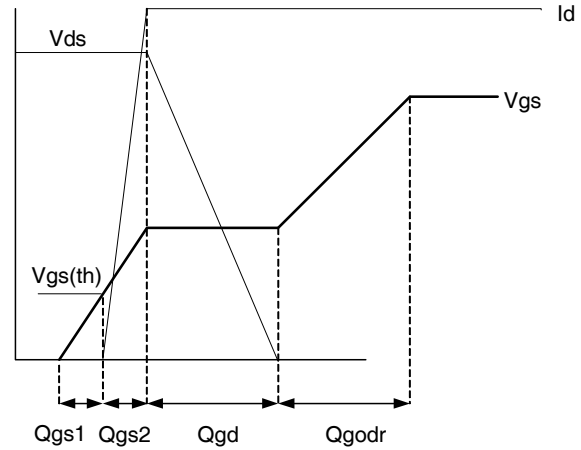
**Fig 15a.** Switching Time Test Circuit



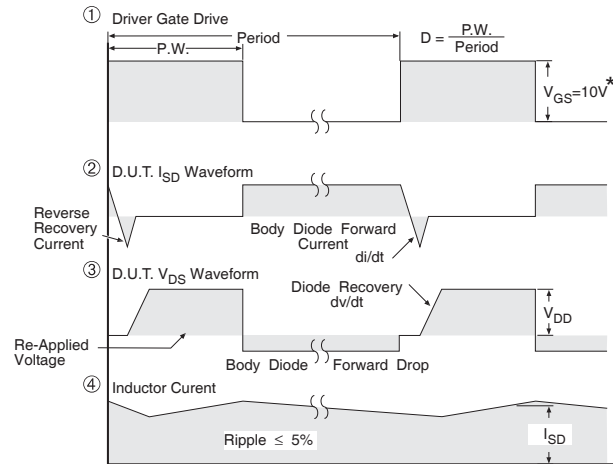
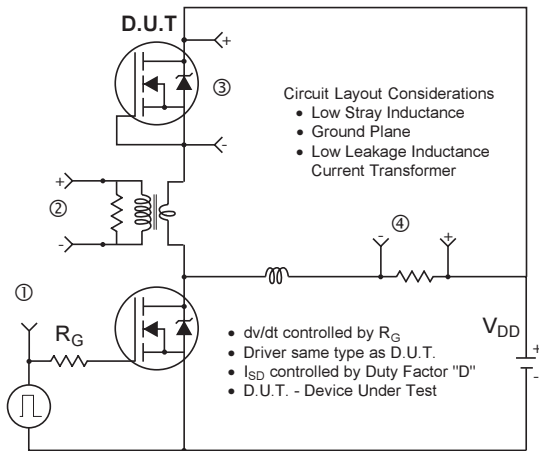
**Fig 15b.** Switching Time Waveforms



**Fig 16a.** Gate Charge Test Circuit



**Fig 16b.** Gate Charge Waveform



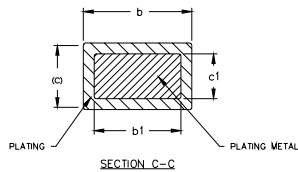
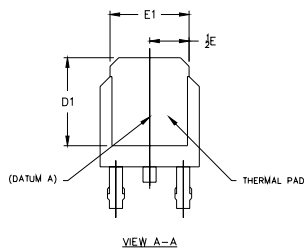
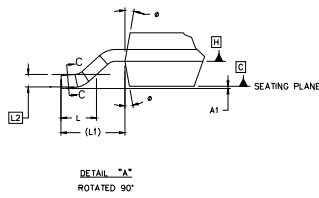
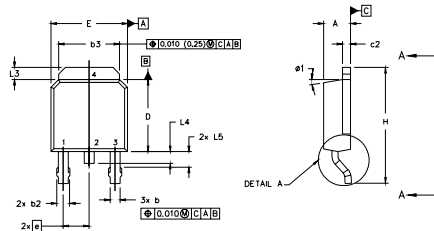
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

# IRLR/U8713PbF

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**IR** Rectifier

## D-Pak (TO-252AA) Package Outline



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5.
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.15		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.093 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	
ø	0"	10"	0"	10"	
ø1	0"	15"	0"	15"	

**LEAD ASSIGNMENTS**

**HEXFET**

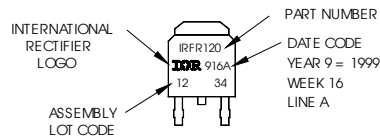
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBTs, CoPACK**

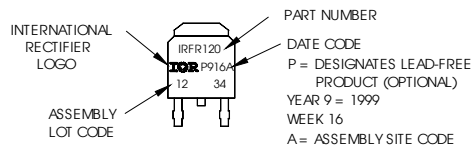
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 1999  
IN THE ASSEMBLY LINE "A"  
Note: "P" in assembly line  
position indicates "Lead-Free"

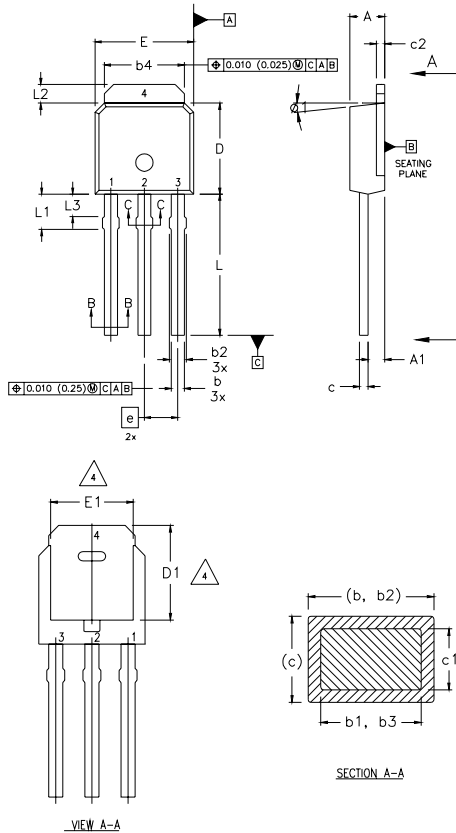


**OR**





## I-Pak (TO-251AA) Package Outline



**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

**LEAD ASSIGNMENTS**

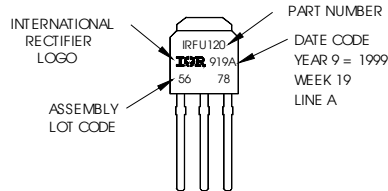
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

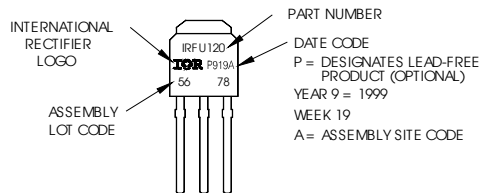
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	Ø	15'	Ø	15'	

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 6678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"  
**Note:** "P" in assembly line  
position indicates "Lead-Free"



**OR**

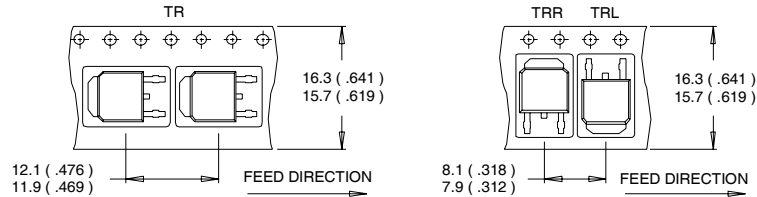


# IRLR/U8713PbF

International  
**IR** Rectifier

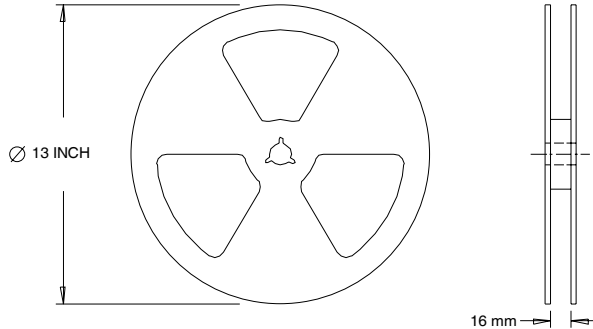
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.77\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 17\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.
- ⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥  $R_\theta$  is measured at  $T_J$  approximately at  $90^\circ\text{C}$

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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