Data Sheet July 1999 File Number 4501.2

52A, 30V, 0.019 Ohm, N-Channel Logic Level, Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Ordering Information

PART NUMBER	PACKAGE	BRAND
HPLU3103	TO-251AA	HP3103
HPLR3103	TO-252AA	HP3103

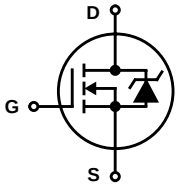
NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HPLR3103T.

Features

- Logic Level Gate Drive
- 52A†, 30V
- Low On-Resistance, $r_{DS(ON)} = 0.019\Omega$
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

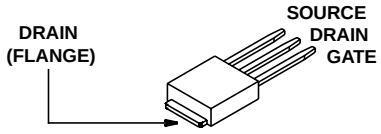
† Calculated continuous current based on maximum allowable junction temperature. Package limited to 20A continuous, see Figure 9.

Symbol

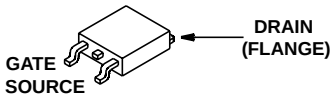


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Othewise Specified

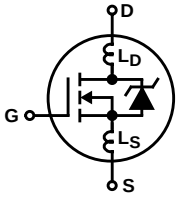
		HPLR3103, HPLU3103	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±16V	V
Continuous Drain Current	I_D	52	A
Pulsed Drain Current (Note 2)	I_{DM}	390	A
Single Pulse Avalanche Energy (Note 4)	E_{AS}	240	mj
Power Dissipation	P_D	89	W
Derate Above 25^oC		0.71	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

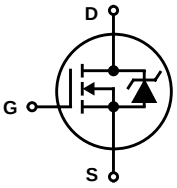
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 24V, V_{GS} = 0V, $T_C = 125^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V		-	-	100	nA
Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25^oC, I_D = 1mA		-	0.037	-	V
Drain to Source On Resistance (Note 3)	$r_{DS(ON)}$	I_D = 28A, V_{GS} = 10V		-	-	0.019	Ω
		I_D = 23A, V_{GS} = 4.5V		-	-	0.024	Ω
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 15V, $I_D \cong$ 34A, R_L = 0.441Ω, V_{GS} = 4.5V, R_{GS} =3.4Ω, $I_{g(REF)}$ = 3mA		-	9	-	ns
Rise Time	t_r			-	210	-	ns
Turn-Off Delay Time (Note 3)	$t_{d(OFF)}$			-	20	-	ns
Fall Time	t_f			-	54	-	ns
Total Gate Charge	Q_g	V_{DD} = 24V, $I_D \cong$ 34A, V_{GS} = 4.5V (Figure 6)		-	-	50	nC
Gate to Source Charge	Q_{gs}			-	-	14	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	-	28	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 5)		-	1600	-	pF
Output Capacitance	C_{OSS}			-	640	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	320	-	pF
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) From Package to Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances	-	7.5	-	nH
Internal Drain Inductance	L_D	Measured From the Drain-Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.4	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	110	$^oC/W$
		(PCB Mount Steady State)	-	-	50	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	MOSFET Symbol Showing The Integral Reverse P-N Junction Diode 	-	-	52 (Note 1)	A
Pulsed Source to Drain Current (Note 2)	I_{SDM}		-	-	220	A
Source to Drain Diode Voltage (Note 3)	V_{SD}	I_{SD} = 28A	-	-	1.3	V
Reverse Recovery Time (Note 3)	t_{rr}	I_{SD} = 34A, dI_{SD}/dt = 100A/µs	-	81	120	ns
Reverse Recovered Charge (Note 3)	Q_{RR}	I_{SD} = 34A, dI_{SD}/dt = 100A/µs	-	210	310	nC

NOTES:

2. Repetitive rating; pulse width limited by maximum junction temperature (See Figure 11).
3. Pulse width ≤ 300µs; duty cycle ≤ 2%.
4. V_{DD} = 15V, starting $T_J = 25^oC$, L = 300µH, $R_G = 25\Omega$, peak I_{AS} = 34A, (Figure 10).

Typical Performance Curves

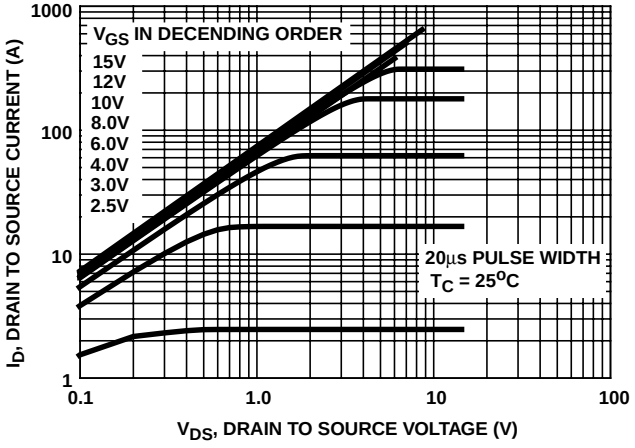


FIGURE 1. OUTPUT CHARACTERISTICS

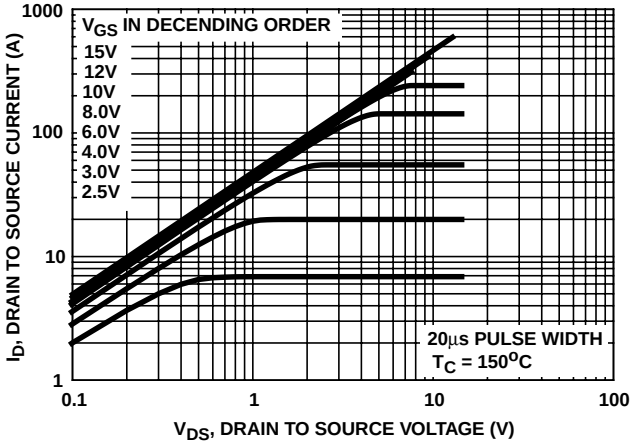


FIGURE 2. OUTPUT CHARACTERISTICS

Typical Performance Curves (Continued)

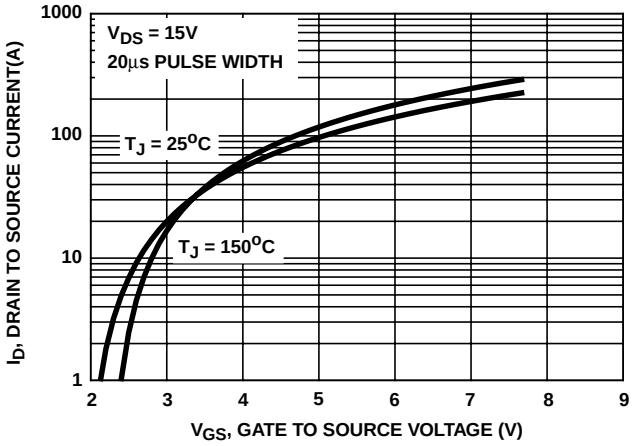


FIGURE 3. TRANSFER CHARACTERISTICS

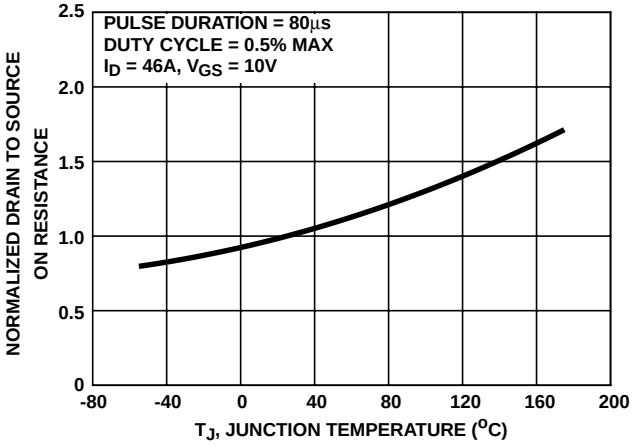


FIGURE 4. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

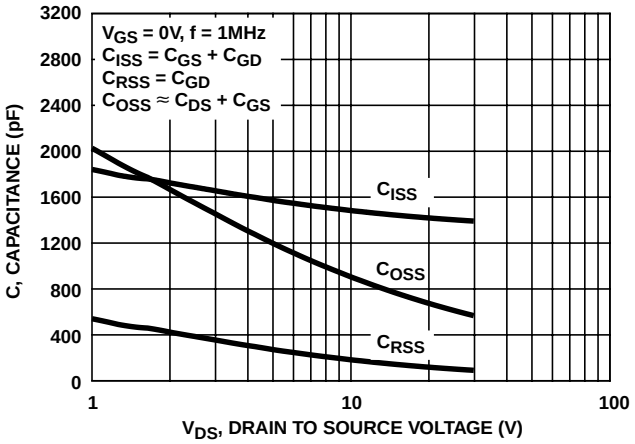


FIGURE 5. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

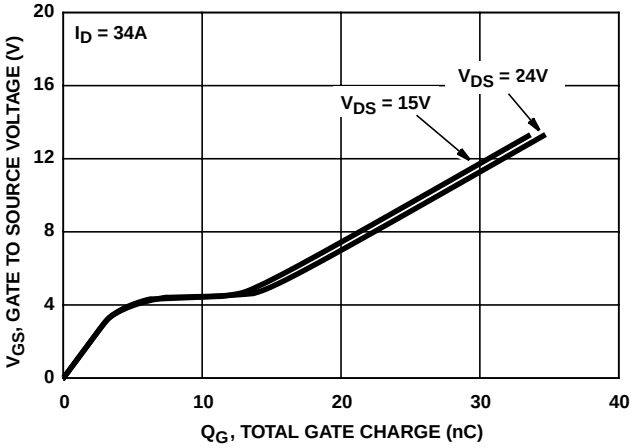


FIGURE 6. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

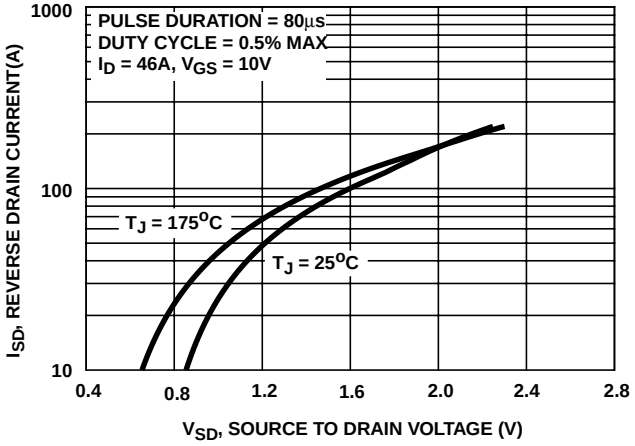


FIGURE 7. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

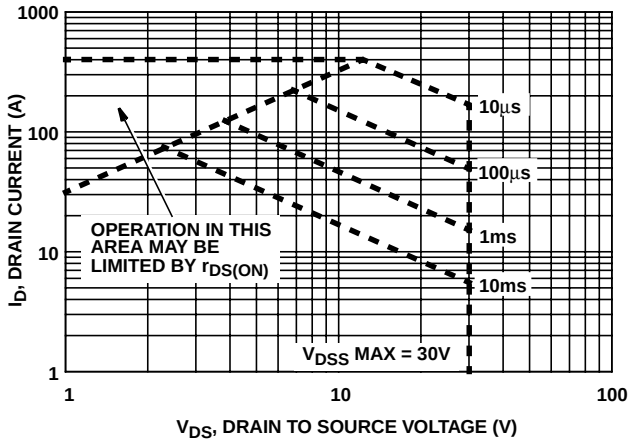


FIGURE 8. FORWARD BIAS SAFE OPERATING AREA

Typical Performance Curves (Continued)

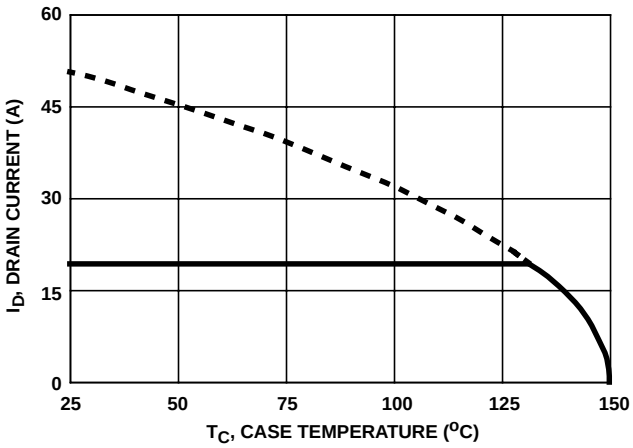


FIGURE 9. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

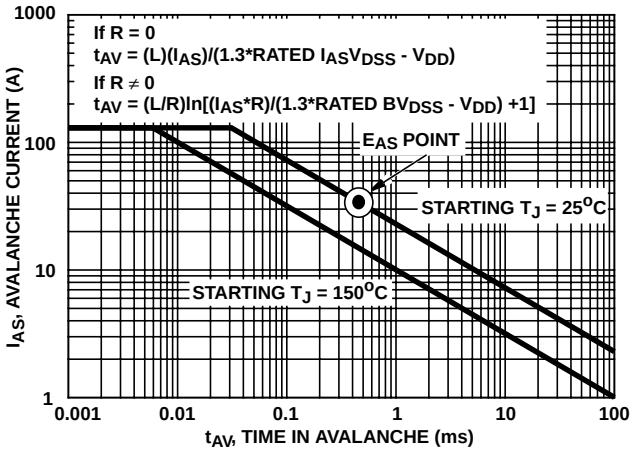


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

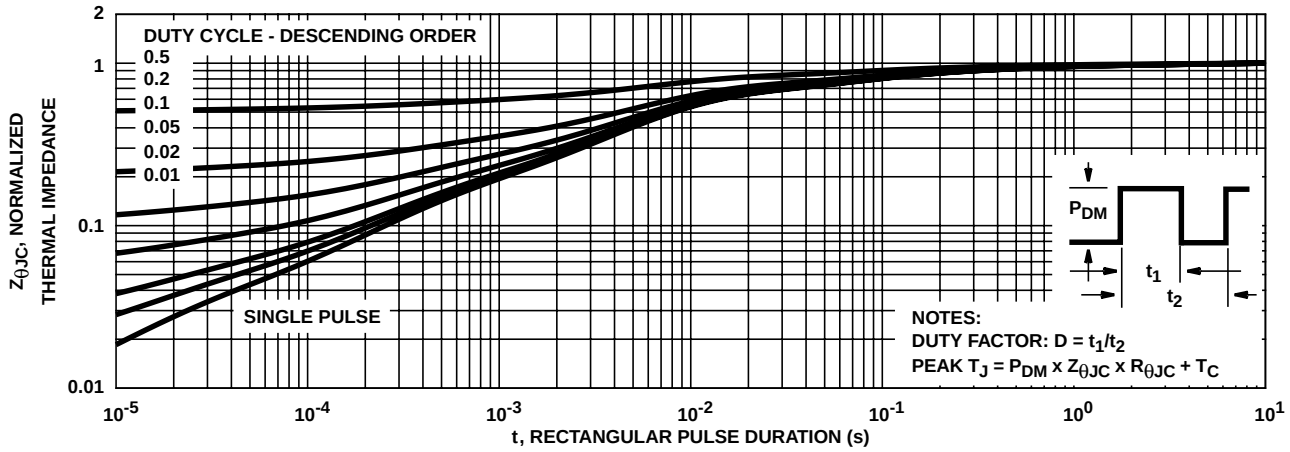


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

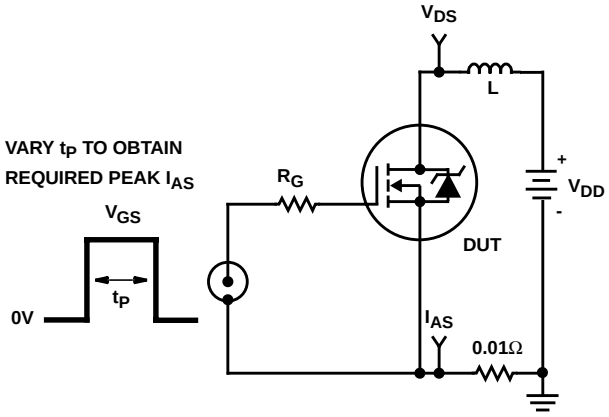


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

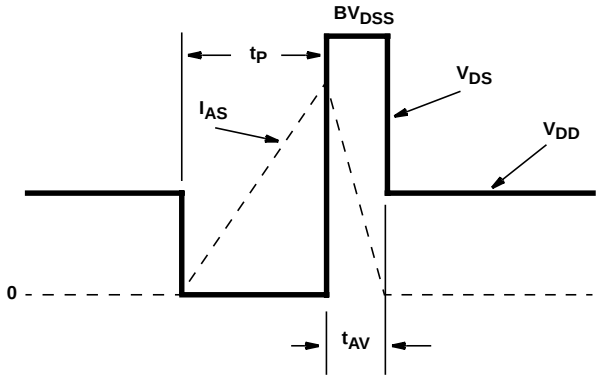


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

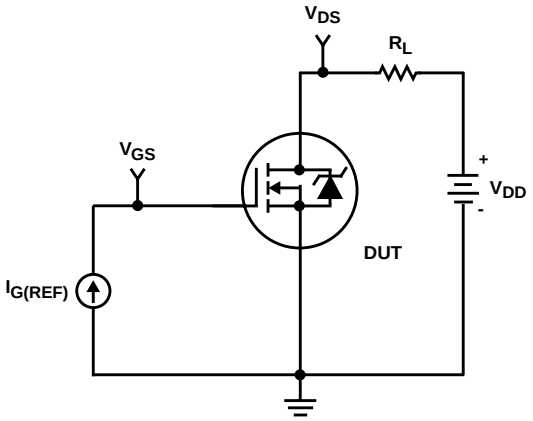


FIGURE 14. GATE CHARGE TEST CIRCUIT

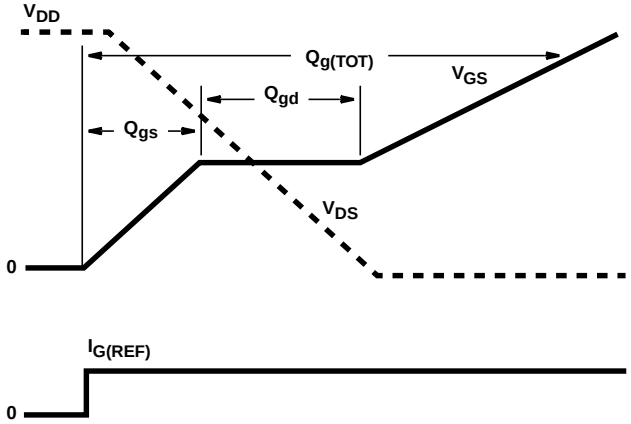


FIGURE 15. GATE CHARGE WAVEFORMS

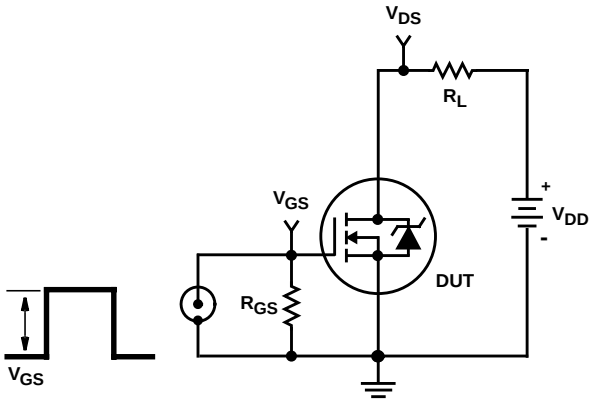


FIGURE 16. SWITCHING TIME TEST CIRCUIT

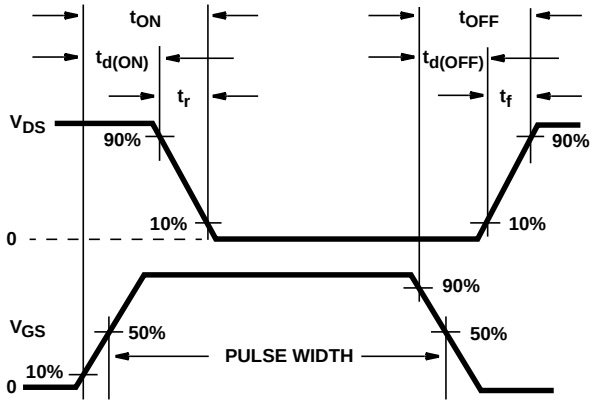


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

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