八路同步采样 24 位模数转换器

查询样品: ADS1278-EP

特性

- 同时测量八个通道
- 高达 **128kSPS** 数据速率
- **AC** 性能：
  62kHz 带宽
  111dB 信噪比 **(SNR)**（高分辨率模式）
  -108dB 总谐波失真 **(THD)**
- **DC** 精度：
  0.8-μV/°C 偏移漂移
  1.3-ppm/°C 增益漂移
- 可选运行模式：
  高速：**128kSPS**，**106dB SNR**
  高分辨率：**52kSPS**，**111dB SNR**
  低功耗：**52kSPS**，**31mW/ch**
  低速：**10kSPS**，**7mW/ch**
- 线性相位数字滤波器
- **SPI™** 或者帧同步串行接口
- 低采样孔径错误
- 调制器输出选项（数字滤波器旁通）
- 模拟电源：**5V**
- 数字内核：**1.8V**
- **I/O** 电源：**1.8V** 至 **3.3V**
- 当前提供散热增强薄型四方扁平封装 **(HTQFP)-64** 封装 **PowerPAD™** 封装

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装**/**测试场所
- 一个制造场所
- 军用温度范围 **(-55°C/125°C)** 内可用 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可提供额外温度范围-请与厂家联系

应用范围

- 振动**/**模式分析
- 多通道数据采集
- 声学**/**动态应变仪
- 压力传感器

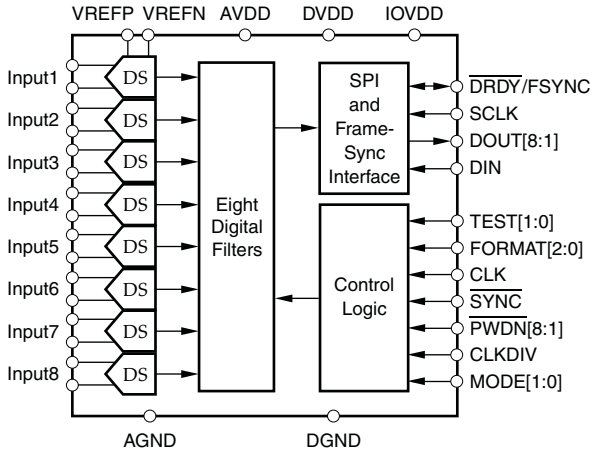
说明

基于单通道ADS1271，ADS1278（八通道）是一款 24 位、三角积分 (ΔΣ) 模数转换器 (ADC)，其数据速率高达每秒 128k 次采样 (SPS)，从而可实现八通道同时采样。

传统上来讲，提供良好漂移性能的工业用三角积分 ADC 使用带有较大通带衰减的数字滤波器。 因此，它们的信号带宽有限并且主要适合于 dc 测量。 音频应用中的高分辨 ADC 提供更大的可用带宽，但是与工业用 ADC 相比，它的偏移和漂移技术规格被大大削弱。 ADS1278 将三种类型的转换器组合在一起，从而实现带有出色 dc 和 ac 技术规格的高精度工业测量。

高阶、斩波稳定调制器在低带内噪声情况下实现极低漂移。 板载抽取滤波器抑制调制器和信号带外噪声。 这些 ADC 在纹波小于 0.005dB 的情况下提供高达那奎斯特速率 90% 的可用信号带宽。

四个运行模式可实现速度、分辨率和功率的优化。 所有操作直接由引脚控制；无需寄存器编程。 器件可在军用温度范围（-55°C 至 125°C）内运行并且采用 HTQFP-64 PowerPAD 封装。



ADS1278

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TQFP - PAP	Reel of 250	ADS1278MPAPTEP	ADS1278EP	V62/12611-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PIN ASSIGNMENTS

PAP PACKAGE
TQFP-64
(TOP VIEW)

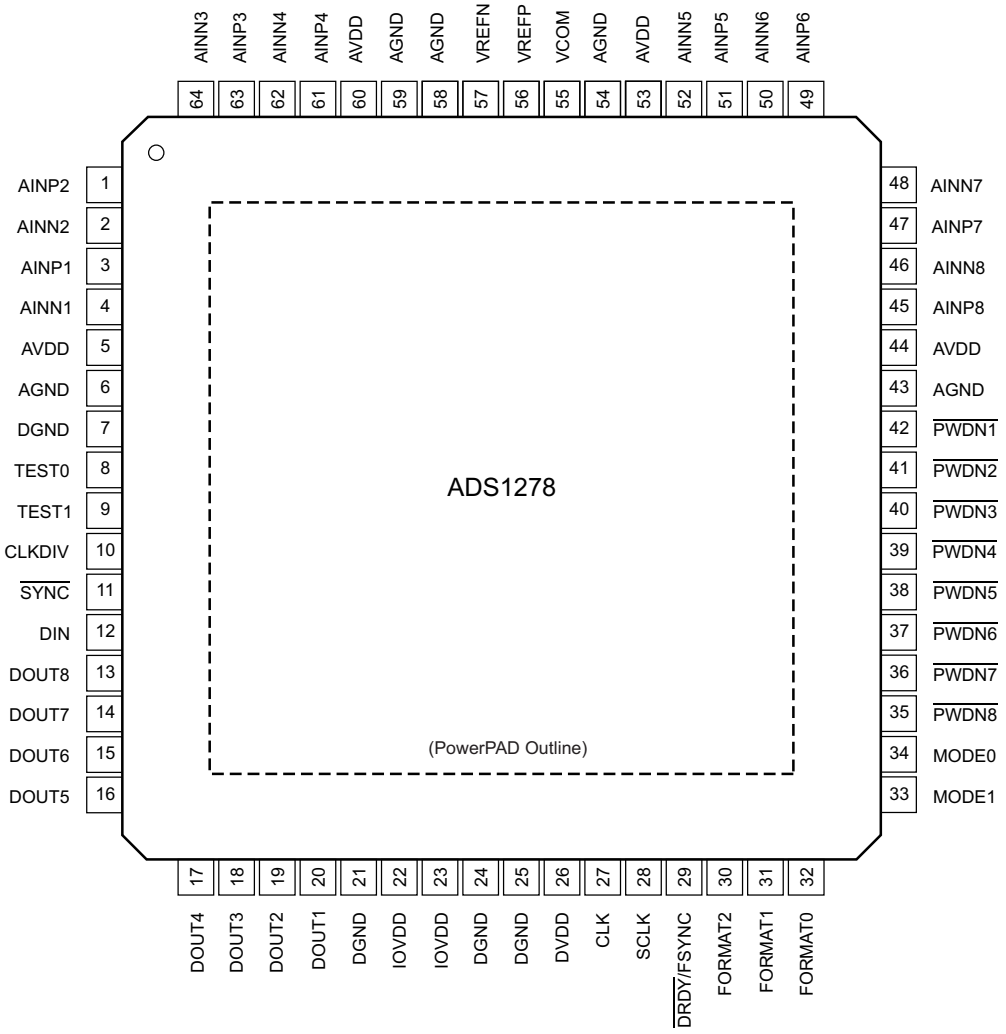


Table 1. PIN DESCRIPTIONS

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AGND	6, 43, 54, 58, 59	Analog ground	Analog ground; connect to DGND using a single plane.
AINP1	3	Analog input	AINP[8:1] Positive analog input, channels 8 through 1.
AINP2	1	Analog input	
AINP3	63	Analog input	
AINP4	61	Analog input	
AINP5	51	Analog input	
AINP6	49	Analog input	
AINP7	47	Analog input	
AINP8	45	Analog input	

Table 1. PIN DESCRIPTIONS (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AINN1	4	Analog input	AINN[8:1] Negative analog input, channels 8 through 1.
AINN2	2	Analog input	
AINN3	64	Analog input	
AINN4	62	Analog input	
AINN5	52	Analog input	
AINN6	50	Analog input	
AINN7	48	Analog input	
AINN8	46	Analog input	
AVDD	5, 44, 53, 60	Analog power supply	Analog power supply (4.75V to 5.25V).
VCOM	55	Analog output	AVDD/2 Unbuffered voltage output.
VREFN	57	Analog input	Negative reference input.
VREFP	56	Analog input	Positive reference input.
CLK	27	Digital input	Master clock input (f_{CLK}).
CLKDIV	10	Digital input	CLK input divider control: 1 = 37MHz (High-Speed mode)/otherwise 27MHz 0 = 13.5MHz (low-power)/5.4MHz (low-speed)
DGND	7, 21, 24, 25	Digital ground	Digital ground power supply.
DIN	12	Digital input	Daisy-chain data input.
DOUT1	20	Digital output	DOUT1 is TDM data output (TDM mode).
DOUT2	19	Digital output	DOUT[8:1] Data output for channels 8 through 1.
DOUT3	18	Digital output	
DOUT4	17	Digital output	
DOUT5	16	Digital output	
DOUT6	15	Digital output	
DOUT7	14	Digital output	
DOUT8	13	Digital output	
$\overline{\text{DRDY}}$/ FSYNC	29	Digital input/output	Frame-Sync protocol: frame clock input; SPI protocol: data ready output.
DVDD	26	Digital power supply	Digital core power supply.
FORMAT0	32	Digital input	FORMAT[2:0] Selects Frame-Sync/SPI protocol, TDM/discrete data outputs, fixed/dynamic position TDM data, and modulator mode/normal operating mode.
FORMAT1	31	Digital input	
FORMAT2	30	Digital input	
IOVDD	22, 23	Digital power supply	I/O power supply (+1.65V to +3.6V).
MODE0	34	Digital input	MODE[1:0] Selects High-Speed, High-Resolution, Low-Power, or Low-Speed mode operation.
MODE1	33	Digital input	
$\overline{\text{PWDN1}}$	42	Digital input	$\overline{\text{PWDN}}$[8:1] Power-down control for channels 8 through 1.
$\overline{\text{PWDN2}}$	41	Digital input	
$\overline{\text{PWDN3}}$	40	Digital input	
$\overline{\text{PWDN4}}$	39	Digital input	
$\overline{\text{PWDN5}}$	38	Digital input	
$\overline{\text{PWDN6}}$	37	Digital input	
$\overline{\text{PWDN7}}$	36	Digital input	
$\overline{\text{PWDN8}}$	35	Digital input	
SCLK	28	Digital input/output	Serial clock input, Modulator clock output.
$\overline{\text{SYNC}}$	11	Digital input	Synchronize input (all channels).
TEST0	8	Digital input	TEST[1:0] Test mode select: 00 = Normal operation; 01 = Do not use; 10 = Do not use; 11 = Test mode
TEST1	9	Digital input	

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted(1)

			UNIT
AVDD to AGND		–0.3 to 6.0	V
DVDD, IOVDD to DGND		–0.3 to 3.6	V
AGND to DGND		–0.3 to 0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog input to AGND		–0.3 to AVDD + 0.3	V
Digital input or output to DGND		–0.3 to DVDD + 0.3	V
Maximum junction temperature, T_J		150	°C
Storage temperature range		–60 to 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS1278 PAP 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	33.1	°C/W
θ_{JC}	Junction-to-case thermal resistance	6.2	
θ_{JB}	Junction-to-board thermal resistance(3)	7.9	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(5)	7.8	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(4) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(5) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA} 。

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –55°C to 125°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating temperature range, T_A			-55		125	°C
Analog Inputs						
Full-scale input voltage (FSR(1))		V_{IN} = (AINP – AINN)		±V_{REF}		V
Absolute input voltage		AINP or AINN to AGND	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage (V_{CM})		V_{CM} = (AINP + AINN)/2		2.5		V
Differential input impedance	High-Speed mode			14		kΩ
	High-Resolution mode			14		kΩ
	Low-Power mode			28		kΩ
	Low-Speed mode			140		kΩ
DC Performance						
Resolution		No missing codes	24			Bits
Data rate (f_{DATA})	High-Speed mode	f_{CLK} = 32.768MHz(2)		128,000		SPS
		f_{CLK} = 27MHz		105,469		SPS(3)
	High-Resolution mode			52,734		SPS
	Low-Power mode			52,734		SPS
	Low-Speed mode			10,547		SPS
Integral nonlinearity (INL)(4)		Differential input, V_{CM} = 2.5V		±0.0003	±0.0014	% FSR(1)
Offset error				0.25	2	mV
Offset drift				0.8		µV/°C
Gain error				0.1	0.5	% FSR
Gain drift				1.3		ppm/°C
Noise	High-Speed mode	Shorted input		8.5	68	µV, rms
	High-Resolution mode	Shorted input		5.5	13	µV, rms
	Low-Power mode	Shorted input		8.5	21	µV, rms
	Low-Speed mode	Shorted input		8.0	21	µV, rms
Common-mode rejection		f_{CM} = 60Hz	90	108		dB
Power-supply rejection	AVDD	f_{PS} = 60Hz		80		dB
	DVDD			85		dB
	IOVDD			105		dB
V_{COM} output voltage		No load		AVDD/2		V
AC Performance						
Crosstalk		f = 1kHz, –0.5dBFS(5)		–107		dB
Signal-to-noise ratio (SNR)(6) (unweighted)	High-Speed mode		88.3	106		dB
	High-Resolution mode	V_{REF} = 2.5V	101	110		dB
		V_{REF} = 3V		111		dB
	Low-Power mode		98	106		dB
	Low-Speed mode		98	107		dB
Total harmonic distortion (THD)(7)		V_{IN} = 1kHz, –0.5dBFS		–108	–96	dB
Spurious-free dynamic range				109		dB
Passband ripple				±0.005		dB
Passband				0.453 f_{DATA}		Hz
–3dB Bandwidth				0.49 f_{DATA}		Hz

(1) FSR = full-scale range = $2V_{REF}$.
(2) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes. When f_{CLK} > 27MHz, operation is limited to Frame-Sync mode and V_{REF} ≤ 2.6V.
(3) SPS = samples per second.
(4) Best fit method.
(5) Worst-case channel crosstalk between one or more channels.
(6) Minimum SNR is ensured by the limit of the *DC noise* specification.
(7) THD includes the first nine harmonics of the input signal; Low-Speed mode includes the first five harmonics.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –55°C to 125°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stop band attenuation	High-Resolution mode		95			dB
	All other modes		100			
Stop band	High-Resolution mode		0.547 f_{DATA}		127.453 f_{DATA}	Hz
	All other modes		0.547 f_{DATA}		63.453 f_{DATA}	Hz
Group delay	High-Resolution mode			39/f_{DATA}		s
	All other modes			38/f_{DATA}		s
Settling time (latency)	High-Resolution mode	Complete settling		78/f_{DATA}		s
	All other modes	Complete settling		76/f_{DATA}		s
Voltage Reference Inputs						
Reference input voltage (V_{REF}) (V_{REF} = VREFP – VREFN)		f_{CLK} = 27MHz	0.5	2.5	3.1	V
		f_{CLK} = 32.768MHz (2)	0.5	2.5	2.6	V
Negative reference input (VREFN)			AGND – 0.1		AGND + 0.1	V
Positive reference input (VREFP)			VREFN + 0.5		AVDD + 0.1	V
Reference Input impedance	High-Speed mode			0.65		kΩ
	High-Resolution mode			0.65		kΩ
	Low-Power mode			1.3		kΩ
	Low-Speed mode			6.5		kΩ
Digital Input/Output (IOVDD = 1.8V to 3.6V)						
V_{IH}			0.7 IOVDD		IOVDD	V
V_{IL}			DGND		0.3 IOVDD	V
V_{OH}		I_{OH} = 4mA	0.8 IOVDD		IOVDD	V
V_{OL}		I_{OL} = 4mA	DGND		0.2 IOVDD	V
Input leakage		0 < $V_{IN\ DIGITAL}$ < IOVDD			±10	µA
Master clock rate (f_{CLK})		High-Speed mode (8)	0.1		32.768	MHz
		Other modes	0.1		27	MHz
Power Supply						
AVDD			4.75	5	5.25	V
DVDD			1.65	1.8	1.95	V
IOVDD			1.65		3.6	V
Power-down current	AVDD			1	10	µA
	DVDD			1	50	µA
	IOVDD			1	11	µA
AVDD current	High-Speed mode			97	145	mA
	High-Resolution mode			97	145	mA
	Low-Power mode			44	64	mA
	Low-Speed mode			9	14	mA
DVDD current	High-Speed mode			23	30	mA
	High-Resolution mode			16	20	mA
	Low-Power mode			12	17	mA
	Low-Speed mode			2.5	4.5	mA
IOVDD current	High-Speed mode			0.25	1	mA
	High-Resolution mode			0.125	0.6	mA
	Low-Power mode			0.125	0.6	mA
	Low-Speed mode			0.035	0.3	mA

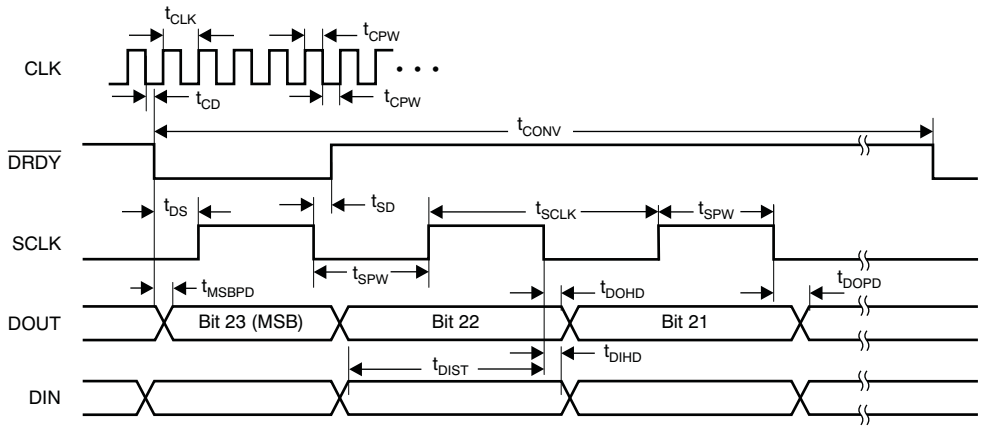
(8) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes. When f_{CLK} > 27MHz, operation is limited to Frame-Sync mode and V_{REF} ≤ 2.6V.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = –55°C to 125°C, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, VREFN = 0 V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation	High-Speed mode			530	785	mW
	High-Resolution mode			515	765	mW
	Low-Power mode			245	355	mW
	Low-Speed mode			50	80	mW

TIMING CHARACTERISTICS: SPI FORMAT



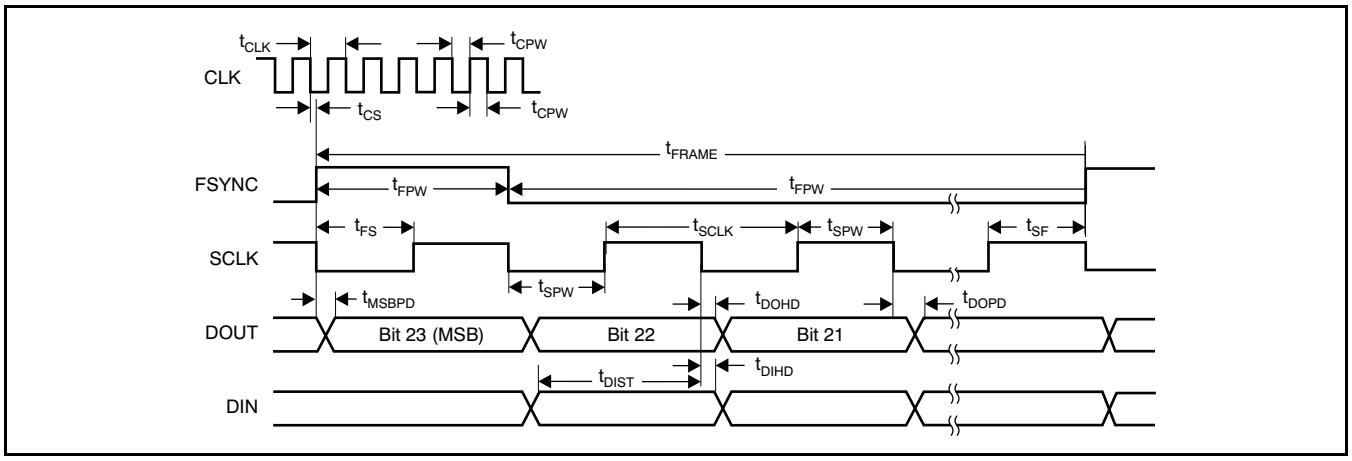
TIMING REQUIREMENTS: SPI FORMAT

For T_A = –40°C to 125°C, IOVDD = 1.65 V to 3.6 V, and DVDD = 1.65 V to 1.95 V.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$) (1)	37		10,000	ns
t_{CPW}	CLK positive or negative pulse width	15			ns
t_{CONV}	Conversion period ($1/f_{DATA}$) (2)	256		2560	t_{CLK}
t_{CD} (3)	Falling edge of CLK to falling edge of $\overline{DRDY}$		22		ns
t_{DS} (3)	Falling edge of $\overline{DRDY}$ to rising edge of first SCLK to retrieve data	1			t_{CLK}
t_{MSBPD}	$\overline{DRDY}$ falling edge to DOUT MSB valid (propagation delay)			16	ns
t_{SD} (3)	Falling edge of SCLK to rising edge of $\overline{DRDY}$		18		ns
t_{SCLK} (4)	SCLK period	1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width	0.4			t_{CLK}
t_{DOHD} (5) (3) (6)	SCLK falling edge to new DOUT invalid (hold time)	10			ns
t_{DOPD} (5) (3)	SCLK falling edge to new DOUT valid (propagation delay)			32	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)	6			ns
t_{DIHD} (6)	Old DIN valid to falling edge of SCLK (hold time)	6			ns

(1) f_{CLK} = 27MHz maximum.
(2) Depends on MODE[1:0] and CLKDIV selection. See Table 7 (f_{CLK}/f_{DATA}).
(3) Load on $\overline{DRDY}$ and DOUT = 20pF.
(4) For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc.
(5) Timing parameters are characerized or guranteed by design for specified temperature but not production tested.
(6) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4ns.

Figure 1. TIMING CHARACTERISTICS: FRAME-SYNC FORMAT



TIMING REQUIREMENTS: FRAME-SYNC FORMAT(1)

For T_A = –40°C to 125°C, IOVDD = 1.65 V to 3.6 V, and DVDD = 1.65 V to 1.95 V.

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	All modes	37		10,000	ns
		High-Speed mode only	30.5			ns
t_{CPW}	CLK positive or negative pulse width		12			ns
t_{CS}	Falling edge of CLK to falling edge of SCLK		–0.25		0.25	t_{CLK}
t_{FRAME}	Frame period ($1/f_{DATA}$)(2)		256		2560	t_{CLK}
t_{FPW}	FSYNC positive or negative pulse width		1			t_{SCLK}
t_{FS}	Rising edge of FSYNC to rising edge of SCLK		5			ns
t_{SF}	Rising edge of SCLK to rising edge of FSYNC		5			ns
t_{SCLK}	SCLK period(3)		1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width		0.4			t_{CLK}
t_{DOHD} (4)(5) (6)	SCLK falling edge to old DOUT invalid (hold time)		10			ns
t_{DOPD} (4)(6)	SCLK falling edge to new DOUT valid (propagation delay)				31	ns
t_{MSBPD} (4)	FSYNC rising edge to DOUT MSB valid (propagation delay)				31	ns
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD} (5)	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) Timing parameters are characerized or guranteed by design for specified temperature but not production tested.
(2) Depends on MODE[1:0] and CLKDIV selection. See Table 7 (f_{CLK}/f_{DATA}).
(3) SCLK must be continuously running and limited to ratios of 1, 1/2, 1/4, and 1/8 of f_{CLK}.
(4) Timing parameters are characerized or guranteed by design for specified temperature but not production tested.
(5) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is >4 ns.
(6) Load on DOUT = 20 pF.

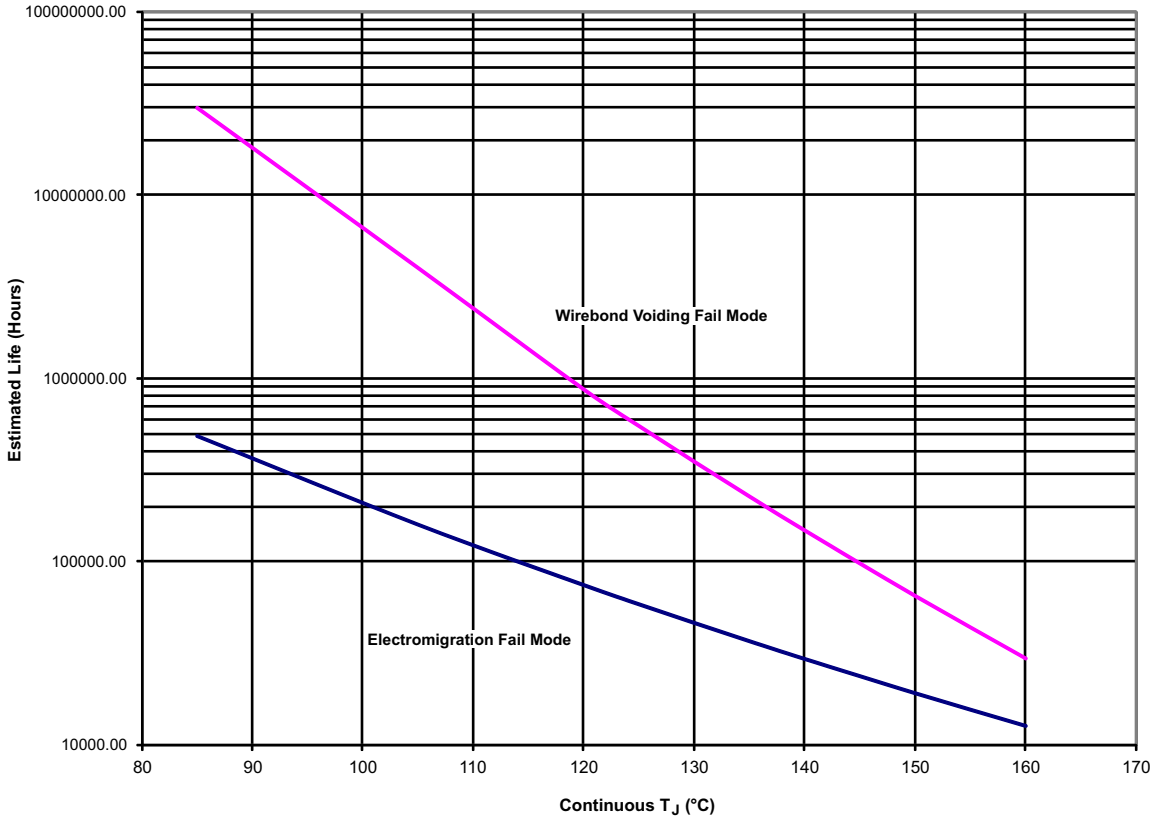


Figure 2. ADS1278 Operating Life Derating and Wirebond Voiding Fail Mode Chart

Notes:

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Sillicon operating life design goal is 10 years at 110°C junction temperature.

TYPICAL CHARACTERISTICS

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

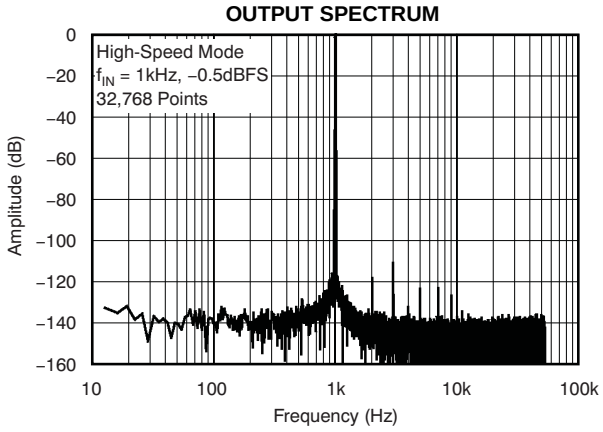


Figure 3.

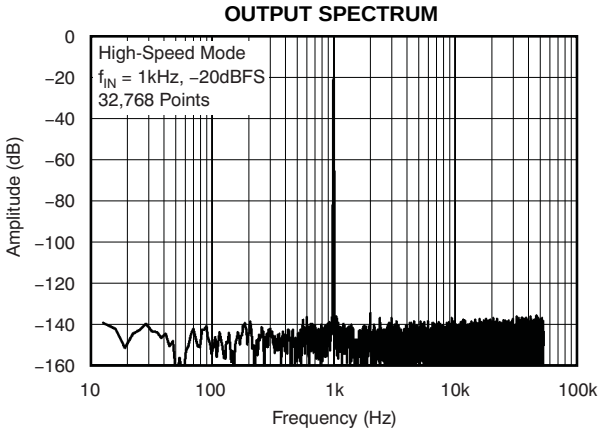


Figure 4.

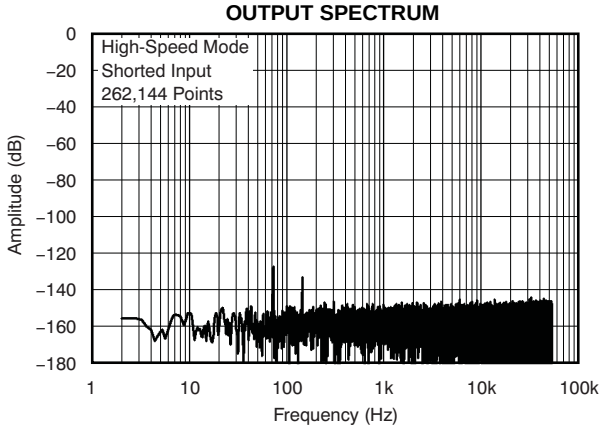


Figure 5.

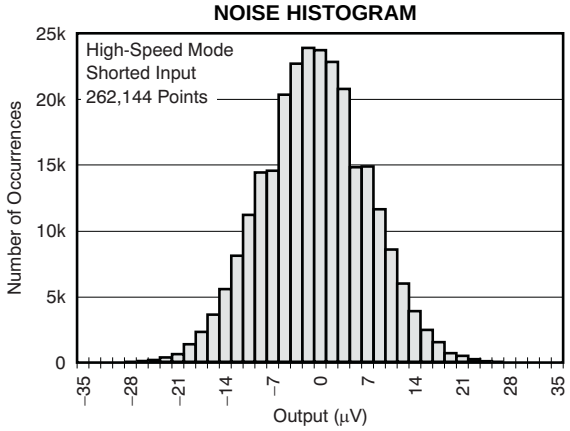


Figure 6.

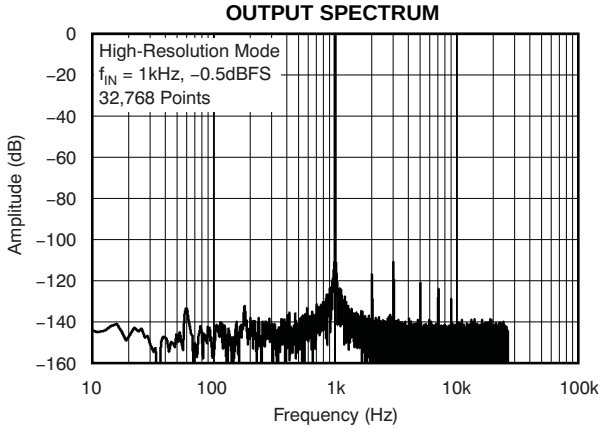


Figure 7.

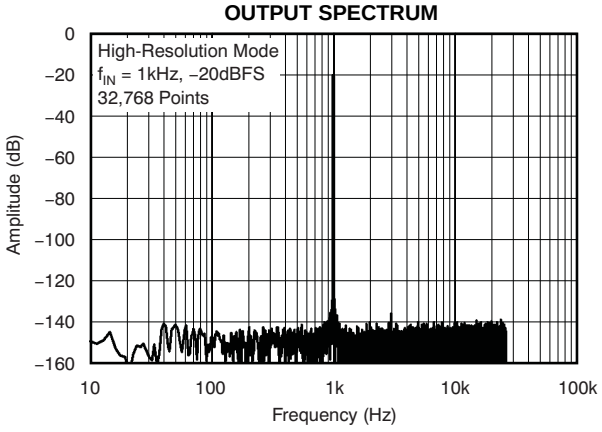


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

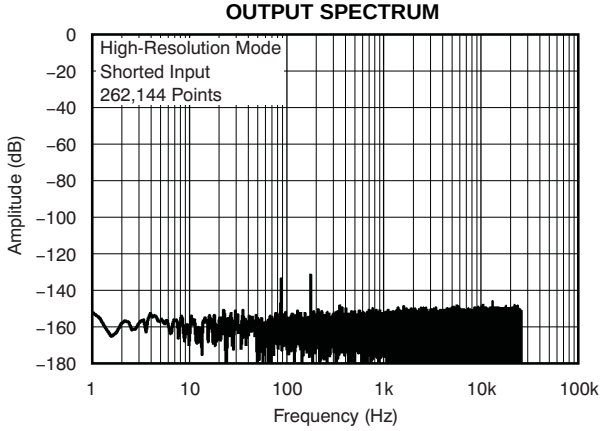


Figure 9.

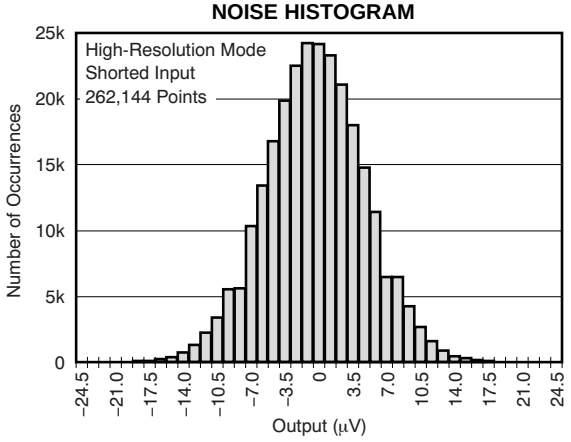


Figure 10.

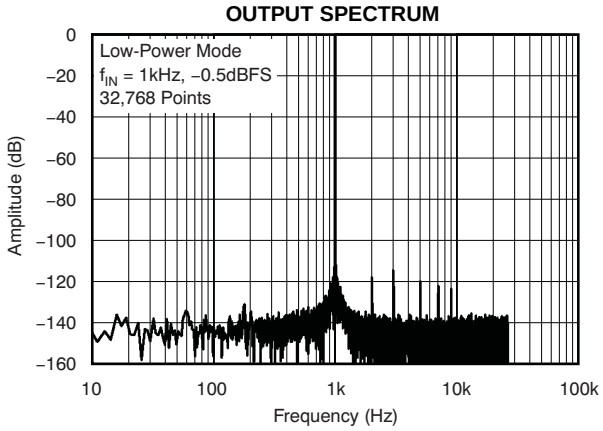


Figure 11.

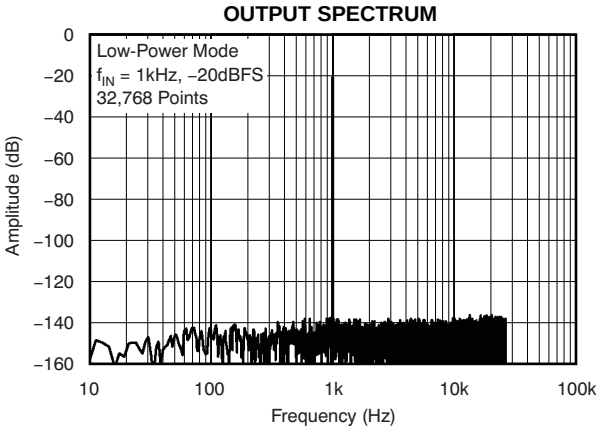


Figure 12.

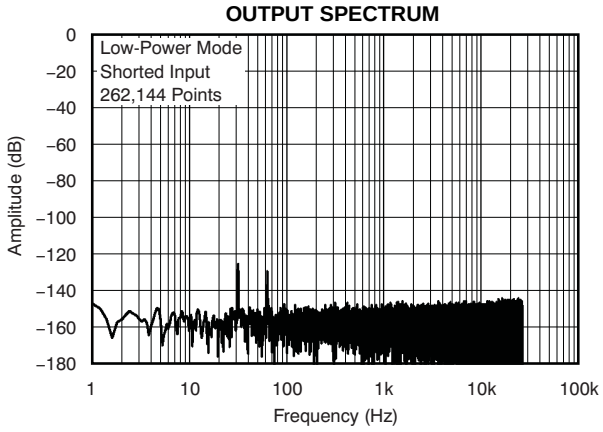


Figure 13.

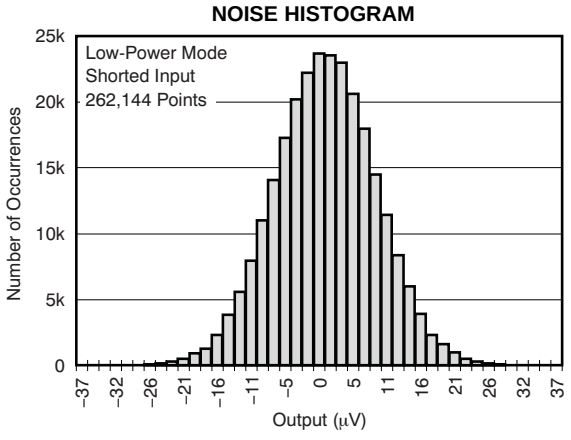


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

OUTPUT SPECTRUM

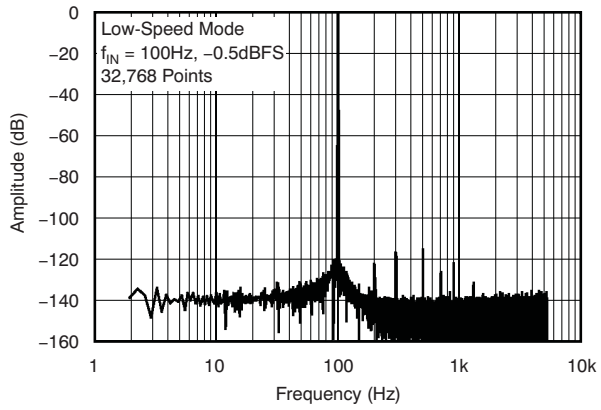


Figure 15.

OUTPUT SPECTRUM

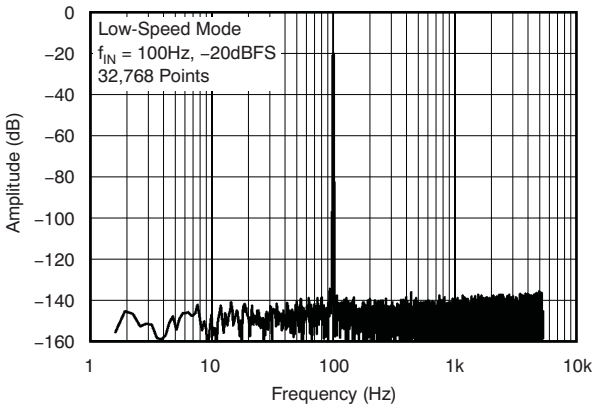


Figure 16.

OUTPUT SPECTRUM

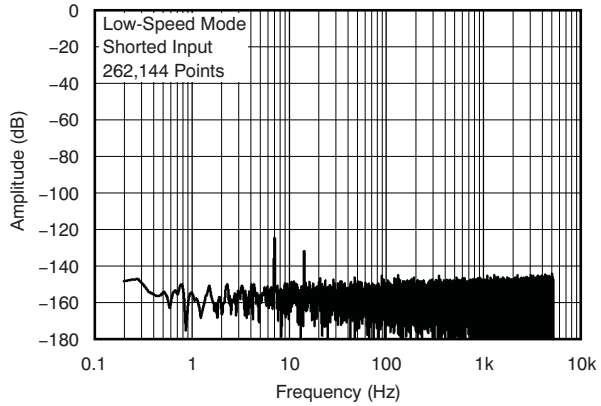


Figure 17.

NOISE HISTOGRAM

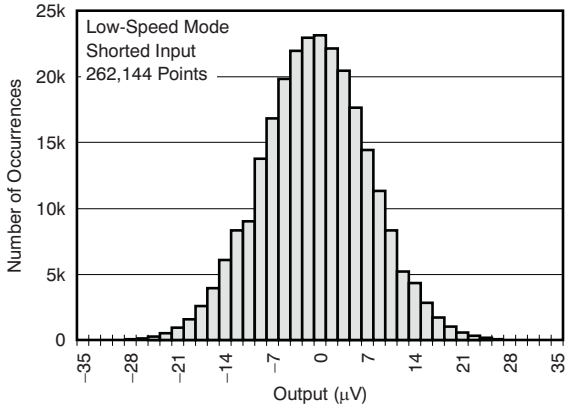


Figure 18.

TOTAL HARMONIC DISTORTION vs FREQUENCY

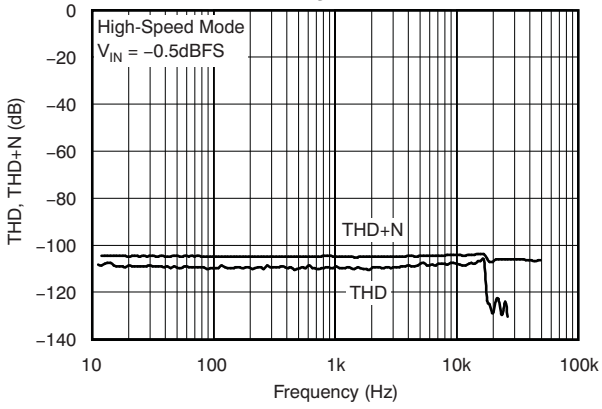


Figure 19.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

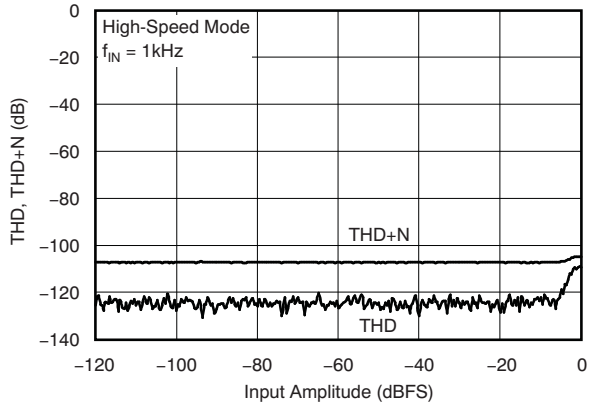


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

TOTAL HARMONIC DISTORTION vs FREQUENCY

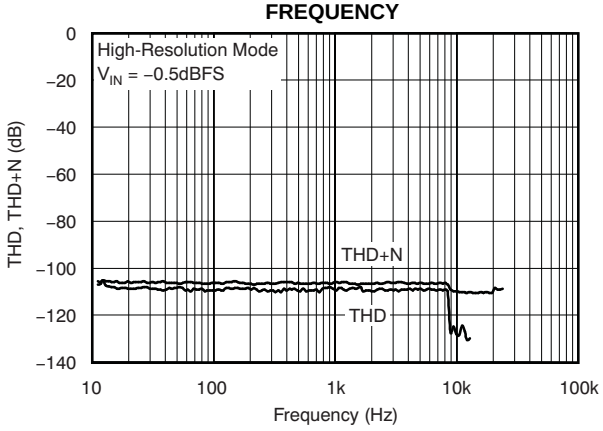


Figure 21.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

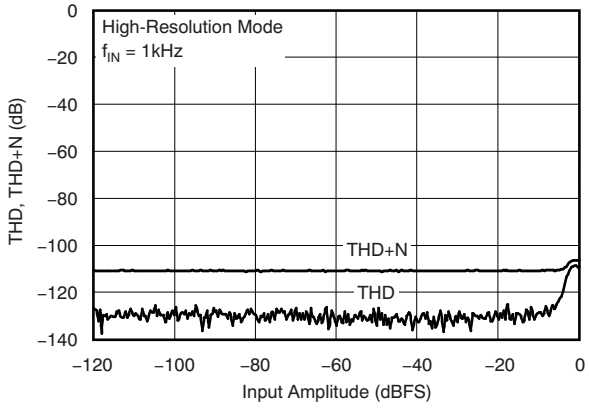


Figure 22.

TOTAL HARMONIC DISTORTION vs FREQUENCY

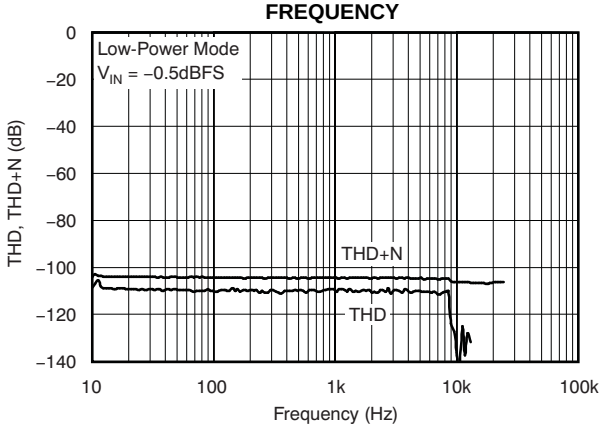


Figure 23.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

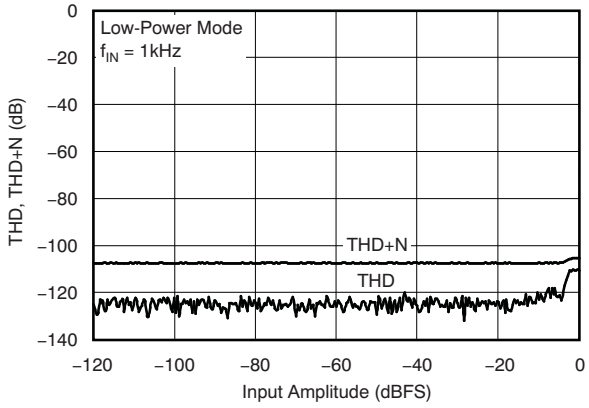


Figure 24.

TOTAL HARMONIC DISTORTION vs FREQUENCY

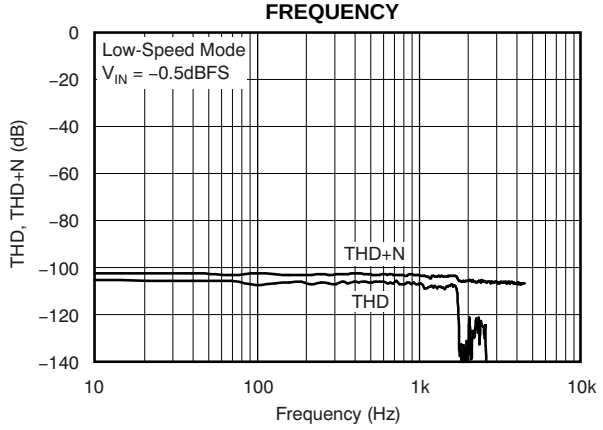


Figure 25.

TOTAL HARMONIC DISTORTION vs INPUT AMPLITUDE

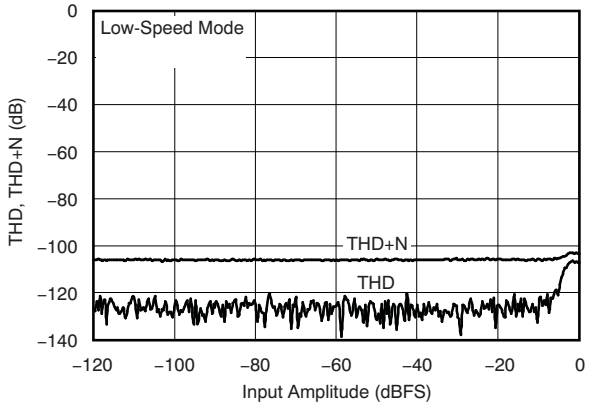


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

OFFSET DRIFT HISTOGRAM

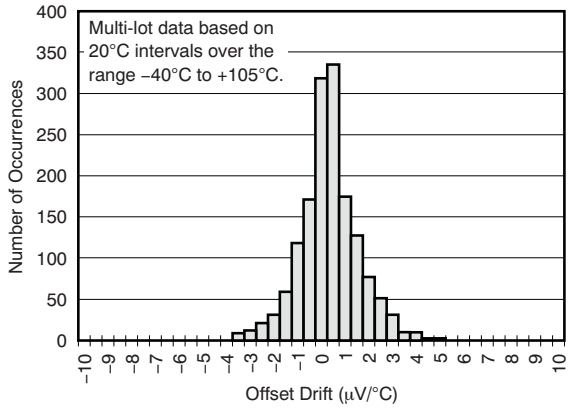


Figure 27.

GAIN DRIFT HISTOGRAM

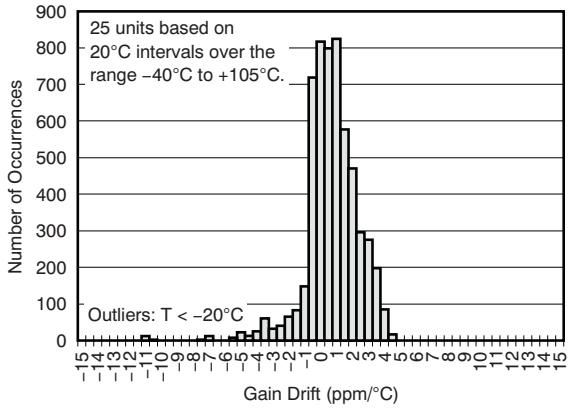


Figure 28.

OFFSET WARMUP DRIFT RESPONSE BAND

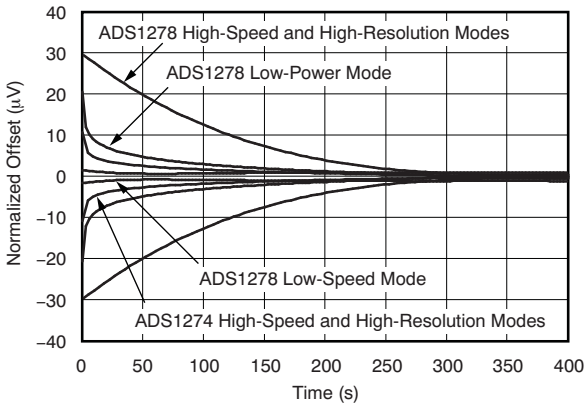


Figure 29.

GAIN WARMUP DRIFT RESPONSE BAND

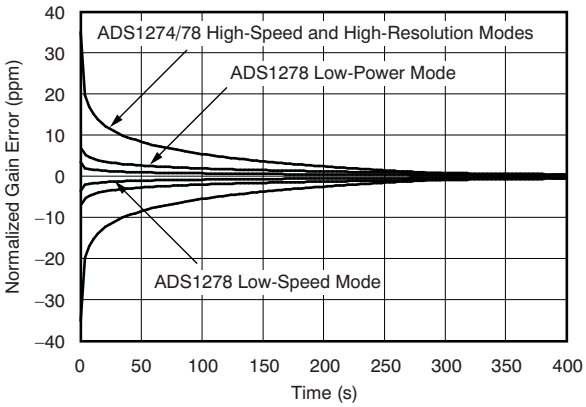


Figure 30.

OFFSET ERROR HISTOGRAM

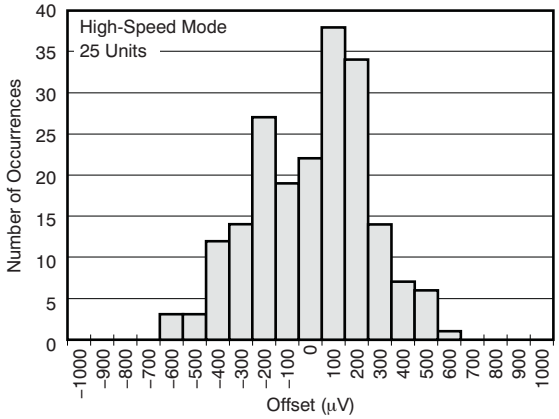


Figure 31.

GAIN ERROR HISTOGRAM

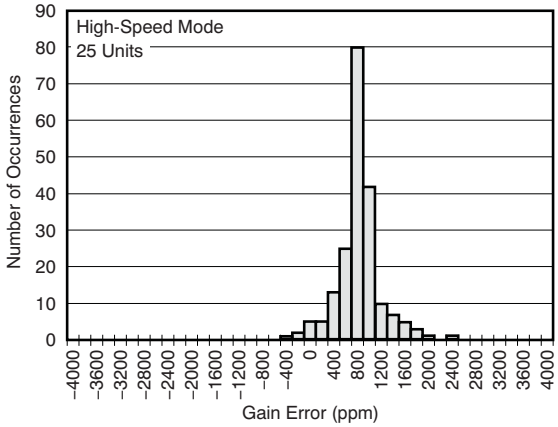


Figure 32.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

CHANNEL GAIN MATCH HISTOGRAM

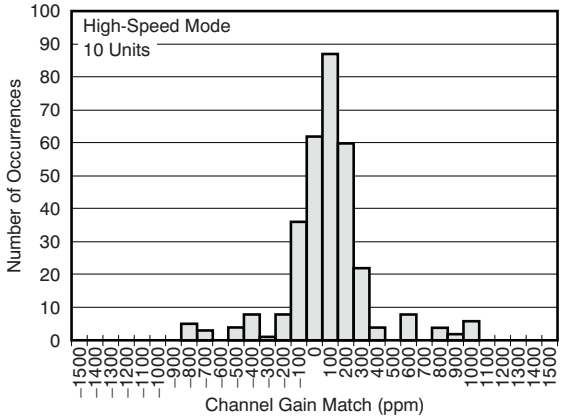


Figure 33.

CHANNEL OFFSET MATCH HISTOGRAM

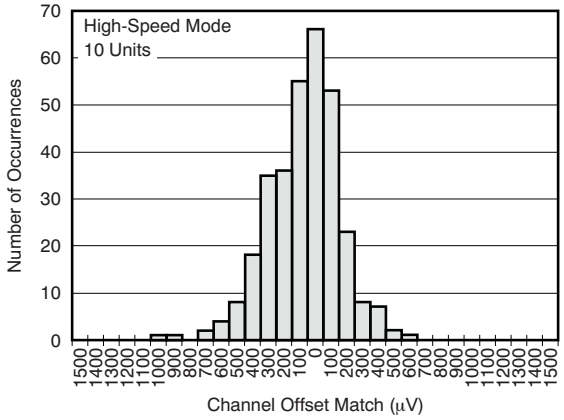


Figure 34.

OFFSET AND GAIN vs TEMPERATURE

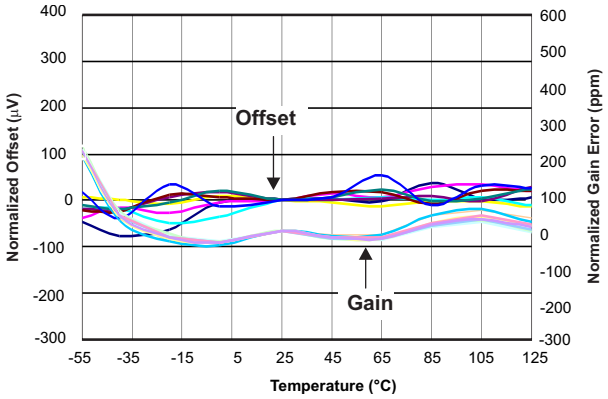


Figure 35.

VCOM VOLTAGE OUTPUT HISTOGRAM

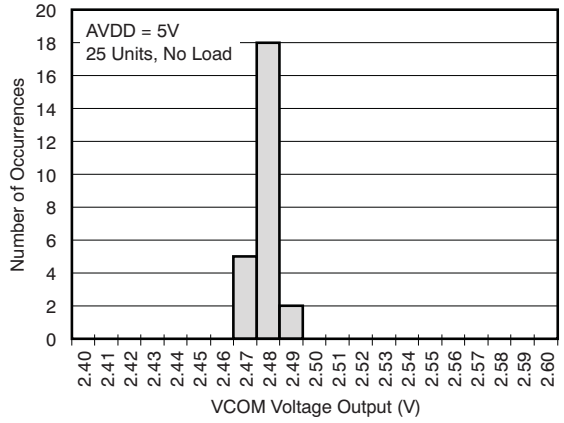


Figure 36.

SAMPLING MATCH ERROR HISTOGRAM

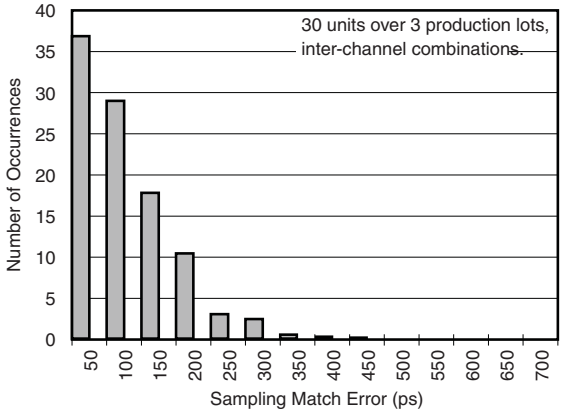


Figure 37.

REFERENCE INPUT DIFFERENTIAL IMPEDANCE vs TEMPERATURE

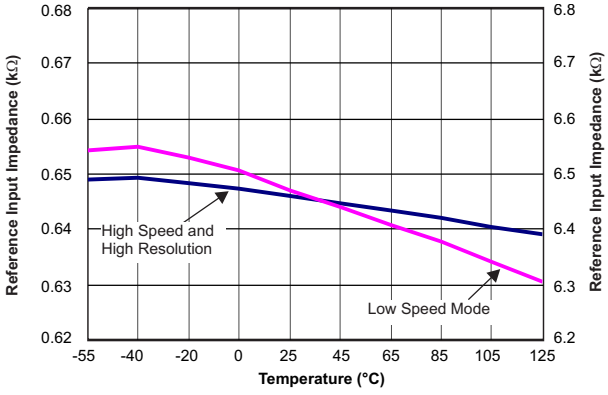


Figure 38.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

ANALOG INPUT DIFFERENTIAL IMPEDANCE vs TEMPERATURE

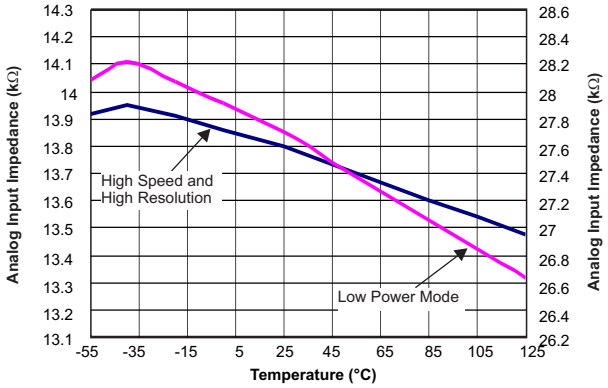


Figure 39.

ANALOG INPUT DIFFERENTIAL IMPEDANCE vs TEMPERATURE

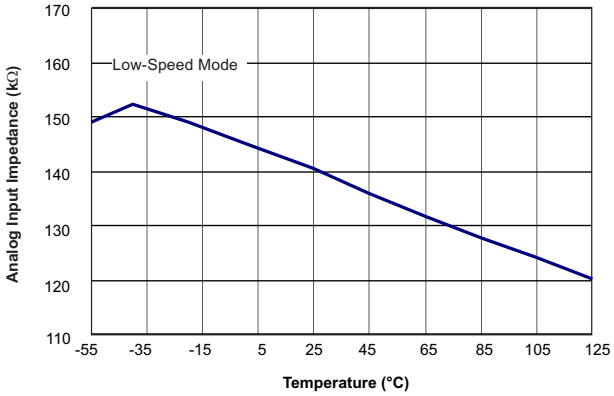


Figure 40.

INTEGRAL NONLINEARITY vs TEMPERATURE

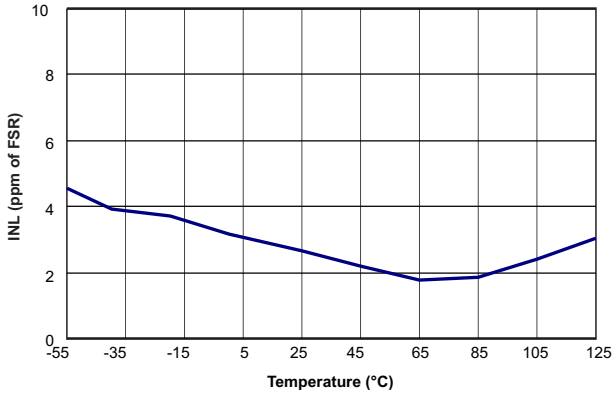


Figure 41.

LINEARITY ERROR vs INPUT LEVEL

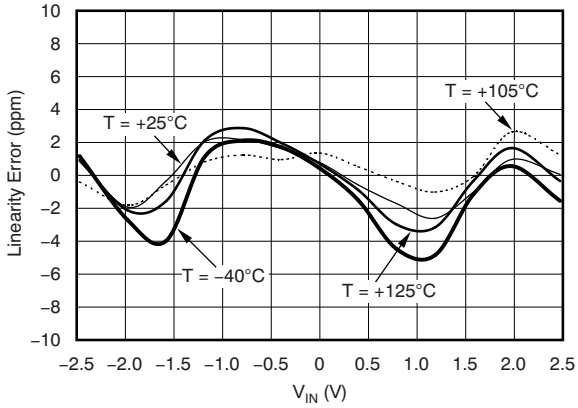


Figure 42.

LINEARITY AND TOTAL HARMONIC DISTORTION vs REFERENCE VOLTAGE

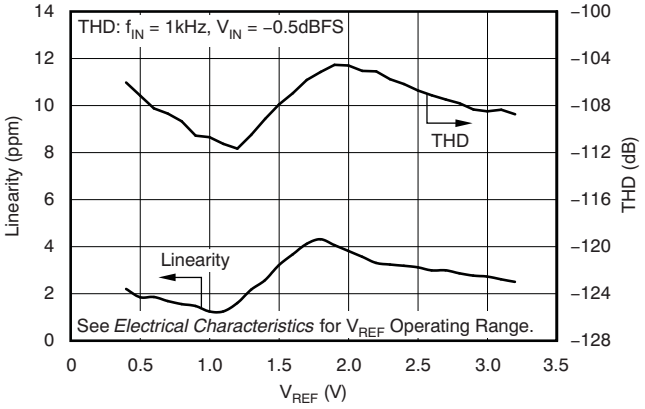


Figure 43.

NOISE AND LINEARITY vs INPUT COMMON-MODE VOLTAGE

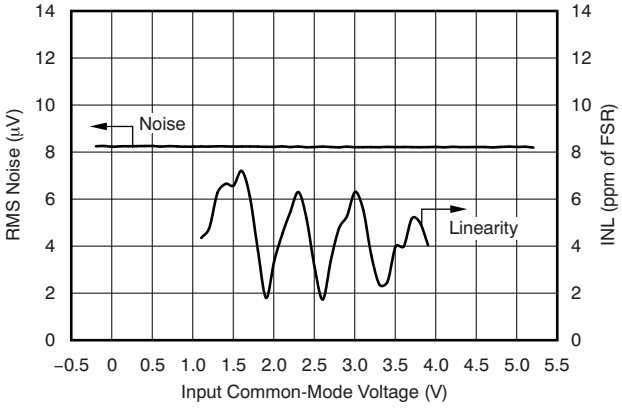


Figure 44.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

NOISE vs TEMPERATURE

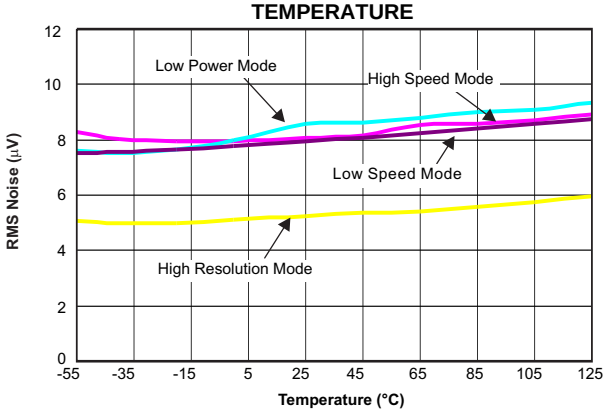


Figure 45.

NOISE vs REFERENCE VOLTAGE

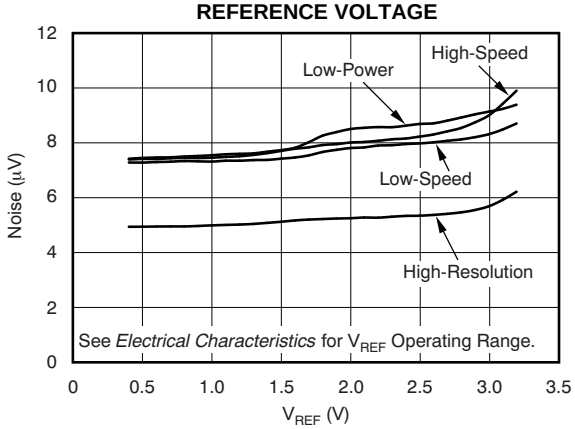


Figure 46.

TOTAL HARMONIC DISTORTION AND NOISE vs CLK

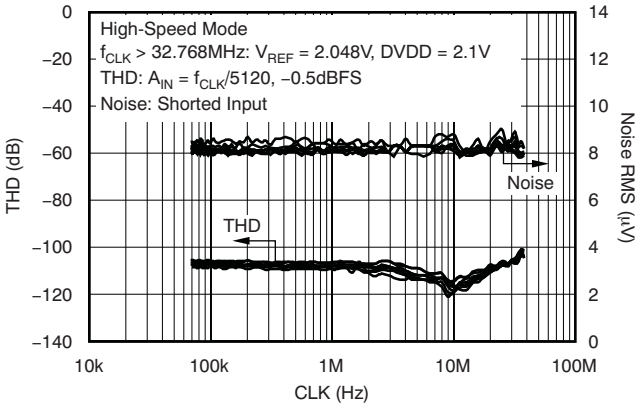


Figure 47.

COMMON-MODE REJECTION vs INPUT FREQUENCY

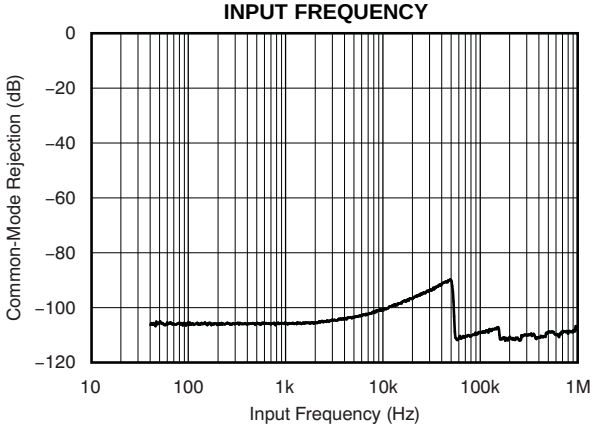


Figure 48.

POWER-SUPPLY REJECTION vs POWER-SUPPLY FREQUENCY

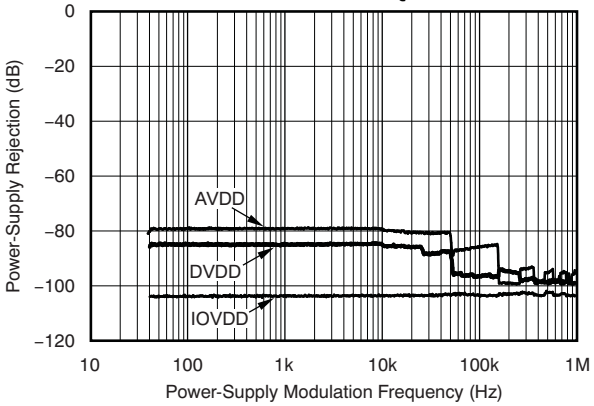


Figure 49.

AVDD CURRENT vs TEMPERATURE

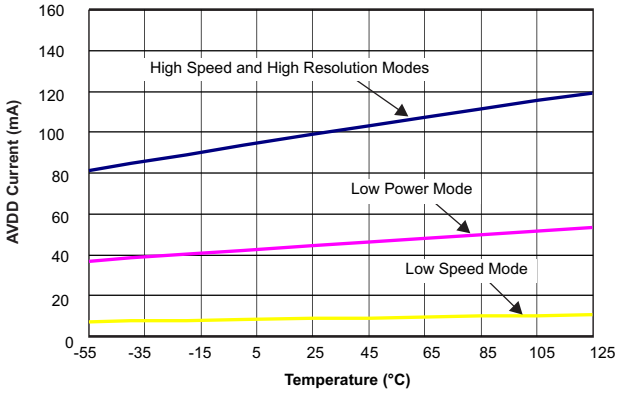


Figure 50.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, High-Speed mode, AVDD = 5 V, DVDD = 1.8 V, IOVDD = 3.3 V, f_{CLK} = 27 MHz, VREFP = 2.5 V, and VREFN = 0 V, unless otherwise noted.

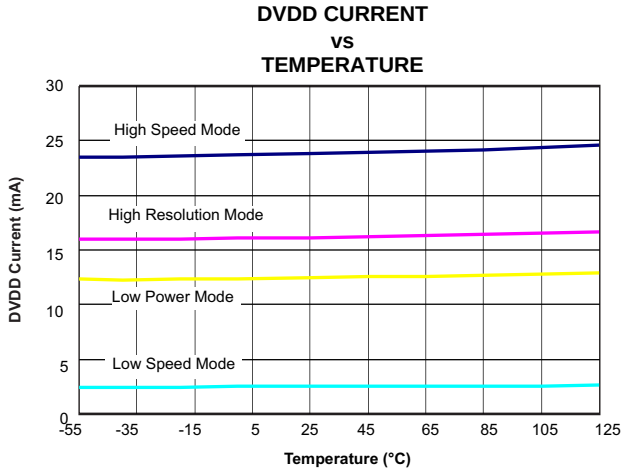


Figure 51.

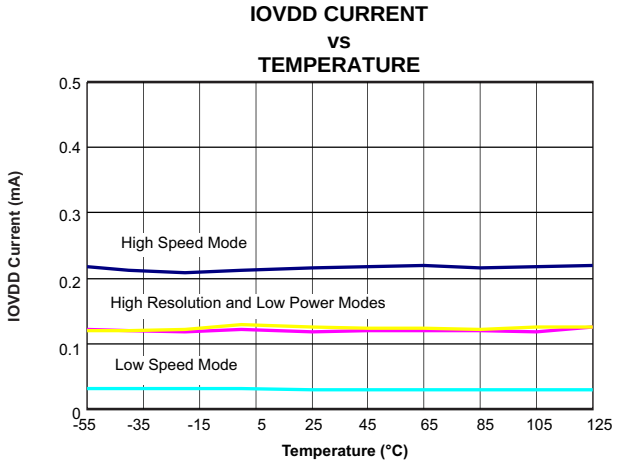


Figure 52.

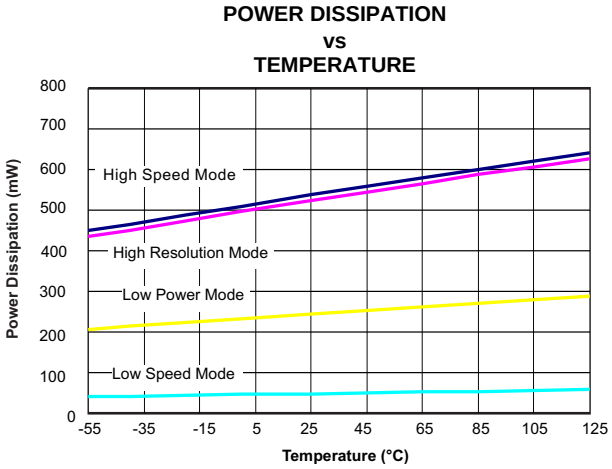


Figure 53.

OVERVIEW

The ADS1278 is an octal 24-bit, delta-sigma ADC based on the single-channel ADS1271. It offers the combination of outstanding dc accuracy and superior ac performance. Figure 54 shows the block diagram. The converter is comprised of eight advanced, 6th-order, chopper-stabilized, delta-sigma modulators followed by low-ripple, linear phase FIR filters. The modulators measure the differential input signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output. To allow tradeoffs among speed, resolution, and power, four operating modes are supported:

High-Speed, High-Resolution, Low-Power, and Low-Speed. Table 2 summarizes the performance of each mode.

In High-Speed mode, the maximum data rate is 128 kSPS (when operating at 128 kSPS, Frame-Sync format must be used). In High-Resolution mode, the SNR = 111dB (V_{REF} = 3.0 V); in Low-Power mode, the power dissipation is 31 mW/channel; and in Low-Speed mode, the power dissipation is only 7 mW/channel at 10.5 kSPS. The digital filters can be bypassed, enabling direct access to the modulator output.

The ADS1278 is configured by simply setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that supports both SPI and Frame-Sync formats. The ADS1278 has a daisy-chainable output and the ability to synchronize externally, so it can be used conveniently in systems requiring more than eight channels.

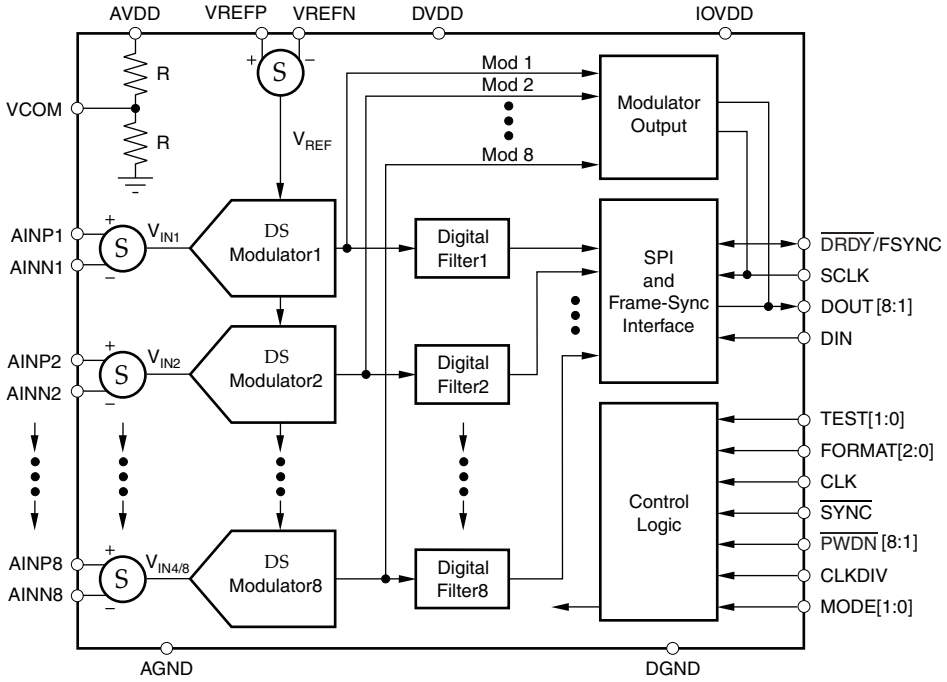


Figure 54. Block Diagram

Table 2. Operating Mode Performance Summary

MODE	MAX DATA RATE (SPS)	PASSBAND (kHz)	SNR (dB)	NOISE (μV_{RMS})	POWER/CHANNEL (mW)
High-Speed	128,000	57,984	106	8.5	70
High-Resolution	52,734	23,889	110	5.5	64
Low-Power	52,734	23,889	106	8.5	31
Low-Speed	10,547	4,798	107	8.0	7

FUNCTIONAL DESCRIPTION

The ADS1278 is a delta-sigma ADC consisting of eight independent converters that digitize eight input signals in parallel.

The converter is composed of two main functional blocks to perform the ADC conversions: the modulator and the digital filter. The modulator samples the input signal together with sampling the reference voltage to produce a 1s density output stream. The density of the output stream is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by the internal digital filter where the output conversion result is produced.

In operation, the input signal is sampled by the modulator at a high rate (typically 64x higher than the final output data rate). The quantization noise of the modulator is moved to a higher frequency range where the internal digital filter removes it. Oversampling results in very low levels of noise within the signal passband.

Since the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency is at the modulator sampling rate. This architecture greatly relaxes the requirement of external antialiasing filters because of the high modulator sampling rate.

SAMPLING APERTURE MATCHING

The ADS1278 converter operates from the same CLK input. The CLK input controls the timing of the modulator sampling instant. The converter is designed such that the sampling skew, or modulator sampling aperture match between channels, is controlled. Furthermore, the digital filters are synchronized to start the convolution phase at the same modulator clock cycle. This design results in excellent phase match among the ADS1278 channels.

Figure 37 shows the inter-device channel sample matching for the ADS1278.

FREQUENCY RESPONSE

The digital filter sets the overall frequency response. The filter uses a multi-stage FIR topology to provide linear phase with minimal passband ripple and high stop band attenuation. The filter coefficients are identical to the coefficients used in the ADS1271. The oversampling ratio of the digital filter (that is, the ratio of the modulator sampling to the output data rate, or f_{MOD}/f_{DATA}) is a function of the selected mode, as shown in Table 3.

Table 3. Oversampling Ratio versus Mode

MODE SELECTION	OVERSAMPLING RATIO (f_{MOD}/f_{DATA})
High-Speed	64
High-Resolution	128
Low-Power	64
Low-Speed	64

High-Speed, Low-Power, and Low-Speed Modes

The digital filter configuration is the same in High-Speed, Low-Power, and Low-Speed modes with the oversampling ratio set to 64. Figure 55 shows the frequency response in High-Speed, Low-Power, and Low-Speed modes normalized to f_{DATA}. Figure 56 shows the passband ripple. The transition from passband to stop band is shown in Figure 57. The overall frequency response repeats at 64x multiples of the modulator frequency f_{MOD}, as shown in Figure 58.

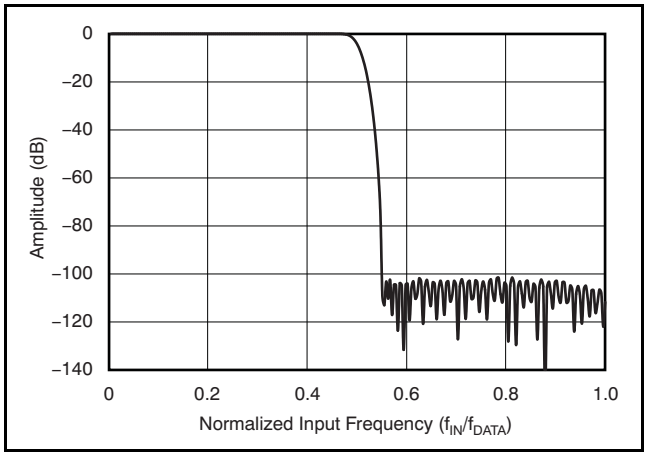


Figure 55. Frequency Response for High-Speed, Low-Power, and Low-Speed Modes

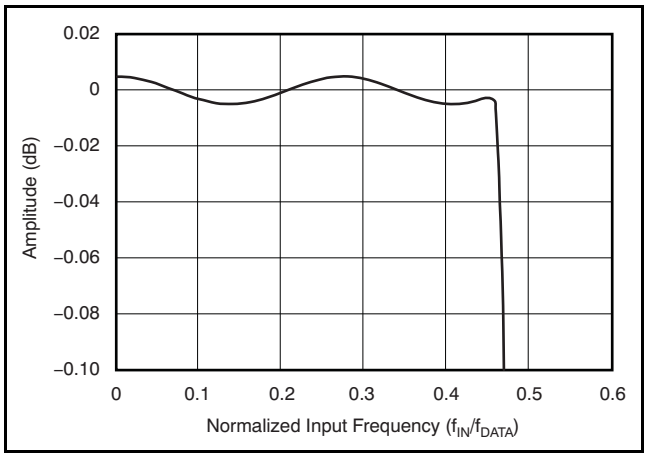


Figure 56. Passband Response for High-Speed, Low-Power, and Low-Speed Modes

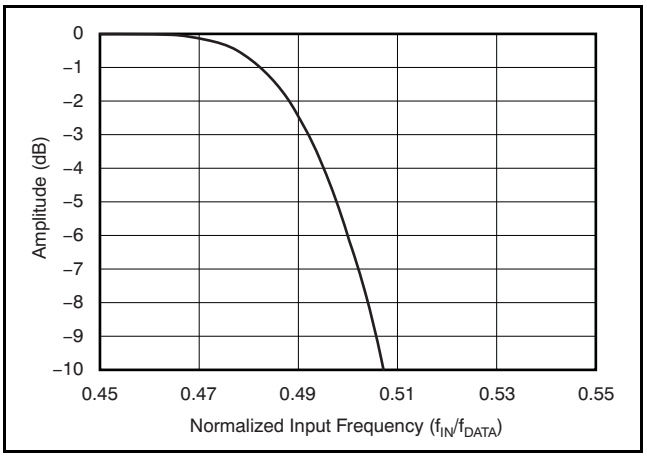


Figure 57. Transition Band Response for High-Speed, Low-Power, and Low-Speed Modes

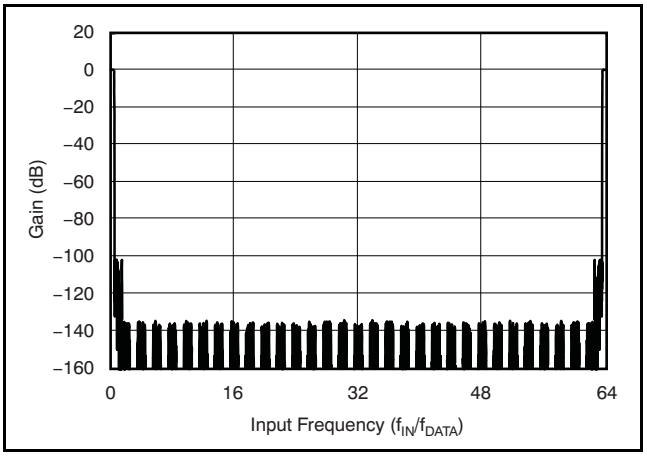


Figure 58. Frequency Response Out to f_{MOD} for High-Speed, Low-Power, and Low-Speed Modes

These image frequencies, if present in the signal and not externally filtered, will fold back (or alias) into the passband, causing errors. The stop band of the ADS1278 provides 100 dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1278 inputs is recommended to limit possible high-amplitude, out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 4 lists the image rejection versus external filter order.

Table 4. Antialiasing Filter Order Image Rejection

ANTIALIASING FILTER ORDER	IMAGE REJECTION (dB) (f_{-3dB} at f_{DATA})	
	HS, LP, LS	HR
1	39	45
2	75	87
3	111	129

High-Resolution Mode

The oversampling ratio is 128 in High-Resolution mode. Figure 59 shows the frequency response in High-Resolution mode normalized to f_{DATA}. Figure 60 shows the passband ripple, and the transition from passband to stop band is shown in Figure 61. The overall frequency response repeats at multiples of the modulator frequency f_{MOD} (128 × f_{DATA}), as shown in Figure 62. The stop band of the ADS1278 provides 100 dB attenuation of frequencies that begin just beyond the passband and continue out to f_{MOD}. Placing an antialiasing, low-pass filter in front of the ADS1278 inputs is recommended to limit possible high-amplitude out-of-band signals and noise. Often, a simple RC filter is sufficient. Table 4 lists the image rejection versus external filter order.

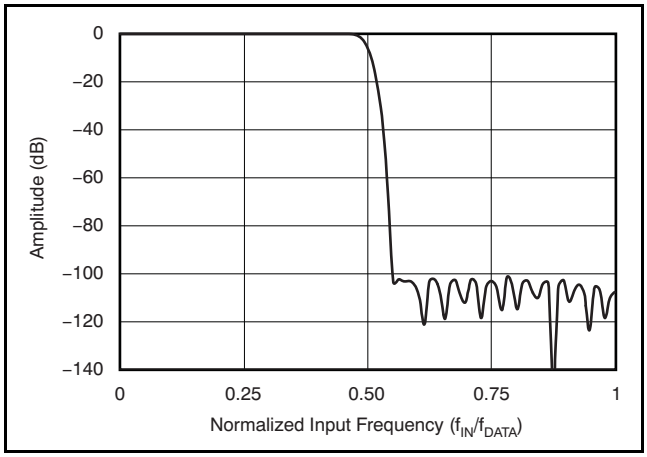


Figure 59. Frequency Response for High-Resolution Mode

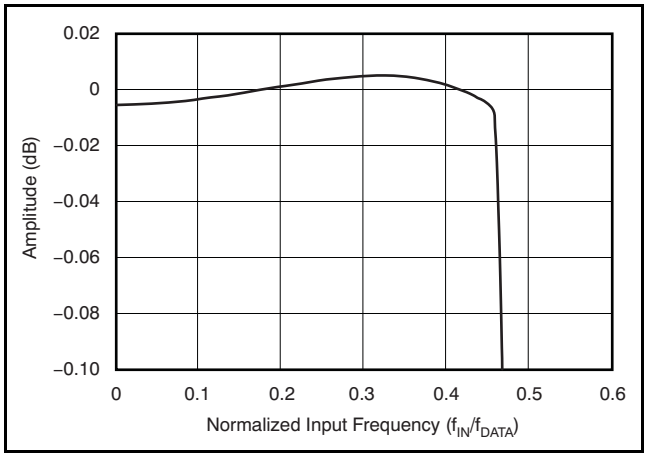


Figure 60. Passband Response for High-Resolution Mode

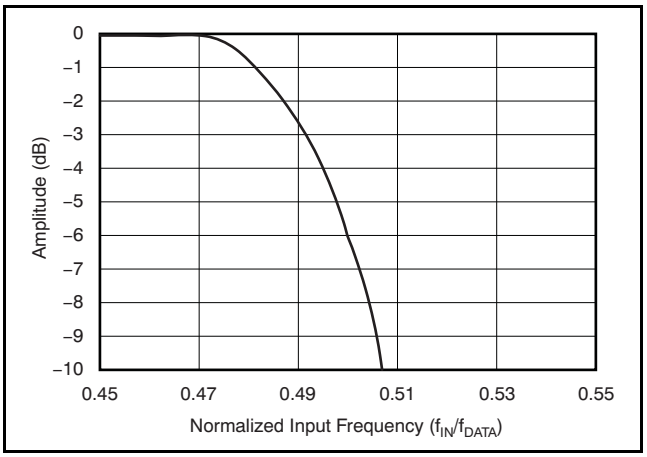


Figure 61. Transition Band Response for High-Resolution mode

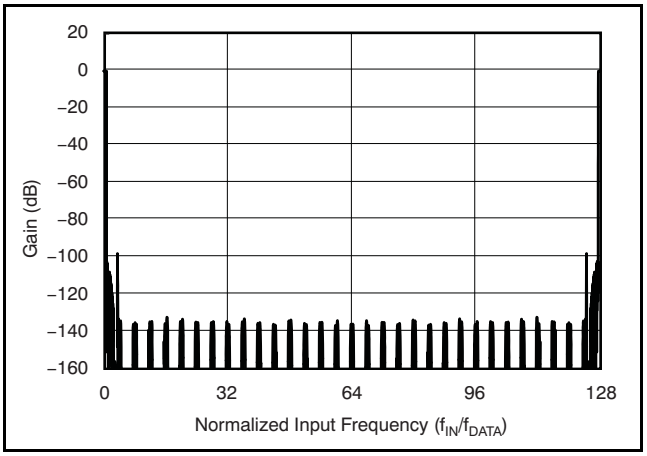


Figure 62. Frequency Response Out to f_{MOD} for High-Resolution Mode

PHASE RESPONSE

The ADS1278 incorporates a multiple stage, linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (constant group delay). This characteristic means the time delay from any instant of the input signal to the same instant of the output data is constant and is independent of input signal frequency. This behavior results in essentially zero phase errors when analyzing multi-tone signals.

SETTLING TIME

As with frequency and phase response, the digital filter also determines settling time. Figure 63 shows the output settling behavior after a step change on the analog inputs normalized to conversion periods. The X-axis is given in units of conversion. Note that after the step change on the input occurs, the output data change very little prior to 30 conversion periods. The output data are fully settled after 76 conversion periods for High-Speed and Low-Power modes, and 78 conversion periods for High-Resolution mode.

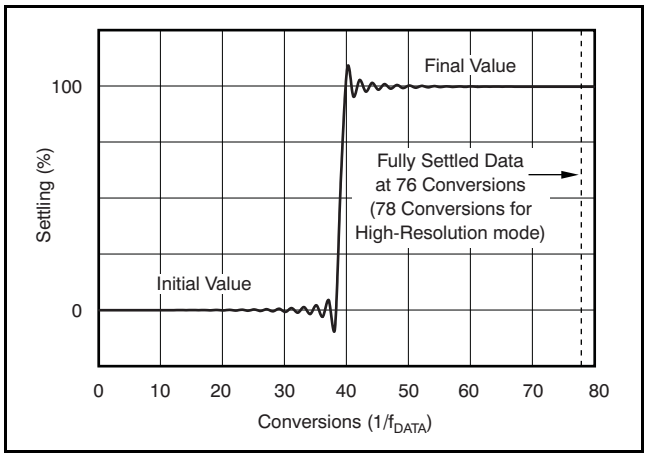


Figure 63. Step Response

DATA FORMAT

The ADS1278 outputs 24 bits of data in twos complement format.

A positive full-scale input produces an ideal output code of 7FFFFFh, and the negative full-scale input produces an ideal output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 5 summarizes the ideal output codes for different input signals.

Table 5. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ $+V_{REF}$	7FFFFFh
$\frac{+V_{REF}}{2^{23}-1}$	000001h
0	000000h
$\frac{-V_{REF}}{2^{23}-1}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

ANALOG INPUTS (AINP, AINN)

The ADS1278 measures each differential input signal V_{IN} = (AINP – AINN) against the common differential reference V_{REF} = (VREFP – VREFN). The most positive measurable differential input is $+V_{REF}$, which produces the most positive digital output code of 7FFFFFh. Likewise, the most negative measurable differential input is $–V_{REF}$, which produces the most negative digital output code of 800000h.

For optimum performance, the inputs of the ADS1278 are intended to be driven differentially. For single-ended applications, one of the inputs (AINP or AINN) can be driven while the other input is fixed (typically to AGND or 2.5 V). Fixing the input to 2.5 V permits bipolar operation, thereby allowing full use of the entire converter range.

While the ADS1278 measures the differential input signal, the absolute input voltage is also important. This value is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

–0.1 V < (AINN or AINP) < AVDD + 0.1 V

If either input is taken below –0.4 V or above (AVDD + 0.4 V), ESD protection diodes on the inputs may turn on. If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

The ADS1278 is a very high-performance ADC. For optimum performance, it is critical that the appropriate circuitry be used to drive the ADS1278 inputs. See the *Application Information* section for several recommended circuits.

The ADS1278 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged. Figure 64 shows a conceptual diagram of these circuits. Switch S_2 represents the net effect of the modulator circuitry in discharging the sampling capacitor; the actual implementation is different. The timing for switches S_1 and S_2 is shown in Figure 65. The sampling time (t_{SAMPLE}) is the inverse of modulator sampling frequency (f_{MOD}) and is a function of the mode, the CLKDIV input, and CLK frequency, as shown in Table 6.

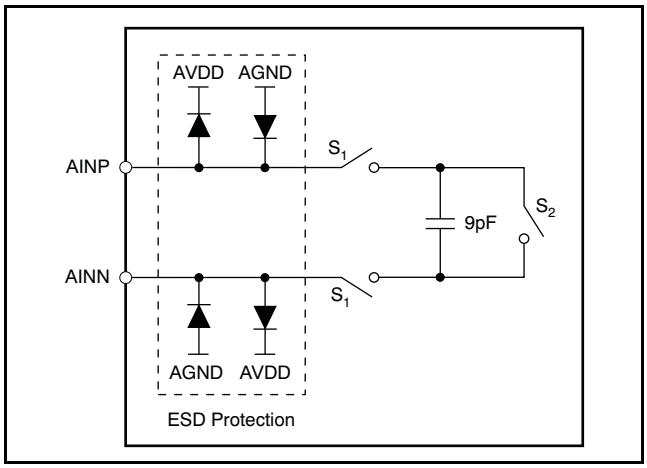


Figure 64. Equivalent Analog Input Circuitry

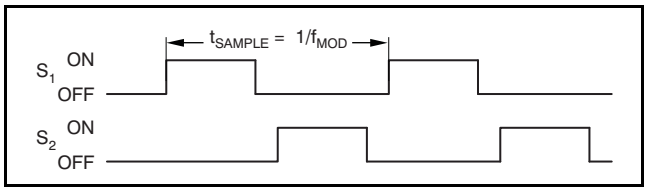


Figure 65. S_1 and S_2 Switch Timing for Figure 64

Table 6. Modulator Frequency (f_{MOD}) Mode Selection

MODE SELECTION	CLKDIV	f_{MOD}
High-Speed	1	$f_{CLK}/4$
High-Resolution	1	$f_{CLK}/4$
Low-Power	1	$f_{CLK}/8$
	0	$f_{CLK}/4$
Low-Speed	1	$f_{CLK}/40$
	0	$f_{CLK}/8$

The average load presented by the switched capacitor input can be modeled with an effective differential impedance, as shown in Figure 66. Note that the effective impedance is a function of f_{MOD}.

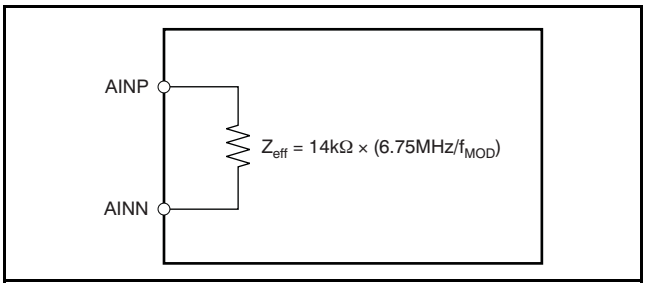


Figure 66. Effective Input Impedances

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1278 ADC is the differential voltage between VREFP and VREFN: V_{REF} = (VREFP – VREFN). The voltage reference is common to all channels. The reference inputs use a structure similar to that of the analog inputs with the equivalent circuitry on the reference inputs shown in Figure 67. As with the analog inputs, the load presented by the switched capacitor can be modeled with an effective impedance, as shown in Figure 68. However, the reference input impedance depends on the number of active (enabled) channels in addition to f_{MOD}. As a result of the change of reference input impedance caused by enabling and disabling channels, the regulation and setting time of the external reference should be noted, so as not to affect the readings.

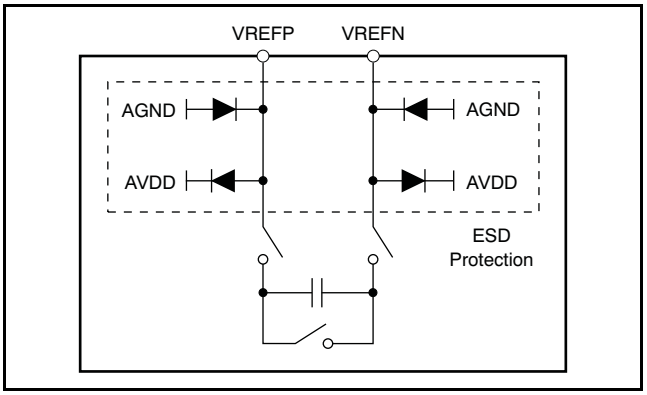


Figure 67. Equivalent Reference Input Circuitry

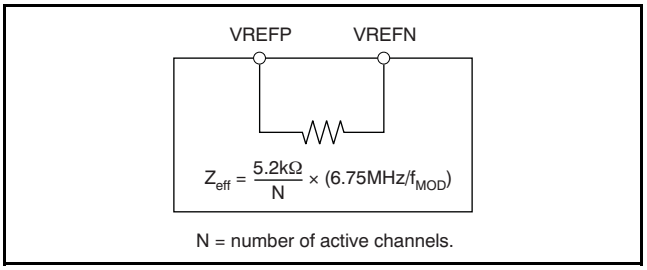


Figure 68. Effective Reference Impedance

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.4 V, and likewise do not exceed AVDD by 0.4 V. If these conditions are possible, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table).

Note that the valid operating range of the reference inputs is limited to the following parameters:

–0.1 V ≤ VREFN ≤ +0.1 V

VREFN + 0.5 V ≤ VREFP ≤ AVDD + 0.1 V

CLOCK INPUT (CLK)

The ADS1278 requires a clock input for operation. The individual converters of the ADS1278 operate from the same clock input. At the maximum data rate, the clock input can be either 27 MHz or 13.5 MHz for Low-Power mode, or 2 7MHz or 5.4 MHz for Low-Speed mode, determined by the setting of the CLKDIV input. For High-Speed mode, the maximum CLK input frequency is 32.768 MHz. For High-Resolution mode, the maximum CLK input frequency is 27 MHz. The selection of the external clock frequency (f_{CLK}) does not affect the resolution of the ADS1278. Use of a slower f_{CLK} can reduce the power consumption of an external clock buffer. The output data rate scales with clock frequency, down to a minimum clock frequency of f_{CLK} = 100 kHz. Table 7 summarizes the ratio of the clock input frequency (f_{CLK}) to data rate (f_{DATA}), maximum data rate and corresponding maximum clock input for the four operating modes.

As with any high-speed data converter, a high-quality, low-jitter clock is essential for optimum performance. Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input; keeping the clock trace as short as possible, and using a 50-Ω series resistor placed close to the source end, often helps.

Table 7. Clock Input Options

MODE SELECTION	MAX f_{CLK} (MHz)	CLKDIV	f_{CLK}/f_{DATA}	DATA RATE (SPS)
High-Speed	32.768	1	256	128,000
High-Resolution	27	1	512	52,734
Low-Power	27	1	512	52,734
	13.5	0	256	
Low-Speed	27	1	2,560	10,547
	5.4	0	512	

MODE SELECTION (MODE)

The ADS1278 supports four modes of operation: High-Speed, High-Resolution, Low-Power, and Low-Speed. The modes offer optimization of speed, resolution, and power. Mode selection is determined by the status of the digital input MODE[1:0] pins, as shown in Table 8. The ADS1278 continually monitors the status of the MODE pin during operation.

Table 8. Mode Selection

MODE[1:0]	MODE SELECTION	MAX f_{DATA} (1)
00	High-Speed	128,000
01	High-Resolution	52,734
10	Low-Power	52,734
11	Low-Speed	10,547

(1) f_{CLK} = 27 MHz max (32.768MHz max in High-Speed mode).

When using the SPI protocol, $\overline{DRDY}$ is held high after a mode change occurs until settled (or valid) data are ready; see Figure 69 and Table 9.

In Frame-Sync protocol, the DOUT pins are held low after a mode change occurs until settled data are ready; see Figure 69 and Table 9. Data can be read from the device to detect when DOUT changes to logic 1, indicating that the data are valid.

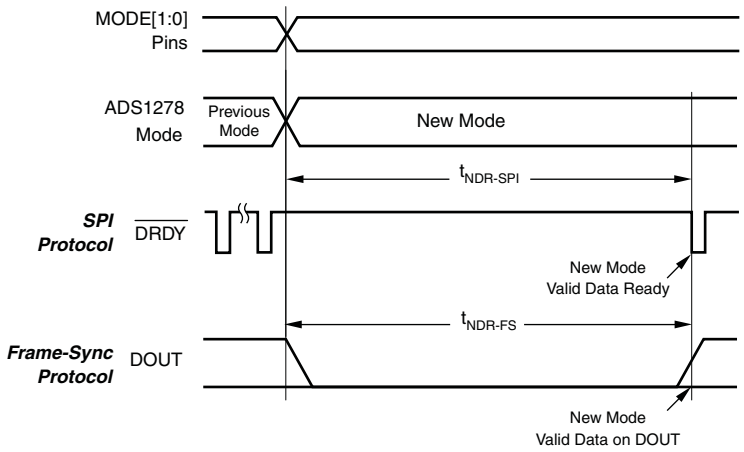


Figure 69. Mode Change Timing

Table 9. New Data After Mode Change

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{NDR-SPI}$	Time for new data to be ready (SPI)			129	Conversions ($1/f_{DATA}$)
t_{NDR-FS}	Time for new data to be ready (Frame-Sync)	127		128	Conversions ($1/f_{DATA}$)

SYNCHRONIZATION ($\overline{SYNC}$)

The ADS1278 can be synchronized by pulsing the $\overline{SYNC}$ pin low and then returning the pin high. When the pin goes low, the conversion process stops, and the internal counters used by the digital filter are reset. When the $\overline{SYNC}$ pin returns high, the conversion process restarts. Synchronization allows the conversion to be aligned with an external event, such as the changing of an external multiplexer on the analog inputs, or by a reference timing pulse.

Because the ADS1278 converters operate in parallel from the same master clock and use the same $\overline{SYNC}$ input control, they are always in synchronization with each other. The aperture match among internal channels is typically less than 500 ps. However, the synchronization of multiple devices is somewhat different. At device power-on, variations in internal reset thresholds from device to device may result in uncertainty in conversion timing.

The $\overline{SYNC}$ pin can be used to synchronize multiple devices to within the same CLK cycle. Figure 70 illustrates the timing requirement of $\overline{SYNC}$ and CLK in SPI format.

See Figure 71 for the Frame-Sync format timing requirement.

After synchronization, indication of valid data depends on whether SPI or Frame-Sync format was used.

In the SPI format, $\overline{DRDY}$ goes high as soon as $\overline{SYNC}$ is taken low; see Figure 70. After $\overline{SYNC}$ is returned high, $\overline{DRDY}$ stays high while the digital filter is settling. Once valid data are ready for retrieval, $\overline{DRDY}$ goes low.

In the Frame-Sync format, DOUT goes low as soon as $\overline{SYNC}$ is taken low; see Figure 71. After $\overline{SYNC}$ is returned high, DOUT stays low while the digital filter is settling. Once valid data are ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking $\overline{SYNC}$ high, and must then remain running. If the clock inputs (CLK, FSYNC or SCLK) are subsequently interrupted or reset, re-assert the $\overline{SYNC}$ pin.

For consistent performance, re-assert $\overline{SYNC}$ after device power-on when data first appear.

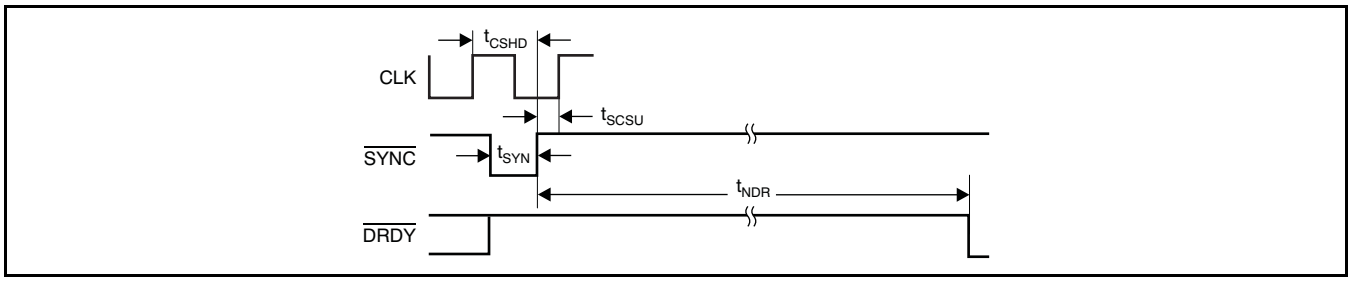


Figure 70. Synchronization Timing (SPI Protocol)

Table 10. SPI Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{SYNC}$ hold time	10			ns
t_{SCSU}	$\overline{SYNC}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready			129	Conversions ($1/f_{DATA}$)

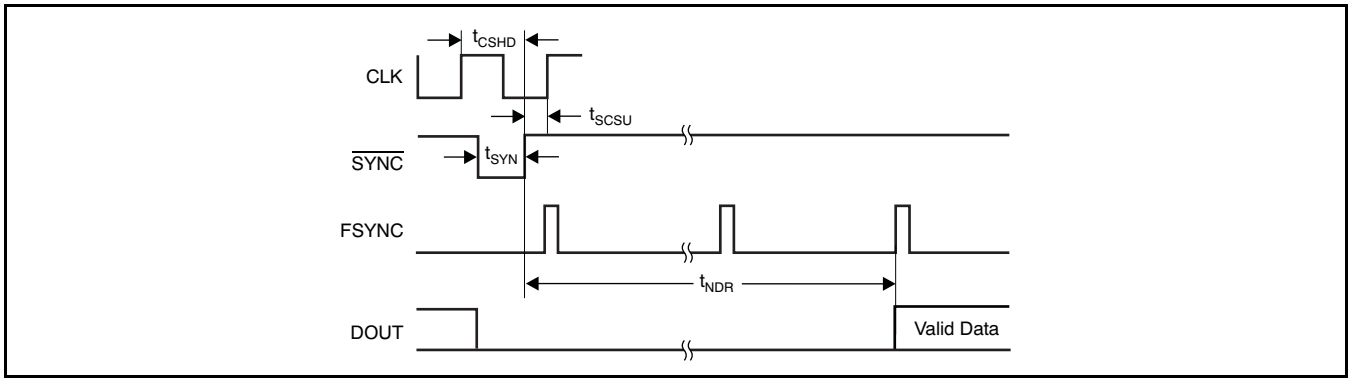


Figure 71. Synchronization Timing (Frame-Sync Protocol)

Table 11. Frame-Sync Protocol

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CSHD}	CLK to $\overline{SYNC}$ hold time	10			ns
t_{SCSU}	$\overline{SYNC}$ to CLK setup time	5			ns
t_{SYN}	Synchronize pulse width	1			CLK periods
t_{NDR}	Time for new data to be ready	127		128	Conversions ($1/f_{DATA}$)

POWER-DOWN (PWDN)

The channels of the ADS1278 can be independently powered down by use of the PWDN inputs. To enter the power-down mode, hold the respective PWDN pin low for at least two CLK cycles. To exit power-down, return the corresponding PWDN pin high. Note that when all channels are powered down, the ADS1278 enters a microwatt (μW) power state where all internal biasing is disabled. In this state, the TEST[1:0] input pins must be driven; all other input pins can float. The ADS1278 outputs remain driven.

As shown in Figure 72 and Table 12, a maximum of 130 conversion cycles must elapse for SPI interface, and 129 conversion cycles must elapse for Frame-Sync, before reading data after exiting power-down. Data from channels already running are not affected. The user software can perform the required delay time in any of the following ways:

1. Count the number of data conversions after taking the PWDN pin high.
2. Delay 129/f_{DATA} or 130/f_{DATA} after taking the PWDN pins high, then read data.
3. Detect for non-zero data in the powered-up channel.

After powering up one or more channels, the channels are synchronized to each other. It is not necessary to use the SYNC pin to synchronize them.

When a channel is powered down in TDM data format, the data for that channel are either forced to zero (fixed-position TDM data mode) or replaced by shifting the data from the next channel into the vacated data position (dynamic-position TDM data mode).

In Discrete data format, the data are always forced to zero. When powering-up a channel in dynamic-position TDM data format mode, the channel data remain packed until the data are ready, at which time the data frame is expanded to include the just-powered channel data. See the *Data Format* section for details.

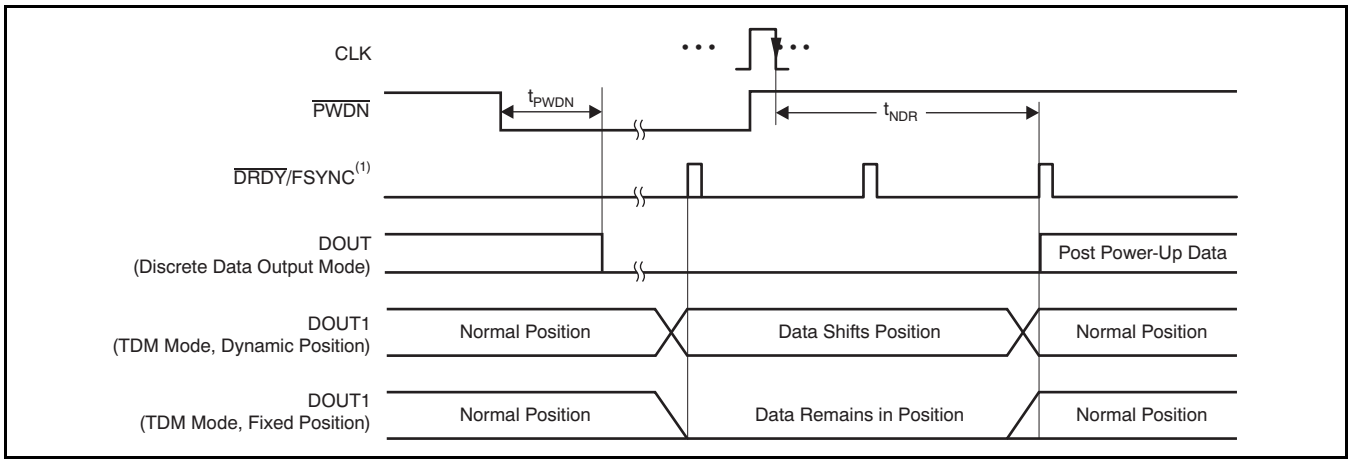


Figure 72. Power-Down Timing

Table 12. Power-Down Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PWDN}	PWDN pulse width to enter Power-Down mode	2			CLK periods
t_{NDR}	Time for new data ready (SPI)	129		130	Conversions (1/f_{DATA})
t_{NDR}	Time for new data ready (Frame-Sync)	128		129	Conversions (1/f_{DATA})

FORMAT[2:0]

Data can be read from the ADS1278 with two interface protocols (SPI or Frame-Sync) and several options of data formats (TDM/Discrete and Fixed/Dynamic data positions). The FORMAT[2:0] inputs are used to select among the options. Table 13 lists the available options. See the *DOUT Modes* section for details of the DOUT Mode and Data Position.

Table 13. Data Output Format

FORMAT[2:0]	INTERFACE PROTOCOL	DOUT MODE	DATA POSITION
000	SPI	TDM	Dynamic
001	SPI	TDM	Fixed
010	SPI	Discrete	—
011	Frame-Sync	TDM	Dynamic
100	Frame-Sync	TDM	Fixed
101	Frame-Sync	Discrete	—
110	Modulator Mode	—	—

SERIAL INTERFACE PROTOCOLS

Data are retrieved from the ADS1278 using the serial interface. Two protocols are available: SPI and Frame-Sync. The same pins are used for both interfaces: SCLK, $\overline{\text{DRDY}}$/FSYNC, DOUT[8:1], and DIN. The FORMAT[2:0] pins select the desired interface protocol.

SPI SERIAL INTERFACE

The SPI-compatible format is a read-only interface. Data ready for retrieval are indicated by the falling $\overline{\text{DRDY}}$ output and are shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple devices. See the *Daisy-Chaining* section for more information.

NOTE: The SPI format is limited to a CLK input frequency of 27 MHz, maximum. For CLK input operation above 27 MHz (High-Speed mode only), use Frame-Sync format.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user normally shifts this data in on the rising edge.

Even though the SCLK input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data.

SCLK may be run as fast as the CLK frequency. SCLK may be either in free-running or stop-clock operation between conversions. Note that one f_{CLK} is required after the falling edge of $\overline{\text{DRDY}}$ until the first rising edge of SCLK. For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

$\overline{\text{DRDY}}$/FSYNC (SPI Format)

In the SPI format, this pin functions as the $\overline{\text{DRDY}}$ output. It goes low when data are ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data are not retrieved (that is, SCLK is held low), $\overline{\text{DRDY}}$ pulses high just before the next conversion data are ready, as shown in Figure 73. The new data are loaded within one CLK cycle before $\overline{\text{DRDY}}$ goes low. All data must be shifted out before this time to avoid being overwritten.

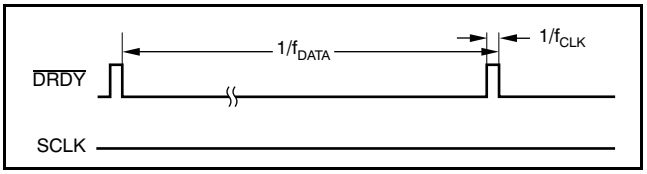


Figure 73. $\overline{\text{DRDY}}$ Timing with No Readback

DOUT

The conversion data are output on DOUT[8:1]. The MSB data are valid on DOUT[8:1] after $\overline{\text{DRDY}}$ goes low. Subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT after all channel data have been shifted out. When the device is configured for modulator output, DOUT[8:1] becomes the modulator data output for each channel (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1278s are to be daisy-chained together. The DOUT1 pin of the first device connects to the DIN pin of the next, etc. It can be used with either the SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278, tie DIN low. See the *Daisy-Chaining* section for more information.

FRAME-SYNC SERIAL INTERFACE

Frame-Sync format is similar to the interface often used on audio ADCs. It operates in slave fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data are output MSB first or *left-justified* on the rising edge of FSYNC. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the relationships shown in the Frame-Sync Timing Requirements.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously. If it is shut down, the data readback will be corrupted. The number of SCLKs within a frame period (FSYNC clock) can be any power-of-2 ratio of CLK cycles (1, 1/2, 1/4, etc), as long as the number of cycles is sufficient to shift the data output from all channels within one frame. When the device is configured for modulator output, SCLK becomes the modulator clock output (see the *Modulator Output* section).

$\overline{\text{DRDY}}$/FSYNC (Frame-Sync Format)

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period, which must be the same as the data rate. The required number of f_{CLK} cycles to each FSYNC period depends on the mode selection and the CLKDIV input. Table 7 indicates the number of CLK cycles to each frame (f_{CLK}/f_{DATA}). If the FSYNC period is not the proper value, data readback will be corrupted.

DOUT

The conversion data are shifted out on DOUT[8:1]. The MSB data become valid on DOUT[8:1] after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT[8:1] after all channel data have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output (see the *Modulator Output* section).

DIN

This input is used when multiple ADS1278s are to be daisy-chained together. It can be used with either SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one ADS1278, tie DIN low. See the *Daisy-Chaining* section for more information.

DOUT MODES

For both SPI and Frame-Sync interface protocols, the data are shifted out either through individual channel DOUT pins, in a parallel data format (Discrete mode), or the data for all channels are shifted out, in a serial format, through a common pin, DOUT1 (TDM mode).

TDM Mode

In TDM (time-division multiplexed) data output mode, the data for all channels are shifted out, in sequence, on a single pin (DOUT1). As shown in Figure 74, the data from channel 1 are shifted out first, followed by channel 2 data, etc. After the data from the last channel are shifted out, the data from the DIN input follow. The DIN is used to daisy-chain the data output from an additional ADS1278 or other compatible device. Note that when all channels of the ADS1278 are disabled, the interface is disabled, rendering the DIN input disabled as well. When one or more channels of the device are powered down, the data format of the TDM mode can be fixed or dynamic.

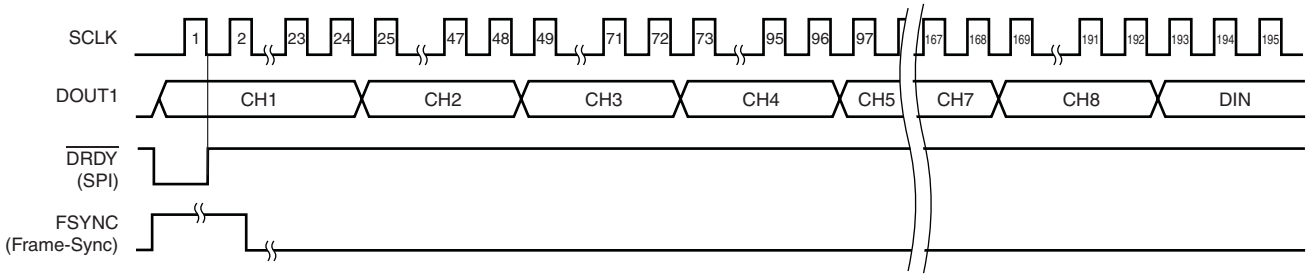


Figure 74. TDM Mode (All Channels Enabled)

TDM Mode, Fixed-Position Data

In this TDM data output mode, the data position of the channels remain fixed, regardless of whether the channels are powered down. If a channel is powered down, the data are forced to zero but occupy the same position within the data stream. Figure 75 shows the data stream with channel 1 and channel 3 powered down.

TDM Mode, Dynamic Position Data

In this TDM data output mode, when a channel is powered down, the data from higher channels shift one position in the data stream to fill the vacated data slot. Figure 76 shows the data stream with channel 1 and channel 3 powered down.

Discrete Data Output Mode

In Discrete data output mode, the channel data are shifted out in parallel using individual channel data output pins DOUT[8:1]. After the 24th SCLK, the channel data are forced to zero. The data are also forced to zero for powered down channels. Figure 77 shows the discrete data output format.

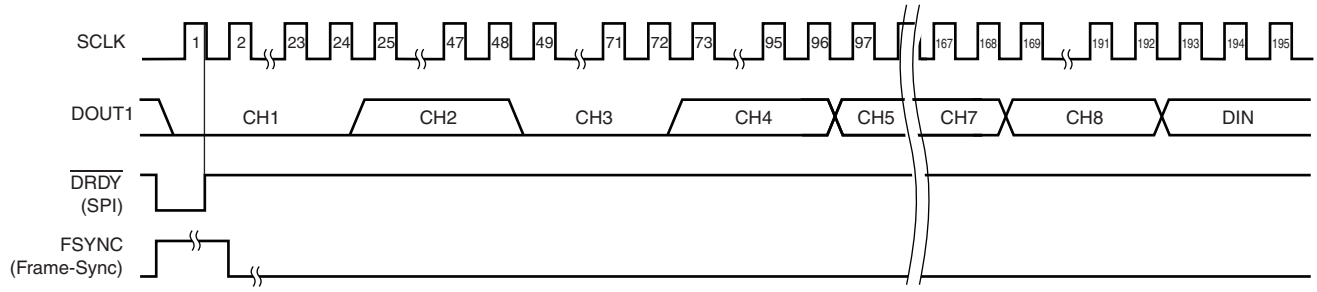


Figure 75. TDM Mode, Fixed-Position Data (Channels 1 and 3 Shown Powered Down)

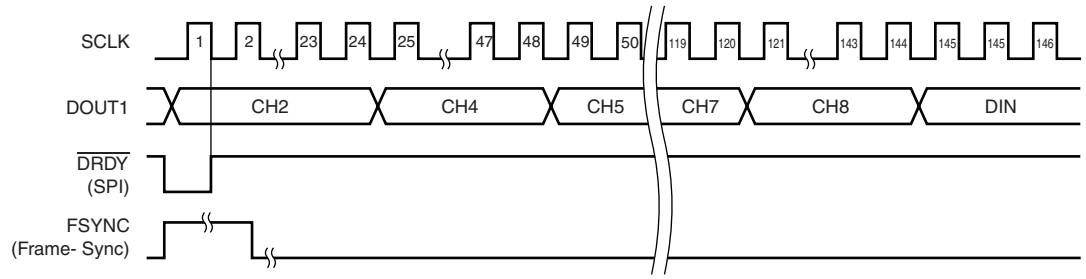


Figure 76. TDM Mode, Dynamic Position Data (Channels 1 and 3 Shown Powered Down)

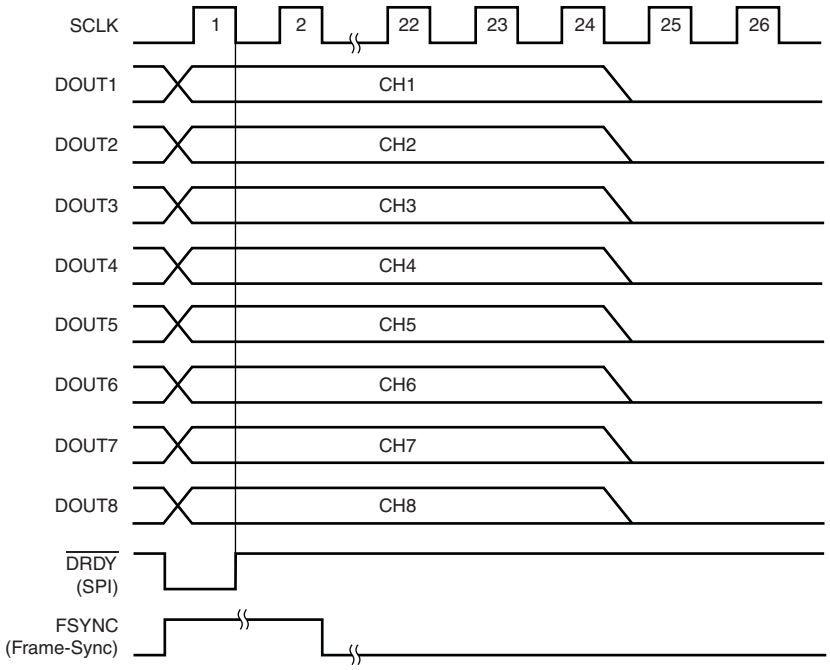


Figure 77. Discrete Data Output Mode

DAISY-CHAINING

Multiple ADS1278s can be daisy-chained together to output data on a single pin. The DOUT1 data output pin of one device is connected to the DIN of the next device. As shown in Figure 78, the DOUT1 pin of device 1 provides the output data to a controller, and the DIN of device 2 is grounded. Figure 79 shows the data format when reading back data.

The maximum number of channels that may be daisy-chained in this way is limited by the frequency of f_{SCLK}, the mode selection, and the CLKDIV input. The frequency of f_{SCLK} must be high enough to completely shift the data out from all channels within one f_{DATA} period. Table 14 lists the maximum number of daisy-chained channels when $f_{SCLK} = f_{CLK}$.

To increase the number of data channels possible in a chain, a segmented DOUT scheme may be used, producing two data streams. Figure 80 illustrates four ADS1278s, with pairs of ADS1278s daisy-chained together. The channel data of each daisy-chained pair are shifted out in parallel and received by the processor through independent data channels.

Table 14. Maximum Channels in a Daisy-Chain

Table 14. Maximum Channels in a Daisy-Chain ($f_{SCLK} = f_{CLK}$) (continued)

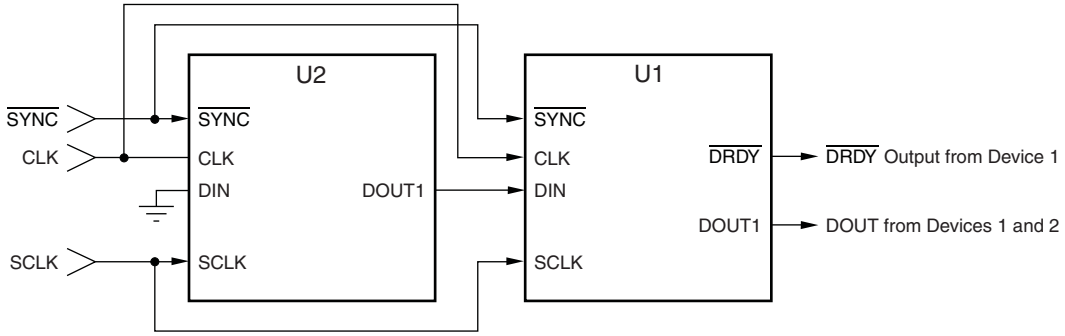
($f_{SCLK} = f_{CLK}$)

MODE SELECTION	CLKDIV	MAXIMUM NUMBER OF CHANNELS
High-Speed	1	10
High-Resolution	1	21
Low-Power	1	21
	0	10
Low-Speed	1	106
	0	21

Whether the interface protocol is SPI or Frame-Sync, it is recommended to synchronize all devices by tying the SYNC inputs together. When synchronized in SPI protocol, it is only necessary to monitor the DRDY output of one ADS1278.

In Frame-Sync interface protocol, the data from all devices are ready after the rising edge of FSYNC.

Since DOUT1 and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT1 creates a setup time on DIN. Minimize the skew in SCLK to avoid timing violations.



Note: The number of chained devices is limited by the SCLK rate and device mode.

Figure 78. Daisy-Chaining of Two Devices, SPI Protocol (FORMAT[2:0] = 000 or 001)

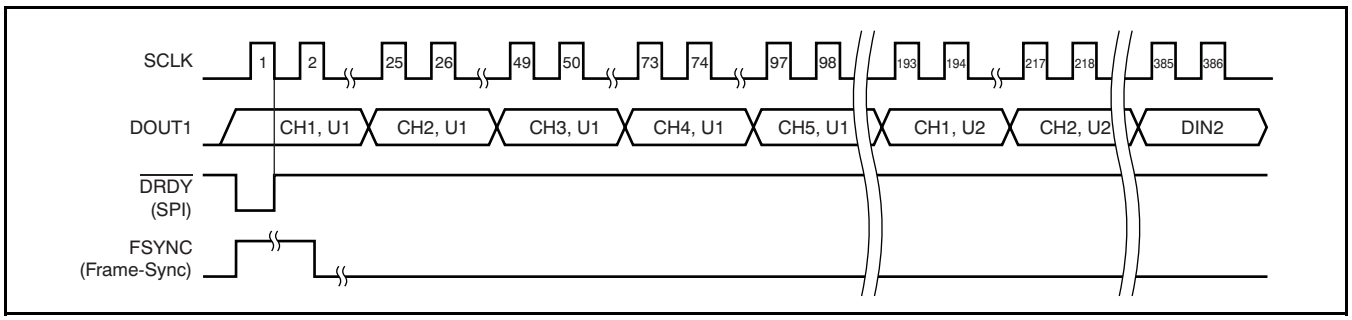
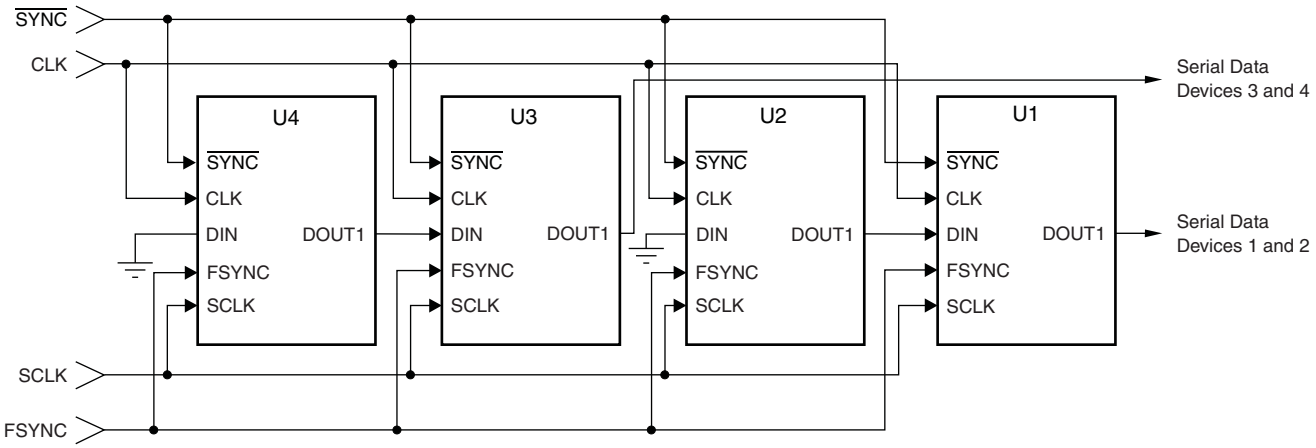


Figure 79. Daisy-Chain Data Format of Figure 78



Note: The number of chained devices is limited by the SCLK rate and device mode.

Figure 80. Segmented DOUT Daisy-Chain, Frame-Sync Protocol (FORMAT[2:0] = 011 or 100)

POWER SUPPLIES

The ADS1278 has three power supplies: AVDD, DVDD, and IOVDD. AVDD is the analog supply that powers the modulator, DVDD is the digital supply that powers the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be tied together if desired (1.8 V). To achieve rated performance, it is critical that the power supplies are bypassed with 0.1-µF and 10-µF capacitors placed as close as possible to the supply pins. A single 10-µF ceramic capacitor may be substituted in place of the two capacitors.

Figure 81 shows the start-up sequence of the ADS1278. At power-on, bring up the DVDD supply first, followed by IOVDD and then AVDD. Check the power-supply sequence for proper order, including the ramp rate of each supply. DVDD and IOVDD may be sequenced at the same time if the supplies are tied together. Each supply has an internal reset circuit whose outputs are summed together to generate a global power-on reset. After the supplies have exceeded the reset thresholds, 2^{18} f_{CLK} cycles are counted before the converter initiates the conversion process. Following the CLK cycles, the data for 129 conversions are suppressed by the ADS1278 to allow output of fully-settled data. In SPI protocol, $\overline{DRDY}$ is held high during this interval. In frame-sync protocol, DOUT is forced to zero. The power supplies should be applied before any analog or digital pin is driven. For consistent performance, assert $\overline{SYNC}$ after device power-on when data first appear.

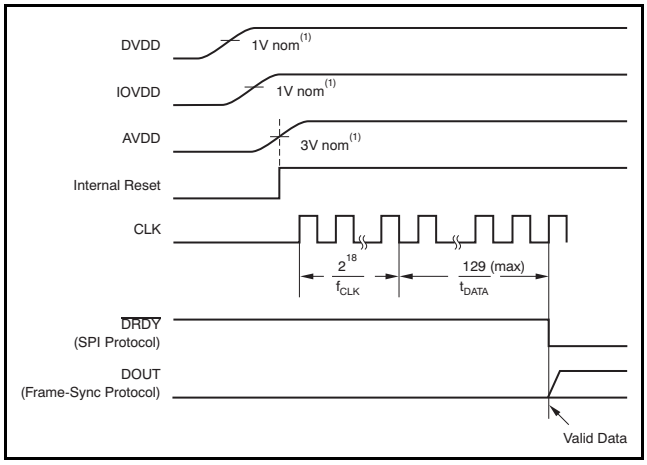


Figure 81. Start-Up Sequence

MODULATOR OUTPUT

The ADS1278 incorporates a 6th-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter that yields the conversion results. The data stream output of the modulator is available directly, bypassing the internal digital filter. The digital filter is disabled, reducing the DVDD current, as shown in Table 15. In this mode, an external digital filter implemented in an ASIC, FPGA, or similar device is required. To invoke the modulator output, tie FORMAT[2:0], as shown in Figure 82. DOUT[8:1] then becomes the modulator data stream outputs for each channel and $\overline{SCLK}$ becomes the modulator clock output. The $\overline{DRDY}$/FSYNC pin becomes an unused output and can be ignored. The normal operation of the Frame-Sync and SPI interfaces is disabled, and the functionality of SCLK changes from an input to an output, as shown in Figure 82.

Table 15. Modulator Output Clock Frequencies

MODE [1:0]	CLKDIV	MODULATOR CLOCK OUTPUT (SCLK)	DVDD (mA)
00	1	$f_{CLK}/4$	8
01	1	$f_{CLK}/4$	7
10	1	$f_{CLK}/8$	4
	0	$f_{CLK}/4$	4
11	1	$f_{CLK}/40$	1
	0	$f_{CLK}/8$	1

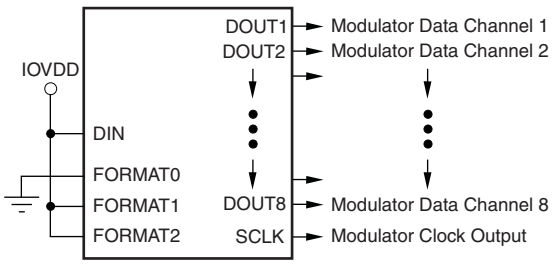


Figure 82. Modulator Output

In modulator output mode, the frequency of the modulator clock output (SCLK) depends on the mode selection of the ADS1278. Table 15 lists the modulator clock output frequency and DVDD current versus device mode.

Figure 83 shows the timing relationship of the modulator clock and data outputs.

The data output is a modulated 1s density data stream. When V_{IN} = $+V_{REF}$, the 1s density is approximately 80% and when V_{IN} = $–V_{REF}$, the 1s density is approximately 20%.

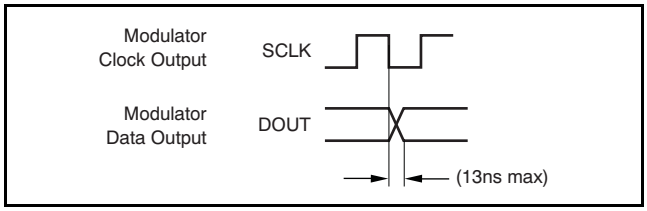


Figure 83. Modulator Output Timing

PIN TEST USING TEST[1:0] INPUTS

The test mode feature of the ADS1278 allows continuity testing of the digital I/O pins. In this mode, the normal functions of the digital pins are disabled and routed to each other as pairs through internal logic, as shown in Table 16. The pins in the left column drive the output pins in the right column. **Note:** some of the digital input pins become outputs; these outputs must be accommodated in the design. The analog input, power supply, and ground pins all remain connected as normal. The test mode is engaged by setting the pins TEST [1:0] = 11. For normal converter operation, set TEST[1:0] = 00. Do not use '01' or '10'.

Table 16. Test Mode Pin Map (TEST[1:0] = 11)

TEST MODE PIN MAP	
INPUT PINS	**OUTPUT PINS**
$\overline{\text{PWDN1}}$	DOUT1
$\overline{\text{PWDN2}}$	DOUT2
$\overline{\text{PWDN3}}$	DOUT3
$\overline{\text{PWDN4}}$	DOUT4
$\overline{\text{PWDN5}}$	DOUT5
$\overline{\text{PWDN6}}$	DOUT6
$\overline{\text{PWDN7}}$	DOUT7
$\overline{\text{PWDN8}}$	DOUT8
MODE0	DIN
MODE1	$\overline{\text{SYNC}}$
FORMAT0	CLKDIV
FORMAT1	FSYNC/$\overline{\text{DRDY}}$
FORMAT2	SCLK

VCOM OUTPUT

The VCOM pin provides a voltage output equal to AVDD/2. The intended use of this output is to set the output common-mode level of the analog input drivers. The drive capability of the output is limited; therefore, the output should only be used to drive high-impedance nodes (> 1 MΩ). In some cases, an external buffer may be necessary. A 0.1-µF bypass capacitor is recommended to reduce noise pickup.

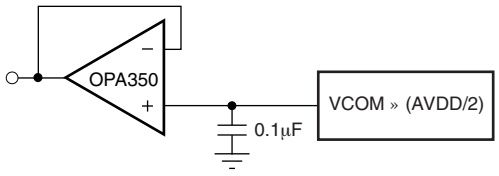


Figure 84. VCOM Output

APPLICATION INFORMATION

To obtain the specified performance from the ADS1278, the following layout and component guidelines should be considered.

1. **Power Supplies:** The device requires three power supplies for operation: DVDD, IOVDD, and AVDD. The allowed range for DVDD is 1.65 V to 1.95 V; the range of IOVDD is 1.65 V to 3.6 V; AVDD is restricted to 4.75 V to 5.25 V. For all supplies, use a 10-µF tantalum capacitor, bypassed with a 0.1-µF ceramic capacitor, placed close to the device pins. Alternatively, a single 10-µF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power-supply source is used, the voltage ripple should be low (less than 2 mV) and the switching frequency outside the passband of the converter.
2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
3. **Digital Inputs:** It is recommended to source-terminate the digital inputs to the device with 50-Ω series resistors. The resistors should be placed close to the driving end of digital source (oscillator, logic gates, DSP, etc.) This placement helps to reduce ringing on the digital lines (ringing may lead to degraded ADC performance).
4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
5. **Reference Inputs:** It is recommended to use a minimum 10-µF tantalum with a 0.1-µF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should have less than 3 μV_{RMS} in-band noise. For references with noise higher than this level, external reference filtering may be necessary.
6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 1-nF to 10-nF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground can be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100 pF) to preserve the ac common-mode performance.
7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This layout is particularly important for small-value ceramic capacitors. Larger (bulk) decoupling capacitors can be located farther from the device than the smaller ceramic capacitors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1278MPAPTEP	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS1278EP	Samples
V62/12611-01XE	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ADS1278EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

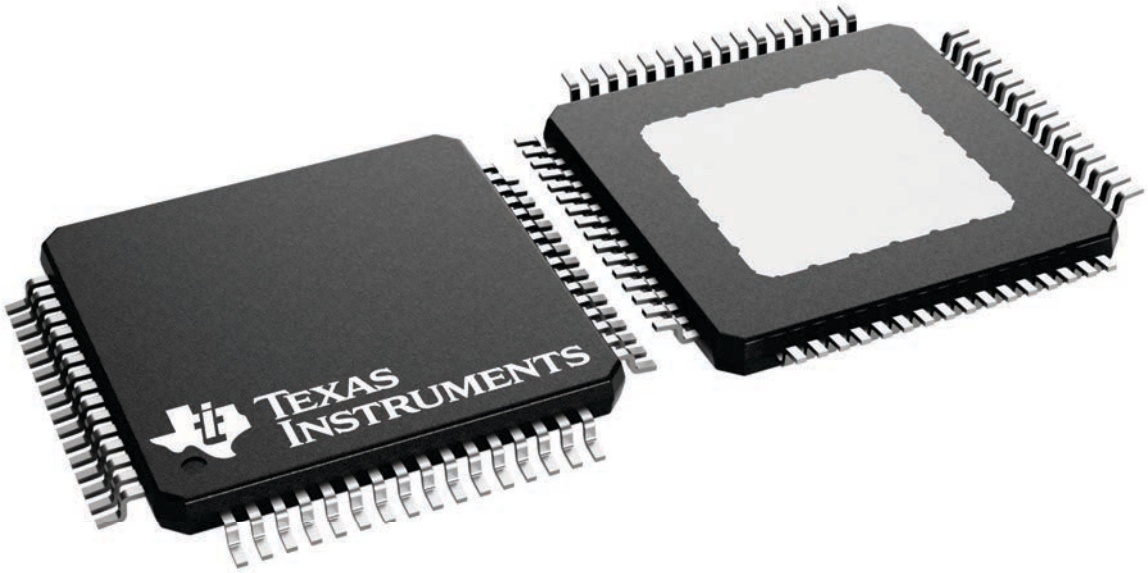
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

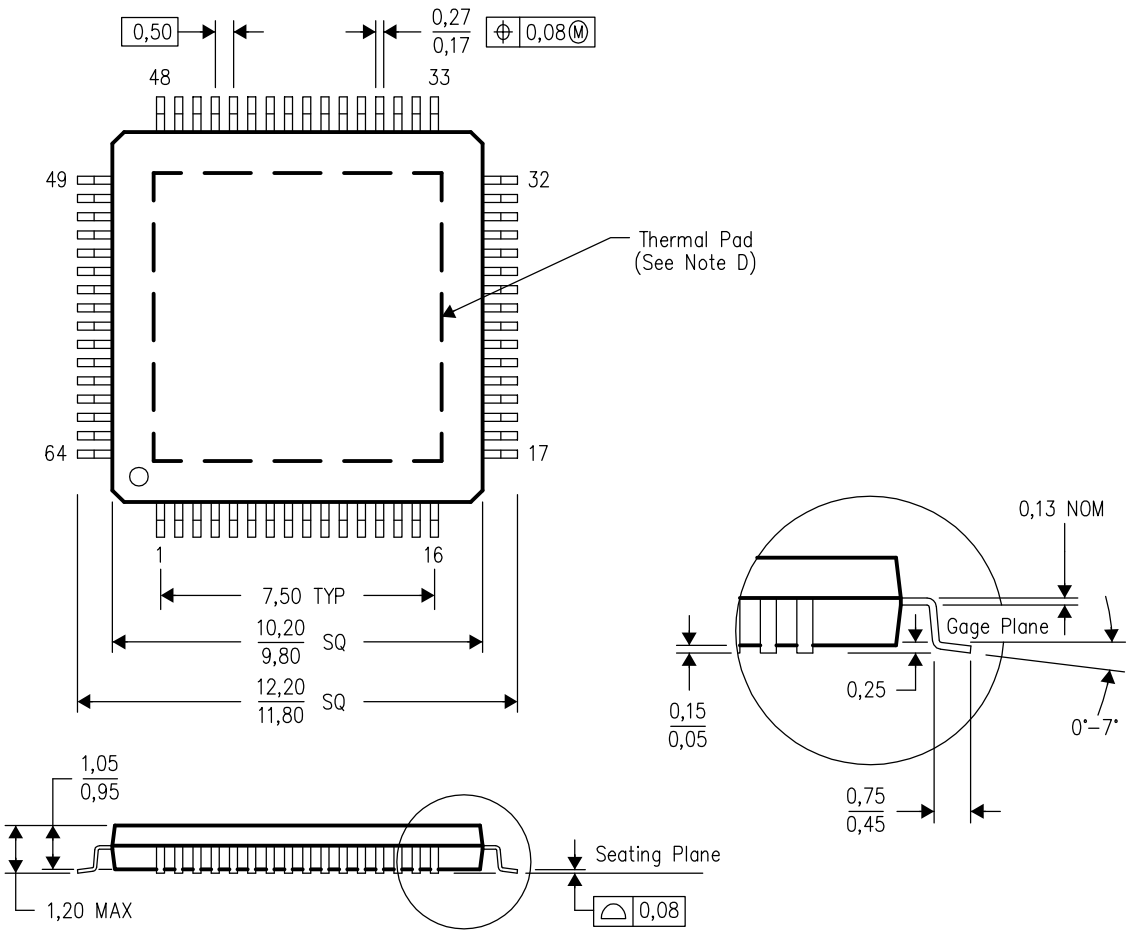
QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

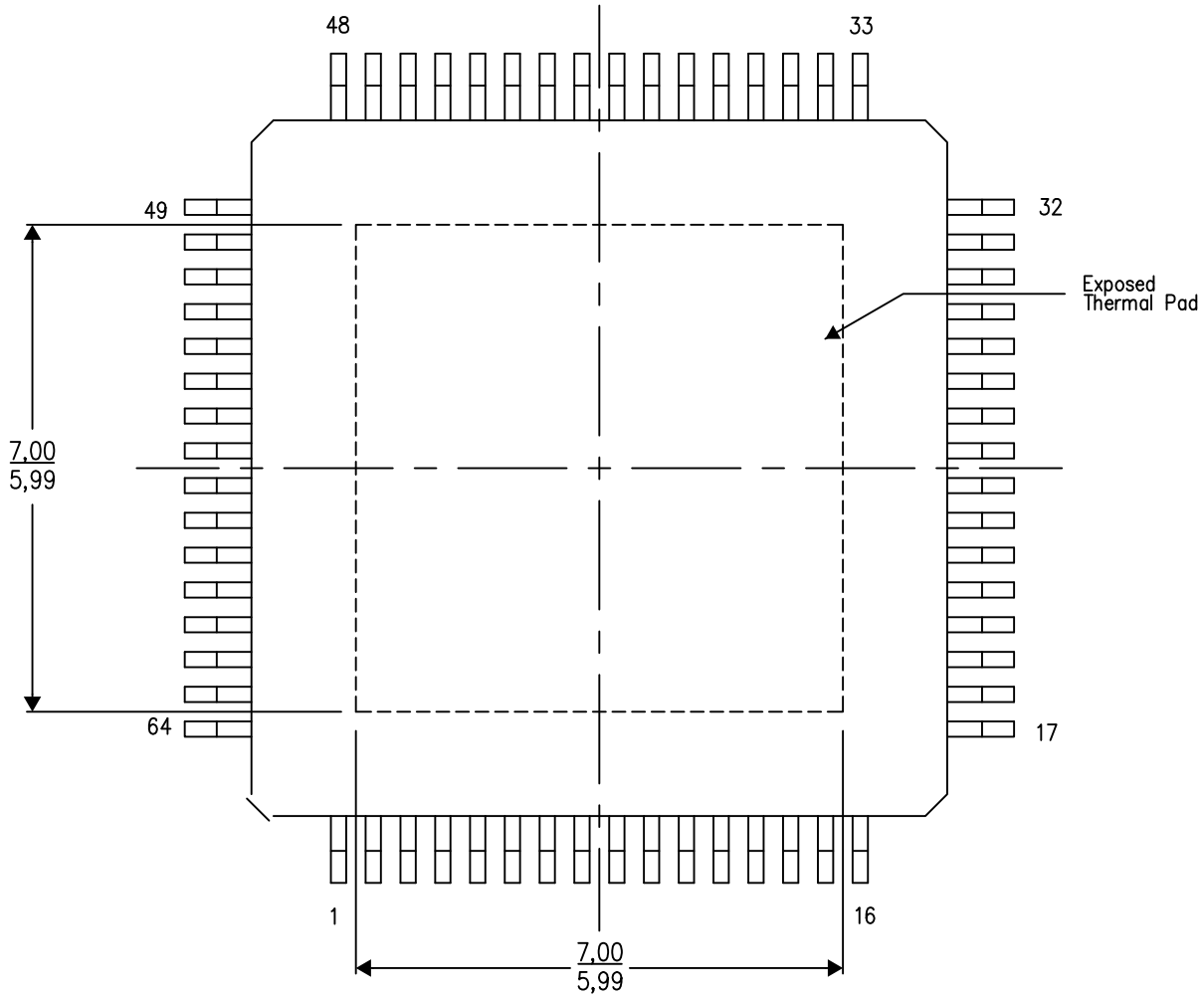
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

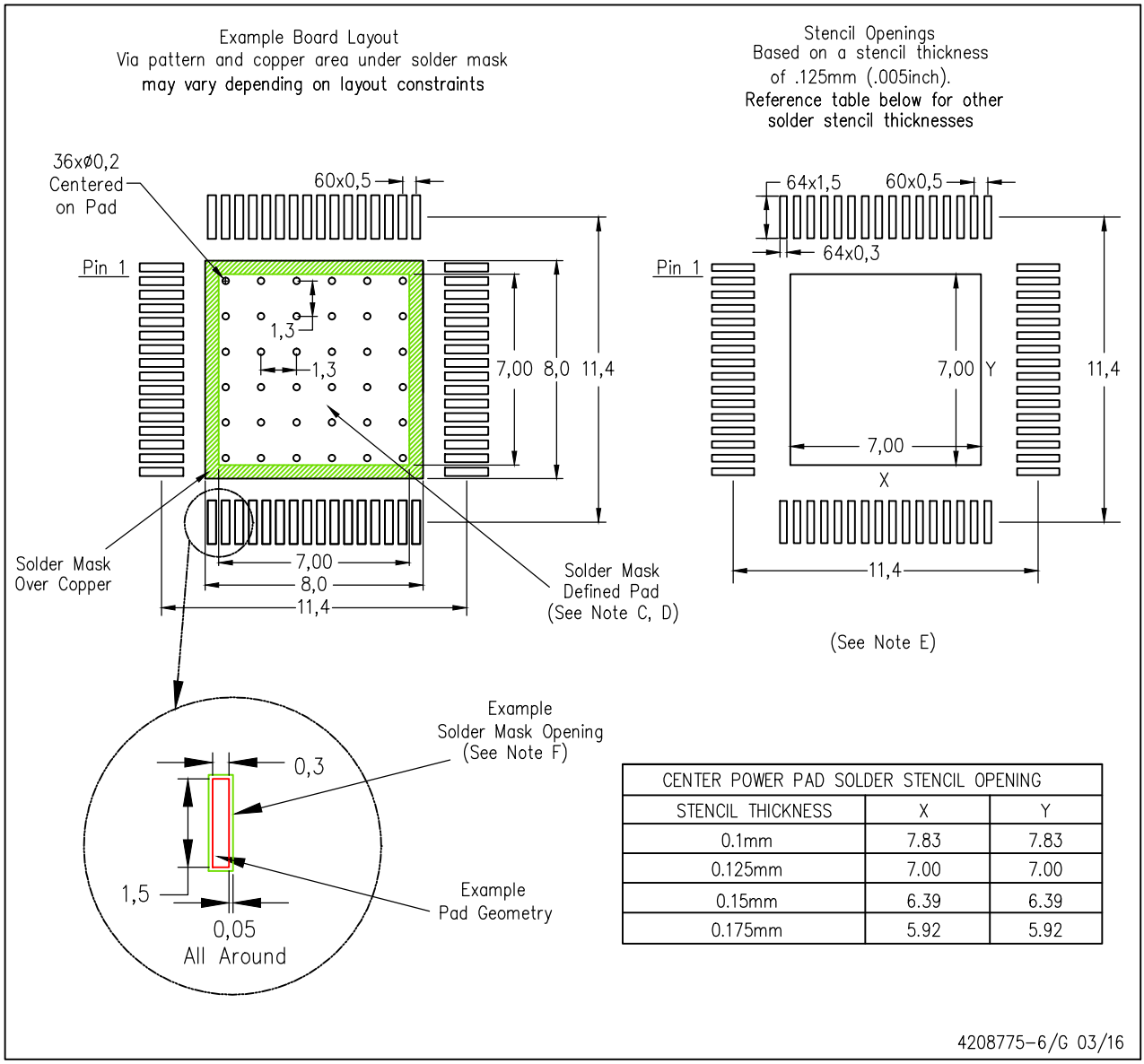
Exposed Thermal Pad Dimensions

4206326–5/P 05/14

NOTES: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	7.83	7.83
0.125mm	7.00	7.00
0.15mm	6.39	6.39
0.175mm	5.92	5.92

4208775–6/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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