Description

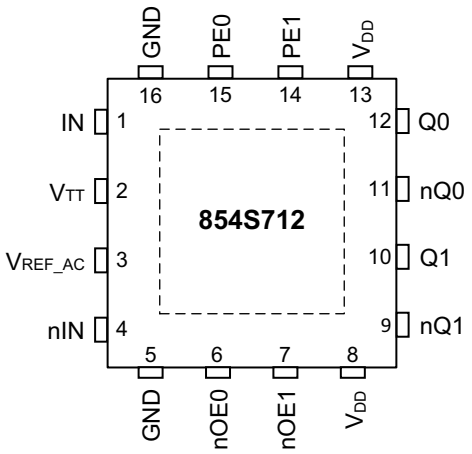
The 854S712 is a differential, high-speed 1:2 data/clock fanout buffer and line driver. The outputs support pre-emphasis in order to drive backplanes and long transmission lines while reducing inter-symbol interference effects. The pre-emphasis level is configurable to optimize for low bit error rate or power consumption. Pre-emphasis utilizes an increased output voltage swing for transition bits.

The device is optimized for data rates up to 4.5 Gbps (NRZ) and for deterministic jitter in data applications and low additive jitter in clock applications. The outputs are LVDS-compliant while the differential input is compatible with a variety of signal levels such as LVDS, LVPECL and CML. Internal input termination, a bias voltage output for AC-coupling and small packaging (VFQFN) supports space-efficient board designs. The 854S712 operates from a 3.3V power supply and supports the industrial temperature range of -40°C to +85°C.

Features

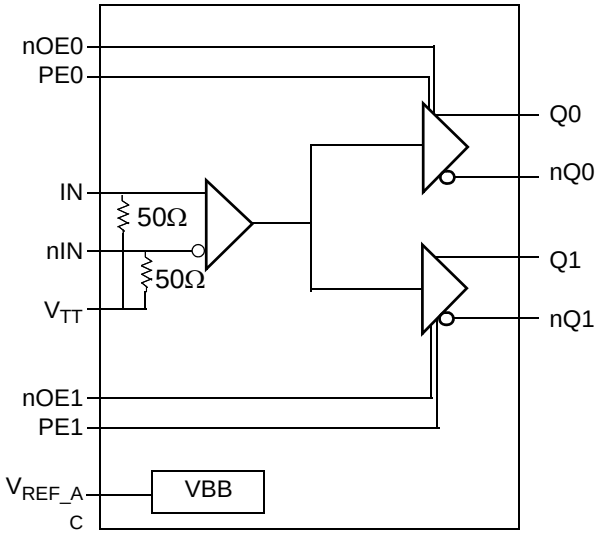
- 1:2 differential data/clock fanout buffer and line driver
- 4.5 Gbps data rate (NRZ) (maximum)
- Differential LVDS outputs
- Differential input supporting LVDS, LVPECL and CML levels
- Configurable output pre-emphasis
- Low-skew outputs: 10ps (maximum)
- Low data deterministic jitter: 4ps (maximum)
- LVCMOS interface levels for the control inputs
- Asynchronous output disable into high-impedance state
- Internal input termination: 100Ω (Differential)
- Additive phase jitter, RMS: 0.08ps (typical)
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



16-pin, 3mm x 3mm VFQFN Package

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1 Pin Description

Number	Name	Type		Description
1	IN	Input		Non-inverting differential data and clock input. LVDS, LVPECL or CML interface levels. 50Ω to $V_{TT.}$
4	nIN	Input		Inverting differential data and clock input. LVDS, LVPECL or CML interface levels. 50Ω to $V_{TT.}$
6, 7	nOE0, nOE1	Input	Pulldown	Output enable control. LVCMOS/LVTTL interface levels.
15, 14	PE0, PE1	Input	Pulldown	Pre-emphasis control. LVCMOS/LVTTL interface levels.
12, 11	Q0, nQ0	Output		Differential output pair. LVDS interface levels.
10, 9	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
3	V_{REF_AC}	Output		Bias voltage reference for AC-coupling.
2	V_{TT}			Center tap for input termination. Leave floating for LVDS input, connect to 50Ω to GND for LVPECL inputs and to the V_{REF_AC} output for AC-coupled applications.
5, 16	GND	Power		Power supply ground.
8, 13	V_{DD}	Power		Power supply pins.

NOTE: *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Device Configuration

Table 3A. Output Enable Control

Inputs		Outputs	
nOE1	**nOE0**	**Q1, nQ1**	**Q0, nQ0**
0 (default)	0 (default)	Enabled	Enabled
0	1	Enabled	Disabled (Logic 0)
1	0	Disabled (Logic 0)	Enabled
1	1	Disabled (Logic 0)	Disabled (Logic 0)

NOTE: nOEx are asynchronous controls.

Table 3B. Output Pre-Emphasis Control

Input		Pre-Emphasis	
PE1	**PE0**	**Q1, nQ1**	**Q0, nQ0**
0 (default)	0 (default)	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On

NOTE: PEx are asynchronous controls.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
I_{IN}, Input Current, IN, nIN	±50mA
V_{TT}, Current, I_{VT}	±100mA
V_{REF_AC}, Input Sink/Source Current, I_{REF_AC}	±2mA
Package Thermal Impedance, θ_{JA}	74.7°C (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				90	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	PE0, PE1, nOE0, nOE1	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PE0, PE1, nOE0, nOE1	V_{DD} = 3.465V, V_{IN} = 0V	10			µA

Table 4C. DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Input Resistance	IN, nIN	IN to V_{TT}	40	50	60	Ω
V_{IH}	Input High Voltage	IN, nIN		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	IN, nIN		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing; NOTE 1			0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		2.4	V
V_{REF_AC}	Bias voltage reference			V_{DD} - 1.35	V_{DD} - 1.30	V_{DD} - 1.25	V
I_{IN}	Input Current; NOTE 2	IN, nIN				35	mA

NOTE 1: Refer to Parameter Measurement Information, Input Voltage Swing Diagram.
NOTE 2: Guaranteed by design.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	Pre-Emphasis off (PE0=PE1=0)	300	450	650	mV
ΔV_{OD}	V_{OD} Magnitude Change	Pre-Emphasis off (PE0=PE1=0)			50	mV
V_{OS}	Offset Voltage	Pre-Emphasis off (PE0=PE1=0)	1.10	1.25	1.40	V
ΔV_{OS}	V_{OS} Magnitude Change	Pre-Emphasis off (PE0=PE1=0)			50	mV

AC Electrical Characteristics

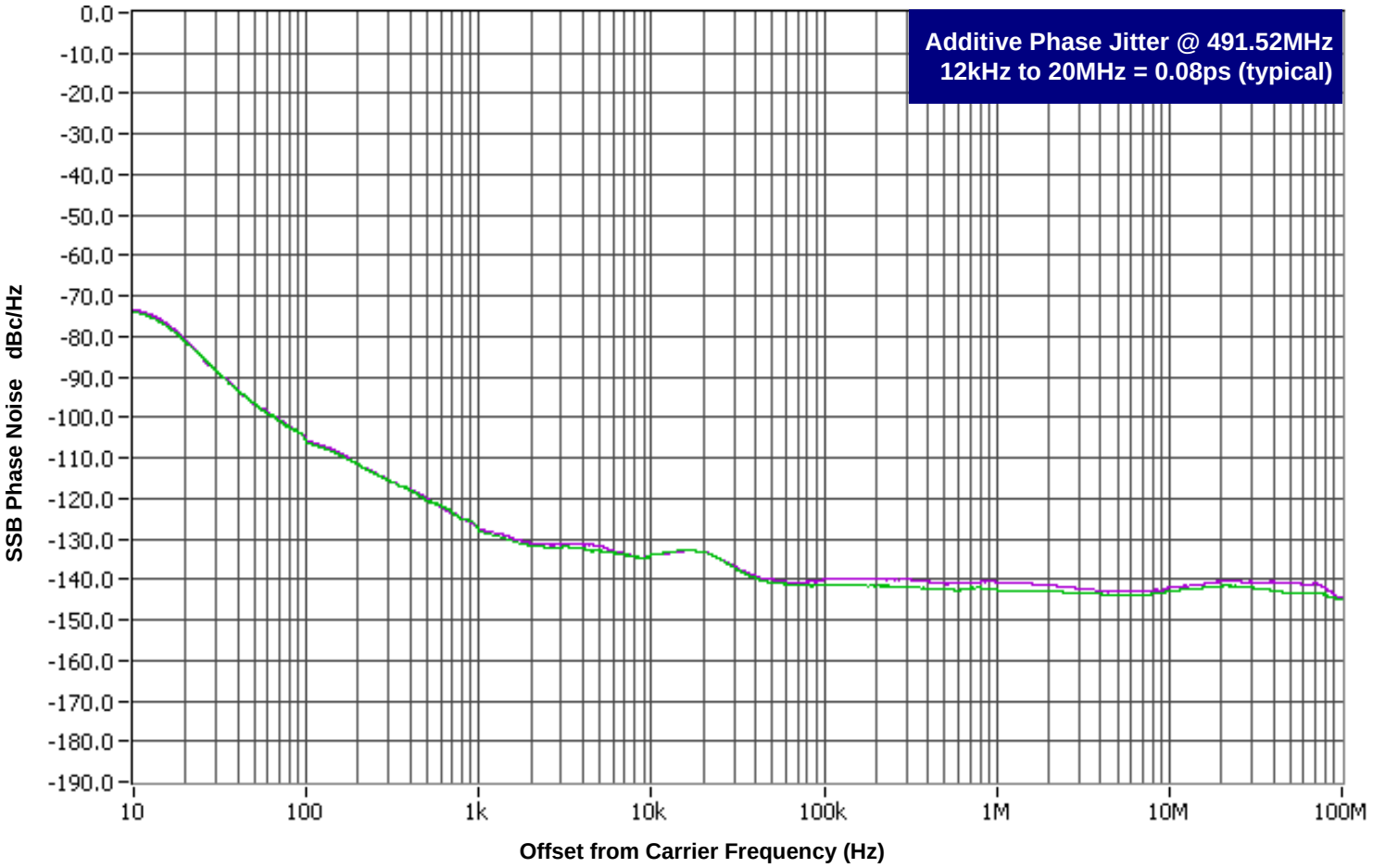
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency		Alternating 01 pattern (Clock)			3.0	GHz
f_{OUT}	Output Frequency		Alternating 01 pattern (Clock)			3.0	GHz
	Operating Data Rate		NRZ (PRBS 2^7-1 Pattern)			4.5	Gbps
t_{PD}	Propagation Delay; NOTE 1		Alternating 01 pattern (Clock)	300		500	ps
*t*sk(p)	Output Pulse Skew		Alternating 01 pattern (Clock)			20	ps
*t*sk(o)	Output Skew, NOTE 2, 4		Alternating 01 pattern (Clock)			10	ps
*t*sk(pp)	Part-to-Part Skew: NOTE 3, 4		Alternating 01 pattern (Clock)			150	ps
t_{EN}	Output Enable Time: NOTE 5					1.25	ns
t_{DIS}	Output Disable Time: NOTE 5					1.35	ns
V_{PE}	Output Pre-Emphasis Voltage Ratio; NOTE 5		f_{OUT} = 300MHz, Pre-Emphasis Off		0		dB
			f_{OUT} = 300MHz,Pre-Emphasis On		2		dB
Δt_{PE}	Output Pre-Emphasis Duration; NOTE 5		f_{OUT} = 300MHz, Pre-Emphasis On		300		ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		Alternating 01 pattern (Clock), 491.52MHz, Integration Range: 12kHz - 20MHz		0.08		ps
t_{DJ}	Deterministic Jitter Peak-Peak; NOTE 5, 6		K28.5 Pattern, 1.5 Gbps, Pre-Emphasis On			4	ps
t_{TJ}	Total Jitter Peak-Peak; NOTE 5		NRZ (PRBS 2^7-1 Pattern), 1.5 Gbps, Pre-Emphasis On			4	ps
t_R / t_F	Output Rise/ Fall Time	$f_{OUT} \leq$ 625MHz	20% to 80%, 491.52MHz Alternating 01 pattern (Clock)	50		400	ps
		f_{OUT} = 1.25GHz		65		200	ps
		f_{OUT} = 2.25GHz		80		100	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters characterized at $f_{OUT} \leq$ 1.25GHz and pre-emphasis off, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency, and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined according with JEDEC Standard 65.
NOTE 5: These parameters are guaranteed by characterization.
NOTE 6: A repeating K28.5 sequence (composed of alternating K28.5+ and K28.5-) contains the symbols 0011111010 1100000101. This pattern contains five consecutive 1's and five consecutive 0's, (the longest consecutive identical digits found in 8B/10B coded data)

Additive Phase Jitter

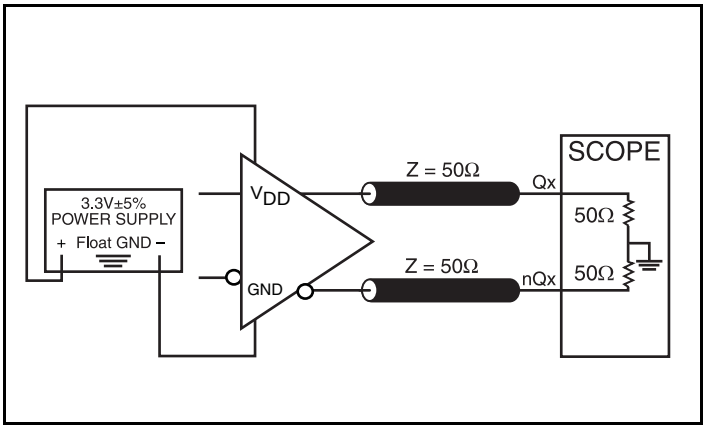
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



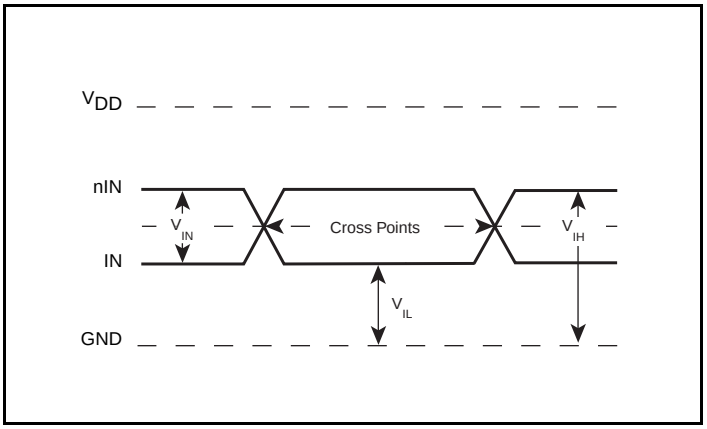
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “IFR2042 10kHz – 6.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”.

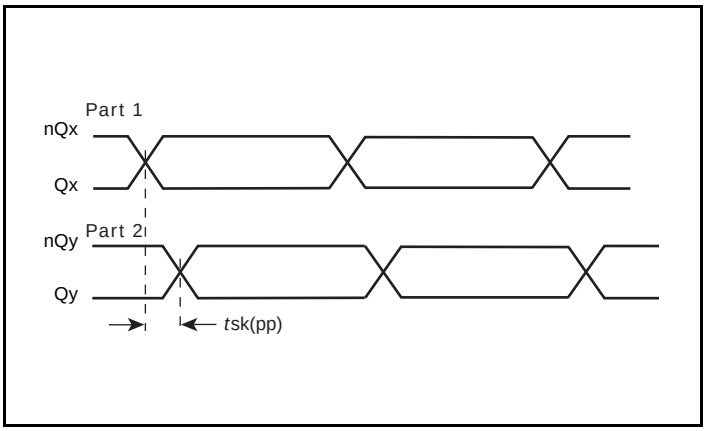
Parameter Measurement Information



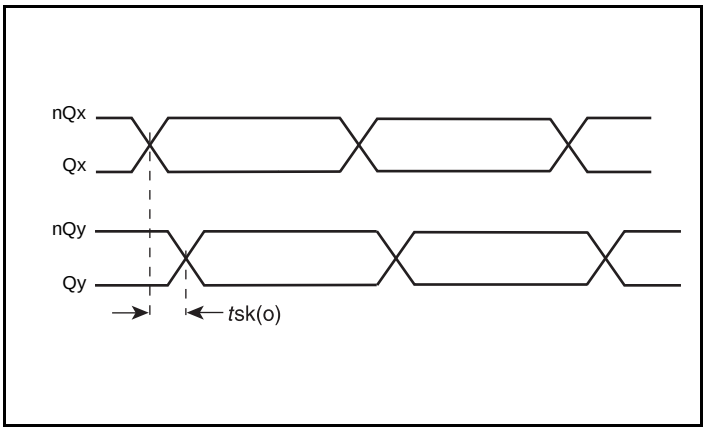
LVDS Output Load AC Test Circuit



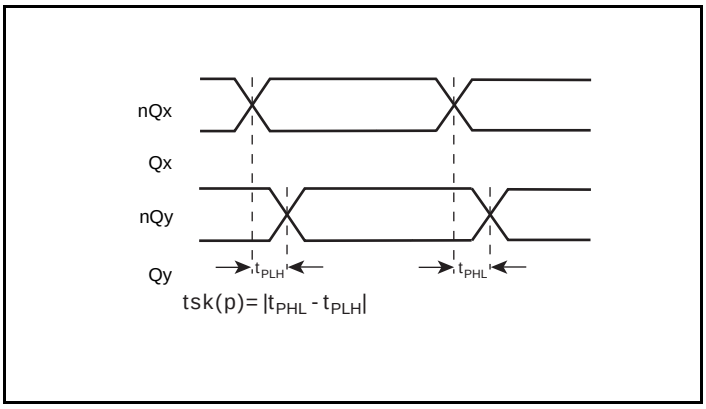
Differential Input Level



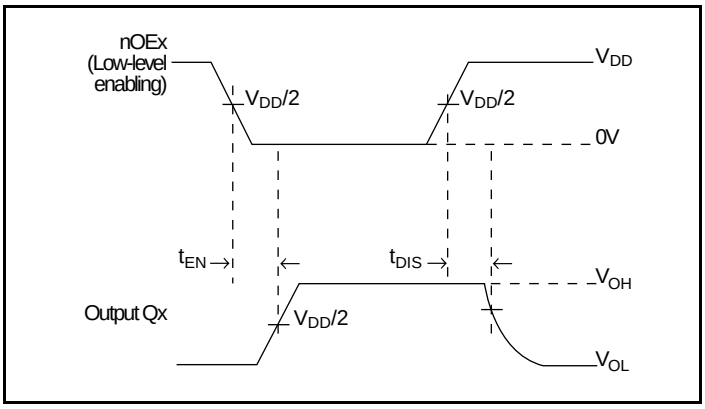
Part-to-Part Skew



Output Skew

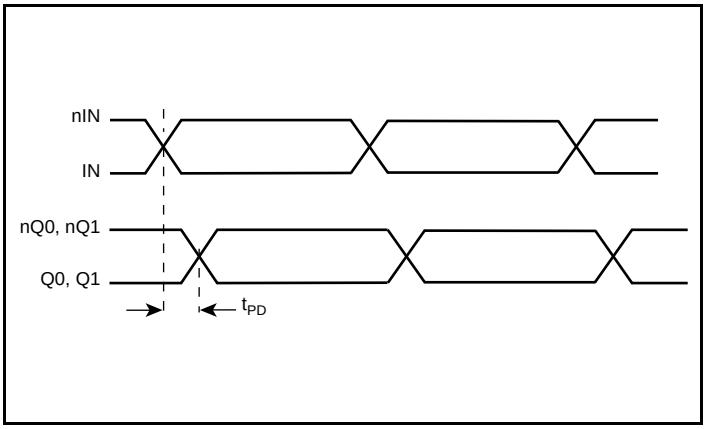


Output Pulse Skew

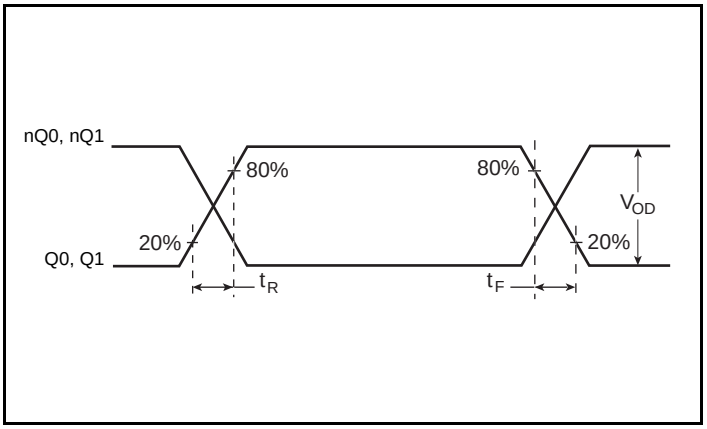


Output Enable/Disable Time

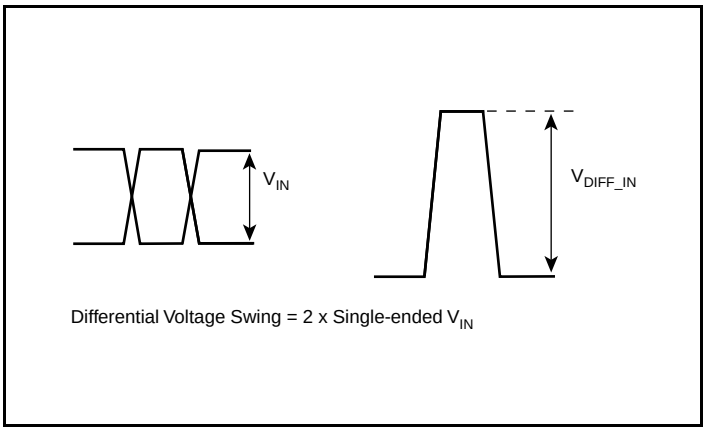
Parameter Measurement Information, continued



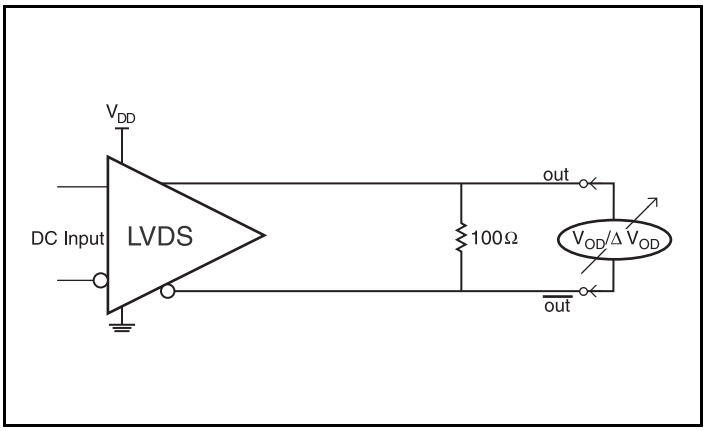
Propagation Delay



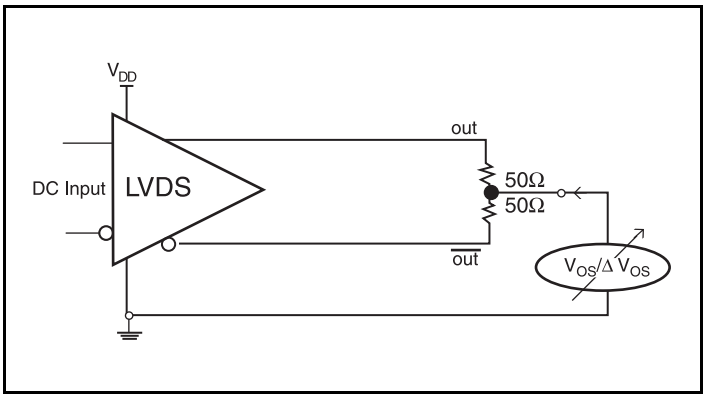
Output Rise/Fall Time



Single-Ended & Differential Input Voltage Swing

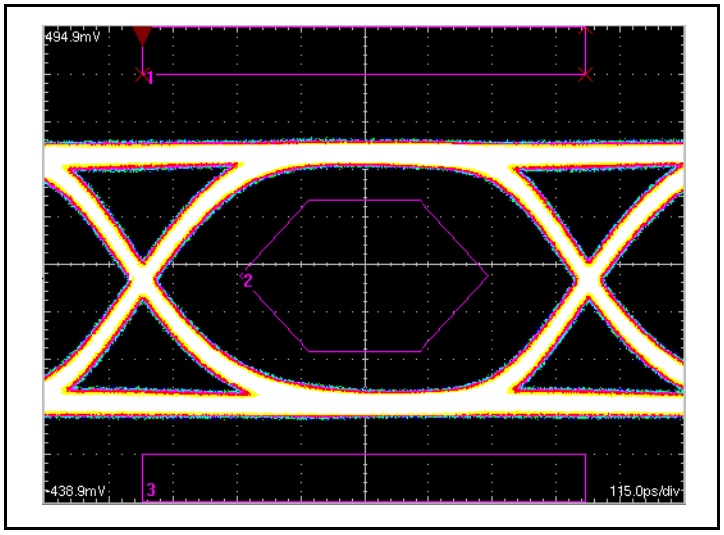


Differential Output Voltage Setup

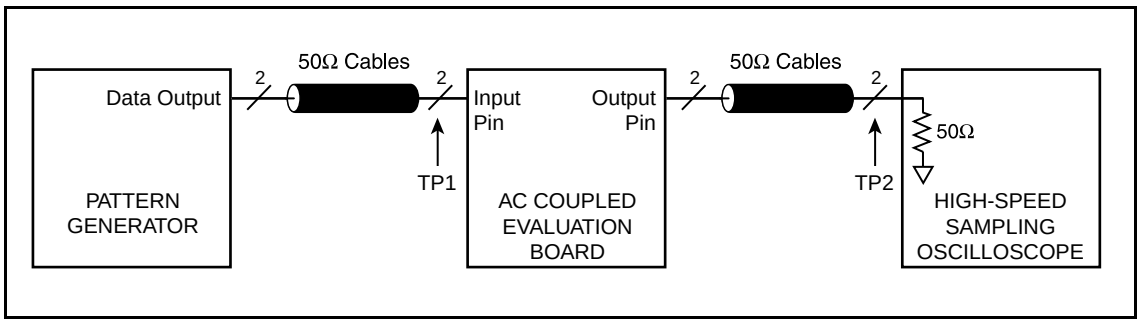


Offset Voltage Setup

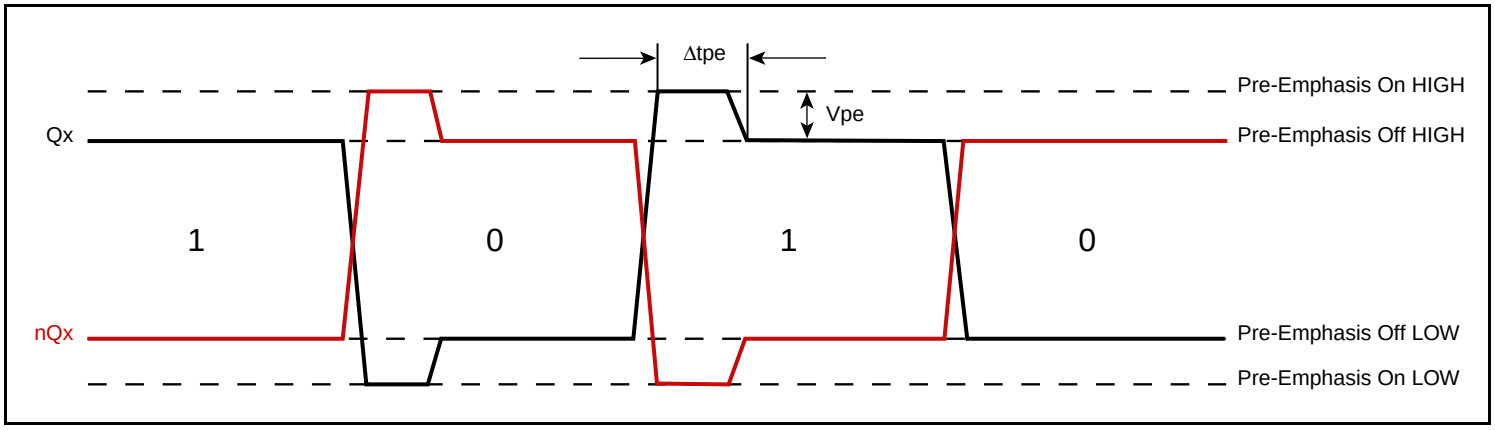
Parameter Measurement Information, continued



1.2GHz NRZ (PRBS Pattern) GbE Mask, Pre-Emphasis On



Deterministic Jitter and Total Jitter (peak-to-peak)



Output Pre-Emphasis Voltage Ratio & Duration

Applications Information

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{IN} and V_{IH} input requirements. *Figure 1A to* Figure 1D show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

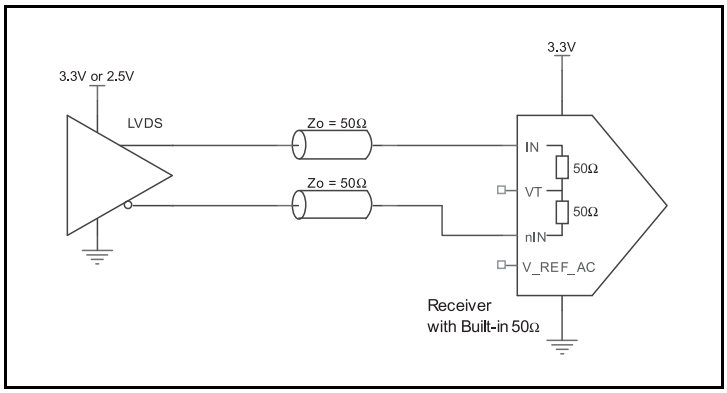


Figure1A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

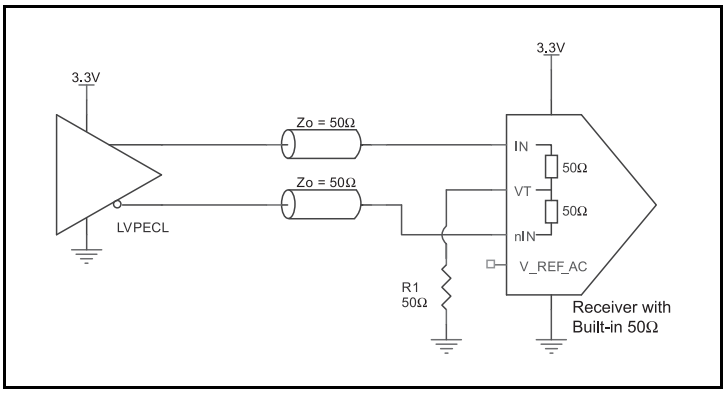


Figure1C. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

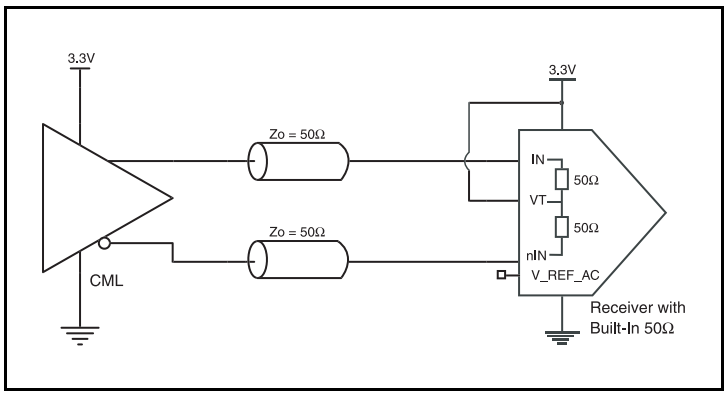


Figure1B. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

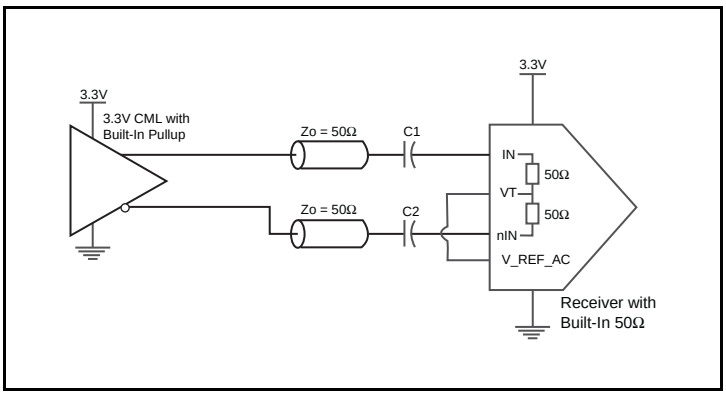


Figure1D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

Recommendations for Unused Input and Output Pins

Inputs

LVCMOS Select Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

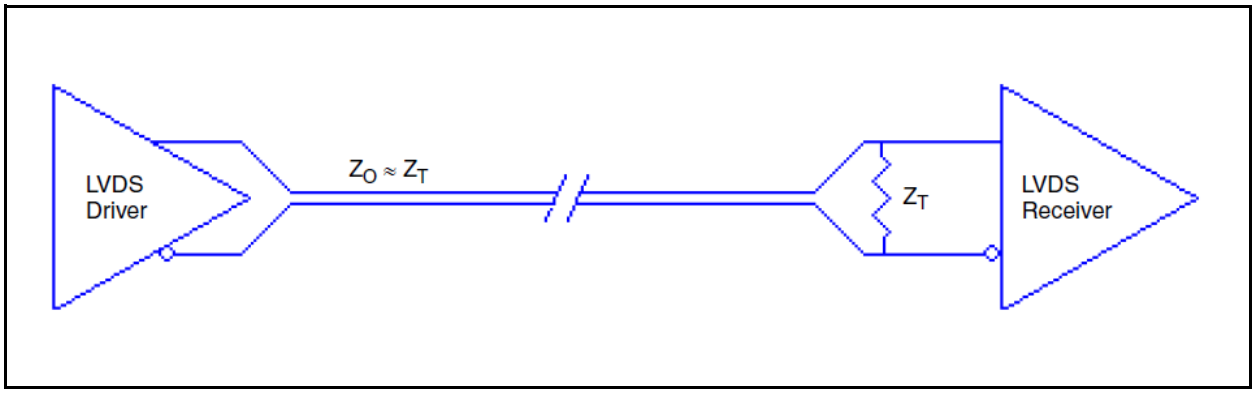


Figure2A. Standard LVDS Termination

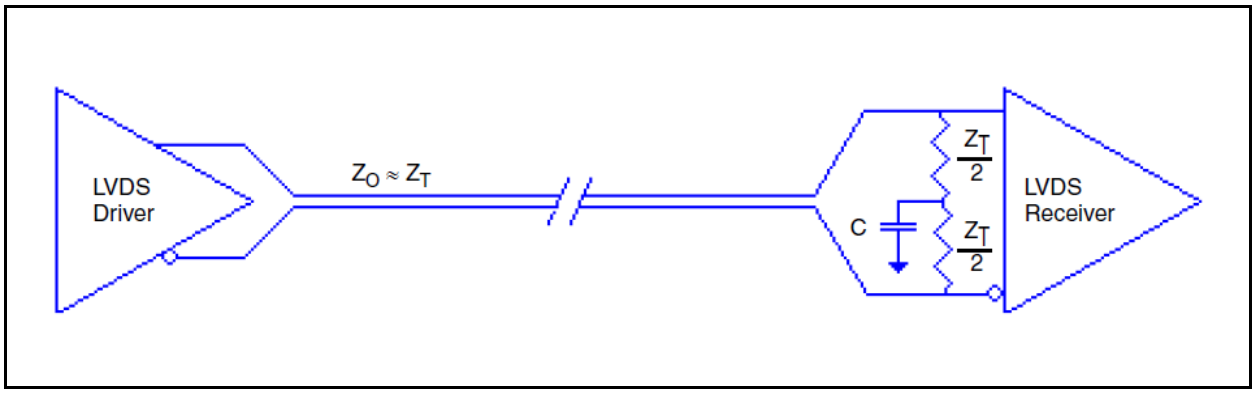


Figure2B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

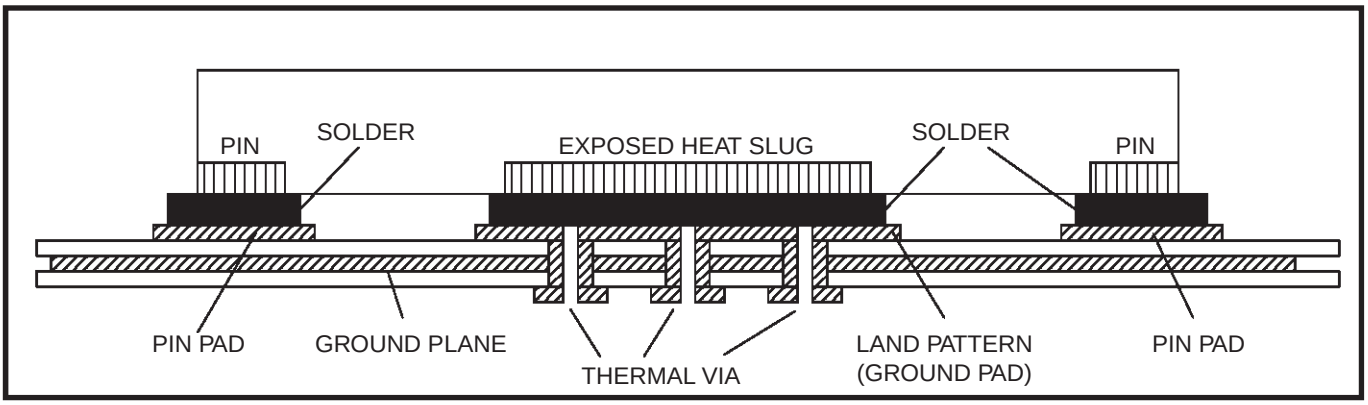


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 854S712.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 854S712 is the sum of the core power plus the power dissipated into the load.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 90mA = **311.85mW**
- Power Dissipation for internal termination R_T
  Power $(R_T)_{MAX} = (V_{IN\_MAX})^2 / R_{T\_MIN} = (1.2V)^2 / 80\Omega$ = **18mW**

Total Power$_{\_MAX}$ = 311.85mW + 18mW = **329.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.330W * 74.7°C/W = 109.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 854S712 is: 439

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S712AKILF	2AIL	16 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
854S712AKILFT	2AIL	16 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Revision Date	Description of Change
October 10, 2017	Updated the package outline drawings; however, no mechanical changes Completed other minor improvements
December 18, 2014	Updated “Wiring the Differential output” application section. Updated LVDS Termination. Updated header/footer throughout the datasheet.

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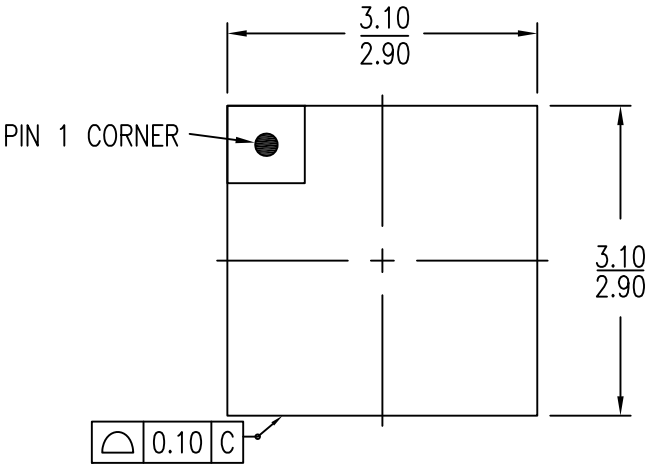
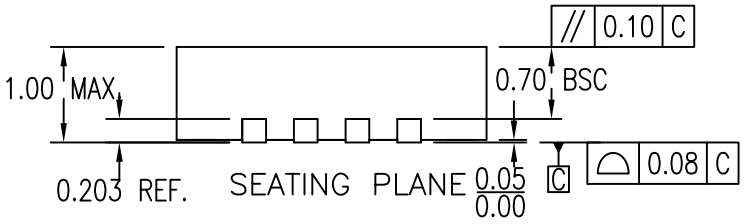
16L-QFN Package Outline Drawing

3.0 x 3.0 x 1.0 mm, 0.5 mm Pitch, 1.70 x 1.70 mm Epad

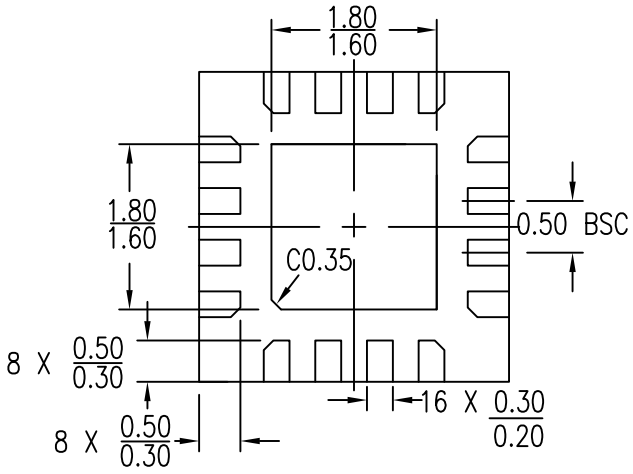
NL/NLG16P2, PSC-4169-02, Rev 03, Page 1



TOP VIEW



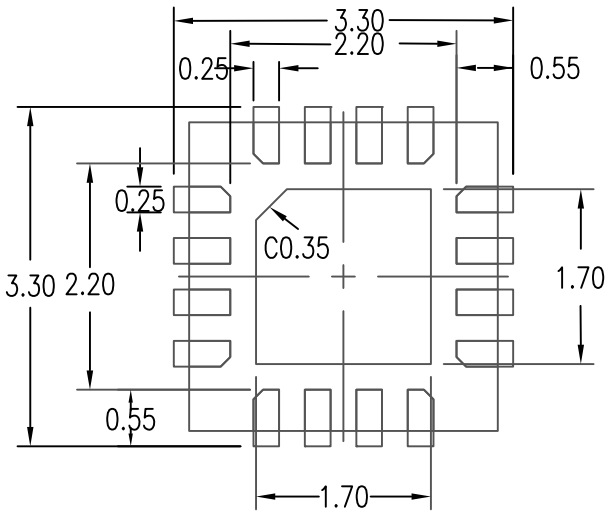
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES



RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSIONS ARE IN mm.ANGLES IN DEGREES
2. TOP DOWN VIEW–AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Aug 15, 2017	Rev 03	Update Epad Range
Jul 28, 2017	Rev 02	New format