MC10H605, MC100H605

Registered Hex ECL to TTL Translator

ON Semiconductor®

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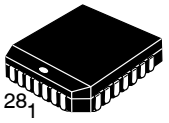
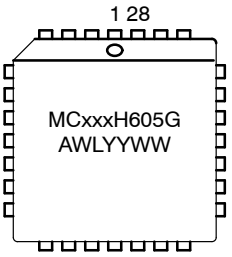


PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Description

The MC10/100H605 is a 6−bit, registered, dual supply ECL to TTL translator. The device features differential ECL inputs for both data and clock. The TTL outputs feature balanced 24 mA sink/source capabilities for driving transmission lines.

With its differential ECL inputs and TTL outputs the H605 device is ideally suited for the receive function of a HPPI bus type board−to−board interface application. The on chip registers simplify the task of synchronizing the data between the two boards.

A V_{BB} reference voltage is supplied for use with single−ended data or clock. For single−ended applications the V_{BB} output should be connected to the "bar" inputs ($\overline{Dn}$ or $\overline{CLK}$) and bypassed to ground via a 0.01 μF capacitor. To minimize the skew of the device differential clocks should be used.

The ECL level Master Reset pin is asynchronous and common to all flip−flops. A "HIGH" on the Master Reset forces the Q outputs "LOW".

The device is available in either ECL standard: the 10H device is compatible with MECL 10H™ logic levels while the 100H device is compatible with 100K logic levels.

Features

- Differential ECL Data and Clock Inputs
- 24 mA Sink, 24 mA Source TTL Outputs
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- 2.0 ns Part−to−Part Skew
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

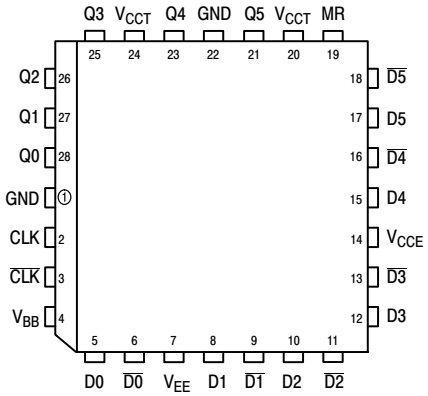


Figure 1. Pinout: PLCC−28
(Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0−D5	True ECL Data Inputs
$\overline{D0}$−$\overline{D5}$	Inverted ECL Data Inputs
CLK, $\overline{CLK}$	Differential ECL Clock Input
MR	ECL Master Reset Input
Q0−Q5	TTL Outputs
V_{CCE}	ECL V_{CC} (0 V)
V_{CCT}	TTL V_{CC} (+5 V)
GND	TTL Ground (0 V)
V_{EE}	ECL V_{EE} (−5.2 V)

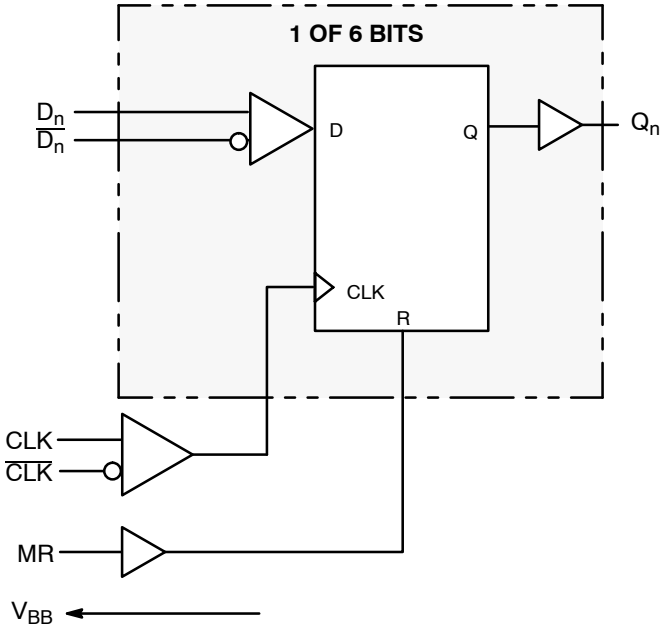


Figure 2. Logic Diagram

Table 2. TRUTH TABLE

Dn	MR	TCLK/CLK	Qn+1
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

Table 3. 10H ECL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.20 V ±5%; V_{CCE} = GND = 0 V)

			0°C			25°C			85°C			
Symbol	Characteristic	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Supply Current			63	75		63	75		61	75	mA
I_{INH}	Input HIgh Current				255			175			175	μA
I_{INL}	Input Low Current		0.5			0.5			0.5			μA
V_{IH}	Input High Voltage		−1170		−840	−1130		−810	−1060		−720	mV
V_{IL}	Input Low Voltage		−1950		−1480	−1950		−1480	−1950		−1480	mV
V_{BB}	Output Bias Voltage		−1400		−1280	−1370		−1270	−1330		−1210	mV
V_{Diff}	Input Differential Voltage		150			150			150			mV
V_{max} CMRR	Input Common Mode Reject Range				0			0			0	mV
V_{min} CMRR	Input Common Mode Reject Range	V_{EE} = −4.94 V_{EE} = −5.20 V_{EE} = −5.46	−2800 −3000 −3300			−2800 −3000 −3300			−2800 −3000 −3300			mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 4. 100H ECL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±5%; V_{EE} = −4.2 V to 5.5 V; V_{CCE} = GND = 0 V)

			0°C			25°C			85°C			
Symbol	Characteristic	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Supply Current			65	75		65	75		70	85	mA
I_{INH}	Input HIgh Current				255			175			175	μA
I_{INL}	Input Low Current		0.5			0.5			0.5			μA
V_{IH}	Input High Voltage		−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input Low Voltage		−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Reference Voltage		−1400		−1280	−1400		−1280	−1400		−1200	mV
V_{Diff}	Input Differential Voltage		150			150			150			mV
V_{max} CMRR	Input Common Mode Reject Range				0			0			0	mV
V_{min} CMRR	Input Common Mode Reject Range	V_{EE} = −4.20 V_{EE} = −4.50 V_{EE} = −4.80	−2000 −2200 −2400			−2000 −2200 −2400			−2000 −2200 −2400			mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. TTL DC CHARACTERISTICS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.2 V ±5% (10H); V_{EE} = −4.2 V to 5.5 V (100H); V_{CCE} = GND = 0 V)

			0°C			25°C			85°C			
Symbol	Characteristic	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CCL}	Supply Current	Outputs Low		65	75		65	75		65	75	mA
I_{CCH}	Supply Current	Outputs High		65	75		65	75		65	75	mA
V_{OL}	Output Low Voltage	I_{OL} = 24 mA			500			500			500	mV
V_{OH}	Output High Voltage	I_{OH} = 24 mA	2.5			2.5			2.5			mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V	100		225	100		225	100		225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. AC TEST LIMITS (V_{CCT} = +5.0 V ±10%; V_{EE} = −5.2 V ±5% (10H); V_{EE} = −4.2 V to 5.5 V (100H); V_{CCE} = GND = 0 V)

			0°C			25°C			85°C			
Symbol	Characteristic	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{PLH}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	Across P.S. and Temp C_L = 50 pF	 4.5 4.3	 5.3 5.3	 6.5 6.7	 4.5 4.3	 5.4 5.4	 6.5 6.7	 4.5 4.3	 5.6 5.6	 6.5 6.7	ns
t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE)	Across P.S. and Temp C_L = 50 pF	 4.0 3.8	 5.0 5.0	 6.0 6.2	 4.0 3.8	 5.1 5.1	 6.0 6.2	 4.0 3.8	 5.5 5.5	 6.0 6.2	ns
t_{PHL}	Propagation Delay MR to Q	Across P.S. and Temp C_L = 50 pF	 2.5	 4.9	 7.0	 2.5	 5.2	 7.0	 3.0	 5.8	 7.5	ns
t_{SKEW}	Device Skew Part−to−Part (Diff) Within−Device	C_L = 50 pF		 1.0 0.3	 2.0 0.7		 1.0 0.3	 2.0 0.7		 1.0 0.3	 2.0 0.7	ns
t_S	Setup Time		1.5			1.5			1.5			ns
t_H	Hold Time		1.5			1.5			1.5			ns
t_{PW}	Minimum Pulse Width CLK		1.0			1.0			1.0			ns
t_{PW}	Minimum Pulse Width MR		1.0			1.0			1.0			ns
V_{PP}	Minimum Input Swing	Peak−to−Peak	150			150			150			mV
t_r	Rise Time	1.0 V to 2.0 V	0.7	1.0	1.5	0.7	1.0	1.5	0.7	1.0	1.5	ns
t_f	Fall Time	1.0 V to 2.0 V	0.5	0.7	1.2	0.5	0.7	1.2	0.5	0.7	1.2	ns
t_{RR}	Reset/Recovery Time		2.5			2.5			2.5			ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H605FN	PLCC−28	37 Units / Rail
MC10H605FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H605FNR2	PLCC−28	500 / Tape & Reel
MC10H605FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H605FN	PLCC−28	37 Units / Rail
MC100H605FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H605FNR2	PLCC−28	500 / Tape & Reel
MC100H605FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

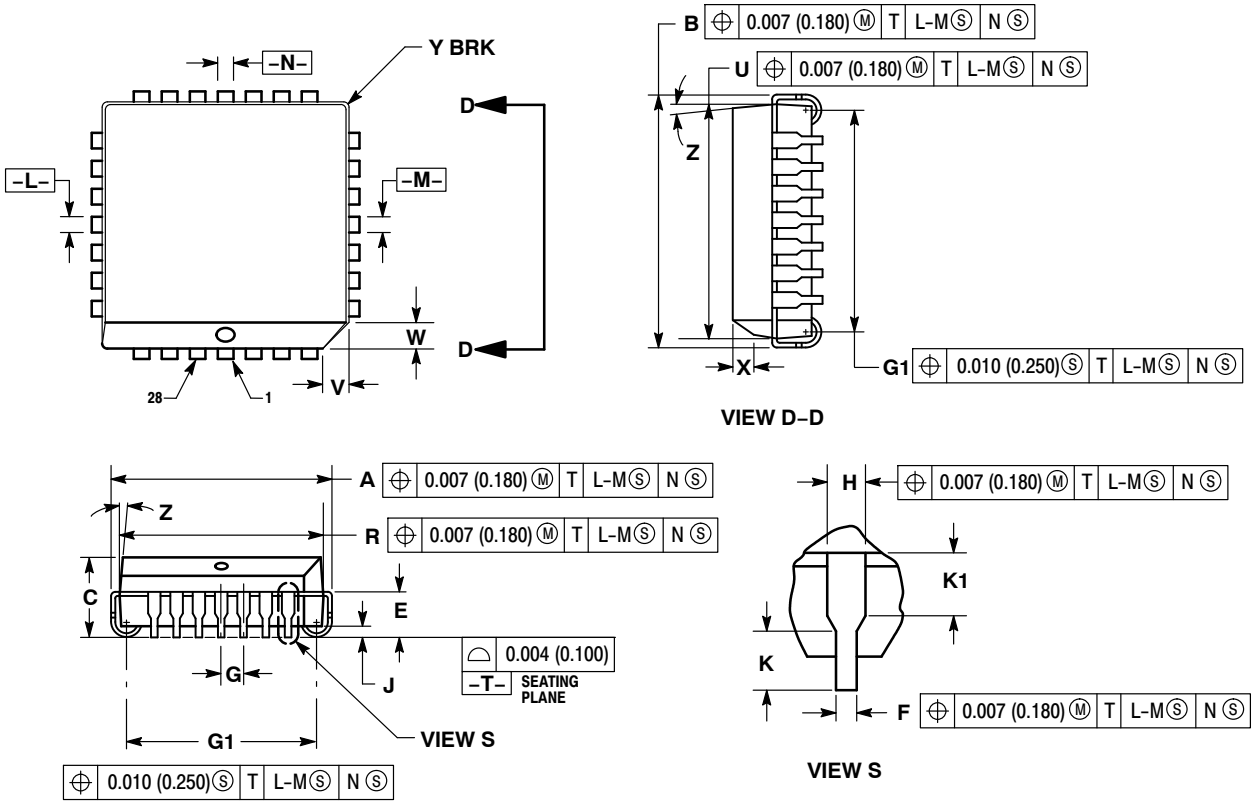
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

28 LEAD PLLC
CASE 776−02
ISSUE F



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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MECL 10H is a trademark of Motorola, Inc.

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