RTG4™ FPGA

Introduction

RTG4 FPGAs integrate Microchip's fourth-generation flash-based FPGA fabric and high-performance interfaces such as serialization/deserialization (SerDes) on a single-chip while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, deep space), high altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced single-event upsets (SEUs). Each RTG4 logic element includes a 4-input LookUp Table (LUT4) with fast carry chains providing high-performance FPGA fabric up to 300 MHz.

Multiple embedded memory options and embedded multiply-accumulate blocks perform Digital Signal Processing (DSP) up to 300 MHz. A high-speed serial interface provides 3.125 Gbps native SerDes communication, while double data rate DDR2/DDR3/LPDDR memory controllers provide high-speed memory interfaces.

Device Status

The following table lists the development status of the RTG4 FPGA devices.

Table 1. Device Status

Device	Package	Status
RT4G150	CG/LG/CB1657	Production
RT4G150	CQ352	Production
RT4G150	FCG/FC1657	Production

Note: For CQ352 package qualification, Group D5, which includes the salt atmosphere test, is only done with the device's lid face down.

Technical Briefs and Pin Descriptions

The following list shows the technical brief and pin descriptions of the RTG4 FPGAs that are published separately.

- RTG4 FPGAs Technical Brief
- RTG4 FPGA Pin Descriptions
- RTG4 Plastic Pin Assignment

Table of Contents

1. General Specifications

The following sections describe general specifications of the RTG4 FPGA devices.

1.1 Operating Conditions

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in table Recommended Operating Conditions is not implied.

Note: Stresses beyond those listed in the following table might cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD	DC FPGA core supply voltage. It must always power this pin.	–0.3	1.36	V
	AC FPGA core supply voltage[1]	–0.3	1.45	V
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V
VDDPLL	Power for eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL.	–0.3	3.63	V
SERDES_x_Lyz_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for lane-y and lane-z of SERDES_x. It is a 1.2V SerDes PMA supply.	–0.3	1.32	V
SERDES_x_Lyz_VDDAPLL	Analog power for SERDES_x PLL lanes yz. It is a 2.5V SerDes internal PLL supply.	–0.3	2.75	V
SERDES_VDDI	Power for SerDes reference clock receiver supply. Must always power this pin.	–0.3	3.63	V
VDDIx	DC FPGA I/O bank supply voltage for MSIO and JTAG I/O Banks	–0.3	3.63	V
	AC FPGA I/O buffer supply voltage for MSIO/ JTAG I/O Bank[2]	–0.3	3.75	V
	DC FPGA I/O bank supply voltage for MSIOD and DDRIO I/O Banks	–0.3	2.75	V
	AC FPGA I/O buffer supply voltage for MSIOD/ DDRIO I/O Bank[2]	–0.3	2.85	V
VI	I/O Input voltage for MSIO and JTAG I/O Banks	–0.3	3.63	V
	I/O Input voltage for MSIOD and DDRIO I/O Banks	–0.3	2.75	V
	Single ended voltage on SerDes RX pads	–0.3	1.32	V
T_{STG}	Storage temperature[3]	–65	150	°C

.....continued				
Symbol	**Parameter**	**Min**	**Max**	**Units**
T_J	Junction temperature	—	135	°C

Notes:

1. The AC transient V_{DD} limit is for radiation-induced transients less than 10 µs duration and not intended for repetitive. Core voltage that spikes from a single event transient does not negatively affect the reliability of the device if, for this non-repetitive event, the transient does not exceed 1.45V at any time and the total time that the transient exceeds 1.26V does not exceed 10 µs in duration.
2. The AC transient V_{DDI} limit is for radiation-induced transients less than 10 µs duration and not intended for repetitive.
3. For Flash programming and retention maximum limits, see table Operating Limits. The following table lists the recommended operating conditions.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
T_J	Operating junction temperature	–55	25	125	°C
	Programming junction temperature	0	25	85	°C
VDD	DC FPGA core supply voltage. It must always power this pin.	1.14	1.2	1.26	V
VPP	Power supply for charge pumps (for normal operation and programming). It must always power this pin.	3.15	3.3	3.45	V
VDDPLL	Power for eight corner PLLs, PLLs in SerDes PCIe/PCS blocks, and FDDR PLL.	3.15	3.3	3.45	V
SERDES_x_ Lyz_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for lane-y and lane-z of SERDES_x. It is a 1.2V SerDes PMA supply.	1.14	1.2	1.26	V
SERDES_x_ Lyz_VDDAPLL	Analog power for SERDES_x PLL lanes yz. It is a 2.5V SerDes internal PLL supply.	2.375	2.5	2.625	V
SERDES_VDDI	Power for SerDes reference clock receiver 1.8V supply. Must always power this pin.	1.71	1.8	1.89	V
	Power for SerDes reference clock receiver 2.5V supply. Must always power this pin.	2.375	2.5	2.625	V
	Power for SerDes reference clock receiver 3.3V supply. Must always power this pin.	3.15	3.3	3.45	V
SERDES_VREF[1]	Reference voltage for SerDes receiver reference clocks.	0.49 × SERDES_VDDI	0.5 × SERDES_VDDI	0.51 × SERDES_VDDI	V

.....continued					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**
VDDIx	1.2V DC supply voltage for FPGA I/O Banks	1.14	1.2	1.26	V
	1.5V DC supply voltage for FPGA I/O Banks	1.425	1.5	1.575	V
	1.8V DC supply voltage for FPGA and JTAG I/O Banks	1.71	1.8	1.89	V
	2.5V DC supply voltage for FPGA and JTAG I/O Banks	2.375	2.5	2.625	V
	3.3V DC supply voltage for FPGA and JTAG I/O Banks	3.15	3.3	3.45	V
	DC supply voltage for LVDS25 differential I/O Banks	2.375	2.5	2.625	V
	DC supply voltage for LVDS33 differential I/O Banks	3.15	3.3	3.45	V
	DC supply voltage for BLVDS, MLVDS, Mini-LVDS, and RSDS differential I/O Banks	2.375	2.5	2.625	V
	DC supply voltage for LVPECL differential I/O Banks	3.15	3.3	3.45	V

Note:

1. Maximum input leakage current for SERDES_VREF is 10 µA.

The recommended power supply tolerances in the preceeding table include DC offset of the supply plus any power supply ripple over the customer design frequencies of interest, as measured at the device package pins. An example for a valid power supply that meets the recommendations for the VDD supply is 1.2 V ±2% for DC offset with an additional power supply ripple of ±3% for a total of 1.2 V ±5%.

For more information about power supply grouping requirements, see AC439: Board Design Guidelines for RTG4 FPGA Application Note. Power supply ramps must all be strictly monotonic and without plateaus.

Table 1-3. Operating Limits

Programming Temperature	Operating Temperature	Programming Cycles	Verify Cycles per Program Cycle	In-Flight Reprogramming TID (Maximum)	Retention[1] (Biased/ Unbiased)
Min T_J = 0 °C Max T_J = 85 °C	Min T_J = –55 °C Max T_J = 125 °C	200	200	50 Krad	10 years

Notes:

1. For retention limits at other T_J points, see Table 1-4 and Figure 1-1.
2. Stand-alone verify must be performed immediately after in-flight programming to ensure programming integrity. For more information, see UG0602: RTG4 FPGA Programming User Guide. When not performing in-flight programming, stand-alone verify must not be attempted after the part has been deployed in space or exposed to radiation as it might result in false failures.

3. Stand-alone erase is not required because erase is always performed on RTG4 devices prior to programming. If a stand-alone erase is applied, it increases the programming cycle count by two. For flight units, ensure that the programming cycle count stays within 200 cycles including program and stand-alone erase cycles.
4. RTG4 µPROM has an unlimited number of read cycles. The µPROM write cycle limit, retention limit, in-flight reprogramming TID, and verify cycles per program cycle limit is the same as the FPGA fabric programming cycles listed in Table 1-3 (since it's part of the fabric).

The following table and figure show retention at different junction temperatures.

Table 1-4. High Temperature Data Retention (HTR) Lifetime

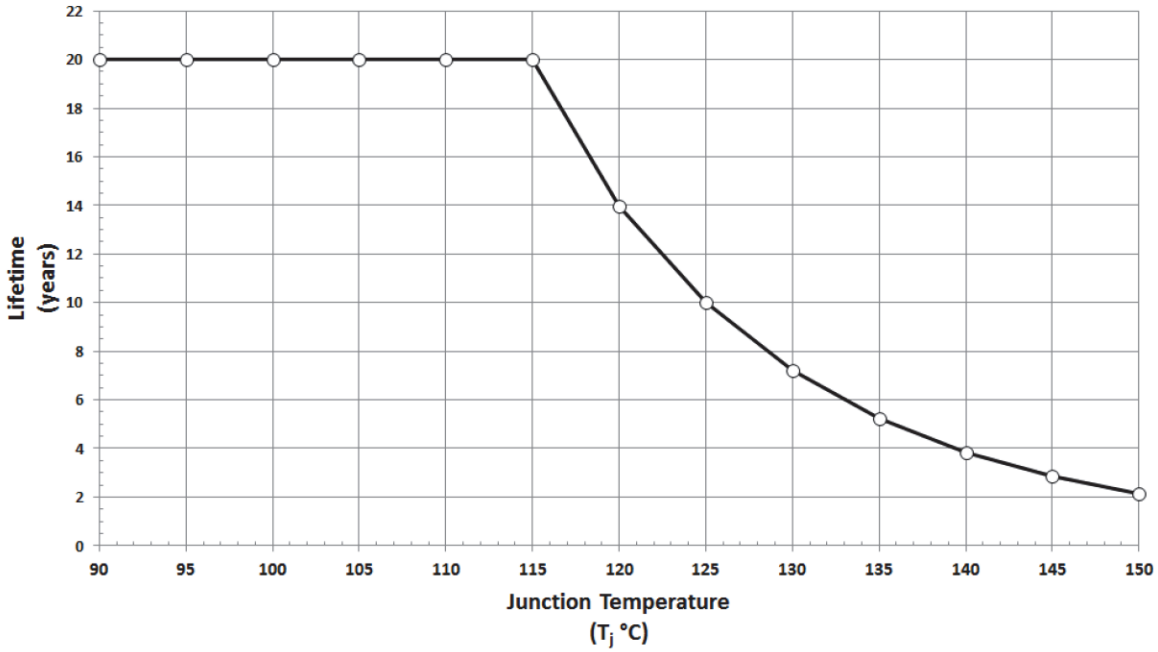
Tj (°C)	Flash HTR[1] (Years)
90	20
95	20
100	20
105	20
110	20
115	20
120	14
125	10
130	7.2
135	5.3
140	3.9
145	2.8
150	2.1

Note:

1. HTR lifetime is the period during which a verify failure is not expected due to flash leakage.

The following figure shows HTR (derived junction temperature versus lifetime).

Figure 1-1. High Temperature Data Retention (HTR) Lifetime



1.1.1 Overshoot/Undershoot Limits

For AC signals, the input signal might undershoot during transitions to –0.8V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

For AC signals, the input signal might overshoot during transitions to V_{DDIx} + 0.8V for no longer than 10% of the period. The current during the transition must not exceed 100 mA.

Note: The preceeding specification does not apply to the PCI standard. The RTG4 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

1.1.2 Power-Up and Power-Down Sequence

The following sections show the power-up and power-down sequences of the RTG4 FPGA devices.

1.1.2.1 Power-Up Sequence

VDDPLL Requirements

No power-up sequence is required if the device is held in reset by asserting DEVRST_N until V_{DDPLL} supplies reach their minimum recommended level as shown in Recommended Operating Conditions.

If the device cannot be held in reset, either of the following power-up requirements apply.

- All PLLs are held in reset until V_{DDPLL} supply reaches its minimum recommended level. To meet this requirement, see the UG0586: RTG4 Clocking Resources User Guide for suggested methods using the READY_VDDPLL input to the RTG4 Fabric CCC.
- V_{DDPLL} must not be the last supply to ramp up and must reach its minimum recommended level before the last supply (V_{DD} or V_{DDIx}) starts ramping up.

SERDES_x_Lyz_VDDAIO Requirements

No power-up sequence occurs if SERDES_x_Lyz_VDDAIO supplies are tied to V_{DD}. If SERDES_x_Lyz_VDDAIO and V_{DD} cannot be tied together, then the SERDES_x_Lyz_VDDAIO must be powered up at the same time as V_{DD}.

For more information, see the AC439: Board Design Guidelines for RTG4 FPGA Application Note and the associated AC439 Addendum.

1.1.2.2 Power-Down Sequence

There is no power-down sequence if an external 1 kΩ pull-down resistor is used for each critical output, which cannot tolerate an output glitch during power-down or DEVRST_N assertion. If an external resistor cannot be used, either of the following requirements apply.

- V_{DDIx} supplies are powered down first all the way to 0V.
- V_{PP} is powered down last.

If V_{PP} or V_{DD} falls below the minimum recommended level, then both V_{PP} and V_{DD} must be powered down all the way to 0V before powering back up. Powering down V_{PP} without powering down V_{DD} is not allowed.

For more information, see the AC439: Board Design Guidelines for RTG4 FPGA Application Note and the associated AC439 Addendum.

1.1.3 Thermal Characteristics

The temperature variable in the Microchip SoC Products Group Libero® SoC software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

The following equations show the relationship between thermal resistance, temperature gradient, and power.

$\Theta_{JB} = (T_J – T_B)/P$

$\Theta_{JC} = (T_J – T_c)/P$

where:

Θ_{JB} = Junction-to-board thermal resistance

Θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

The following table lists the details of package thermal resistance.

Table 1-5. Package Thermal Resistance

RTG4 Product	Θ_{JA}	Θ_{JB}	Θ_{JC}	Units
CCGA1657[1, 2, 4]	7.75	2.50	0.33	°C/W
LGA1657[1, 3, 4]	7.77	0.22	0.33	°C/W
CQFP352[1, 3, 4]	7.85	0.26	3.12	°C/W
FCG/FC1657[1, 2, 4]	7.52	1.31	0.075	°C/W

Notes: Theta-JC and Theta-JB values are simulated with conduction heat transfer only.

1. Theta-JA values are simulated for still air.
2. Theta-JB for CCGA1657 and FCG/FC1657 refers to the thermal resistance between the junction to the board as defined in the JESD51 standards.
3. Theta-JB for CQFP352 and LGA1657 refers to the thermal resistance between the junction and the bottom surface of the package.
4. Theta-JC refers to the thermal resistance between the junction and the top surface (package lid).

1.1.3.1 Theta-JB

Junction-to-board thermal resistance (Θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

1.1.3.2 Theta-JC

Junction-to-case thermal resistance (Θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface under consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface under consideration.

2. Power Consumption

The following sections describe the power consumption of the RTG4 FPGA devices.

2.1 Quiescent Supply Current

Table 2-1. Quiescent Supply Current Characteristics

Power Supplies/Blocks	Standby Mode
FPGA Core VDD	On
VPP	On
VDDPLL	0V
SERDES_x_Lyz_VDDAPLL[1]	0V
SERDES_x_Lyz_VDDAIO[1]	On
VDDIx[2, 3]	On
VREF0, VREF9[4]	On
50 MHz Oscillator	Enabled

Notes:

1. SerDes and DDR blocks are in RESET states.
2. V_{DDIx} supplies to all I/O Banks are set to ON in standby mode.
3. No differential I/O or On-Die Termination (ODT) resistor is used.
4. Maximum input leakage current for $V_{REF}0$ and $V_{REF}9$ is 10 µA.

Table 2-2. RTG4 Quiescent Supply Current

Devices	Conditions	IDC[1]	Units
RT4G150	Typical (T_J = 25 °C), VDD = 1.2V	410	mA
	Worst-case (T_J = 125 °C), VDD = 1.26V	4100	mA
RT4G150L	Typical (T_J = 25 °C), VDD = 1.2V	310	mA
	Worst-case (T_J = 125 °C), VDD = 1.26V	3100	mA

Note:

1. IDC is the current measured on the V_{DD} supply in standby mode.

2.1.1 Programming Currents

The following table lists the device programming currents. Worst-case conditions: 0 °C ≤ T_J ≤ 85 °C.

Table 2-3. Programming Currents

Supply	Voltage (V)	Programming Current (mA)
VDD	1.14	756
VDDI	2.375	41

.....continued		
Supply	**Voltage (V)**	**Programming Current (mA)**
VDDPLL	3.15	1
VPP	3.15	6
SerDes VDDAIO	1.14	5
SerDes VDDI	2.375	2
SerDes VDDAPLL	2.375	1

3. Junction Temperature and Derating Factors

The following table lists the junction temperature and derating factors for fabric timing delays normalized to T_J = 125 °C. In worst-case, V_{DD} = 1.14V.

Table 3-1. JunctionTemperature and Voltage Derating Factors for Fabric Timing Delays

Core Voltage VDD (V)	–55 °C	–40 °C	0 °C	25 °C	70 °C	85 °C	100 °C	125 °C
1.14	0.83	0.84	0.89	0.91	0.93	0.97	0.97	1.00
1.2	0.79	0.80	0.84	0.86	0.88	0.91	0.92	0.95
1.26	0.75	0.76	0.80	0.82	0.84	0.87	0.88	0.90

4. User I/O Characteristics

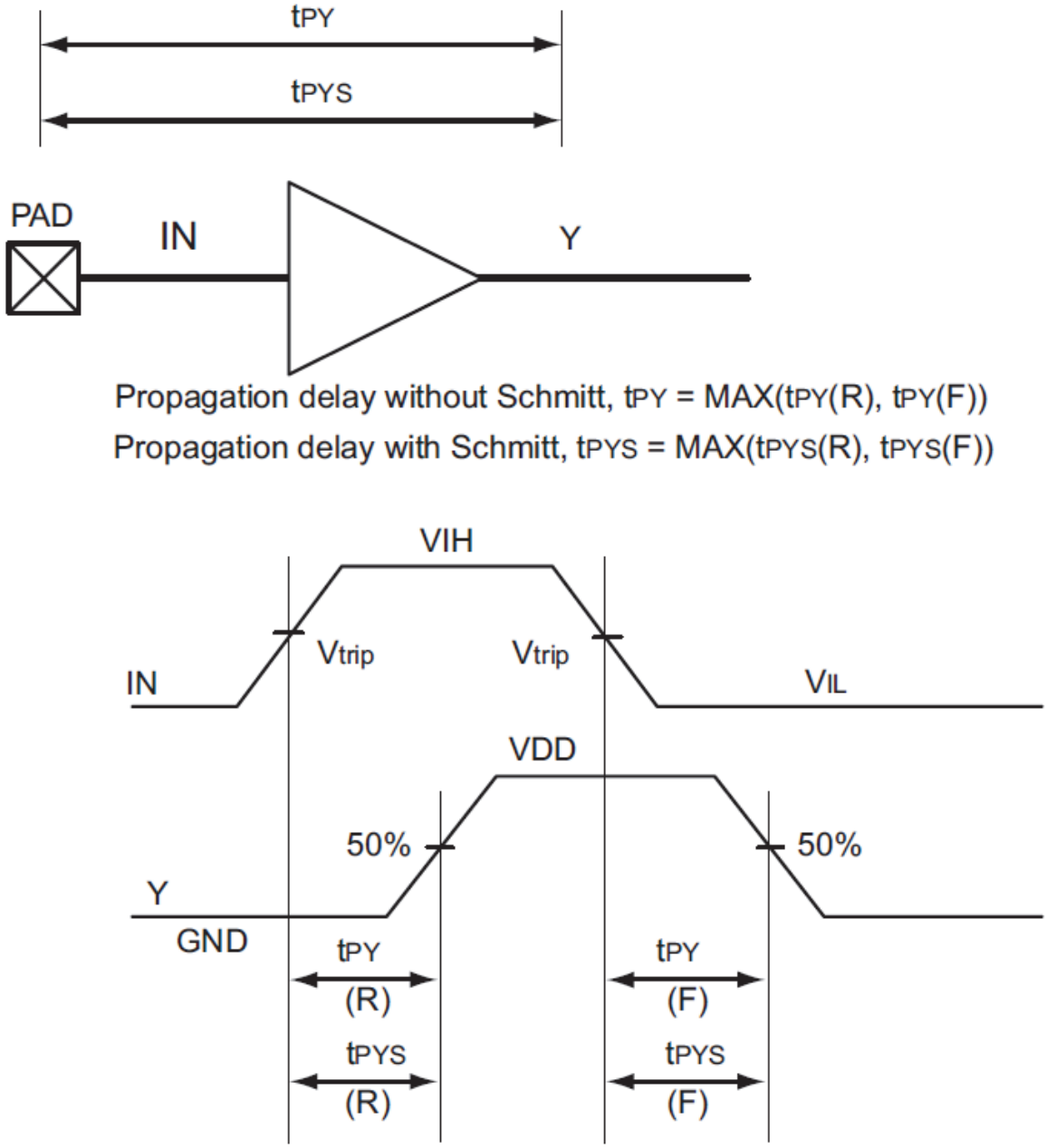
Three types of I/Os supported in the RTG4 FPGA families are: MSIO, MSIOD, and DDRIO. The I/O standards supported by the different I/O banks is described in the UG0741: RTG4 FPGA I/O User Guide. The Libero SoC automatically configures unused user I/Os with the input buffer disabled and output buffer tristated with weak pull-up enabled.

For information about I/O states during programming, see the UG0602: RTG4 FPGA Programming User's Guide.

4.1 Input Buffer

The following figure shows the input buffer delays.

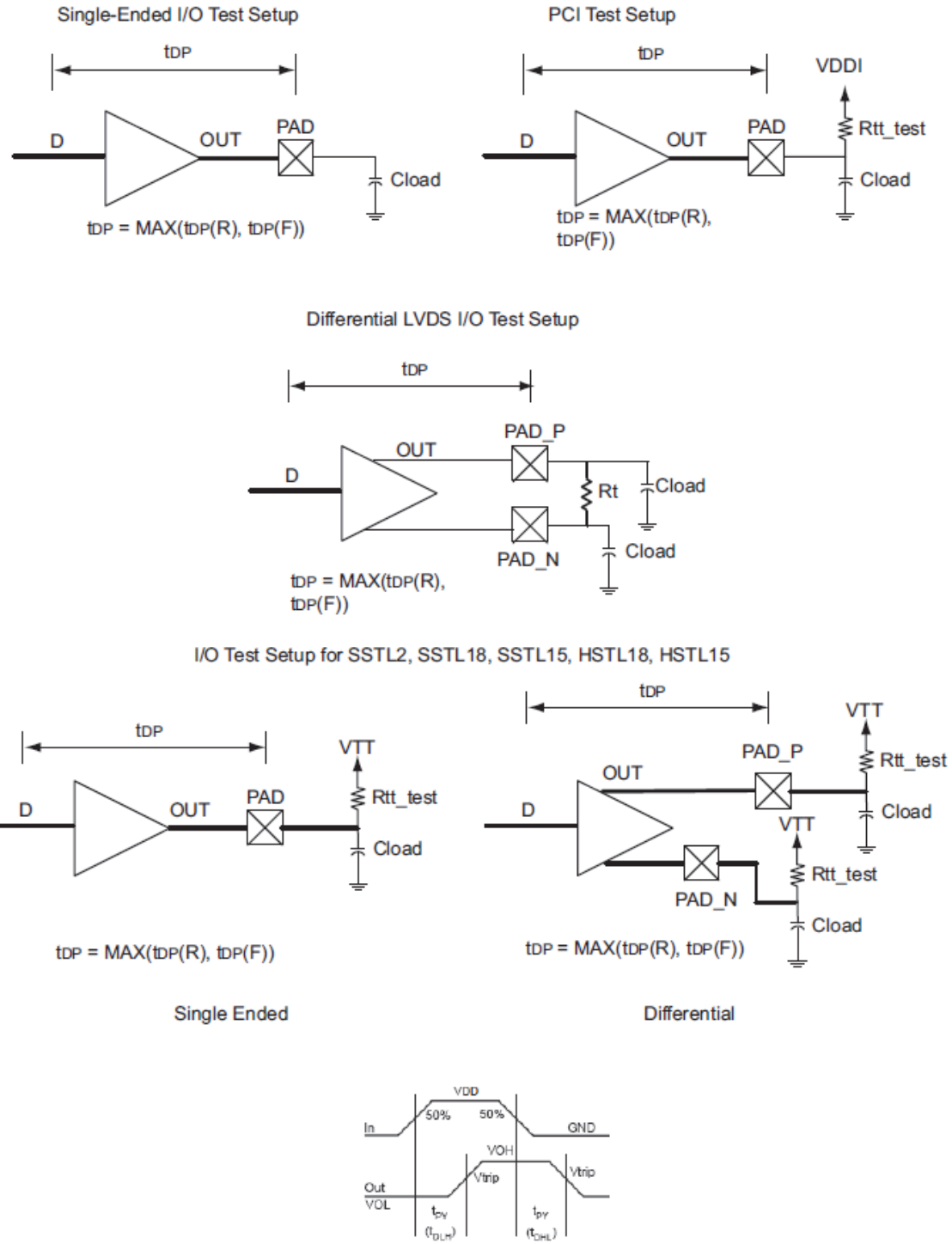
Figure 4-1. Input Buffer



4.2 Output Buffer and AC Loading

The following figure shows the output buffer delays and AC loading.

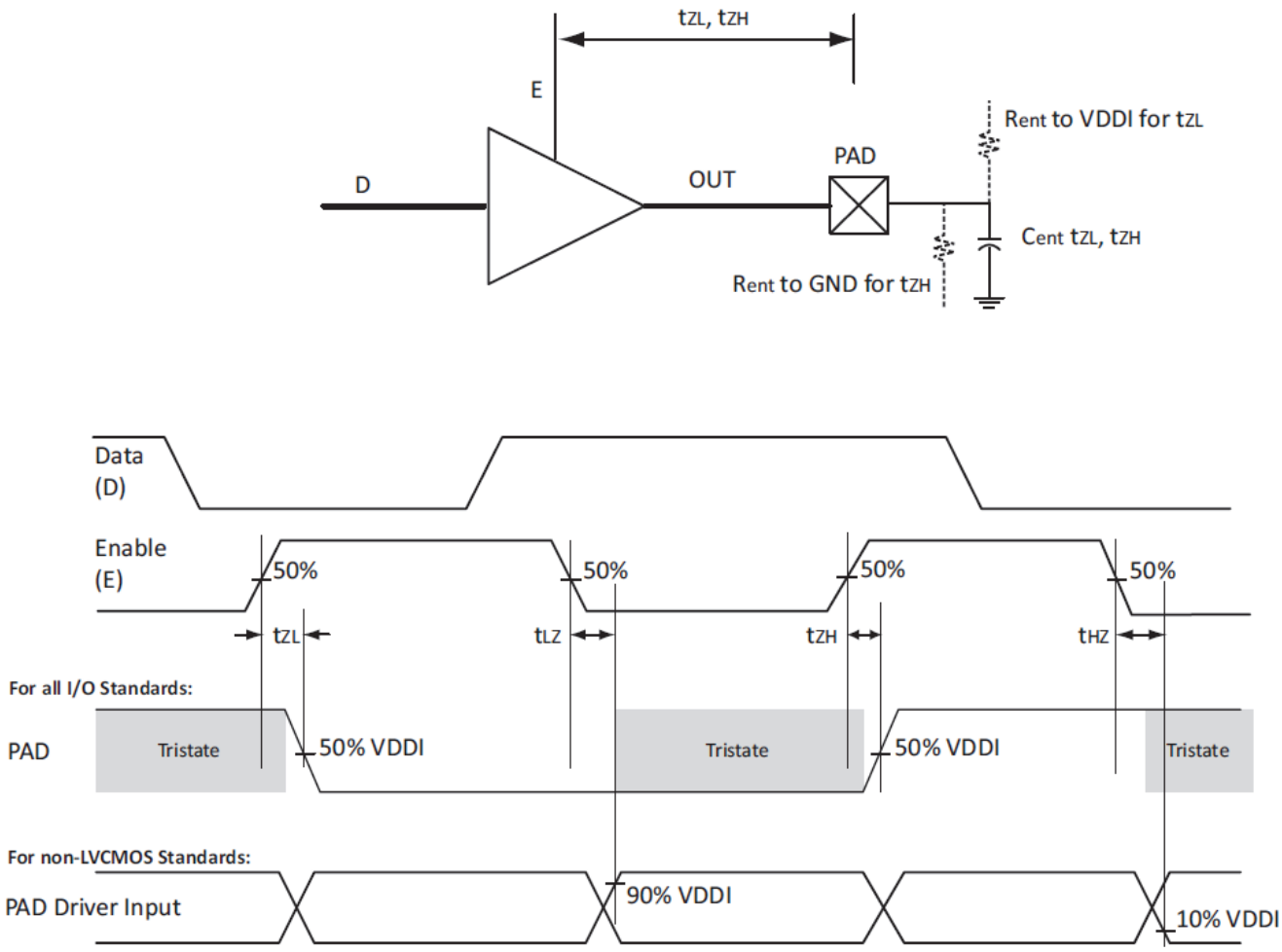
Figure 4-2. Output Buffer and AC Loading



4.3 Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The following figure shows the methodology of characterization illustrated by the enable path test point.

Figure 4-3. Tristate Buffer for Enable Path Test Point



Note: For LVTTL/LVCMOS standards: tLZ and tHZ = Time taken from 50% of enable de-assertion to driver leakage current reduction to 10 µA or less.

4.4 I/O Speeds

The following section describes the maximum data rate summary of I/O in worst-case military conditions.

T_J = 125 °C, V_{DD} = 1.14V, and V_{DDIx} at minimum recommended value shown in Recommended Operating Conditions is for respective I/O standard.

Table 4-1. Maximum I/O Data Rate for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3V	630	—	—	Mbps
LVTTL 3.3V	600	—	—	Mbps
LVCMOS 3.3V	600	—	—	Mbps
LVCMOS 2.5V	410	420	700	Mbps
LVCMOS 1.8V	295	320	700	Mbps
LVCMOS 1.5V	200	200	400	Mbps
LVCMOS 1.2V	140	140	360	Mbps
LPDDR–LVCMOS 1.8V mode	—	—	266	Mbps
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	—	—	266	Mbps
HSTL1.5V Class I	140	180	400	Mbps
HSTL1.5V Class II	—	—	400	Mbps
HSTL 1.8V	432	432	500	Mbps
SSTL 2.5V	575	700	800	Mbps
SSTL 1.8V	432	430	800	Mbps
SSTL 1.5V	—	—	800	Mbps
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	700	—	—	Mbps
LVDS 3.3V	700	—	—	Mbps
LVDS 2.5V	750	750	—	Mbps
RSDS	520	700	—	Mbps
BLVDS	500	500	—	Mbps
MLVDS	500	500	—	Mbps
Mini-LVDS	520	700	—	Mbps
HCSL (input only)	350	350	—	Mbps

Table 4-2. Maximum I/O Frequency Summary for Worst-Case Military Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3V	315	—	—	MHz
LVTTL 3.3V	300	—	—	MHz
LVCMOS 3.3V	300	—	—	MHz
LVCMOS 2.5V	205	210	350	MHz
LVCMOS 1.8V	147.5	160	350	MHz
LVCMOS 1.5V	100	100	200	MHz
LVCMOS 1.2V	70	70	180	MHz
LPDDR–LVCMOS 1.8V mode	—	—	133	MHz
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	—	—	133	MHz
HSTL1.5V Class I	70	90	200	MHz
HSTL1.5V Class II	—	—	200	MHz
HSTL 1.8V	216	216	250	MHz
SSTL 2.5V	287.5	350	400	MHz
SSTL 1.8V	216	215	400	MHz
SSTL 1.5V	—	—	400	MHz
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	350	—	—	MHz
LVDS 3.3V	350	—	—	MHz
LVDS 2.5V	375	375	—	MHz
RSDS	260	350	—	MHz
BLVDS	250	250	—	MHz
MLVDS	250	250	—	MHz
Mini-LVDS	260	350	—	MHz
HCSL (input only)	175	175	—	MHz

4.5 Detailed I/O Characteristics

The following section shows the I/O characteristics of the RTG4 FPGA devices.

Table 4-3. Input Capacitance

Symbol	Definition	Min	Max	Units
CIN	Input capacitance	—	20	pF
T_{RAMPIN} [1]	Input ramp time (Applicable to all digital inputs)	—	50	ns

Note:

1. Voltage ramp must be monotonic.

Table 4-4. I/O Weak Pull-Up/Pull-Down Resistance Values for DDRIO, MSIO, and MSIOD Banks

VDDI	DDRIO I/O Bank				MSIO I/O Bank				MSIOD I/O Bank			
	$R_{(WEAK\ PULL\text{-}UP)}$ at VOH KΩ		$R_{(WEAK\ PULL\text{-}DOWN)}$ at VOL KΩ		$R_{(WEAK\ PULL\text{-}UP)}$ at VOH KΩ		$R_{(WEAK\ PULL\text{-}DOWN)}$ at VOL KΩ		$R_{(WEAK\ PULL\text{-}UP)}$ at VOL KΩ		$R_{(WEAK\ PULL\text{-}DOWN)}$ at VOL KΩ	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
3.3V	—	—	—	—	9.9	17.1	9.98	17.5	—	—	—	—
2.5V	9.98	17.8	10	18	10	17.6	10.1	18.4	9.6	16.6	9.5	16.4
1.8V	11.1	19.1	11.2	19.5	10.4	19.1	10.4	20.4	9.7	17.3	9.7	17.1
1.5V	10	20.2	9.99	21.1	10.7	20.4	10.8	22.2	9.9	18	9.8	17.6
1.2V	10.3	22.7	10.3	24.6	11.3	23.2	11.5	26.7	10.3	19.6	10	19.1

Notes:

- $R_{(WEAK\ PULL–DOWN\ MAX)} = (VOLspec)/I_{(WEAK\ PULL–DOWN\ MIN)}$
- $R_{(WEAK\ PULL\text{-}UP\ MAX)} = (VDDImax–VOHspec)/I_{(WEAK\ PULL\text{-}UP\ MIN)}$

The following table lists the hysteresis voltage value for schmitt trigger mode input buffers.

Table 4-5. Schmitt Trigger Input Hysteresis

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3V LVTTL/LVCMOS/PCI/PCI-X	0.05 × V_{DDI} (worst-case)
2.5V LVCMOS	0.05 × V_{DDI} (worst-case)
1.8V LVCMOS	0.05 × V_{DDI} (worst-case)
1.5V LVCMOS	60 mV
1.2V LVCMOS	20 mV

4.6 Single-Ended I/O Standards

The follwoing sections describe the single-ended I/O standards of the RTG4 FPGA devices.

4.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in RTG4 FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

4.6.2 3.3V LVCMOS/LVTTL

LVCMOS 3.3V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3V applications.

4.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

All edits in the following table are as per SAR 114840.

Table 4-6. LVTTL/LVCMOS 3.3V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3V Recommended DC Operating Conditions						
VDDI	Supply voltage	—	3.15	3.3	3.45	V
LVTTL/LVCMOS 3.3V DC Input Voltage Specification						
VIH (DC)	DC input logic high	—	2.0	—	3.45	V
VIL (DC)	DC input logic low	—	–0.3	—	0.8	V
IIH (DC)	Input leakage current high	—	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	—	10	µA
LVCMOS 3.3V DC Output Voltage Specification[1]						
VOH	DC output logic high	IOH = 100 µA	VDDI – 0.2	—	—	V
		IOH ≥ 2 mA	2.4	—	—	V
VOL	DC output logic low	IOL = 100 µA	—	—	0.2	V
		IOL ≥ 2 mA	—	—	0.4	V
LVTTL 3.3V DC Output Voltage Specification						
VOH	DC output logic high	—	2.4	—	—	V
VOL	DC output logic low	—	—	—	0.4	V

Note:

1. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3V JESD8-B requirements.

Table 4-7. LVTTL/LVCMOS 3.3V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for MSIO I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	600	Mbps

Table 4-8. LVTTL/LVCMOS 3.3V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

Symbol	Parameters	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path	—	1.4	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})	—	5	—	pF

Table 4-9. LVTTL/LVCMOS 3.3V Transmitter Drive Strength Specifications (Applicable to MSIO Bank Only)

Output Drive Selection	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	VDDI–0.2	0.2	0.1	0.1
2 mA	2.4	0.4	2	2
4 mA	2.4	0.4	4	4
8 mA	2.4	0.4	8	8
12 mA	2.4	0.4	12	12
16 mA	2.4	0.4	16	16

4.6.2.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 3.15V.

Table 4-10. LVTTL/LVCMOS 3.3V Receiver Characteristics (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY}		t_{PYS}		Units
		Speed Grade –1	Speed Grade STD	Speed Grade –1	Speed Grade STD	
MSIO	None	1.993	2.345	2.122	2.497	ns

Table 4-11. LVTTL/LVCMOS 3.3V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Output Drive Selection	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade 1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade 1	t_{LZ} Speed Grade STD	Units
2 mA	4.324	5.086	4.456	5.242	3.633	4.274	3.157	3.714	2.872	3.379	ns
4 mA	3.199	3.763	3.264	3.840	2.904	3.417	3.255	3.828	2.895	3.405	ns
8 mA	2.653	3.120	2.682	3.156	2.548	2.998	3.408	4.008	2.975	3.499	ns
12 mA	2.505	2.946	2.491	2.931	2.438	2.868	3.510	4.129	2.999	3.528	ns
16 mA	2.461	2.894	2.399	2.823	2.388	2.809	3.525	4.147	3.107	3.655	ns

4.6.3 2.5V LVCMOS

LVCMOS 2.5V is a general standard for 2.5V applications and is supported in RTG4 FPGAs in compliance to the JEDEC specification JESD8-5A.

4.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 4-12. LVCMOS 2.5V DC Voltage Specification

Symbol	Parameters	Min	Typ	Max	Units
LVCMOS 2.5V Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
LVCMOS 2.5V DC Input Voltage Specification					
VIH (DC)	DC input logic high	1.7	—	2.625	V
VIL (DC)	DC input logic low	–0.3	—	0.7	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LVCMOS 2.5V DC Output Voltage Specification[1]					
VOH	DC output logic high	VDDI – 0.4	—	—	V
VOL	DC output logic low	—	—	0.4	V

Note:

1. The selected V_{OH}/V_{OL} test points ensure compliance with the LVCMOS 2.5V JEDEC8-5A requirements.

Table 4-13. LVCMOS 2.5V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	700	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	410	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	420	Mbps

Table 4-14. LVCMOS 2.5V AC Test Parameters and Driver Impedance Specifications

Symbol	Parameters	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path	—	1.2	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})	—	5	—	pF

Table 4-15. LVCMOS 2.5V Transmitter Drive Strength Specifications

MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Software Default Fixed Calibration Codes)	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	2 mA	2 mA	VDDI–0.4	0.4	2	2
4 mA	4 mA	4 mA	VDDI–0.4	0.4	4	4
6 mA	6 mA	6 mA	VDDI–0.4	0.4	6	6
8 mA	8 mA	8 mA	VDDI–0.4	0.4	8	8
—	10 mA	—	VDDI–0.4	0.4	10	10
12 mA	—	12 mA	VDDI–0.4	0.4	12	12
14 mA	—	—	VDDI–0.4	0.4	14	14
—	—	16 mA	VDDI–0.4	0.4	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at www.microchip.com.

4.6.3.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-16. LVCMOS 2.5V AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	t_{PYS} Speed Grade –1	t_{PYS} Speed Grade STD	Units
DDRIO	None	0.877	1.032	0.877	1.032	ns
MSIO	None	1.951	2.296	2.000	2.353	ns
MSIOD	None	1.721	2.025	1.785	2.100	ns

Table 4-17. LVCMOS 2.5V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Output Drive Selection	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
LVCMOS 2.5V (for DDRIO I/O Bank with Fixed Code)											
2 mA	3.574	4.205	3.521	4.141	3.394	3.992	3.279	3.857	3.129	3.680	ns
4 mA	3.052	3.590	2.958	3.479	2.929	3.446	3.367	3.961	3.140	3.693	ns
6 mA	2.894	3.405	2.779	3.269	2.781	3.271	3.483	4.098	3.260	3.835	ns
8 mA	2.853	3.357	2.729	3.210	2.739	3.221	3.531	4.154	3.297	3.879	ns
12 mA	2.747	3.232	2.615	3.076	2.631	3.094	3.535	4.158	3.292	3.872	ns
16 mA	2.692	3.167	2.545	2.993	2.569	3.021	3.611	4.248	3.350	3.941	ns

.....continued

Output Drive Selection	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
LVCMOS 2.5V (for MSIO I/O Bank)											
2 mA	4.752	5.590	4.867	5.726	4.582	5.391	3.600	4.235	3.253	3.827	ns
4 mA	3.232	3.802	3.257	3.832	3.217	3.786	3.704	4.358	3.338	3.927	ns
6 mA	3.050	3.588	3.060	3.600	3.054	3.593	3.807	4.479	3.361	3.954	ns
8 mA	2.944	3.463	2.945	3.465	2.961	3.483	3.835	4.512	3.370	3.965	ns
12 mA	2.897	3.407	2.815	3.312	2.854	3.358	3.886	4.572	3.385	3.982	ns
16 mA	2.884	3.392	2.776	3.266	2.824	3.322	3.912	4.602	3.427	4.031	ns
LVCMOS 2.5V (for MSIOD I/O Bank)											
2 mA	2.613	3.074	3.356	3.949	3.295	3.876	2.754	3.239	2.513	2.956	ns
4 mA	2.129	2.504	2.772	3.261	2.776	3.266	2.751	3.236	2.515	2.959	ns
6 mA	1.831	2.153	2.409	2.834	2.461	2.896	2.778	3.268	2.535	2.982	ns
8 mA	1.789	2.104	2.262	2.661	2.330	2.741	2.817	3.313	2.557	3.008	ns
10 mA	1.807	2.125	2.246	2.642	2.317	2.727	2.838	3.338	2.563	3.015	ns

4.6.4 1.8V LVCMOS

LVCMOS 1.8 is a general standard for 1.8V applications and is supported in RTG4 FPGAs in compliance to the JEDEC specification JESD8-7A.

4.6.4.1 Minimum and Maximum AC/DC Input and Output Levels

Table 4-18. LVCMOS 1.8V DC Voltage Specification

Symbol	Parameters	Min	Typ	Max	Units
LVCMOS 1.8V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.710	1.8	1.89	V
LVCMOS 1.8V DC Input Voltage Specification					
VIH (DC)	DC input logic high	0.65 × VDDI	—	1.89	V
VIL (DC)	DC input logic low	–0.3	—	0.35 × VDDI	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LVCMOS 2.5V DC Output Voltage Specification					
VOH	DC output logic high	VDDI – 0.45	—	—	V

.....continued					
Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Units**
VOL	DC output logic low	—	—	0.45	V

Table 4-19. LVCMOS 1.8V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive and slew	—	—	700	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	295	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC Loading: 10 pF/500Ω load, maximum drive	—	—	320	Mbps

Table 4-20. LVCMOS 1.8V Transmitter Drive Strength Specifications

MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	2 mA	2 mA	VDDI–0.45	0.45	2	2
4 mA	4 mA	4 mA	VDDI–0.45	0.45	4	4
6 mA	6 mA	6 mA	VDDI–0.45	0.45	6	6
8 mA	8 mA	8 mA	VDDI–0.45	0.45	8	8
10 mA	—	10 mA	VDDI–0.45	0.45	10	10
12 mA	—	12 mA	VDDI–0.45	0.45	12	12
—	—	16 mA	VDDI–0.45	0.45	16	16

Table 4-21. LVCMOS 1.8V AC Test Parameters and Driver Impedance Specifications

Symbol	Parameters	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path	—	0.9	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})	—	5	—	pF

4.6.4.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.71V.

Table 4-22. LVCMOS 1.8V AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	t_{PYS} Speed Grade –1	t_{PYS} Speed Grade STD	Units
DDRIO with fixed codes	None	1.028	1.209	1.028	1.209	ns
MSIO	None	2.261	2.660	2.253	2.650	ns
MSIOD	None	1.966	2.314	1.961	2.308	ns

Table 4-23. LVCMOS 1.8V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Output Drive Selection	Slew Control	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
LVCMOS 1.8V (for DDRIO I/O Bank with Fixed Code)												
2 mA	Slow	4.088	4.809	4.054	4.769	4.101	4.824	3.815	4.489	3.609	4.246	ns
	Med.	3.710	4.364	3.685	4.336	3.670	4.317	3.203	3.768	3.009	3.541	ns
4 mA	Slow	3.757	4.419	3.692	4.343	3.752	4.414	3.952	4.649	3.751	4.413	ns
	Med.	3.373	3.968	3.331	3.918	3.328	3.915	3.288	3.869	3.072	3.614	ns
6 mA	Slow	3.438	4.045	3.357	3.949	3.424	4.028	4.026	4.737	3.783	4.450	ns
	Med.	3.086	3.630	3.030	3.564	3.035	3.570	3.319	3.906	3.080	3.624	ns
8 mA	Slow	3.362	3.955	3.272	3.849	3.345	3.935	4.073	4.792	3.799	4.470	ns
	Med.	3.015	3.546	2.955	3.476	2.966	3.490	3.338	3.928	3.096	3.643	ns
10 mA	Slow	3.228	3.797	3.146	3.701	3.205	3.771	4.077	4.797	3.788	4.456	ns
	Med.	2.917	3.431	2.855	3.359	2.848	3.350	3.331	3.919	3.080	3.624	ns
12 mA	Slow	3.179	3.739	3.087	3.631	3.150	3.706	4.155	4.888	3.881	4.566	ns
	Med.	2.870	3.376	2.802	3.296	2.802	3.296	3.383	3.980	3.130	3.683	ns
16 mA	Slow	3.126	3.677	3.025	3.559	3.087	3.632	4.237	4.986	3.948	4.645	ns
	Med.	2.826	3.324	2.750	3.235	2.752	3.238	3.415	4.018	3.158	3.716	ns
LVCMOS 1.8V (for MSIO I/O Bank)												
2 mA	Default	4.936	5.808	5.003	5.885	4.975	5.852	4.761	5.601	4.308	5.068	ns
4 mA	Default	4.457	5.244	4.467	5.254	4.472	5.261	4.803	5.650	4.351	5.118	ns
6 mA	Default	4.219	4.964	4.201	4.941	4.230	4.975	4.878	5.737	4.379	5.151	ns

.....continued												
Output Drive Selection	Slew Control	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
8 mA	Default	4.049	4.764	3.942	4.637	3.995	4.699	4.897	5.760	4.374	5.145	ns
10 mA	Default	4.030	4.742	3.869	4.550	3.932	4.625	4.946	5.818	4.391	5.165	ns
12 mA	Default	4.017	4.727	3.817	4.489	3.888	4.573	4.964	5.839	4.367	5.137	ns
LVCMOS 1.8V (for MSIOD I/O Bank)												
2 mA	Default	3.287	3.867	4.112	4.837	4.358	5.127	3.301	3.884	3.007	3.538	ns
4 mA	Default	2.407	2.831	3.218	3.785	3.421	4.024	3.344	3.934	3.032	3.567	ns
6 mA	Default	2.245	2.641	2.936	3.454	3.128	3.679	3.385	3.982	3.054	3.593	ns
8 mA	Default	2.227	2.620	2.806	3.300	2.999	3.527	3.384	3.981	3.056	3.595	ns

4.6.5 1.5V LVCMOS

LVCMOS 1.5 is a general standard for 1.5V applications and is supported in RTG4 FPGAs in compliance to the JEDEC specification JESD8-11A.

4.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 4-24. LVCMOS 1.5V Minimum and Maximum DC Input and Output Levels

Symbol	Parameters	Min	Typ	Max	Units
LVCMOS 1.5V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5V DC Input Voltage Specification					
VIH (DC)	DC input logic high	0.65 × VDDI	—	1.575	V
VIL (DC)	DC input logic low	–0.3	—	0.35 × VDDI	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LVCMOS 1.5V DC Output Voltage Specification					
VOH	DC output logic high	VDDI × 0.75	—	—	V
VOL	DC output logic low	—	—	VDDI × 0.25	V

Table 4-25. LVCMOS 1.5V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 5 pF load/ maximum drive/fast slew	—	—	400	Mbps

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 5 pF load/ maximum drive	—	—	200	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 5 pF/maximum drive	—	—	200	Mbps

Table 4-26. LVCMOS 1.5V AC Test Parameters and Driver Impedance Specifications

Symbol	Parameters	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path	—	0.75	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})	—	5	—	pF

Table 4-27. LVCMOS 1.5V Transmitter Drive Strength Specifications

MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
6 mA	6 mA	6 mA	VDDI × 0.75	VDDI × 0.25	6	6
8 mA	—	8 mA	VDDI × 0.75	VDDI × 0.25	8	8
—	—	10 mA	VDDI × 0.75	VDDI × 0.25	10	10
—	—	12 mA	VDDI × 0.75	VDDI × 0.25	12	12

4.6.5.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.425V.

Table 4-28. LVCMOS 1.5V AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	t_{PYS} Speed Grade –1	t_{PYS} Speed Grade STD	Units
DDRIO with fixed codes	None	1.155	1.359	1.155	1.359	ns
MSIO	None	2.523	2.968	2.500	2.941	ns
MSIOD	None	2.130	2.505	2.117	2.490	ns

Table 4-29. LVCMOS 1.5V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Output Drive Selection	Slew Control	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
LVCMOS 1.5V (for DDRIO I/O Bank with Fixed Code)												
2 mA	Slow	4.823	5.673	4.774	5.617	4.851	5.707	4.357	5.125	4.086	4.808	ns
	Med.	4.283	5.040	4.274	5.028	4.285	5.042	3.672	4.320	3.450	4.058	ns
	Fast	4.027	4.738	4.016	4.725	3.981	4.683	3.208	3.774	3.076	3.618	ns
4 mA	Slow	4.180	4.917	4.101	4.825	4.185	4.924	4.533	5.333	4.212	4.955	ns
	Med.	3.693	4.345	3.654	4.299	3.672	4.320	3.764	4.428	3.476	4.090	ns
	Fast	3.453	4.063	3.415	4.018	3.390	3.989	3.253	3.828	3.094	3.640	ns
6 mA	Slow	3.980	4.682	3.887	4.573	3.977	4.679	4.669	5.493	4.363	5.133	ns
	Med.	3.505	4.124	3.457	4.067	3.483	4.098	3.831	4.508	3.554	4.182	ns
	Fast	3.267	3.844	3.222	3.791	3.207	3.773	3.285	3.864	3.135	3.688	ns
8 mA	Slow	3.813	4.486	3.734	4.394	3.806	4.478	4.675	5.500	4.355	5.123	ns
	Med.	3.392	3.990	3.341	3.931	3.340	3.929	3.828	4.504	3.546	4.172	ns
	Fast	3.171	3.731	3.124	3.675	3.078	3.621	3.293	3.875	3.140	3.694	ns
10 mA	Slow	3.755	4.417	3.667	4.315	3.743	4.403	4.799	5.646	4.421	5.202	ns
	Med.	3.338	3.928	3.282	3.862	3.289	3.869	3.901	4.590	3.597	4.232	ns
	Fast	3.119	3.669	3.067	3.609	3.031	3.566	3.326	3.913	3.170	3.730	ns
12 mA	Slow	3.698	4.350	3.612	4.250	3.685	4.336	4.862	5.720	4.445	5.229	ns
	Med.	3.297	3.880	3.238	3.809	3.245	3.817	3.921	4.613	3.595	4.230	ns
	Fast	3.082	3.627	3.028	3.563	2.994	3.523	3.316	3.902	3.186	3.748	ns
LVCMOS 1.5V (for MSIO I/O Bank)												
2 mA	Default	5.870	6.905	5.836	6.867	5.797	6.820	6.009	7.068	5.494	6.463	ns
4 mA	Default	5.356	6.301	5.268	6.198	5.291	6.225	6.091	7.165	5.543	6.521	ns
6 mA	Default	5.287	6.220	5.029	5.917	5.078	5.974	6.134	7.215	5.562	6.542	ns
8 mA	Default	5.270	6.200	4.958	5.833	5.021	5.907	6.175	7.264	5.559	6.539	ns
LVCMOS 1.5V (for MSIOD I/O Bank)												
2 mA	Default	3.262	3.837	4.134	4.864	4.495	5.289	3.920	4.612	3.567	4.197	ns
4 mA	Default	2.771	3.259	3.578	4.209	3.861	4.542	4.011	4.718	3.622	4.261	ns
6 mA	Default	2.799	3.292	3.394	3.993	3.673	4.321	4.029	4.740	3.641	4.283	ns

4.6.6 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2V applications and is supported in RTG4 FPGAs in compliance to the JEDEC specification JESD8-12A.

4.6.6.1 Minimum and Maximum Input and Output Levels Specification

Table 4-30. LVCMOS 1.2V Minimum and Maximum DC Input and Output Levels

Symbol	Parameters	Min	Typ	Max	Units
LVCMOS 1.2V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.140	1.2	1.26	V
LVCMOS 1.2V DC Input Voltage Specification					
VIH (DC)	DC input logic high	0.65 × VDDI	—	1.26	V
VIL (DC)	DC input logic low	–0.3	—	0.35 × VDDI	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LVCMOS 1.2V DC Output Voltage Specification					
VOH	DC output logic high	VDDI × 0.75	—	—	V
VOL	DC output logic low	—	—	VDDI × 0.25	V

Table 4-31. LVCMOS 1.2V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 2.5 pF load/ maximum drive/fast slew	—	—	550	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2.5 pF load/ maximum drive	—	—	140	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 2.5 pF/maximum drive	—	—	140	Mbps

Table 4-32. LVCMOS 1.2V AC Test Parameters and Driver Impedance Specifications

Symbol	Parameters	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path	—	0.6	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})	—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})	—	5	—	pF

Table 4-33. LVCMOS 1.2V Transmitter Drive Strength Specifications

MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
—	—	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

4.6.6.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.14V.

Table 4-34. LVCMOS 1.2V AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	t_{PYS} Speed Grade –1	t_{PYS} Speed Grade STD	Units
DDRIO with fixed codes	None	1.347	1.585	1.347	1.585	ns
MSIO	None	3.228	3.797	3.193	3.756	ns
MSIOD	None	2.555	3.007	2.531	2.978	ns

Table 4-35. LVCMOS 1.2V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Output Drive Selection	Slew Control	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
LVCMOS 1.2V (for DDRIO I/O Bank with Fixed Code)												
2 mA	Slow	5.841	6.871	5.837	6.868	5.832	6.862	5.628	6.621	5.248	6.174	ns
	Medium	5.105	6.006	5.094	5.993	5.066	5.960	4.752	5.590	4.431	5.212	ns
	Fast	4.710	5.540	4.695	5.524	4.641	5.461	4.137	4.867	3.938	4.633	ns
4 mA	Slow	5.241	6.165	5.205	6.124	5.264	6.193	5.957	7.008	5.414	6.369	ns
	Medium	4.598	5.409	4.565	5.371	4.536	5.337	4.928	5.797	4.491	5.283	ns
	Fast	4.247	4.996	4.211	4.955	4.121	4.848	4.200	4.941	3.977	4.679	ns
6 mA	Slow	5.065	5.959	5.029	5.917	5.063	5.957	6.080	7.153	5.604	6.593	ns
	Medium	4.450	5.235	4.411	5.190	4.379	5.152	4.980	5.858	4.577	5.385	ns
	Fast	4.106	4.830	4.063	4.780	3.982	4.685	4.235	4.982	4.018	4.727	ns
LVCMOS 1.2V (for MSIO I/O Bank)												
2 mA	Default	8.666	10.194	8.512	10.013	8.403	9.886	8.824	10.380	8.132	9.567	ns
4 mA	Default	8.182	9.625	7.642	8.990	7.670	9.023	8.954	10.534	8.173	9.615	ns

.....continued												
Output Drive Selection	Slew Control	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
LVCMOS 1.2V (for MSIOD I/O Bank)												
2 mA	Default	3.996	4.701	5.094	5.992	5.644	6.639	5.408	6.362	4.884	5.745	ns
4 mA	Default	4.029	4.739	4.757	5.596	5.255	6.182	5.510	6.482	4.937	5.808	ns

4.6.7 3.3V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3V standards specify support for 33 MHz and 66 MHz PCI bus applications.

4.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 4-36. PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbol	Parameters	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions					
VDDI	Supply voltage	3.15	3.3	3.45	V
PCI/PCIX Input Voltage Specification					
VI	DC input voltage	0	—	3.45	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
PCI/PCIX DC Output Voltage Specification					
VOH	DC output logic high	Per PCI specification			V
VOL	DC output logic low	Per PCI specification			V

Table 4-37. PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: as per JEDEC specifications	—	—	630	Mbps
PCI/PCI-X AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path (falling edge)		—	0.615 × VDDI	—	V
Vtrip	Measuring/trip point for data path (rising edge)		—	0.285 × VDDI	—	V
Rtt_test	Resistance for data test path		—	25	—	Ω

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2 k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})		—	10	—	pF

4.6.7.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 3.15V.

Table 4-38. PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY}		t_{PYS}		Units
		Speed Grade–1	Speed Grade STD	Speed Grade–1	Speed Grade STD	
MSIO	None	2.097	2.467	2.226	2.619	ns

Table 4-39. PCI/PCIX AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	2.446	2.878	2.456	2.889	2.395	2.817	3.387	3.985	3.040	3.576	ns

4.7 Memory Interface and Voltage Reference I/O Standards

The following sections describe the memory interface and voltage reference I/O standards for thr RTG4 FPGA devices.

4.7.1 High-Speed Transceiver Logic

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). The RTG4 FPGA devices support two classes of the 1.5V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer. An RTG4 device also supports a custom 1.8V HSTL.

4.7.1.1 Minimum and Maximum Input and Output Levels Specification

Table 4-40. HSTL18 Minimum and Maximum DC Input and Output Levels

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	1.71	1.8	1.89	V
VTT	Termination voltage	0.838	0.900	0.964	V
VREF[1]	Input reference voltage	0.838	0.900	0.964	V
HSTL18 DC Input Voltage Specification					

.....continued					
Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Units**
VIH (DC)	DC input logic high	VREF + 0.125	—	1.89	V
VIL (DC)	DC input logic low	–0.3	—	VREF – 0.125	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
HSTL18V DC Output Voltage Specification					
HSTL18 Class I					
VOH	DC output logic high	VTT + 0.603	—	—	V
VOL	DC output logic low	—	—	VTT – 0.603	V
IOH at VOH	Output minimum source DC current (Applicable to MSIO Bank Only)	4.5	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to MSIO Bank Only)	–4.5	—	—	mA
IOH at VOH	Output minimum source DC current (Applicable to MSIOD Bank Only)	4.0	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to MSIOD Bank Only)	–4.0	—	—	mA
IOH at VOH	Output minimum source DC current (Applicable to DDRIO Bank Only)	5.4	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to DDRIO Bank Only)	–5.4	—	—	mA
HSTL18 Class II					
VOH	DC output logic high	VTT + 0.603	—	—	V
VOL	DC output logic low	—	—	VTT – 0.603	V
IOH at VOH	Output minimum source DC current (Applicable to DDRIO Bank Only)	10.0	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to DDRIO Bank Only)	–10.0	—	—	mA
HSTL18V DC Differential Voltage Specifications					
VID	DC input differential voltage	0.2	—	—	V

Note:

1. Maximum input leakage current for V_{REF} is 10 µA.

Table 4-41. HSTL18 AC Specifications

Symbol	Parameters	Conditions	Min	Typ	Max	Units
HSTL18 AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.5	—	—	V
Vx	AC differential cross point voltage		0.5 × VDDI – 0.175	—	(0.5 × VDDI) + 0.175	V
HSTL18 Maximum AC Switching Speed						
Dmax	Maximum Data Rate (for DDRIO IO Bank)	AC loading: 3 pF/50Ω load	—	—	500	Mbps
	Maximum Data Rate (for MSIO IO Bank)	AC loading: 3 pF/50Ω load	—	—	500	Mbps
	Maximum Data Rate (for MSIOD IO Bank)	AC loading: 3 pF/50Ω load	—	—	500	Mbps
Rref	Supported Output Driver Calibrated Impedance (for DDRIO IO Bank)	Reference resistor = 150Ω	—	20, 42	—	Ω
RTT	Effective impedance Value (ODT)	Reference resistor = 150Ω	—	50, 75, 150	—	Ω
HSTL18 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.9	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for HSTL18 Class I (t_{DP})		—	50	—	Ω
Rtt_test	Reference resistance for data test path for HSTL18 Class II (t_{DP})		—	25	—	Ω
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.1.2 AC Switching Characteristics

Table 4-42. HSTL18 AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
HSTL18 (for DDRIO I/O Bank with Fixed Code)				
Pseudo-Differential	None	0.595	0.701	ns
	50	0.595	0.701	ns
	75	0.595	0.701	ns
	150	0.595	0.701	ns
True-Differential	None	0.616	0.725	ns
	50	0.616	0.725	ns
	75	0.616	0.725	ns
	150	0.616	0.725	ns
HSTL18 (for MSIO I/O Bank)				
Pseudo-Differential	None	1.526	1.796	ns
	50	1.526	1.796	ns
	75	1.526	1.796	ns
	150	1.526	1.796	ns
True-Differential	None	1.436	1.689	ns
	50	1.436	1.689	ns
	75	1.436	1.689	ns
	150	1.436	1.689	ns
HSTL18 (For MSIOD I/O Bank)				
Pseudo-Differential	None	1.490	1.753	ns
	50	1.490	1.753	ns
	75	1.490	1.753	ns
	150	1.490	1.753	ns
True-Differential	None	1.421	1.671	ns
	50	1.421	1.671	ns
	75	1.421	1.671	ns
	150	1.421	1.671	ns

Note: Data corresponds to fixed PCODE and NCODE for receiver. For more information, see the UG0741: RTG4 FPGA I/O User Guide.

Table 4-43. HSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
HSTL18 Class I											
For DDRIO I/O Bank											
Single Ended	3.100	3.646	2.776	3.266	2.808	3.303	3.790	4.460	3.846	4.525	ns
Differential	3.089	3.634	2.998	3.527	3.003	3.533	3.850	4.530	3.782	4.450	ns
For MSIO I/O Bank											
Single ended	3.787	4.454	3.428	4.032	3.534	4.157	4.378	5.150	4.051	4.765	ns
Differential	4.022	4.731	3.682	4.332	3.677	4.326	4.047	4.761	4.390	5.165	ns
For MSIOD I/O Bank											
Single ended	2.045	2.406	2.173	2.556	2.331	2.742	3.134	3.687	2.894	3.405	ns
Differential	2.257	2.655	2.666	3.136	2.666	3.137	2.888	3.398	3.141	3.695	ns
HSTL18 Class II											
For DDRIO I/O Bank											
Single ended	3.025	3.558	2.745	3.229	2.778	3.269	3.844	4.523	3.927	4.620	ns
Differential	3.010	3.541	2.919	3.434	2.901	3.413	3.840	4.517	3.913	4.603	ns

4.7.1.3 Minimum and Maximum Input and Output Levels Specification

Table 4-44. HSTL 1.5V DC Voltage Specification

Symbol	Parameters	Min	Typ	Max	Units
HSTL 1.5V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
VTT	Termination voltage	0.698	0.750	0.803	V
VREF[1]	Input reference voltage	0.698	0.750	0.803	V
HSTL 1.5V DC Input Voltage Specification					
VIH (DC)	DC input logic high	VREF + 0.1	—	1.575	V
VIL (DC)	DC input logic low	–0.3	—	VREF – 0.1	V

.....continued					
Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Units**
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
HSTL 1.5V DC Output Voltage Specification					
HSTL 1.5V Class I					
VOH	DC output logic high	VTT – 0.4	—	—	V
VOL	DC output logic low	—	—	—	V
IOH at VOH	Output minimum source DC current (for MSIO Bank)	–8.0	—	—	mA
IOL at VOL	Output minimum sink current (for MSIO Bank)	8.0	—	—	mA
IOH at VOH	Output minimum source DC current (for MSIOD Bank)	–7.0	—	—	mA
IOL at VOL	Output minimum sink current (for MSIOD Bank)	7.0	—	—	mA
IOH at VOH	Output minimum source DC current (for DDRIO Bank)	–8.0	—	—	mA
IOL at VOL	Output minimum sink current (for DDRIO Bank)	8.0	—	—	mA
HSTL 1.5V Class II (Applicable to DDRIO Bank Only)					
VOH	DC output logic high	VDDI – 0.4	—	—	V
VOL	DC output logic low	—	—	0.4	V
IOH at VOH	Output minimum source DC current	–16.0	—	—	mA
IOL at VOL	Output minimum sink current	16.0	—	—	mA
HSTL 1.5V DC Differential Voltage Specifications					
VID	DC input differential voltage	0.2	—	—	V

Note:

1. Maximum input leakage current for V_{REF} is 10 µA.

Table 4-45. HSTL 1.5 AC Specifications

Symbol	Parameters	Conditions	Min	Typ	Max	Units
HSTL 1.5 AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.4	—	—	V
Vx	AC differential cross point voltage		0.68	—	0.9	V

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
HSTL 1.5 Maximum AC Switching Speed						
Dmax	Maximum data rate Class I MSIO bank only	AC loading: 3 pF/50Ω load	—	—	140	Mbps
	Maximum data rate Class I MSIOD bank only	AC loading: 3 pF/50Ω load	—	—	180	Mbps
	Maximum data rate Class I DDRIO bank only	AC loading: per JEDEC specifications	—	—	400	Mbps
	Maximum data rate Class II DDRIO bank only	AC loading: per JEDEC specifications	—	—	400	Mbps
HSTL 1.5V Impedance Specification						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 191Ω	—	25.5, 47.8	—	Ω
RTT	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistor = 191Ω	—	47.8	—	Ω
HSTL 1.5 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.75	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for HSTL15 Class I (t_{DP})		—	50	—	Ω
Rtt_test	Reference resistance for data test path for HSTL15 Class II (t_{DP})		—	25	—	Ω
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.1.4 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.425V.

Table 4-46. HSTL 15V AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
DDRIO with Fixed Code				
Pseudo-Differential	None	0.606	0.712	ns
	47.8	0.606	0.712	ns
True-Differential	None	0.616	0.725	ns
	47.8	0.616	0.725	ns
MSIO				
Pseudo-Differential	None	1.677	1.973	ns
True-Differential	None	1.462	1.720	ns

.....continued				
I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIOD				
Pseudo-Differential	None	1.618	1.902	ns
True-Differential	None	1.445	1.700	ns

Note: Data corresponds to fixed PCODE and NCODE for receiver. For more information, see the UG0741: RTG4 FPGA I/O User Guide.

Table 4-47. HSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
HSTL15 Class I											
For DDRIO I/O Bank											
Single Ended	3.619	4.257	3.304	3.888	3.338	3.927	4.315	5.077	4.513	5.310	ns
Differential	3.612	4.249	3.567	4.197	3.550	4.176	4.306	5.066	4.509	5.304	ns
For MSIO I/O Bank											
Single Ended	4.888	5.751	4.442	5.226	4.554	5.358	5.577	6.560	5.166	6.077	ns
Differential	5.108	6.009	4.743	5.580	4.737	5.572	5.593	6.580	5.175	6.088	ns
For MSIOD I/O Bank											
Single Ended	2.481	2.919	2.631	3.095	2.840	3.341	3.769	4.434	3.463	4.074	ns
Differential	2.670	3.141	3.223	3.793	3.223	3.792	3.778	4.445	3.470	4.082	ns
HSTL15 Class II											
For DDRIO I/O Bank											
Single Ended	3.525	4.147	3.261	3.837	3.300	3.882	4.536	5.337	4.602	5.415	ns
Differential	3.513	4.133	3.471	4.083	3.454	4.064	4.529	5.328	4.598	5.409	ns

4.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5V (SSTL2), 1.8V (SSTL18), and 1.5V (SSTL15) is supported in RTG4 FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. The RTG4 SSTL I/O configurations are designed to meet double data rate standards DDR2/3 for general purpose memory buses. DDR standards are designed to meet their JEDEC specifications as defined by JEDEC standard

JESD79F for DDR, JEDEC standard JESD79-2F for DDR2, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

4.7.2.1 Stub-Series Terminated Logic 2.5V (SSTL2)

SSTL2 Class I and Class II are supported in RTG4 FPGAs and also comply with reduced and full drive of DDR standards. RTG4 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

Table 4-48. DDR/SSTL2 Minimum and Maximum DC Input and Output Levels

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
VTT	Termination voltage	1.164	1.250	1.339	V
VREF[1]	Input reference voltage	1.164	1.250	1.339	V
SSTL2 DC Input Voltage Specification—Applicable to All Banks					
VIH (DC)	DC input logic high	VREF + 0.15	—	2.625	V
VIL (DC)	DC input logic low	–0.3	—	VREF – 0.15	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
SSTL2 DC Output Voltage Specification					
SSTL2 Class I (DDR Reduced Drive)					
VOH	DC output logic high	VTT + 0.608	—	—	V
VOL	DC output logic low	—	—	VTT – 0.608	V
IOH at VOH	Output minimum source DC current	8.1	—	—	mA
IOL at VOL	Output minimum sink current	–8.1	—	—	mA
SSTL2 Class II (DDR Full Drive)					
VOH	DC output logic high	VDDI + 0.81	—	—	V
VOL	DC output logic low	—	—	VTT – 0.81	V
IOH at VOH	Output minimum source DC current	16.2	—	—	mA
IOL at VOL	Output minimum sink current	–16.2	—	—	mA
SSTL2 DC Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.2	—	—	V

Note:

1. Maximum input leakage current for V_{REF} is 10 µA.

Table 4-49. DDR/SSTL2 AC Specifications

Symbol	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.7	—	—	V
Vx	AC differential cross point voltage		0.5 × VDDI – 0.2	—	0.5 × VDDI + 0.2	V
SSTL2 Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	—	—	800	Mbps
	Maximum data rate (for MSIO I/O Bank)	AC loading: 3 pF/25Ω load	—	—	575	Mbps
	Maximum data rate (for MSIOD I/O Bank)	AC loading: 3 pF/25Ω load	—	—	700	Mbps
SSTL2 Impedance Specifications						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference Resistor = 150Ω	—	20, 42	—	Ω
SSTL2 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	1.25	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		—	50	—	Ω
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		—	25	—	Ω
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.2.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-50. DDR/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
SSTL2 (DDRIO I/O Bank)				
Pseudo-Differential	None	0.586	0.690	ns
True-Differential	None	0.589	0.693	ns

.....continued				
	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
SSTL2 (MSIO I/O Bank)				
Pseudo-Differential	None	1.328	1.562	ns
True-Differential	None	1.264	1.486	ns
SSTL2 (MSIOD I/O Bank)				
Pseudo-Differential	None	1.301	1.530	ns
True-Differential	None	1.254	1.476	ns

Table 4-51. DDR/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
SSTL2 Class I											
DDRIO I/O Bank											
Single Ended	2.736	3.219	2.376	2.795	2.393	2.815	3.179	3.740	3.258	3.832	ns
Differential	2.672	3.143	2.551	3.001	2.565	3.019	3.173	3.732	3.247	3.819	ns
MSIO I/O Bank											
Single Ended	2.731	3.214	2.532	2.979	2.616	3.077	3.276	3.853	3.037	3.573	ns
Differential	2.977	3.503	2.802	3.296	2.799	3.293	3.288	3.868	3.044	3.581	ns
MSIOD I/O Bank											
Single Ended	1.523	1.792	1.846	2.171	1.940	2.282	2.559	3.011	2.391	2.813	ns
Differential	1.745	2.053	2.262	2.662	2.263	2.662	2.572	3.026	2.396	2.819	ns
SSTL2 Class II											
DDRIO I/O Bank											
Single Ended	2.625	3.088	2.325	2.735	2.328	2.738	3.183	3.745	3.256	3.831	ns
Differential	2.558	3.010	2.432	2.861	2.409	2.834	3.264	3.839	3.220	3.787	ns
MSIO I/O Bank											

.....continued											
	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
Single Ended	2.684	3.159	2.495	2.935	2.590	3.046	3.273	3.850	3.035	3.571	ns
Differential	2.927	3.444	2.673	3.143	2.671	3.141	3.030	3.566	3.280	3.860	ns
MSIOD I/O Bank											
Single Ended	1.592	1.873	1.764	2.075	1.872	2.202	2.561	3.014	2.391	2.813	ns
Differential	1.805	2.123	2.102	2.473	2.102	2.473	2.386	2.806	2.570	3.023	ns

4.7.3 Stub-Series Terminated Logic 1.8V (SSTL18)

SSTL18 Class I and Class II are supported in RTG4 FPGAs. They also comply with the reduced and full DDR2 standard. The RTG4 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

4.7.3.1 Minimum and Maximum Input and Output Levels Specification

Table 4-52. DDR2/SSTL18 DC Minimum and Maximum Input and Output Levels Specification

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	1.71	1.8	1.89	V
VTT	Termination voltage	0.838	0.900	0.964	V
VREF[1]	Input reference voltage	0.838	0.900	0.964	V
SSTL18 DC Input Voltage Specification					
VIH (DC)	DC input logic high	VREF + 0.125	—	1.89	V
VIL (DC)	DC input logic low	–0.3	—	VREF – 0.125	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
SSTL18 DC Output Voltage Specification					
SSTL18 Class I (DDR2 Reduced Drive)					
VOH	DC output logic high	VTT + 0.603	—	—	V
VOL	DC output logic low	—	—	VTT – 0.603	V

.....continued					
Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Units**
IOH at VOH	Output minimum source DC current (Applicable to MSIO and MSIOD banks)[2]	4.7	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to MSIO and MSIOD banks)[2]	–4.7	—	—	mA
IOH at VOH	Output minimum source DC current (Applicable to DDRIO bank only)[2]	6.3	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to DDRIO bank only)[2]	–6.3	—	—	mA
SSTL18 Class II (DDR2 Full Drive)[3]					
VOH	DC output logic high	VTT + 0.603	—	—	V
VOL	DC output logic low	—	—	VTT – 0.603	V
IOH at VOH	Output minimum source DC current (Applicable to MSIO and MSIOD banks)[4]	9.3	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to MSIO and MSIOD banks)[4]	–9.3	—	—	mA
IOH at VOH	Output minimum source DC current (Applicable to DDRIO bank only)	13.4	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to DDRIO bank only)	–13.4	—	—	mA
SSTL18 DC Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.2	—	—	V

Notes:

1. Maximum input leakage current for V_{REF} is 10 µA.
2. MSIO and MSIOD Bank SSTL18/DDR2 reduced drive does not have a standard test point. This is defined to fit within the DDR2 "Reduced Drive" IV curve minimums.
3. DDR2 full drive transmitter is used to meet the JEDEC electrical compliance.
4. MSIO IO Bank SSTL18/DDR2 Class II does not meet the standard JEDEC test points. Use provided lower current values as specified.

Table 4-53. DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
SSTL18 AC Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.5	—	—	V

.....continued

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vx (AC)	AC differential cross point voltage		0.5 × VDDI – 0.175	—	0.5 × VDDI + 0.175	V
SSTL18 Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specification	—	—	800	Mbps
	Maximum data rate (for MSIO I/O Bank)	AC loading: 3 pF/25Ω load	—	—	432	Mbps
	Maximum data rate (for MSIOD I/O Bank)	AC loading: 3 pF/25Ω load	—	—	430	Mbps
SSTL18 Impedance Specifications						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150Ω	—	20, 42	—	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 150Ω	—	50, 75, 150	—	Ω
SSTL18 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.9	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		—	50	—	Ω
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		—	25	—	Ω
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.3.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.71V.

Table 4-54. DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
SSTL18 (for DDRIO I/O Bank with Fixed Codes)				
Pseudo-Differential	None	0.595	0.701	ns
	50	0.595	0.701	ns
	75	0.595	0.701	ns
	150	0.595	0.701	ns
True-Differential	None	0.616	0.725	ns
	50	0.616	0.725	ns
	75	0.616	0.725	ns
	150	0.616	0.725	ns
SSTL18 (For MSIO IO Bank)				
Pseudo-Differential	None	1.526	1.796	ns
	50	1.526	1.796	ns
	75	1.526	1.796	ns
	150	1.526	1.796	ns
True-Differential	None	1.436	1.689	ns
	50	1.436	1.689	ns
	75	1.436	1.689	ns
	150	1.436	1.689	ns
SSTL18 (For MSIOD IO Bank)				
Pseudo-Differential	None	1.490	1.753	ns
	50	1.490	1.753	ns
	75	1.490	1.753	ns
	150	1.490	1.753	ns
True-Differential	None	1.421	1.671	ns
	50	1.421	1.671	ns
	75	1.421	1.671	ns
	150	1.421	1.671	ns

Note: Data corresponds to fixed PCODE and NCODE for receiver. For more information, see UG0741: RTG4 FPGA I/O User Guide.

Table 4-55. DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Unit
SSTL18 Class I											
DDRIO I/O Bank											
Single ended	3.100	3.646	2.776	3.266	2.808	3.303	3.790	4.460	3.846	4.525	ns
Differential	3.089	3.634	2.998	3.527	2.979	3.505	3.786	4.454	3.837	4.514	ns
MSIO I/O Bank											
Single ended	3.729	4.386	3.488	4.102	3.569	4.198	4.374	5.145	4.049	4.763	ns
Differential	3.959	4.658	3.799	4.470	3.795	4.465	4.386	5.160	4.054	4.770	ns
MSIOD I/O Bank											
Single ended	1.853	2.180	2.206	2.595	2.362	2.778	3.125	3.676	2.887	3.397	ns
Differential	2.070	2.436	2.689	3.163	2.690	3.165	3.136	3.689	2.895	3.405	ns
SSTL18 Class II											
DDRIO I/O Bank											
Single ended	3.025	3.558	2.745	3.229	2.778	3.269	3.844	4.523	3.927	4.620	ns
Differential	3.010	3.541	2.919	3.434	2.925	3.440	3.926	4.619	3.830	4.507	ns
MSIO I/O Bank											
Single ended	3.675	4.322	3.433	4.038	3.538	4.162	4.373	5.144	4.047	4.760	ns
Differential	3.898	4.586	3.647	4.290	3.642	4.284	4.042	4.755	4.384	5.157	ns
MSIOD I/O Bank											
Single ended	1.949	2.293	2.192	2.578	2.354	2.769	3.130	3.682	2.893	3.404	ns
Differential	2.160	2.542	2.617	3.079	2.616	3.078	2.887	3.396	3.138	3.692	ns

4.7.4 Stub-Series Terminated Logic 1.5V (SSTL15)

SSTL15 Class I and Class II are supported in RTG4 FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. The RTG4 FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

4.7.4.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 4-56. DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
VTT	Termination voltage	0.698	0.750	0.803	V
VREF[1]	Input reference voltage	0.698	0.750	0.803	V
SSTL15 DC Input Voltage Specification					
VIH (DC)	DC input logic high	VREF + 0.1	—	1.575	V
VIL (DC)	DC input logic low	–0.3	—	VREF – 0.1	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
SSTL15 DC Output Voltage Specification					
SSTL15 Class II (DDR3 Full Drive)					
VOH	DC output logic high	0.8 × VDDI	—	—	V
VOL	DC output logic low	—	—	0.2 × VDDI	V
IOH at VOH	Output minimum source DC current (Applicable to MSIO and MSIOD banks)	13.4	—	—	mA
IOL at VOL	Output minimum sink current (Applicable to MSIO and MSIOD banks)	–13.4	—	—	mA
SSTL15 Differential Voltage Specification					
VID	DC input differential voltage	0.2	—	—	V

Notes:

1. Maximum input leakage current for V_{REF} is 10 µA.
2. DDR3 full drive transmitter must be used to meet JEDEC Electrical Compliance.

Table 4-57. DDR3/SSTL15 AC Specifications

Symbol	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 AC Differential Voltage Specification						
VDIFF	AC input differential voltage		0.7	—	—	V

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vx	AC differential cross point voltage		0.5 × VDDI – 0.150	—	0.5 × VDDI + 0.150	V
SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	—	—	800	Mbps
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.75	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		—	50	—	Ω
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		—	25	—	Ω
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.4.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.425V.

Table 4-58. DDR3/STTL15 AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT) in Ω	**t_{PY} Speed Grade –1**	**t_{PY} Speed Grade STD**	**Units**
DDR3/SSTL15 (for DDRIO I/O Bank)—Calibration Mode Only				
Pseudo-Differential	None	0.606	0.713	ns
	20	0.606	0.713	ns
	30	0.606	0.713	ns
	40	0.606	0.713	ns
	60	0.606	0.713	ns
	120	0.606	0.713	ns
True-Differential	None	0.616	0.725	ns
	20	0.616	0.725	ns
	30	0.616	0.725	ns
	40	0.616	0.725	ns
	60	0.616	0.725	ns
	120	0.616	0.725	ns

Table 4-59. DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)											
Single Ended	3.380	3.976	3.079	3.622	3.129	3.681	4.186	4.924	4.270	5.024	ns
Differential	3.327	3.913	3.369	3.963	3.353	3.945	4.194	4.933	4.295	5.052	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)											
Single Ended	3.269	3.846	3.085	3.629	3.140	3.693	4.185	4.924	4.270	5.024	ns
Differential	3.222	3.790	3.305	3.888	3.290	3.871	4.189	4.927	4.279	5.033	ns

4.7.5 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power DDR standards are supported in the RTG4 FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in the DDRIO I/O Bank only.

4.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 4-60. LPDDR DC Specifications (for DDRIO IO Bank Only)

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	1.71	1.8	1.89	V
VTT	Termination voltage	0.838	0.900	0.964	V
VREF[1]	Input reference voltage	0.838	0.900	0.964	V
LPDDR DC Input Voltage Specification					
VIH (DC)	DC input logic high	0.7 × VDDI	—	1.89	V
VIL (DC)	DC input logic low	–0.3	—	0.3 × VDDI	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LPDDR DC Output Voltage Specification					
LPDDR Reduced Drive					
VOH	DC output logic high	0.9 × VDDI	—	—	V
VOL	DC output logic low	—	—	0.1 × VDDI	V

.....continued					
Symbol	**Parameters**	**Min**	**Typ**	**Max**	**Units**
IOH at VOH	Output minimum source DC current	0.1	—	—	mA
IOL at VOL	Output minimum sink current	–0.1	—	—	mA
LPDDR Full Drive[2]					
VOH	DC output logic high	0.9 × VDDI	—	—	V
VOL	DC output logic low	—	—	0.1 × VDDI	V
IOH at VOH	Output minimum source DC current	0.1	—	—	mA
IOL at VOL	Output minimum sink current	–0.1	—	—	mA
SSTL15 Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.2	—	—	V

Notes:

1. Maximum input leakage current for LPDDR is 10 µA.
2. LPDDR full drive transmitter is used to meet JEDEC Electrical Compliance.

Table 4-61. LPDDR Minimum and Maximum AC Switching Speeds (for DDRIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LPDDR AC Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.6 × VDDI	—	—	V
Vx (AC)	AC differential cross point voltage		0.4 × VDDI	—	0.6 × VDDI	V
LPDDR Maximum AC Switching Speed						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	—	—	266	Mbps
LPDDR Impedance Specifications						
Rref	Supported output driver calibrated impedance	Reference Resistor = 150Ω	—	20, 42	—	Ω
RTT	Effective impedance value (ODT)	Reference Resistor = 150Ω	—	50, 75, 150	—	Ω
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.9	—	V
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		—	50	—	Ω

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

4.7.5.2 AC Switching Characteristics

Worst-case military conditions: T_J =125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.71V.

Table 4-62. LPDDR AC Switching Characteristics for Receiver (Input Buffers)

	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
LPDDR (for DDRIO I/O Bank with Fixed Codes)				
Pseudo-Differential	None	0.596	0.700	ns
	50	0.596	0.700	ns
	75	0.596	0.700	ns
	150	0.596	0.700	ns
True-Differential	None	0.617	0.726	ns
	50	0.617	0.726	ns
	75	0.617	0.726	ns
	150	0.617	0.726	ns

Note: The data corresponds to fixed PCODE and NCODE for receiver. For more information, see the UG0741: RTG4 FPGA I/O User Guide.

Table 4-63. LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
LPDDR Reduced Drive (for DDRIO I/O Bank)											
Single Ended	3.100	3.646	2.776	3.266	2.808	3.303	3.790	4.460	3.846	4.525	ns
Differential	3.089	3.634	2.998	3.527	3.003	3.533	3.850	4.530	3.782	4.450	ns
LPDDR Full Drive (for DDRIO I/O Bank)											
Single Ended	3.025	3.558	2.745	3.229	2.778	3.269	3.844	4.523	3.927	4.620	ns
Differential	3.010	3.541	2.919	3.434	2.925	3.440	3.926	4.619	3.830	4.507	ns

4.7.5.3 Minimum and Maximum AC/DC Input and Output Levels Specification Using LPDDR-LVCMOS 1.8V Mode

Table 4-64. LPDDR-LVCMOS 1.8V Mode, Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO I/O Bank Only)

Symbol	Parameters	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8V Mode DC Input Voltage Specification					
VIH (DC)	DC input logic high	0.65 × VDDI	—	2.75	V
VIL (DC)	DC input logic low	–0.3	—	0.35 × VDDI	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
LPDDR-LVCMOS 1.8V Mode DC Output Voltage Specification					
VOH	DC output logic high	VDDI – 0.45	—	—	V
VOL	DC output logic low	—	—	0.45	V

Table 4-65. LPDDR-LVCMOS 1.8V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8V Maximum AC Switching Speed (for DDRIO I/O Banks Only)						
Dmax	Maximum Data Rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	—	—	266	Mbps
LPDDR-LVCMOS 1.8V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	0.9	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF
Cload	Capacitive loading for data path (t_{DP})		—	5	—	pF

Table 4-66. LPDDR-LVCMOS 1.8V Mode Transmitter Drive Strength Specification (Applicable to the DDRIO I/O Bank Only)

Output Drive Selection	VOH Min (V)	VOL Max (V)	IOH (mA)	IOL (mA)
2 mA	VDDI – 0.45	0.45	2	2
4 mA	VDDI – 0.45	0.45	4	4
6 mA	VDDI – 0.45	0.45	6	6
8 mA	VDDI – 0.45	0.45	8	8

.....continued				
Output Drive Selection	**VOH Min (V)**	**VOL Max (V)**	**IOH (mA)**	**IOL (mA)**
10 mA	VDDI – 0.45	0.45	10	10
12 mA	VDDI – 0.45	0.45	12	12
16 mA	VDDI – 0.45	0.45	16	16

Note:

1. 16 mA drive strengths and all slews meet the LPDDR JEDEC electrical compliance.

4.7.5.4 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 1.71V.

Table 4-67. LPDDR AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	t_{PYS} Speed Grade –1	t_{PYS} Speed Grade STD	Units
DDRIO with fixed codes	None	1.028	1.209	1.028	1.209	ns

Table 4-68. LPDDR—LVCMOS 1.8V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

		t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
Output Drive Selection	**Slew Control**	**Speed Grade –1**	**Speed Grade STD**	**Speed Grade –1**	**Speed Grade STD**	**Speed Grade –1**	**Speed Grade STD**	**Speed Grade –1**	**Speed Grade STD**	**Speed Grade –1**	**Speed Grade STD**	**Unit**
2 mA	Slow	4.088	4.809	4.054	4.769	4.101	4.824	3.815	4.489	3.609	4.246	ns
	Med.	3.710	4.364	3.685	4.336	3.670	4.317	3.203	3.768	3.009	3.541	ns
4 mA	Slow	3.757	4.419	3.692	4.343	3.752	4.414	3.952	4.649	3.751	4.413	ns
	Med.	3.373	3.968	3.331	3.918	3.328	3.915	3.288	3.869	3.072	3.614	ns
6 mA	Slow	3.438	4.045	3.357	3.949	3.424	4.028	4.026	4.737	3.783	4.450	ns
	Med.	3.086	3.630	3.030	3.564	3.035	3.570	3.319	3.906	3.080	3.624	ns
8 mA	Slow	3.362	3.955	3.272	3.849	3.345	3.935	4.073	4.792	3.799	4.470	ns
	Med.	3.015	3.546	2.955	3.476	2.966	3.490	3.338	3.928	3.096	3.643	ns
10 mA	Slow	3.228	3.797	3.146	3.701	3.205	3.771	4.077	4.797	3.788	4.456	ns
	Med.	2.917	3.431	2.855	3.359	2.848	3.350	3.331	3.919	3.080	3.624	ns
12 mA	Slow	3.179	3.739	3.087	3.631	3.150	3.706	4.155	4.888	3.881	4.566	ns
	Med.	2.870	3.376	2.802	3.296	2.802	3.296	3.383	3.980	3.130	3.683	ns

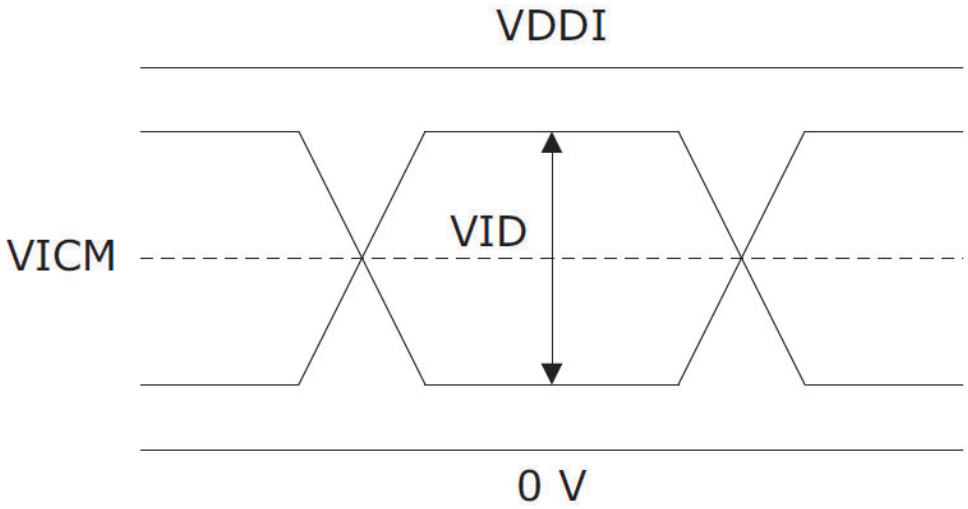
.....continued

		t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		
Output Drive Selection	Slew Control	Speed Grade –1	Speed Grade STD	Speed Grade –1	Speed Grade STD	Speed Grade –1	Speed Grade STD	Speed Grade –1	Speed Grade STD	Speed Grade –1	Speed Grade STD	Unit
16 mA	Slow	3.126	3.677	3.025	3.559	3.087	3.632	4.237	4.986	3.948	4.645	ns
	Med.	2.826	3.324	2.750	3.235	2.752	3.238	3.415	4.018	3.158	3.716	ns

4.8 Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microchip SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate registers (DDR).

Figure 4-4. Differential Input Signaling Waveform Depicting VICM and VID Parameters



Note: V_{ID} = | VinP–VinN |. The full amplitude range for V_{ID} is V_{IDmin} to V_{IDmax}, or $\pm V_{IDmin}/2$ to $\pm V_{IDmax}/2$.

4.8.1 LVDS

Low-Voltage Differential Signaling (LVDS) (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. RTG4 LVDS transmitters are true LVDS drivers that can source and sink current.

4.8.1.1 Minimum and Maximum Input and Output Levels

Table 4-69. LVDS25 DC Voltage Specification (Applicable to MSIO, MSIOD Banks, and SerDes REFCLK Input)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVDS25 Recommended DC Operating Conditions						
VDDI	Supply voltage	—	2.375	2.5	2.625	V
LVDS25 DC Input Voltage Specification						
VI	DC input voltage	—	0	—	2.625	V

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
IIH (DC)	Input leakage current high	—	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	—	10	µA
LVDS25 DC Output Voltage Specification						
VOH	DC output logic high	—	1.25	1.425	1.6	V
VOL	DC output logic low	—	0.9	1.075	1.25	V
LVDS25 Differential Voltage Specification						
VOD	Differential output voltage swing	—	250	350	450	mV
VOCM	Output common mode voltage	—	1.125	1.25	1.375	V
VICM[1]	Input common mode voltage	With On-die termination (Rt)	0.05	1.25	1.5	V
		With external differential termination (Rt)	0.05	1.25	2.2	V
VID[1, 2, 3]	Input differential voltage	—	200	350	2400	mV

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas it produces only 250 mV across a 100 Ω termination.
3. Refer to Figure 4-4 for more information on V_{ID}.

Table 4-70. LVDS25 AC Specifications (Applicable to MSIO, MSIOD Banks and SerDes REFCLK Input)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVDS25 Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 12 pF/100Ω differential load	—	—	750	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF/100Ω differential load	—	—	750	Mbps
LVDS25 Impedance Specification						
Rt	Termination resistance	On-die termination resistance	90	100	150	Ω
		External 100Ω differential termination[2]	95	100	105	Ω
		External 100Ω differential termination[1, 2]	190	200	210	Ω
LVDS25 AC Test Parameters Specifications						

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vtrip	Measuring/trip point for data path		—	Crosspoint	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

Notes:

1. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas it produces only 250 mV across a 100Ω termination.
2. When the external termination is being used, ODT must be disabled using the Libero SoC.

4.8.1.2 LVDS25 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-71. LVDS25 Receiver Characteristics

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.244	1.463	ns
	100	1.244	1.463	ns
MSIOD	None	1.232	1.448	ns
	100	1.232	1.448	ns

Table 4-72. LVDS25 Transmitter Characteristics

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	3.151	3.706	2.765	3.253	2.760	3.248	2.990	3.517	3.211	3.778	ns
MSIOD											
No pre-emphasis	1.919	2.257	2.179	2.563	2.154	2.534	2.538	2.985	2.388	2.809	ns
Min pre-emphasis	1.843	2.167	2.178	2.563	2.154	2.534	2.375	2.793	2.535	2.982	ns
Med pre-emphasis	1.807	2.125	2.179	2.563	2.154	2.534	2.538	2.985	2.388	2.809	ns

4.8.1.3 LVDS33 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14 V, and V_{DDI} = 3.15 V.

Table 4-73. LVDS33 DC Voltage Specification (Applicable to MSIO Banks and SerDes REFCLK Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVDS33 Recommended DC Operating Conditions						
VDDI	Supply voltage	—	3.15	3.3	3.45	V
LVDS33 DC Input Voltage Specification						
VI	DC input voltage	—	0	—	3.45	V
IIH (DC)	Input leakage current high	—	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	—	10	µA
LVDS33 DC Output Voltage Specification						
VOH	DC output logic high	—	1.25	1.425	1.6	V
VOL	DC output logic low	—	0.9	1.075	1.25	V
LVDS33 DC Differential Voltage Specification						
VOD	Differential output voltage swing	—	250	350	450	mV
VOCM	Output common mode voltage	—	1.125	1.25	1.375	V
VICM[1, 2, 3, 4]	Input common mode voltage	With external differential termination Rt	0.06	1.25	1.8	V
VID[1, 2, 3, 4, 5]	Input differential voltage	With external differential termination Rt	500	—	2400	mV

Notes:

1. LVDS33 receiver in V_{DDI} = 3.3V supply range does not support ODT.
2. The termination resistance value depends on the current drive capability of the external LVDS transmitter. For example, using a worst-case 2.5 mA current driver, a 200Ω differential termination can be used to effectively double the differential voltage compared to a 100Ω termination, producing 500 mV of differential voltage compared to only 250 mV across a 100Ω termination. A designer must use IBIS models to simulate their circuit and determine the proper termination resistance value that will meet minimum V_{ID} and still have good signal integrity.
3. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
   $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
4. For jitter considerations, see Table 17-11.
5. Refer to Figure 4-4 for more information on V_{ID}.

Table 4-74. LVDS33 AC Specifications (Applicable to MSIO Banks and SerDes REFCLK Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVDS33 Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading for outputs: 12 pF/100Ω Differential load for inputs: VID ≥ 500 mV	—	—	700	Mbps
LVDS33 Impedance Specification						
Rt[1, 2]	Termination resistance	External differential termination	190	200	210	Ω
LVDS33 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	Crosspoint	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

Notes:

1. LVDS33 receiver in V_{DDI} = 3.3V supply range does not support ODT.
2. The termination resistance value depends on the current drive capability of the external LVDS transmitter. For example, using a worst-case 2.5 mA current driver, a 200Ω differential termination can effectively double the differential voltage compared to a 100Ω termination, producing 500 mV of differential voltage compared to only 250 mV across a 100Ω termination. Designers must use IBIS models to simulate their circuit and determine the proper termination resistance value that meets minimum V_{ID} and still has good signal integrity.

Table 4-75. LVDS33 Receiver Characteristics

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.204	1.416	ns

Table 4-76. LVDS33 Transmitter Characteristics

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	2.816	3.313	2.330	2.741	2.329	2.741	2.604	3.063	2.749	3.234	ns

4.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations might contain any combination of drivers, receivers, and transceivers.

4.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 4-77. B-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification					
VI	DC input voltage	0	—	2.625	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)					
VOH	DC output logic high	1.25	1.425	1.6	V
VOL	DC output logic low	0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification					
VOD	Differential output voltage swing	65	—	460	mV
VOCM	Output common mode voltage	1.1	—	1.5	V
VICM[1]	Input common mode voltage	0.05	—	2.2	V
VID[1]	Input differential voltage	0.2	—	VDDI	V

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.

Table 4-78. B-LVDS AC Specifications (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF/100Ω differential load	—	—	500	Mbps
Dmax	Maximum data rate (for MSIOD IO Bank)	AC loading: 2 pF/100Ω differential load	—	—	500	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance	External differential termination	25.65	27	28.35	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	Crosspoint	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

4.8.2.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-79. B-LVDS AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.244	1.463	ns
MSIOD	None	1.232	1.448	ns

Table 4-80. B-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	3.193	3.756	2.756	3.243	2.749	3.234	3.008	3.539	3.240	3.811	ns

4.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations might contain any combination of drivers, receivers, and transceivers.

4.8.3.1 Minimum and Maximum Input and Output Levels

Table 4-81. M-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Min	Typ	Max	Units
M-LVDS Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
M-LVDS DC Input Voltage Specification					
VI	DC input voltage	0	—	2.625	V
IIH (DC)	Input leakage current high	—	—	10	µA
IIL (DC)	Input leakage current low	—	—	10	µA
IOZ (DC)	Tristate leakage current	—	—	10	µA
M-LVDS DC Output Voltage Specification					
VOH	DC output logic high	1.25	1.425	1.6	V
VOL	DC output logic low	0.9	1.075	1.25	V
M-LVDS Differential Voltage Specification					
VOD	Differential output voltage swing	300	—	650	mV
VOCM	Output common mode voltage	0.3	—	2.1	V
VICM[1]	Input common mode voltage	0.05	—	2.2	V
VID[1]	Input differential voltage	200	—	600	mV

Note: Only M-LVDS type I is supported.

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.

Table 4-82. M-LVDS AC Specifications (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF/100Ω differential load	—	—	500	Mbps
Dmax	Maximum data rate (MSIOD IO Bank)	AC loading: 2 pF/100Ω differential load	—	—	500	Mbps
M-LVDS Impedance Specifications						
Rt	Termination resistance	External differential termination	47.5	50	52.5	Ω
M-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	Cross point	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

4.8.3.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, V_{DDI} = 2.375V.

Table 4-83. M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.244	1.463	ns
MSIOD	None	1.232	1.448	ns

Table 4-84. M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	3.193	3.756	2.756	3.243	2.749	3.234	3.008	3.539	3.240	3.811	ns

4.8.4 Mini-LVDS

Mini-LVDS is a unidirectional interface from the timing controller to the column drivers and is designed according to the Texas Instruments Standard SLDA007A.

4.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 4-85. Mini-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage	—	2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC input voltage	—	0	—	2.625	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic high	—	1.25	1.425	1.6	V
VOL	DC output logic low	—	0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing	—	300	—	600	mV
VOCM	Output common mode voltage	—	1	—	1.4	V
VICM[1]	Input common mode voltage	With on-die termination (Rt)	0.05	—	1.5	V
		With external differential termination (Rt)	0.05	—	2.2	V
VID[1, 2]	Input differential voltage	—	200	—	600	mV

Notes:

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas the 2.5 mA current produces only 250 mV across the 100Ω termination.

Table 4-86. Mini-LVDS AC Specifications (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF/100Ω differential load	—	—	520	Mbps
Dmax	Maximum Data Rate (MSIOD IO Bank)	AC loading: 2 pF/100Ω differential load	—	—	700	Mbps
Mini-LVDS Impedance Specifications						

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Rt	Termination resistance	On-die termination resistance	90	100	150	Ω
		External 100Ω differential termination[1]	95	100	105	Ω
		External 200Ω differential termination[1, 2]	190	200	210	Ω
Mini-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	Crosspoint	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

Notes:

1. When the external termination is being used, ODT must be disabled using the Libero SoC.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas the same 2.5 mA current produces only 250 mV across the 100Ω termination.

4.8.4.2 AC Switching Characteristics

Worst-case Military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-87. Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Unit
MSIO	None	1.244	1.463	ns
	100	1.244	1.463	ns
MSIOD	None	1.232	1.448	ns
	100	1.232	1.448	ns

Table 4-88. Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

I/O Bank	t_{DP} Speed Grade –1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade –1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade –1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade –1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade –1	t_{LZ} Speed Grade STD	Units
MSIO	3.177	3.737	2.753	3.238	2.749	3.235	2.998	3.526	3.219	3.786	ns
MSIOD	1.910	2.247	2.079	2.446	2.067	2.432	2.375	2.794	2.537	2.984	ns

4.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

4.8.5.1 Minimum and Maximum Input and Output Levels

Table 4-89. RSDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage	—	2.375	2.5	2.625	V
RSDS DC Input Voltage Specification						
VI	DC input voltage	—	0	—	2.625	V
RSDS DC Output Voltage Specification						
VOH	DC output logic high	—	1.25	1.425	1.6	V
VOL	DC output logic low	—	0.9	1.075	1.25	V
RSDS Differential Voltage Specification						
VOD	Differential output voltage swing	—	100	—	600	mV
VOCM	Output common mode voltage	—	0.5	—	1.5	V
VICM[1]	Input common mode voltage	With on-die termination (Rt)	0.05	—	1.5	V
		With external differential termination (Rt)	0.05	—	2.2	V
VID[1, 2]	Input differential voltage	—	200	—	600	mV

Notes:

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 20Ω termination, whereas the 2.5 mA current produces only 250 mV across the 100Ω termination.

Table 4-90. RSDS AC Specifications (Applicable to MSIO and MSIOD Banks Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
RSDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF/100Ω differential load	—	—	520	Mbps
Dmax	Maximum data rate (MSIOD IO Bank)	AC loading: 10 pF/100Ω differential load	—	—	700	Mbps
RSDS Impedance Specifications						

.....continued						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Rt	Termination resistance	On-die termination resistance	90	100	150	Ω
		External 100Ω differential termination[1]	95	100	105	Ω
		External 200Ω differential termination[1, 2]	190	200	210	Ω
RSDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		—	Crosspoint	—	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	2k	—	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ})		—	5	—	pF

Notes:

1. When the external termination is being used, ODT must be disabled using the Libero SoC.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas the same 2.5 mA current produces only 250 mV across the 100Ω termination.

4.8.5.2 AC Switching Characteristics

Worst-case Military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 2.375V.

Table 4-91. RSDS AC Switching Characteristics for Receiver (Input Buffers)

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.244	1.463	ns
	100	1.244	1.463	ns
MSIOD	None	1.232	1.448	ns
	100	1.232	1.448	ns

Table 4-92. RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

I/O Bank	t_{DP} Speed Grade–1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade–1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade–1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade–1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade–1	t_{LZ} Speed Grade STD	Units
MSIO	3.175	3.736	2.806	3.302	2.800	3.294	2.983	3.509	3.205	3.770	ns
MSIOD											
No pre-emphasis	1.964	2.309	1.952	2.296	1.944	2.287	1.805	2.123	1.887	2.220	ns
Minimum pre-emphasis	1.919	2.257	2.178	2.563	2.154	2.534	2.375	2.793	2.535	2.982	ns

.....continued											
I/O Bank	t_{DP} Speed Grade–1	t_{DP} Speed Grade STD	t_{ZL} Speed Grade–1	t_{ZL} Speed Grade STD	t_{ZH} Speed Grade–1	t_{ZH} Speed Grade STD	t_{HZ} Speed Grade–1	t_{HZ} Speed Grade STD	t_{LZ} Speed Grade–1	t_{LZ} Speed Grade STD	Units
Medium pre-emphasis	1.843	2.167	2.179	2.563	2.154	2.534	2.538	2.985	2.388	2.809	ns
Maximum pre-emphasis	1.807	2.125	2.178	2.563	2.154	2.534	2.375	2.793	2.535	2.982	ns

4.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. RTG4 FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

4.8.6.1 Minimum and Maximum Input Level

Table 4-93. LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks and SerDes REFCLK Only)

Symbol	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	3.15	3.3	3.45	V
LVPECL DC Input Voltage Specification					
VI	DC input voltage	0	—	3.45	V
LVPECL Differential Voltage Specification					
VICM[1]	Input common mode voltage	0.6	—	1.8	V
VID[1, 2]	Input differential voltage	600	—	2400	mV

Notes:

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4V$ and $V_{ICM} – (V_{ID}/2) > –0.3V$.
2. When using LVPECL to input a clock signal, see Table 17-11 and Table 13-3.

Table 4-94. LVPECL Minimum and Maximum AC Switching Speeds (Applicable to MSIO I/O Banks and SerDes REFCLK Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVPECL Impedance Specifications						
Rt	Termination resistance	On-die termination resistance	90	100	150	Ω
LVPECL AC Test Parameters Specifications						
Fmax	Maximum data rate (MSIO I/O Bank)		—	—	700	Mbps

4.8.6.2 AC Switching Characteristics

Worst-case military conditions: T_J = 125 °C, V_{DD} = 1.14V, and V_{DDI} = 3.15V.

Table 4-95. LVPECL Receiver Characteristics

I/O Bank	On-Die Termination (ODT) in Ω	t_{PY} Speed Grade –1	t_{PY} Speed Grade STD	Units
MSIO	None	1.204	1.416	ns
	100	1.204	1.416	ns

4.9 I/O Register Specifications

The following sections describe the input and output register specifications of the RTG4 FPGA devices.

4.9.1 Input Register

Figure 4-5. Timing Model for Input Register

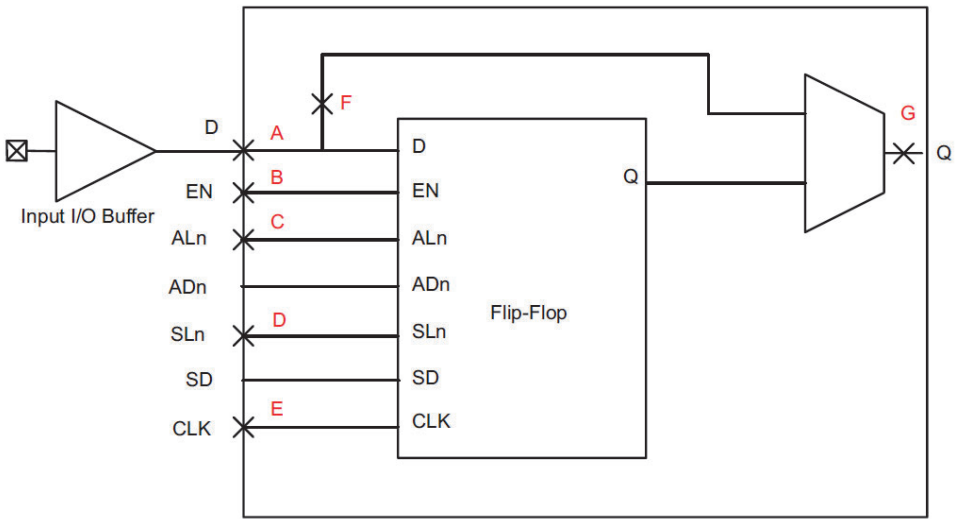
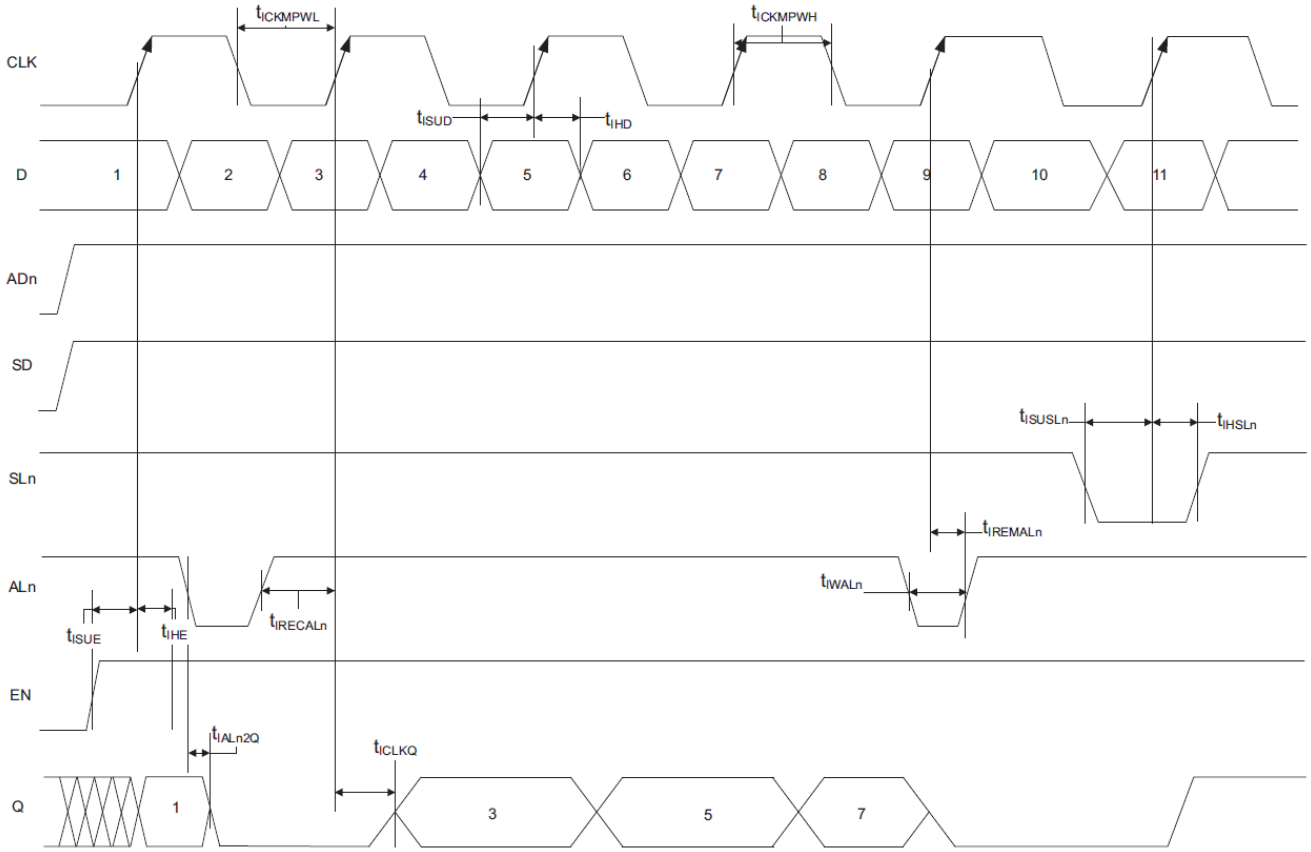


Figure 4-6. I/O Register Input Timing Diagram



The following table lists the input data register propagation delays in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 4-96. Input Data Register Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
t_{ICLKQ}	Clock-to-Q of the Input register	E, G	0.200	0.200	0.235	0.235	ns
t_{ISUD}	Data Setup Time for the Input register	A, E	0.652	1.523	0.767	1.615	ns
t_{IHD}	Data Hold Time for the Input register	A, E	–0.209	0.104	–0.246	0.148	ns
t_{ISUE}	Enable Setup Time for the Input register	B, E	0.968	1.885	1.138	2.106	ns
t_{IHE}	Enable Hold Time for the Input register	B,E	–0.286	–0.006	–0.336	0.019	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input register	D, E	0.828	1.745	0.974	1.941	ns
t_{IHSL}	Synchronous Load Hold Time for the Input register	D, E	–0.212	0.067	–0.250	0.106	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input register (ADn = 1)	C, G	1.013	1.013	1.191	1.191	ns
	Asynchronous Preset-to-Q of the Input register (ADn = 0)	C, G	1.050	1.050	1.236	1.236	ns
$t_{IREMALn}$	Asynchronous Load Removal Time for the Input register	C,E	–0.500	–0.500	–0.588	–0.588	ns
$t_{IRECALn}$	Asynchronous Load Recovery Time for the Input register	C, E	0.948	0.948	1.115	1.115	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input register	C, C	1.041	1.041	1.225	1.225	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input register	E, E	0.320	0.320	0.377	0.377	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input register	E, E	0.333	0.333	0.391	0.391	ns

4.9.2 Output/Enable Register

Figure 4-7. Timing Model for Output/Enable Register

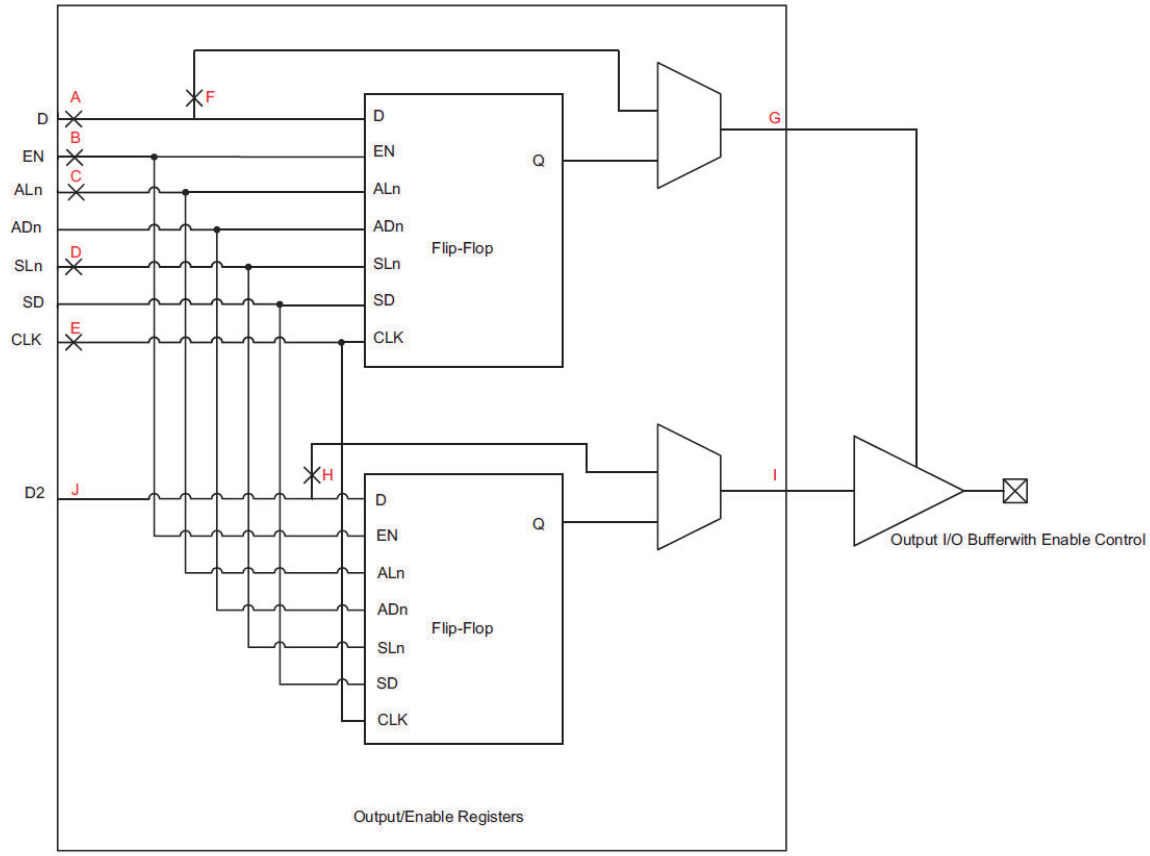
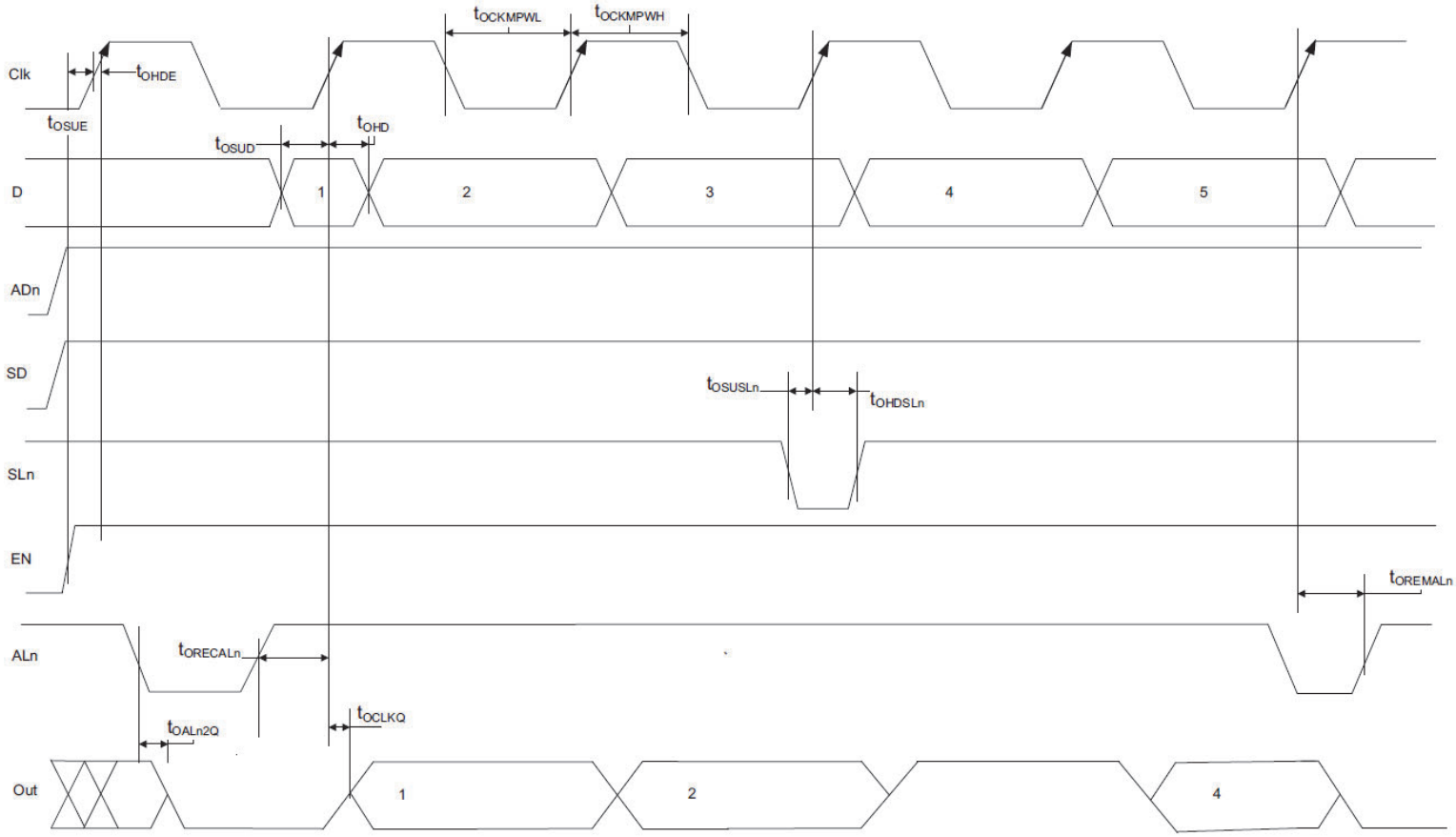


Figure 4-8. I/O Register Output Timing Diagram



The following table lists the input data register propagation delays in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 4-97. Input Data Register Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	Speed Grade–1 SET Filter OFF	Speed Grade–1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Unit
t_{OCLKQ}	Clock-to-Q of the Output/Enable register	E, G or E, I	0.375	0.375	0.441	0.441	ns
t_{OSUD}	Data Setup Time for the Output/Enable register	A, E or J, E	0.622	1.540	0.732	1.700	ns
t_{OHD}	Data Hold Time for the Output/Enable register	A, E or J, E	–0.147	0.132	–0.173	0.182	ns
t_{OSUE}	Enable Setup Time for the Output/Enable register	B, E	0.972	1.890	1.144	2.111	ns

.....continued

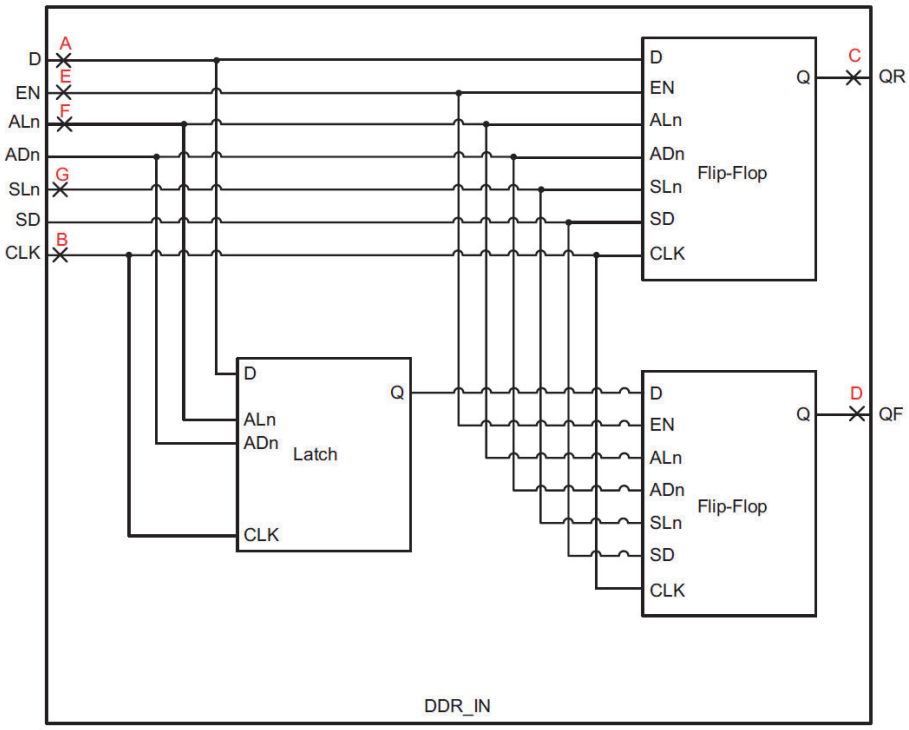
Parameter	Description	Measuring Nodes (from, to)	Speed Grade–1 SET Filter OFF	Speed Grade–1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Unit
t_{OHE}	Enable Hold Time for the Output/Enable register	B, E	–0.280	0.000	–0.329	0.026	ns
t_{OSUSL}	Synchronous load setup time for the Output/Enable register	D, E	0.833	1.750	0.980	1.947	ns
t_{OHSL}	Synchronous load Hold Time for the Output/Enable register	D, E	–0.211	0.069	–0.248	0.108	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/ Enable register (ADn = 1)	C, G or C, I	1.250	1.250	1.471	1.471	ns
	Asynchronous Preset-to-Q of the Output/Enable register (ADn = 0)	C, G or C,I	1.129	1.129	1.329	1.329	ns
$t_{OREMALn}$	Asynchronous Load Removal for the Output/Enable register	C, E	–0.500	–0.500	–0.588	–0.588	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable register	C, E	0.918	0.918	1.079	1.079	ns
t_{OWALn}	Asynchronous Load Minimum Pulse width for the Output/Enable register	C, C	1.034	1.034	1.216	1.216	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable register	E, E	0.322	0.322	0.379	0.379	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable register	E, E	0.334	0.334	0.393	0.393	ns

4.10 DDR Module Specification

The following sections describe input and output DDR module and timing specifications of the RTG 4FPGA devices.

4.10.1 Input DDR Module

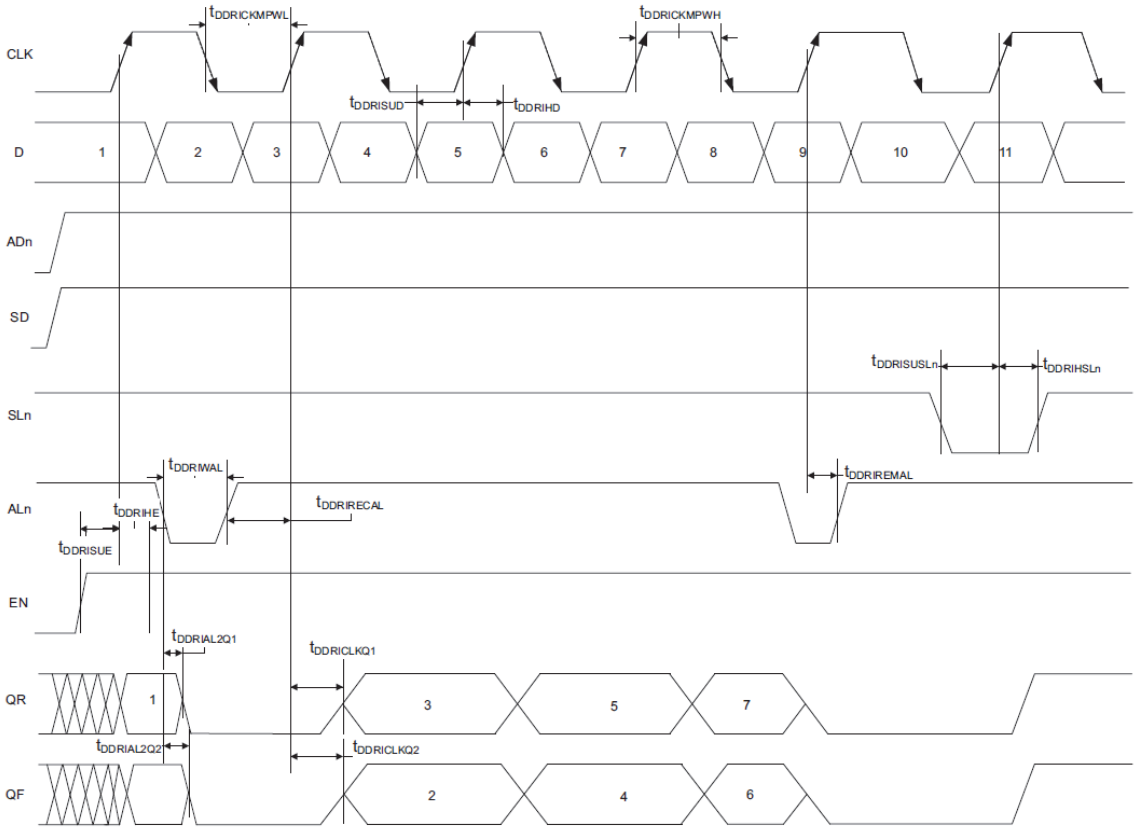
Figure 4-9. Input DDR Module



4.10.2 Input DDR Timing Diagram

The following figure shows the input DDR timing diagram of the RTG4 FPGA devices.

Figure 4-10. Input DDR Timing Diagram



4.10.3 Timing Characteristics

The following table lists the input DDR propagation delays in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 4-98. Input DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	B, C	0.200	0.200	0.235	0.235	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	B, D	0.197	0.197	0.232	0.232	ns
$t_{DDRISUD}$	Data Setup for Input DDR	A, B	0.652	1.523	0.767	1.615	ns
t_{DDRIHD}	Data Hold for Input DDR	A, B	–0.077	0.104	–0.091	0.148	ns
$t_{DDRISUE}$	Enable Setup for Input DDR	E, B	0.968	1.885	1.138	2.106	ns

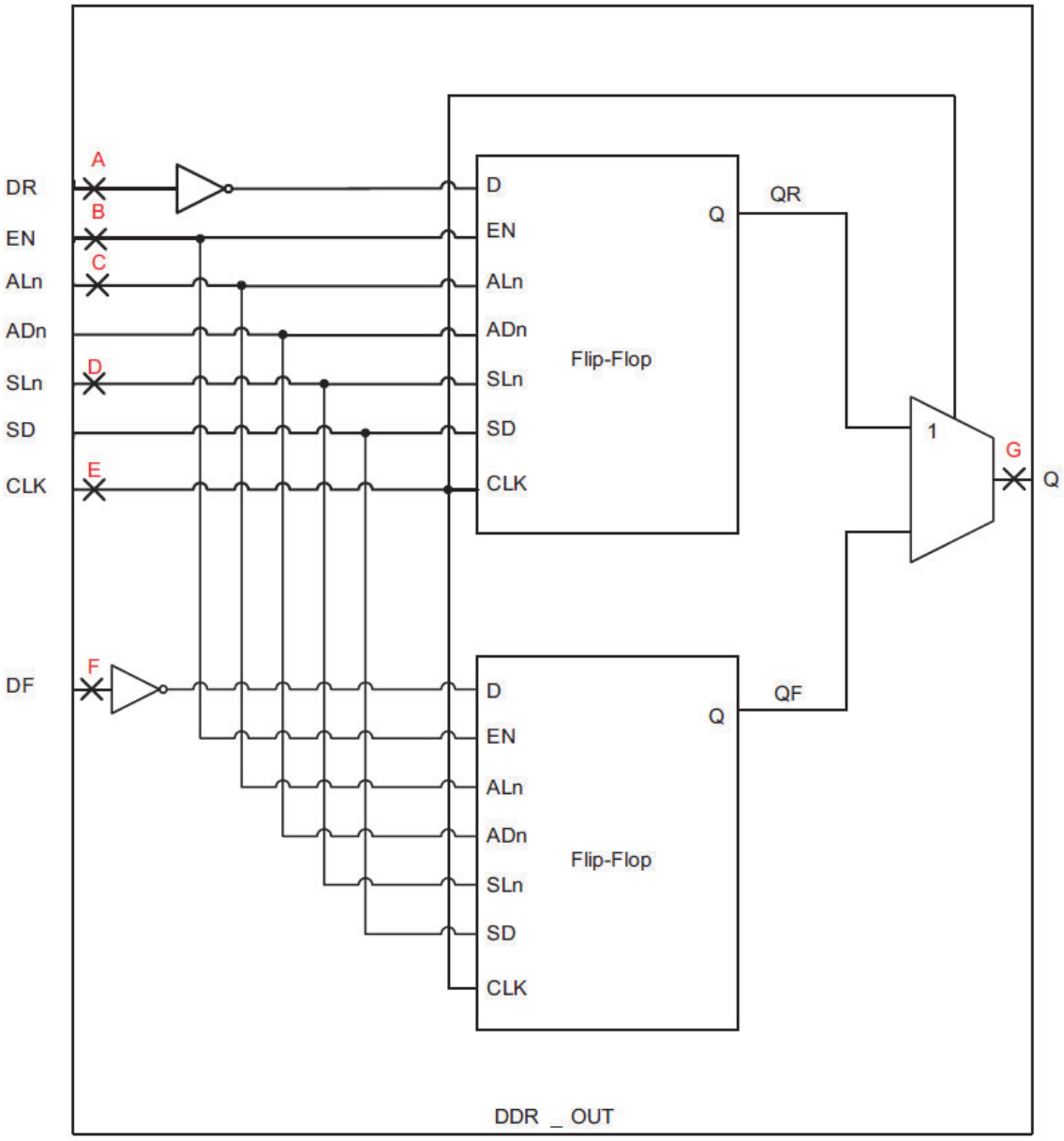
.....continued

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
t_{DDRIHE}	Enable Hold for Input DDR	E, B	–0.286	–0.006	–0.336	0.019	ns
$t_{DDRISUSLn}$	Synchronous Load Setup for Input DDR	G, B	0.828	1.745	0.974	1.941	ns
$t_{DDRIHSLn}$	Synchronous Load Hold for Input DDR	G, B	–0.212	0.067	–0.250	0.106	ns
$t_{DDRIAL2Q1}$	Asynchronous Clear-to-Out QR for Input DDR (ADn = 1)	F, C	1.013	1.013	1.191	1.191	ns
	Asynchronous Preset-to-Out QR for Input DDR (ADn = 0)	F, C	1.050	1.050	1.236	1.236	ns
$t_{DDRIAL2Q2}$	Asynchronous Clear-to-Out QF for Input DDR (ADn=1)	F, D	1.003	1.003	1.180	1.180	ns
	Asynchronous Preset-to-Out QF for Input DDR (ADn=0)	F, D	1.044	1.044	1.228	1.228	ns
$t_{DDRIREMAL}$	Asynchronous Load Removal Time for Input DDR	F, B	–0.500	–0.500	–0.588	–0.588	ns
$t_{DDRIRECAL}$	Asynchronous Load Recovery Time for Input DDR	F, B	0.948	0.948	1.115	1.115	ns
$t_{DDRIWAL}$	Asynchronous Load Minimum Pulse Width for Input DDR	F, F	1.041	1.041	1.225	1.225	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	B, B	0.334	0.320	0.392	0.377	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	B, B	0.333	0.333	0.391	0.391	ns

4.10.4 Output DDR Module

The following figure shows the output DDR module.

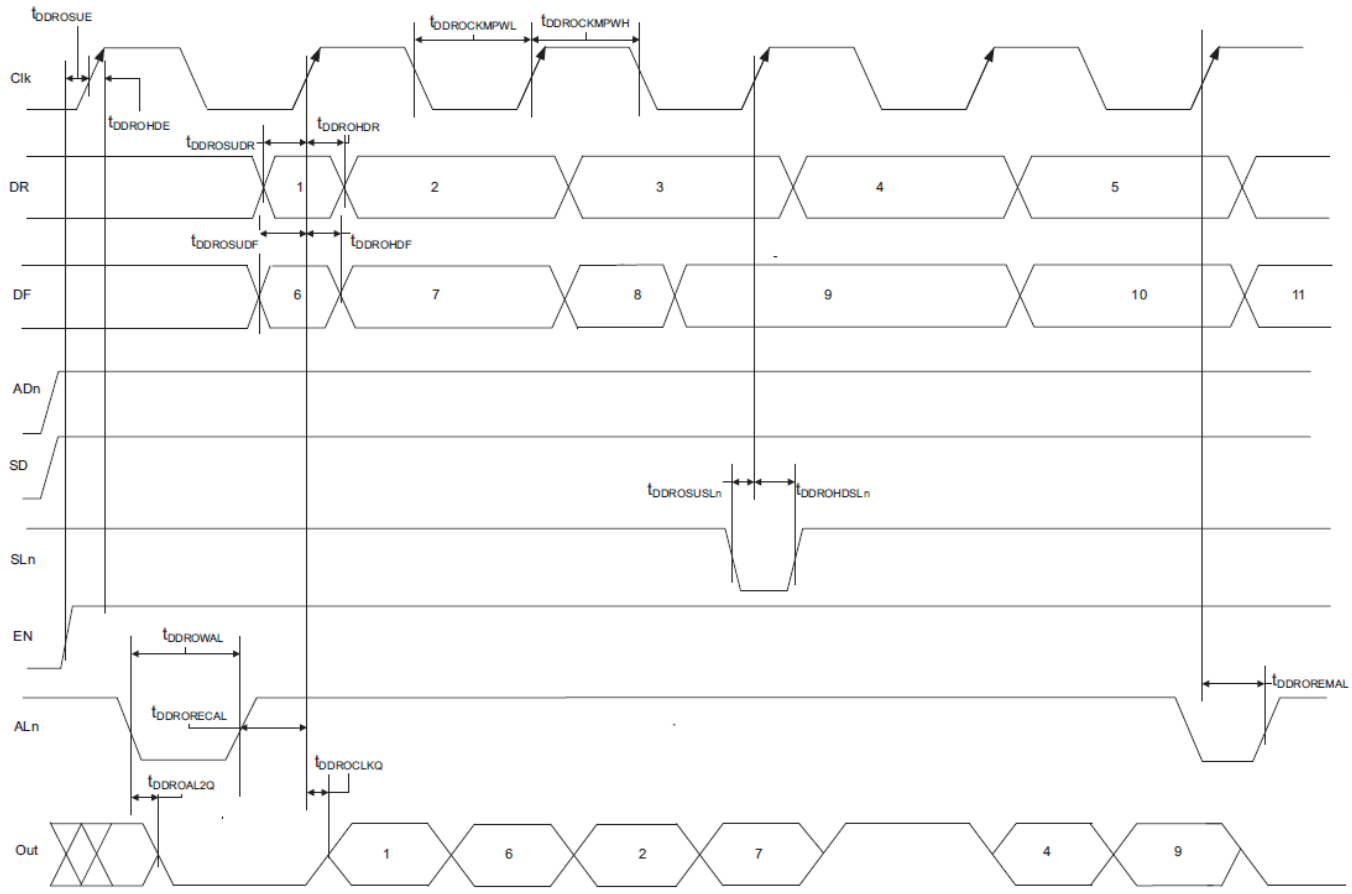
Figure 4-11. Output DDR Module



4.10.5 Output DDR Timing Diagram

The following figure shows the output DDR timing diagram.

Figure 4-12. Output DDR Timing Diagram



4.10.6 Timing Characteristics

The following table lists the input DDR propagation delays in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 4-99. Output DDR Propagation Delays

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$t_{DDROCLKQ}$ [1]	Clock-to-Out of DDR for Output DDR	E, G	0.375	0.375	0.441	0.441	ns
$t_{DDROSUDF}$	DF Data Setup for Output DDR	F, E	0.560	1.478	0.659	1.627	ns
$t_{DDROSUDR}$	DR Data Setup for Output DDR	A, E	0.622	1.540	0.732	1.700	ns
$t_{DDROHDF}$	DF Data Hold for Output DDR	F, E	–0.135	0.145	–0.159	0.197	ns

.....continued

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$t_{DDROHDR}$	DR Data Hold for Output DDR	A, E	–0.147	0.132	–0.173	0.182	ns
$t_{DDROSUE}$	Enable setup for Output DDR	B, E	0.973	1.890	1.145	2.112	ns
t_{DDROHE}	Enable hold for Output DDR	B, E	–0.280	0.000	–0.329	0.026	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Output DDR	D, E	0.833	1.750	0.980	1.947	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Output DDR	D, E	–0.209	0.071	–0.246	0.110	ns
$t_{DDROAL2Q}$	Asynchronous Clear-to-Out for Output DDR (ADn = 1)	C, G	1.235	1.235	1.453	1.453	ns
	Asynchronous Preset-to-Out for Output DDR (ADn = 0)	C, G	1.118	1.118	1.315	1.315	ns
$t_{DDROREMAL}$	Asynchronous Load Removal Time for Output DDR	C, E	–0.500	–0.500	–0.588	–0.588	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery Time for Output DDR	C, E	0.948	0.948	1.115	1.115	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C, C	1.034	1.034	1.216	1.216	ns
$t_{DDROCKMPWH}$	Clock minimum Pulse width high for the Output DDR	E, E	0.335	0.322	0.394	0.379	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E, E	0.334	0.334	0.393	0.393	ns

Note:

1. TDDROCLKQ listed in the datasheet is the worst-case delay. For specific propagation delay values in rising versus falling clock edge analysis, see the *SmartTime Expanded Path Reports*, with the number of parallel paths reported increased from the default value of 1.

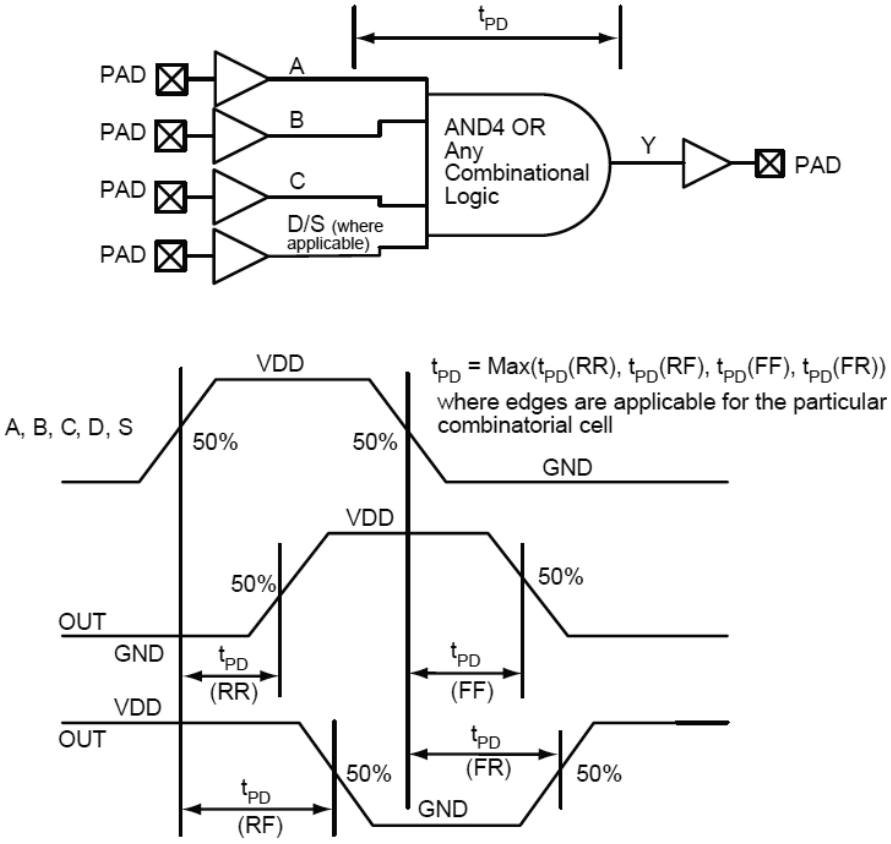
5. Logic Element Specifications

The following sections describe the logic element specifications of the RTG4 FPGA devices.

5.1 LUT4

The RTG4 FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, see the *RTG4 Macro Library Guide*.

Figure 5-1. LUT4



5.1.1 Timing Characteristics

The following table lists the combinatorial cell propagation delays in worst-case military conditions when T_J = 125 °C and V_{DD} = 1.14V.

Table 5-1. Combinatorial Cell Propagation Delays

Combinatorial Cell	Equation	Parameter	Speed Grade –1	Speed Grade STD	Units
BUFD	Y = A	t_{PD}	0.061	0.072	ns
INV	Y = !A	t_{PD}	0.061	0.072	ns
INVD	Y = !A	t_{PD}	0.061	0.072	ns
AND2	Y = A · B	t_{PD}	0.156	0.183	ns

.....continued					
Combinatorial Cell	**Equation**	**Parameter**	**Speed Grade –1**	**Speed Grade STD**	**Units**
NAND2	Y = !(A · B)	t_{PD}	0.131	0.154	ns
OR2	Y = A + B	t_{PD}	0.156	0.183	ns
NOR2	Y = !(A + B)	t_{PD}	0.131	0.154	ns
XOR2	Y = A ⊕ B	t_{PD}	0.156	0.183	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.299	0.352	ns
AND3	Y = A · B · C	t_{PD}	0.299	0.352	ns
AND4	Y = A · B · C · D	t_{PD}	0.418	0.492	ns

5.2 Sequential Module

RTG4 FPGAs offer a separate flip-flop, which can be used independently from the LUT. The flip-flop has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

Figure 5-2. Sequential Module

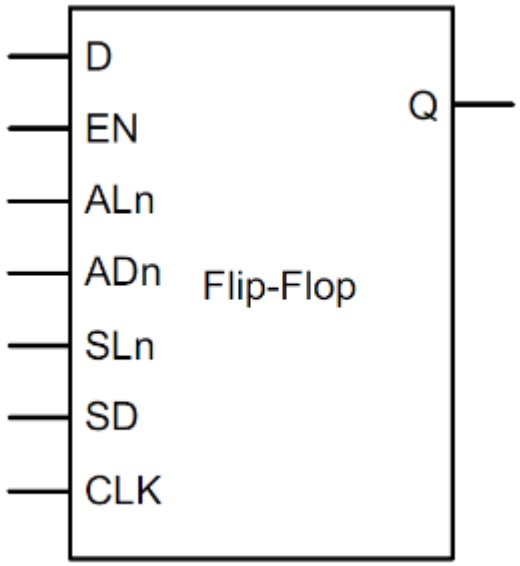
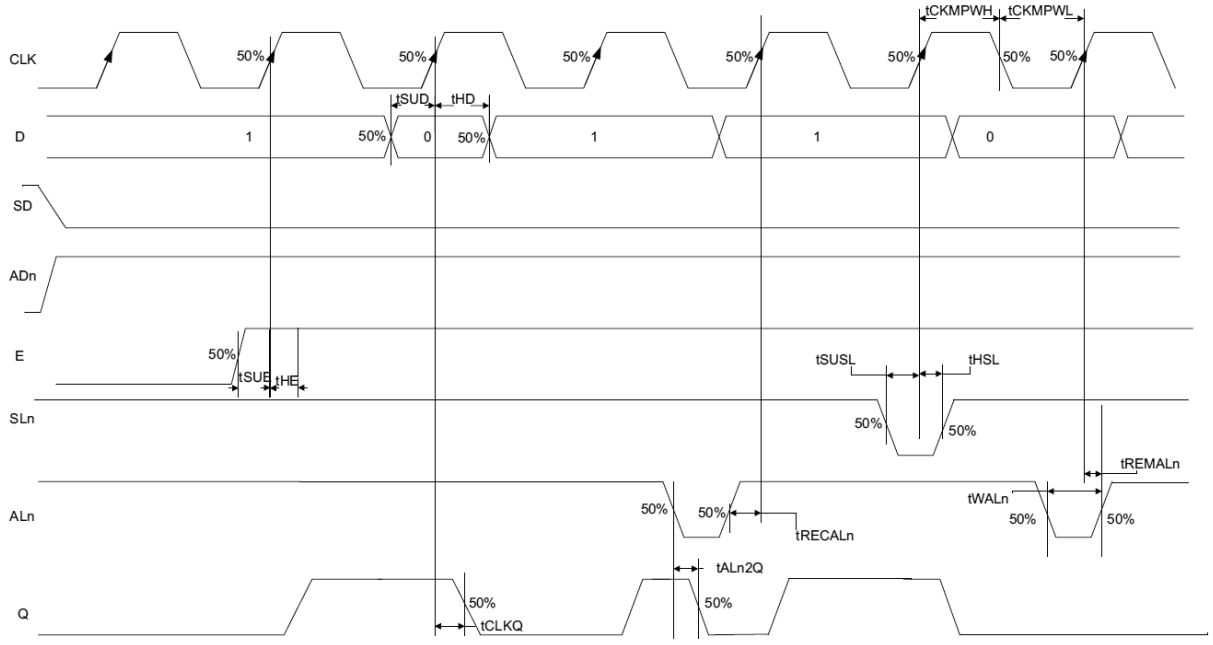


Figure 5-3 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop.

Figure 5-3. Sequential Module Timing Diagram



5.2.1 Timing Characteristics

The following table lists register delays in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 5-2. Register Delays

Parameter	Description	Speed Grade–1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{CLKQ}	Clock-to-Q of the core register	0.207	0.207	0.243	0.243	ns
T_{SUD}	Data setup time for the core register	0.429	1.300	0.505	1.3	ns
T_{HD}	Data hold time for the core register	–0.005	0.275	–0.005	0.35	ns
T_{SUE}	Enable setup time for the core register	1.098	1.968	1.291	2.096	ns
T_{HE}	Enable hold time for the input register	–0.435	–0.155	–0.512	–0.156	ns
T_{SUSL}	Synchronous load setup time for the core Register	0.872	1.789	1.025	1.993	ns
T_{HSL}	Synchronous load hold time for the Core register	–0.144	0.136	–0.169	0.187	ns

.....continued

Parameter	Description	Speed Grade–1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{ALN2Q}	Asynchronous Clear-to-Q of the Core register (ADn = 1)	1.037	1.037	1.220	1.22	ns
	Asynchronous Preset-to-Q of the core register (ADn = 0)	1.066	1.066	1.255	1.255	ns
T_{REMALN}	Asynchronous load removal time for the core register	–0.853	–0.853	–1.003	–1.003	ns
T_{RECALN}	Asynchronous load recovery time for the Core register	0.879	0.879	1.034	1.034	ns
T_{WALN}	Asynchronous load minimum pulse width for the core register	0.129	0.129	0.152	0.152	ns
T_{CKMPWH}	Clock minimum pulse width high for the core register	0.142	0.142	0.167	0.167	ns
T_{CKMPWL}	Clock minimum pulse width low for the core register	0.201	0.201	0.237	0.237	ns

Note: This timing data represents worst-case path delays. See the *SmartTime Static Timing Analysis Expanded Path Reports* for propagation delays with respect to various combinations of rising or falling data and clock.

6. Global Resource Characteristics

The RTG4 FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. See the *RTG4 FPGA Fabric User Guide* for the positions of various global routing resources.

The following table lists the RTG4 150 device global resources in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 6-1. RT4G150 Device Global Resource

Parameter	Description	Speed Grade –1		Speed Grade STD		Units
		Min	Max	Min	Max	
T_{RCKL}	Input Low Delay for Global Clock	3.26	3.649	3.836	4.291	ns
T_{RCKH}	Input High Delay for Global Clock	3.721	4.161	4.377	4.895	ns
T_{RCKSW}	Maximum Skew for Global Clock	—	0.44	—	0.518	ns

7. FPGA Fabric SRAM

The following sections describe the FPGA Fabric SRAM of the RTG4 FPGA devices. See the UG0574: RTG4 FPGA Fabric User Guide for more information.

7.1 FPGA Fabric Large SRAM (LSRAM)

The following table lists the RAM1K18—dual-port mode for depth × width configuration 1K × 18 in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 7-1. RAM1K18—Dual-Port Mode for Depth × Width Configuration 1Kx18

Parameter	Description	Speed Grade–1 SET Filter OFF	Speed Grade–1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{CY}	Clock Period with all pipelines enabled	4.000	4.762	4.717	5.616	ns
$T_{CLKMPWH}$	Clock Minimum Pulse Width High	0.600	0.600	0.600	0.600	ns
$T_{CLKMPWL}$	Clock Minimum pulse Width Low	0.600	0.600	0.600	0.600	ns
T_{ADDRSU}	Address Setup Time (ECC = OFF)	1.996	2.345	2.349	2.759	ns
	Address Setup Time (ECC = BYPASS)[1]	—	2.345	—	2.759	ns
	Address Setup Time (ECC = PIPELINE)	1.760	1.894	2.070	2.228	ns
T_{ADDRHD}	Address Hold Time (ECC = OFF)	–0.006	–0.255	–0.007	–0.299	ns
	Address Hold Time (ECC = BYPASS)[1]	—	–0.255	—	–0.299	ns
	Address Hold Time (ECC = PIPELINE)	–0.123	0.129	–0.145	0.152	ns
T_{DSU}	Data Setup Time	2.127	2.159	2.502	2.539	ns
T_{DHD}	Data Hold Time	–0.218	0.036	–0.257	0.042	ns
T_{BLKSU}	Block Select Setup Time (ECC = OFF)	1.934	1.948	2.286	2.291	ns
	Block Select Setup Time (ECC = BYPASS)[1]	—	1.948	—	2.291	ns
	Block Select Setup Time (ECC = PIPELINE)	1.725	1.831	2.029	2.154	ns
T_{BLKHD}	Block Select Hold Time (ECC = OFF)	–0.375	–0.022	–0.441	–0.026	ns
	Block Select Hold Time (ECC = BYPASS)[1]	—	–0.022	—	–0.026	ns
	Block Select Hold Time (ECC = PIPELINE)	–0.319	–0.078	–0.375	–0.092	ns
$T_{RDENPIPESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	2.128	2.628	2.504	3.091	ns

.....continued

Parameter	Description	Speed Grade–1 SET Filter OFF	Speed Grade–1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$T_{RDENPIPEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.675	–0.911	–0.794	–1.702	ns
T_{RSTREM}	Asynchronous Reset Removal Time	1.118	1.118	1.315	1.315	ns
T_{RSTREC}	Asynchronous Reset Recovery Time	–0.801	–0.801	–0.942	–0.942	ns
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.587	0.587	0.587	0.587	ns
T_{SRSTSU}	Synchronous Reset Setup Time	2.292	2.212	2.696	2.602	ns
T_{SRSTHD}	Synchronous Reset Hold Time	–0.615	–0.250	–0.724	–0.294	ns
T_{RDESU}	Read Enable Setup Time	1.479	1.863	1.740	2.191	ns
T_{RDEHD}	Read Enable Hold Time	0.029	–0.207	0.034	–0.244	ns
T_{WESU}	Write Enable Setup Time with Simple write mode (ECC = OFF)	1.505	2.005	1.771	2.358	ns
	Write Enable Setup Time with Simple write mode (ECC = BYPASS)[1]		2.005		2.358	ns
	Write Enable Setup Time with ECC = PIPELINE	4.015	4.121	4.723	4.848	ns
T_{WEHD}	Write Enable Hold Time with Simple write mode (ECC = OFF)	0.131	–0.105	0.154	–0.124	ns
	Write Enable Hold Time with Simple write mode (ECC = BYPASS)[1]	—	–0.105		–0.124	ns
	Write Enable Hold Time with ECC = PIPELINE	–0.176	0.076	–0.207	0.089	ns
T_{CLK2Q}	Read Access Time with OUTPUT=PIPELINE	2.090	2.090	2.458	2.458	ns
	Read Access Time with ECC=OFF, OUTPUT=BYPASS	5.694	5.694	6.698	6.698	ns
	Read Access Time with ECC=BYPASS, OUTPUT=BYPASS[1]	—	6.607	—	7.773	ns
	Read Access Time with ECC=PIPELINE, OUTPUT=BYPASS	4.204	4.204	4.946	4.946	ns
T_{R2Q}	Asynchronous Reset to Output Propagation Delay	1.373	1.373	1.615	1.615	ns
FMAX	Maximum Frequency with all pipelines enabled	250	210	212	178	MHz

Note:

1. ECC = BYPASS mode, also known as non-pipelined ECC mode, is not supported with SET filter OFF.

The following table lists the RAM1K18—two-port mode for depth × width configuration 512 × 36 in worst-case military conditions when T_J = 125 °C and V_{DD} = 1.14V.

Table 7-2. RAM1K18—Two-Port Mode for Depth x Width Configuration 512 x 36

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{CY}	Clock Period with all pipelines enabled	4.000	4.762	4.717	5.616	ns
$T_{CLKMPWH}$	Clock Minimum Pulse Width High	0.600	0.600	0.600	0.600	ns
$T_{CLKMPWL}$	Clock Minimum pulse Width Low	0.600	0.600	0.600	0.600	ns
T_{ADDRSU}	Address Setup Time (ECC = OFF)	1.996	2.345	2.349	2.759	ns
	Address Setup Time (ECC = BYPASS)[1]	—	2.345	—	2.759	ns
	Address Setup Time (ECC = PIPELINE)	1.760	1.894	2.070	2.228	ns
T_{ADDRHD}	Address Hold Time (ECC = OFF)	–0.006	–0.255	–0.007	–0.299	ns
	Address Hold Time (ECC = BYPASS)[1]	—	–0.255	—	–0.299	ns
	Address Hold Time (ECC = PIPELINE)	–0.123	0.129	–0.145	0.152	ns
T_{DSU}	Data Setup Time	2.128	2.160	2.503	2.541	ns
T_{DHD}	Data Hold Time	–0.219	0.125	–0.152	0.147	ns
T_{BLKSU}	Block Select Setup Time (ECC = OFF)	1.943	1.948	2.286	2.291	ns
	Block Select Setup Time (ECC = BYPASS)[1]	—	1.948	—	2.291	ns
	Block Select Setup Time (ECC = PIPELINE)	1.725	1.831	2.029	2.154	ns
T_{BLKHD}	Block Select Hold Time (ECC = OFF)	–0.375	–0.022	–0.441	–0.026	ns
	Block Select Hold Time (ECC = BYPASS)[1]	—	–0.022	—	–0.026	ns
	Block Select Hold Time (ECC = PIPELINE)	–0.319	–0.078	–0.375	–0.092	ns
$T_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	2.136	2.635	2.513	3.100	ns
$T_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.658	–0.894	–0.774	–1.052	ns
T_{RSTREM}	Asynchronous Reset Removal Time	1.118	1.118	1.315	1.315	ns
T_{RSTREC}	Asynchronous Reset Recovery Time	–0.801	–0.801	–0.942	–0.942	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.587	0.587	0.587	0.587	ns
T_{SRSTSU}	Synchronous Reset Setup Time	2.292	2.212	2.696	2.602	ns
T_{SRSTHD}	Synchronous Reset Hold Time	–0.615	–0.250	–0.724	–0.294	ns
T_{RDESU}	Read Enable Setup Time without ECC pipeline	1.479	1.861	1.740	2.189	ns
T_{RDEHD}	Read Enable Hold Time without ECC pipeline	0.029	–0.207	0.034	–0.244	ns
T_{WESU}	Write Enable Setup Time (ECC = OFF)	1.508	2.007	1.774	2.361	ns
	Write Enable Setup Time (ECC = BYPASS)[1]		2.007		2.361	ns
	Write Enable Setup Time (ECC = PIPELINE)	3.976	4.082	4.678	4.802	ns
T_{WEHD}	Write Enable Hold Time (ECC = OFF)	0.131	–0.105	0.154	–0.124	ns
	Write Enable Hold Time (ECC = BYPASS)[1]	—	–0.105	—	–0.124	ns
	Write Enable Hold Time (ECC = PIPELINE)	–0.176	0.076	–0.207	0.089	ns
T_{CLK2Q}	Read Access Time with OUTPUT=PIPELINE	1.807	1.807	2.125	2.125	ns
	Read Access Time with ECC=OFF, OUTPUT=BYPASS	5.360	5.360	6.306	6.306	ns
	Read Access Time with ECC=BYPASS, OUTPUT=BYPASS[1]	—	6.249	—	7.351	ns
	Read Access Time with ECC=PIPELINE, OUTPUT=BYPASS	3.916	3.916	4.607	4.607	ns
T_{R2Q}	Asynchronous Reset to Output Propagation Delay	1.373	1.373	1.615	1.615	ns
FMAX	Maximum Frequency with all pipelines enabled	250	210	212	178	MHz

Note:

1. ECC = BYPASS mode, also known as non-pipelined ECC mode, is not supported with SET filter OFF.

7.2 FPGA Fabric Micro SRAM (µSRAM)

The following table lists the µSRAM in 64 × 18 mode in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 7-3. RAM1K18—Two-Port Mode for Depth x Width Configuration 512 x 36

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{CY}	Clock Period with all pipelines enabled	3.922	3.922	4.630	4.630	ns
$T_{CLKMPWH}$	Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CLKMPWL}$	Clock Minimum pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{ADDRSU}	Read Address Setup Time with INPUT = PIPELINE	1.828	2.384	2.150	2.805	ns
	Read Address Setup Time with INPUT = BYPASS, ECC = PIPELINE	4.262	4.262	5.013	5.013	ns
	Read Address Setup Time with INPUT = BYPASS, ECC = OFF, OUTPUT = PIPELINE	4.642	5.254	5.461	6.181	ns
	Read Address Setup Time with INPUT = BYPASS, ECC = BYPASS, OUTPUT = PIPELINE	6.929	7.541	8.151	8.871	ns
T_{ADDRHD}	Read Address Hold Time with INPUT = PIPELINE	–0.380	–0.689	–0.447	–0.811	ns
	Read Address Hold Time with INPUT = BYPASS, ECC = PIPELINE	–2.733	–2.733	–3.216	–3.216	ns
	Read Address Hold Time with INPUT = BYPASS, ECC = OFF, OUTPUT = PIPELINE	–2.592	–2.852	–3.049	–3.355	ns
	Read Address Hold Time with INPUT = BYPASS, ECC = BYPASS, OUTPUT = PIPELINE	–4.157	–4.417	–4.890	–5.196	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{BLKSU}	Read Block Select Setup Time with INPUT = PIPELINE	2.032	2.483	2.390	2.922	ns
	Read Block Select Setup Time with INPUT = BYPASS, ECC=PIPELINE	1.614	1.614	1.899	1.899	ns
	Read Block Select Setup Time with INPUT = BYPASS, ECC = OFF, OUTPUT = PIPELINE	1.996	2.608	2.348	3.068	ns
	Read Block Select Setup Time with INPUT = BYPASS, ECC = BYPASS, OUTPUT = PIPELINE	3.493	4.104	4.109	4.828	ns
T_{BLKHD}	Read Block Select Hold Time with INPUT = PIPELINE	–0.618	–0.374	–0.728	–0.440	ns
	Read Block Select Hold Time with INPUT = BYPASS, ECC = PIPELINE	–0.901	–0.901	–1.059	–1.059	ns
	Read Block Select Hold Time with INPUT = BYPASS, ECC = OFF, OUTPUT = PIPELINE	–0.515	–0.774	–0.605	–0.911	ns
	Read Block Select Hold Time with INPUT = BYPASS, ECC = BYPASS, OUTPUT = PIPELINE	–2.109	–2.368	–2.480	–2.786	ns
T_{BLKMPW}	Read Block Select Minimum Pulse Width Low	0.350	0.350	0.350	0.350	ns
T_{RSTREM}	Read Asynchronous Reset Removal Time	0.987	0.987	1.161	1.161	ns
T_{RSTREC}	Read Asynchronous Reset Recovery Time	–0.566	–0.566	–0.666	–0.666	ns
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	1.003	1.003	1.003	1.003	ns
$T_{RDENADDRSU}$	Read Address Read Enable Setup Time (A_ADDR_EN, B_ADDR_EN)	1.538	1.977	1.810	2.326	ns
$T_{RDENADDRHD}$	Read Address Read Enable Hold Time (A_ADDR_EN, B_ADDR_EN)	–0.181	0.063	–0.213	0.075	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$T_{RDSRSTADDRSU}$	Read Address Synchronous Reset Setup Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	1.566	2.005	1.842	2.358	ns
$T_{RDSRSTADDRHD}$	Read Address Synchronous Reset Hold Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	–0.183	0.061	–0.216	0.072	ns
$T_{RDENPIPESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	1.503	1.941	1.768	2.284	ns
$T_{RDENPIPEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.152	0.092	–0.178	0.109	ns
$T_{RDSRSTPIPESU}$	Pipelined Read Synchronous Reset Setup Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	1.837	2.337	2.161	2.750	ns
$T_{RDSRSTPIPEHD}$	Pipelined Read Synchronous Reset Hold Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	–0.835	–1.094	–0.982	–1.288	ns
T_{CCY}	Write Clock Period all pipeline enabled	3.922	3.922	4.630	4.630	ns
$T_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{BLKCSU}	Write Block Setup Time (ECC = OFF or ECC = BYPASS)	1.575	2.083	1.853	2.451	ns
	Write Block Setup Time (ECC = PIPELINE)	1.305	1.908	1.535	2.245	ns
T_{BLKCHD}	Write Block Hold Time (ECC = OFF or ECC = BYPASS)	–0.190	–0.427	–0.224	–0.502	ns
	Write Block Hold Time (ECC = PIPELINE)	–0.320	–0.629	–0.376	–0.740	ns
T_{DINCSU}	Write Input Data setup Time	1.238	1.960	1.456	2.306	ns
T_{DINCHD}	Write Input Data hold Time	0.100	–0.321	0.118	–0.377	ns
$T_{ADDRCSU}$	Write Address Setup Time (ECC = OFF or ECC = BYPASS)	1.591	2.017	1.872	2.373	ns
	Write Address Setup Time (ECC = PIPELINE)	1.337	1.928	1.573	2.268	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$T_{ADDRCHD}$	Write Address Hold Time (ECC = OFF or ECC = BYPASS)	–0.110	–0.453	–0.129	–0.533	ns
	Write Address Hold Time (ECC = PIPELINE)	0.028	–0.281	0.033	–0.331	ns
T_{WECSU}	Write Enable Setup Time (ECC = OFF or ECC = BYPASS)	1.437	1.945	1.690	2.288	ns
	Write Enable Setup Time (ECC = PIPELINE)	1.158	1.760	1.363	2.070	ns
T_{WECHD}	Write Enable Hold Time (ECC = OFF or ECC = BYPASS)	–0.139	–0.376	–0.164	–0.442	ns
	Write Enable Hold Time (ECC = PIPELINE)	–0.054	–0.313	–0.063	–0.369	ns
T_{CLK2Q}	Read Access Time with OUTPUT = PIPELINE	1.726	1.726	2.030	2.030	ns
	Read Access Time with ECC = PIPELINE, OUTPUT = BYPASS	4.557	4.557	5.361	5.361	ns
	Read Access Time with INPUT = PIPELINE, ECC = OFF, OUTPUT = BYPASS	4.371	4.371	5.142	5.142	ns
	Read Access Time with INPUT = PIPELINE, ECC = BYPASS, OUTPUT = BYPASS	6.767	6.767	7.960	7.960	ns
T_{ADDR2Q}	Read Address to Out Data Access time with INPUT = BYPASS, ECC = OFF, OUPUT = BYPASS	6.257	6.257	7.360	7.360	ns
	Read Address to Out Data Access Time with INPUT = BYPASS, ECC = BYPASS, OUPUT = BYPASS	8.651	8.651	10.178	10.178	ns

.....continued						
Parameter	**Description**	**Speed Grade –1 SET Filter OFF**	**Speed Grade –1 SET Filter ON**	**Speed Grade STD SET Filter OFF**	**Speed Grade STD SET Filter ON**	**Units**
T_{BLK2Q}	Read Block Select to Out Disable Time with INPUT = BYPASS, ECC = OFF, OUPUT = BYPASS	3.569	3.569	4.199	4.199	ns
	Read Block Select to Out Disable Time with INPUT = BYPASS, ECC = BYPASS, OUPUT = BYPASS	5.899	5.899	6.940	6.940	ns
T_{R2Q}	Read Asynchronous Reset to Output Propagation Delay	1.237	1.237	1.456	1.456	ns
FMAX	Maximum Frequency with all pipelines enabled	255	255	216	216	MHz

The following table lists the µSRAM in 128 × 12 mode in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 7-4. µSRAM (RAM64 x 18) in 128 x 12 Mode

Parameter	**Description**	**Speed Grade –1 SET Filter OFF**	**Speed Grade –1 SET Filter ON**	**Speed Grade STD SET Filter OFF**	**Speed Grade STD SET Filter ON**	**Units**
T_{CY}	Read Clock Period with all pipelines enabled	3.922	3.922	4.630	4.630	ns
$T_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{ADDRSU}	Read Address Setup Time with INPUT = PIPELINE	1.828	2.384	2.150	2.805	ns
	Read Address Setup Time with INPUT = BYPASS, OUTPUT = PIPELINE	4.642	5.254	5.461	6.181	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{ADDRHD}	Read Address Hold Time with INPUT = PIPELINE	–0.380	–0.689	–0.447	–0.811	ns
	Read Address Hold Time with INPUT = BYPASS, OUTPUT = PIPELINE	–2.592	–2.852	–3.049	–3.355	ns
T_{BLKSU}	Read Block Select Setup Time INPUT = PIPELINE	2.032	2.483	2.390	2.922	ns
	Read Block Select Setup Time INPUT = BYPASS, OUTPUT = PIPELINE	1.996	2.608	2.348	3.068	ns
T_{BLKHD}	Read Block Select Hold Time with INPUT = PIPELINE	–0.618	–0.374	–0.728	–0.440	ns
	Read Block Select Hold Time with INPUT = BYPASS, OUTPUT = PIPELINE	–0.515	–0.774	–0.605	–0.911	ns
T_{BLKMPW}	Read Block Select Minimum Pulse Width Low	0.350	0.350	0.350	0.350	ns
T_{RSTREM}	Read Asynchronous Reset Removal Time	0.987	0.987	1.161	1.161	ns
T_{RSTREC}	Read Asynchronous Reset Recovery Time	–0.566	–0.566	–0.666	–0.666	ns
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	1.003	1.003	1.003	1.003	ns
$T_{RDENADDRSU}$	Read Address Read Enable Setup Time (A_ADDR_EN, B_ADDR_EN)	1.538	1.977	1.810	2.326	ns
$T_{RDENADDRHD}$	Read Address Read Enable Hold Time (A_ADDR_EN, B_ADDR_EN)	–0.181	0.063	–0.213	0.075	ns
$T_{RDSRSTADDRSU}$	Read Address Synchronous Reset Setup Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	1.566	2.005	1.842	2.358	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$T_{RDSRSTADDRHD}$	Read Address Synchronous Reset Hold Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	–0.183	0.061	–0.216	0.072	ns
$T_{RDENPIPESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	1.503	1.941	1.768	2.284	ns
$T_{RDENPIPEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.152	0.092	–0.178	0.109	ns
$T_{RDSRSTPIPESU}$	Pipelined Read Synchronous Reset Setup Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	1.837	2.337	2.161	2.750	ns
$T_{RDSRSTPIPEHD}$	Pipelined Read Synchronous Reset Hold Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	–0.835	–1.094	–0.982	–1.288	ns
T_{CCY}	Write Clock Period all pipeline enabled	3.922	3.922	4.630	4.630	ns
$T_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{BLKCSU}	Write Block Setup Time	1.575	2.083	1.853	2.451	ns
T_{BLKCHD}	Write Block Hold Time	–0.190	–0.427	–0.224	–0.502	ns
T_{DINCSU}	Write Input Data setup Time	1.238	1.960	1.456	2.306	ns
T_{DINCHD}	Write Input Data hold Time	–0.033	–0.404	–0.039	–0.475	ns
$T_{ADDRCSU}$	Write Address Setup Time	1.591	2.017	1.872	2.373	ns
$T_{ADDRCHD}$	Write Address Hold Time	–0.110	–0.453	–0.129	–0.533	ns
T_{WECSU}	Write Enable Setup Time	1.437	1.945	1.690	2.288	ns
T_{WECHD}	Write Enable Hold Time	–0.139	–0.376	–0.164	–0.442	ns
T_{CLK2Q}	Read Access Time with OUTPUT = PIPELINE	1.725	1.725	2.029	2.029	ns
	Read Access Time with INPUT = PIPELINE, OUTPUT = BYPASS	4.296	4.296	5.054	5.054	ns

.....continued						
Parameter	**Description**	**Speed Grade –1 SET Filter OFF**	**Speed Grade –1 SET Filter ON**	**Speed Grade STD SET Filter OFF**	**Speed Grade STD SET Filter ON**	**Units**
T_{ADDR2Q}	Read Address to Out Data Access time with INPUT = BYPASS, OUPUT = BYPASS	6.180	6.180	7.270	7.270	ns
T_{BLK2Q}	Read Block Select to Out Disable Time with INPUT = BYPASS, OUPUT = BYPASS	3.485	3.485	4.100	4.100	ns
T_{R2Q}	Read Asynchronous Reset to Output Propagation Delay	1.231	1.231	1.448	1.448	ns
FMAX	Maximum Frequency with all pipelines enabled	255	255	216	216	MHz

The following table lists the µSRAM in 128 × 9 mode in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 7-5. µSRAM (RAM64 x 18) in 128 x 9 Mode

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{CY}	Read Clock Period with all pipelines enabled	3.922	3.922	4.630	4.630	ns
$T_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CLKMPWL}$	Read Clock Minimum pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{ADDRSU}	Read Address Setup Time with INPUT = PIPELINE	1.828	2.384	2.150	2.805	ns
	Read Address Setup Time with INPUT = BYPASS, OUTPUT = PIPELINE	4.642	5.254	5.461	6.181	ns
T_{ADDRHD}	Read Address Hold Time with INPUT = PIPELINE	–0.380	–0.689	–0.447	–0.811	ns
	Read Address Hold Time with INPUT = BYPASS, OUTPUT = PIPELINE	–2.592	–2.852	–3.049	–3.355	ns

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Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
T_{BLKSU}	Read Block Select Setup Time INPUT = PIPELINE	2.032	2.483	2.390	2.922	ns
	Read Block Select Setup Time INPUT = BYPASS, OUTPUT = PIPELINE	1.996	2.608	2.348	3.068	ns
T_{BLKHD}	Read Block Select Hold Time with INPUT = PIPELINE	–0.618	–0.374	–0.728	–0.440	ns
	Read Block Select Hold Time with INPUT = BYPASS, OUTPUT = PIPELINE	–0.515	–0.774	–0.605	–0.911	ns
T_{BLKMPW}	Read Block Select Minimum Pulse Width Low	0.350	0.350	0.350	0.350	ns
T_{RSTREM}	Read Asynchronous Reset Removal Time	0.987	0.987	1.161	1.161	ns
T_{RSTREC}	Read Asynchronous Reset Recovery Time	–0.566	–0.566	–0.666	–0.666	ns
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	1.003	1.003	1.003	1.003	ns
$T_{RDENADDRSU}$	Read Address Read Enable Setup Time (A_ADDR_EN, B_ADDR_EN)	1.538	1.977	1.810	2.326	ns
$T_{RDENADDRHD}$	Read Address Read Enable Hold Time (A_ADDR_EN, B_ADDR_EN)	–0.181	0.063	–0.213	0.075	ns
$T_{RDSRSTADDRSU}$	Read Address Synchronous Reset Setup Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	1.566	2.005	1.842	2.358	ns
$T_{RDSRSTADDRHD}$	Read Address Synchronous Reset Hold Time (A_ADDR_SRST_N, B_ADDR_SRST_N)	–0.183	0.061	–0.216	0.072	ns
$T_{RDENPIPESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	1.503	1.941	1.768	2.284	ns
$T_{RDENPIPEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	–0.152	0.092	–0.178	0.109	ns
$T_{RDSRSTPIPESU}$	Pipelined Read Synchronous Reset Setup Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	1.837	2.337	2.161	2.750	ns

.....continued

Parameter	Description	Speed Grade –1 SET Filter OFF	Speed Grade –1 SET Filter ON	Speed Grade STD SET Filter OFF	Speed Grade STD SET Filter ON	Units
$T_{RDSRSTPIPEHD}$	Pipelined Read Synchronous Reset Hold Time (A_DOUT_SRST_N, B_DOUT_SRST_N)	–0.835	–1.094	–0.982	–1.288	ns
T_{CCY}	Write Clock Period all pipeline enabled	3.922	3.922	4.630	4.630	ns
$T_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	0.526	0.526	0.526	0.526	ns
$T_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	0.526	0.526	0.526	0.526	ns
T_{BLKCSU}	Write Block Setup Time	1.575	2.083	1.853	2.451	ns
T_{BLKCHD}	Write Block Hold Time	–0.190	–0.427	–0.224	–0.502	ns
T_{DINCSU}	Write Input Data setup Time	1.238	1.960	1.456	2.306	ns
T_{DINCHD}	Write Input Data hold Time	–0.033	–0.404	–0.039	–0.475	ns
$T_{ADDRCSU}$	Write Address Setup Time	1.591	2.017	1.872	2.373	ns
$T_{ADDRCHD}$	Write Address Hold Time	–0.110	–0.453	–0.129	–0.533	ns
T_{WECSU}	Write Enable Setup Time	1.437	1.945	1.690	2.288	ns
T_{WECHD}	Write Enable Hold Time	–0.139	–0.376	–0.164	–0.442	ns
T_{CLK2Q}	Read Access Time with OUTPUT = PIPELINE	1.723	1.723	2.028	2.028	ns
	Read Access Time with INPUT = PIPELINE, OUTPUT = BYPASS	4.286	4.286	5.042	5.042	ns
T_{ADDR2Q}	Read Address to Out Data Access time with INPUT = BYPASS, OUPUT = BYPASS	6.173	6.173	7.262	7.262	ns
T_{BLK2Q}	Read Block Select to Out Disable Time with INPUT = BYPASS, OUPUT = BYPASS	3.481	3.481	4.096	4.096	ns
T_{R2Q}	Read Asynchronous Reset to Output Propagation Delay	1.228	1.228	1.444	1.444	ns
FMAX	Maximum Frequency with all pipelines enabled	255	255	216	216	MHz

8. FPGA Fabric Micro PROM (µPROM)

The following table lists the µPROM in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 8-1. µPROM

Parameter	Description	Speed Grade –1	Speed Grade STD	Units
T_{CY}	Read Clock Period	20	20	ns
$T_{CLKMPWH}$	Read Clock Minimum Pulse Width High	0.153	0.18	ns
$T_{CLKMPWL}$	Read Clock Minimum Pulse Width Low	0.14	0.164	ns
T_{ADDRSU}	Read Address Setup Time	4.74	5.576	ns
T_{ADDRHD}	Read Address Hold Time	0.513	0.604	ns
T_{RSTREC}	Read Asynchronous Reset Recovery Time	7.064	8.31	ns
T_{RSTREM}	Read Asynchronous Reset Removal Time	0	0	ns
T_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	7.034	8.274	ns
T_{CLK2Q}	Read Access Time	1.094	1.287	ns
T_{R2Q}	Read Asynchronous Reset to Output Propagation Delay	5.526	6.501	ns

9. JTAG

The following table lists the JTAG timing characteristics in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 9-1. JTAG/IEEE-1532 Timing Characteristics

Parameter	Description	Speed Grade –1	Speed Grade STD	Units
T_{TCK2Q}	Clock to Q (data out)	13.1	15.41	ns
TR_{STB2Q}	Reset to Q (data out)	32.7	38.47	ns
T_{DISU}	Test Data Input Setup Time	6.36	7.48	ns
T_{DIHD}	Test Data Input Hold Time	2.06	2.43	ns
T_{TMSSU}	Test Mode Select Setup Time	–1.18	–0.97	ns
T_{TMDHD}	Test Mode Select Hold Time	2.67	3.14	ns
$T_{TRSTREM}$	ResetB Removal Time	17.09	20.1	ns
$T_{TRSTREC}$	ResetB Recovery Time	17.08	20.1	ns
F_{TCKMAX}	TCK maximum frequency	25	21.25	MHz

9.1 Live Probe

The following table lists the Live Probe in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 9-2. Live Probe

Symbol	Description	Speed Grade –1	Speed Grade STD	Units
F_{LPROBE}	Live probe maximum frequency	100	85	MHz

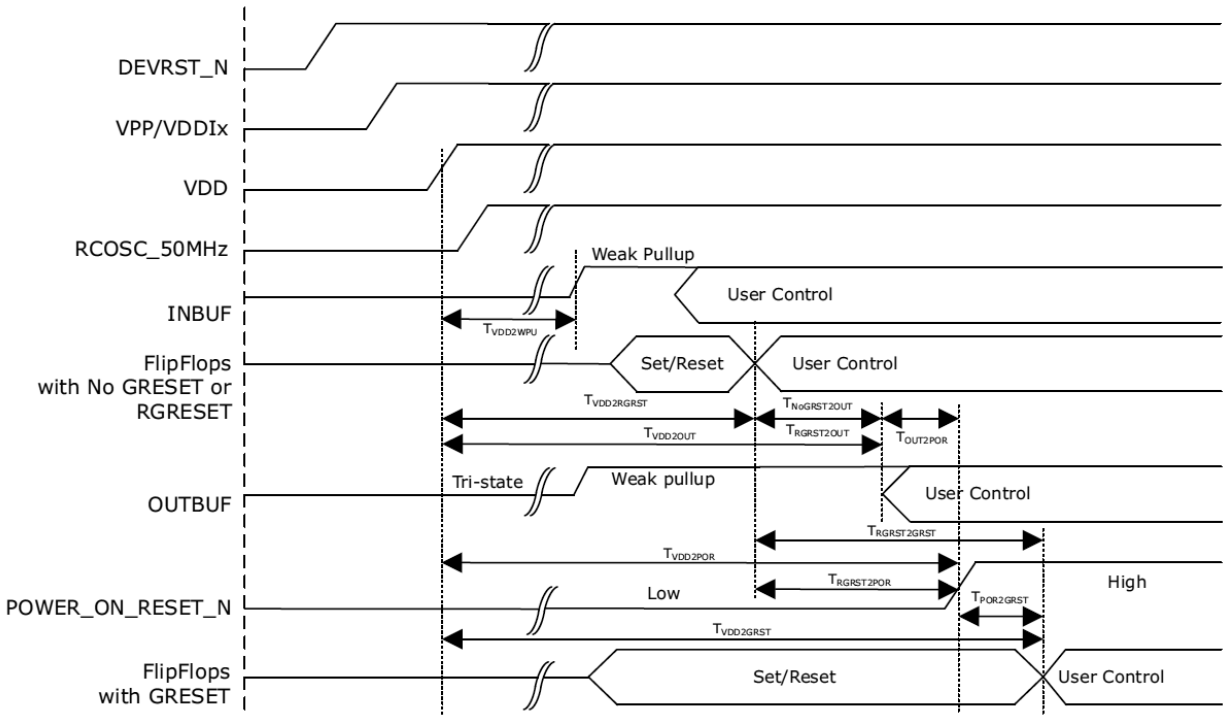
10. Power-up to Functional Times

The following table lists the power-up to functional times in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 10-1. Power-up to Functional Times

Parameter	From	To	Maximum Power-up to Functional Time	Units
TNoGRST2OUT	Flipflops without GRESET or RGRESET	Output available	7.02	µs
TRGRST2OUT	Flipflops with RGRESET active	Output available	7.02	µs
TRGRST2GRST	Flipflops with RGRESET active	Flipflops with GRESET active	7.41	µs
TRGRST2POR	Flipflops with RGRESET active	POWER_ON_RESET_N	7.3	µs
TPOR2GRST	POWER_ON_RESET_N	Flipflops with GRESET	0.07	µs
TVDD2OUT	VDD	Output Available	73.44	ms
TVDD2WPU	VDD	WPU (weak pull-up)	71.66	ms
TVDD2RGRST	VDD	Flipflops without GRESET or RGRESET	73.51	ms
		Flipflops with RGRESET active		
TVDD2GRST	VDD	Flipflops with GRESET active	73.52	ms
TVDD2POR	VDD	POWER_ON_RESET_N	73.52	ms
TOUT2POR	Output available	POWER_ON_RESET_N	0.286	µs

Figure 10-1. Power-up to Functional Times



11. Device Reset DEVRST_N

The following table lists the DEVRST_N in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14 V.

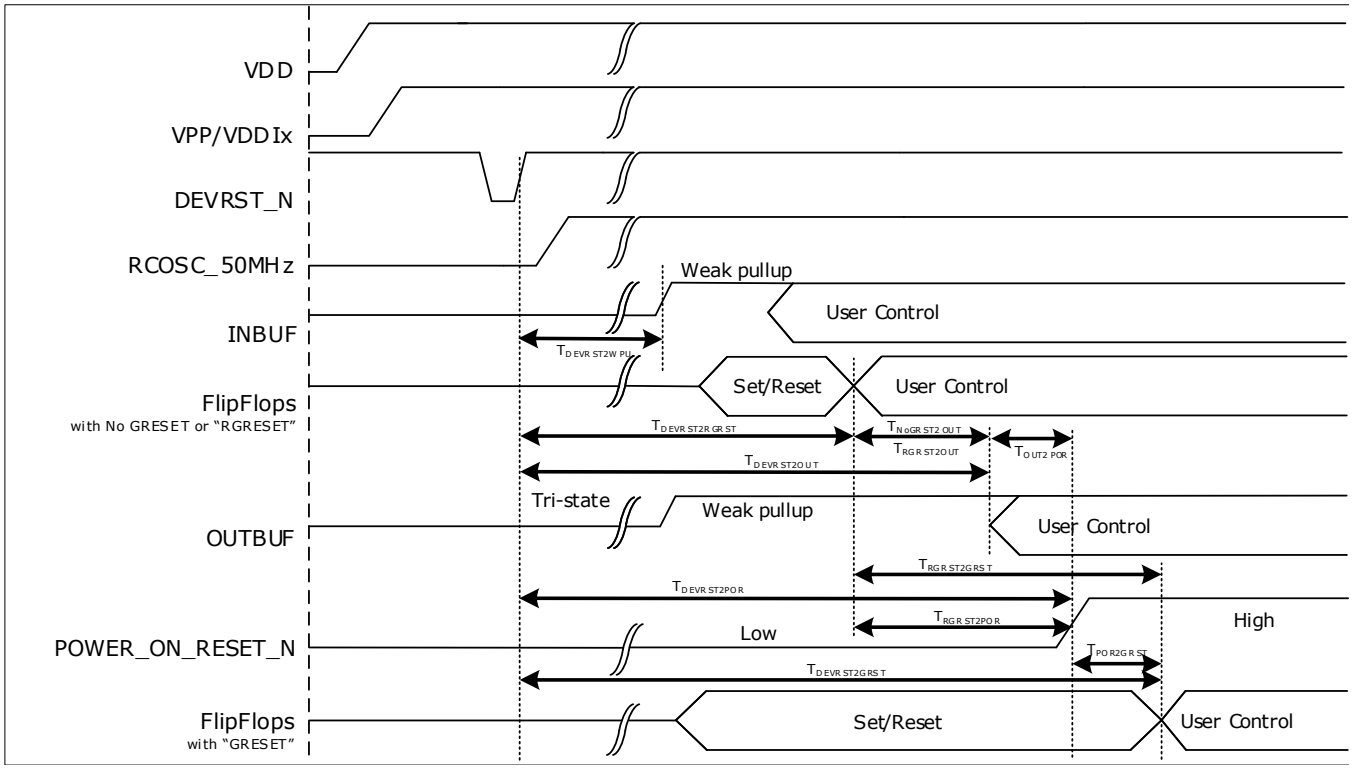
Table 11-1. DEVRST_N Characteristics

Symbol	Description	Min	Typ	Max	Units
TRAMPDEVRSTN	DEVRST_N ramp time (10% to 90%)	—	—	1	µs
FMAXPDEVRSTN	DEVRST_N cycling rate	—	—	100	kHz
MPWDEVRSTN	DEVRST_N pulse width	1	—	—	µs

Table 11-2. DEVRST_N to Functional Times

Parameter	From	To	Maximum DEVRST_N to Functional Time	Units
TNoGRST2OUT	Flipflops without GRESET or RGRESET	Output available	7.02	µs
TRGRST2OUT	Flipflops with RGRESET active	Output available	7.02	µs
TRGRST2GRST	Flipflops with RGRESET active	Flipflops with GRESET active	7.41	µs
TRGRST2POR	Flipflops with RGRESET active	POWER_ON_RESET_N	7.3	µs
TPOR2GRST	POWER_ON_RESET_N	Flipflops with GRESET	0.07	µs
TDEVRST2OUT	DEVRST_N	Output Available	1936	µs
TDEVRST2WPU	DEVRST_N	WPU (weak pull-up)	40.7	µs
TDEVRST2RGRST	DEVRST_N	Flipflops without GRESET or RGRESET	1929	µs
TDEVRST2RGRST	DEVRST_N	Flipflops with RGRESET active	1929	µs
TDEVRST2GRST	DEVRST_N	Flipflops with GRESET active	1936.36	µs
TDEVRST2POR	DEVRST_N	POWER_ON_RESET_N	1936.29	µs
TOUT2POR	Output available	POWER_ON_RESET_N	0.29	µs

Figure 11-1. DEVRST_N to Functional Timing Diagram for RTG4



12. On-Chip Oscillator

The following table describes the electrical characteristics of the available on-chip oscillators in the RTG4 FPGAs. Worst-case military conditions: T_J = 125 °C and V_{DD} = 1.14V.

Table 12-1. Electrical Characteristics of the 50 MHz RC Oscillator

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	—	46.25	50	53.75	MHz
ACC50RC	Accuracy	—	—	1	7.5	%
CYC50RC	Output duty cycle	—	46	—	54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	—	100	200	ps
		Cycle-to-Cycle jitter	—	80	160	ps
	Output jitter (peak to peak) with FPGA fabric switching noise[1]	Period jitter	—	250	350	ps
		Cycle-to-Cycle jitter	—	120	270	ps
IDYN50RC	Operating current	—	—	8.5	—	mA

Note:

1. Noise is generated by 32% of fabric registers with a switching rate of 25% driven by a 100 MHz clock.

13. Clock Conditioning Circuits (CCC)

The following table lists the CCC/PLL specifications in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14 V.

Table 13-1. RTG4 FPGAs CCC/PLL Specification

Parameter	Conditions	Min	Typ	Max	Units
Clock conditioning circuitry input frequency f_{IN_CCC}	PLL is bypassed, or PLL reference divider value is high enough to limit PLL input frequency to within the range of 10 MHz to 200 MHz at PLL Phase and Frequency Detector (PFD)	10	—	400	MHz
Clock conditioning circuitry output frequency f_{OUT_CCC} [1]	—	0.078	—	425	MHz
PLL input frequency f_{IN_PLL}	At the PLL PFD input, after the CCC reference divider	10		200	MHz
PLL VCO frequency[2]	—	500	—	1000	MHz
Delay increments in programmable delay blocks	—	—	100	150	ps
Number of programmable values in each programmable delay block	—	—	—	64	—
Acquisition time	—	—	—	500	µs
Output duty cycle	$f_{OUT\_CCC} \leq 185$ MHz	48	—	54	%
	185 MHz < $f_{OUT\_CCC} \leq 300$ MHz	48	—	56	%
	300 MHz < $f_{OUT\_CCC} \leq 425$ MHz	48	—	58	%
PLL_ARST_N pulse width	—	1	—	—	µs
Loop Bandwidth[3]	—	$f_{PFD}/8$	—	$f_{PFD}/6$	MHz
Output Clock Jitter	Period jitter (peak-to-peak)	—	—	See Table 13-2	ps

Notes:

1. The minimum output clock frequency is limited by the PLL. For more information, see the Fabric PLL Circuitry section in the RTG4 FPGA Clocking Resources User Guide.
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output.
3. f_{PFD} is equivalent to the Input Frequency (f_{IN}) divided by the input reference divider.

Table 13-2. Fabric PLL Output Clock Jitter Specification

Ref Clock I/O Standard	Input Voltage Condition	Operating Temperature (°C)	Max Output Clock Jitter (Peak-To-Peak Period Jitter)	Unit
Single-ended and Voltage Referenced	N/A	–55 ≤ Tj ≤ 125	Max (80 ps, 2% × (1/f_{IN})) + (1.45 × Input jitter)	ps
LVDS25, HCSL, RSDS, BLVDS, M-LVDS, MiniLVDS	V_{ID} and V_{ICM}. See tables: • LVDS25 DC Voltage Specification (Applicable to MSIO, MSIOD Banks, and SerDes REFCLK Input) • B-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • M-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • Mini-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • RSDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • HCSL DC Voltage Specification (Applicable to SerDes REFCLK Only)	–55 ≤ Tj ≤ 125	Max (80 ps, 2% × (1/f_{IN})) + (1.45 × Input jitter)	ps
Differential 3.3V MSIO input: LVPECL, LVDS33	$V_{ID} \geq V_{ICM}$	–55 ≤ Tj ≤ 125	Max (80 ps, 2% × (1/f_{IN})) + (1.45 × Input jitter)	ps
	V_{ID} and V_{ICM}. See tables: • LVDS33 DC Voltage Specification (Applicable to MSIO Banks and SerDes REFCLK Only) • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks and SerDes REFCLK Only)	–55 ≤ Tj ≤ 125	Max (140 ps, 2% × (1/f_{IN})) + (1.45 × Input jitter)	ps
		25 ≤ Tj ≤ 125	Max (80 ps, 2% × (1/f_{IN})) + (1.45 × Input jitter)	ps

Note: For additional worst-case jitter specifications, see Table 17-12. The clock jitter equations apply down to 10 MHz F_{IN}.

Table 13-3. Maximum MSIO Input Buffer Jitter Added to Input Clocks Directly Driving Globals

Ref Clock I/O Standard	Input Voltage Condition	Operating Temperature (°C)	Max Output Clock Jitter (Peak-To-Peak Period Jitter)	Unit
Single-ended and voltage referenced	N/A	–55 ≤ Tj ≤ 125	Max (100 ps, 2% × ($1/f_{IN}$))	ps
LVDS25, HCSL, RSDS, BLVDS, M-LVDS, MiniLVDS	V_{ID} and V_{ICM}. See tables: • LVDS25 DC Voltage Specification (Applicable to MSIO, MSIOD Banks, and SerDes REFCLK Input) • B-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • M-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • Mini-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • RSDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • HCSL DC Voltage Specification (Applicable to SerDes REFCLK Only)	–55 ≤ Tj ≤ 125	Max (100 ps, 2% x× ($1/f_{IN}$))	ps

.....continued				
Ref Clock I/O Standard	**Input Voltage Condition**	**Operating Temperature (°C)**	**Max Output Clock Jitter (Peak-To-Peak Period Jitter)**	**Unit**
Differential 3.3 V MSIO input: LVPECL, LVDS33	$V_{ID} \geq V_{ICM}$	–55 ≤ Tj ≤ 125	Max (150 ps, 4% × ($1/f_{IN}$))	ps
	V_{ID} and V_{ICM}. See tables: • LVDS33 DC Voltage Specification (Applicable to MSIO Banks and SerDes REFCLK Only) • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks and SerDes REFCLK Only)	–55 ≤ Tj ≤ 125	Max (300 ps, 8% × ($1/f_{IN}$))	ps
		25 ≤ Tj ≤ 125	Max (100 ps, 2% × ($1/f_{IN}$))	ps

1. f_{IN} is frequency of the external input clock, which can enter the FPGA fabric through the global input buffers without passing through a CCC/PLL, or through the input buffers going into a CCC for division only (bypassing PLL), before being promoted to global buffers. See jitter specifications in Table 13-2, if the input clock passes through a PLL.
2. The clock jitter equations apply down to 10 MHz f_{IN}.

14. System Controller SPI Characteristics

The following table lists the system controller SPI characteristics in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 14-1. System Controller SPI Characteristics (All Devices/Speed Grades)

Symbol	Description	Conditions	Min	Typ	Max	Units
sp1	SC_SPI_SCK minimum period	—	25	—	—	ns
sp2	SC_SPI_SCK minimum pulse width high	—	10	—	—	ns
sp3	SC_SPI_SCK minimum pulse width low	—	10	—	—	ns
sp41	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%–90%)	IO Configuration: LVTTL 3.3V–16 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C	—	1.43	—	ns
sp51	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%–90%)	IO Configuration: LVTTL 3.3V–16 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25 °C	—	1.45	—	ns
sp6	SC_SPI_SDI setup time	—	2	—	—	ns
sp7	SC_SPI_SDI hold time	—	2	—	—	ns

Note: For specific rise/fall times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models at www.microchip.com. The supported I/O configurations must be used for the system controller SPI, as shown in Table 11-2.

Table 14-2. Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units
3.3V	20	mA
2.5V	16	mA
1.8V	12	mA
1.5V	8	mA
1.2V	4	mA

The following table provides timing information for the APB configuration interface of dynamic CCC, FDDR memory controller, and High-Speed Serial Interface (SerDes) components. It is an embedded APB slave interface within the FPGA fabric that does not use FPGA resources.

Table 14-3. APB Configuration Interface Timing Characteristics

Parameter	Symbol	Max	Unit
APB clock frequency	APB_S_PCLK	53.75	MHz

15. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each RTG4 mathblock supports 18 x 18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently. The following table lists the math blocks with all registers used in worst-case military conditions for T_J = 125 °C and V_{DD} = 1.14V.

Table 15-1. Mathblocks With All Registers Used

		Speed Grade –1		Speed Grade STD		
Parameter	**Description**	**SET Filter OFF**	**SET Filter ON**	**SET Filter OFF**	**SET Filter ON**	**Units**
T_{MISU}	Input, Control Register Setup time	0.073	1.007	0.086	0.956	ns
T_{MIHD}	Input, Control Register Hold time	0.456	0.618	0.536	0.730	ns
$T_{MOCDINSU}$	CDIN Input Setup time	1.514	2.532	1.782	2.749	ns
$T_{MOCDINHD}$	CDIN Input Hold time	0.026	0.156	0.031	0.186	ns
$T_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	1.234	2.105	1.452	2.247	ns
$T_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.228	0.358	0.268	0.424	ns
$T_{MARSTREM}$	Asynchronous Reset Removal time	-0.456	-0.456	-0.536	-0.536	ns
$T_{MARSTREC}$	Asynchronous Reset Recovery time	0.601	0.601	0.707	0.707	ns
T_{MOCQ}	Output Register Clock to Out delay	0.961	0.961	1.131	1.131	ns
T_{MCLKMP}	CLK Minimum period	3.333	4.000	3.333	4.000	ns

The following table lists the mathblock with input bypassed and output registers used in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 15-2. Mathblock With Input Bypassed and Output Registers Used

		Speed Grade –1		Speed Grade STD		
Parameter	**Description**	**SET Filter OFF**	**SET Filter ON**	**SET Filter OFF**	**SET Filter ON**	**Units**
T_{MOSU}	Output Register Setup time	2.383	3.368	2.804	3.732	ns
T_{MOHD}	Output Register Hold time	–0.232	–0.069	–0.273	–0.079	ns
$T_{MOCDINSU}$	CDIN Input Setup time	1.514	2.532	1.782	2.749	ns
$T_{MOCDINHD}$	CDIN Input Hold time	0.026	0.156	0.031	0.186	ns
$T_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	1.234	2.105	1.452	2.247	ns

.....continued

		Speed Grade –1		Speed Grade STD		
Parameter	Description	SET Filter OFF	SET Filter ON	SET Filter OFF	SET Filter ON	Units
$T_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.228	0.358	0.268	0.424	ns
$T_{MARSTREM}$	Asynchronous Reset Removal time	–0.456	–0.456	–0.536	–0.536	ns
$T_{MARSTREC}$	Asynchronous Reset Recovery time	0.601	0.601	0.707	0.707	ns
T_{MOCQ}	Output Register Clock to Out delay	0.961	0.961	1.131	1.131	ns
T_{MCLKMP}	CLK Minimum period	3.333	4.000	3.333	4.000	ns

The following table lists the mathblock with input register used and output in bypass mode in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 15-3. Mathblock with Input Register Used and Output in Bypass Mode

		Speed Grade –1		Speed Grade STD		
Parameter	Description	SET Filter OFF	SET Filter ON	SET Filter OFF	SET Filter ON	Units
T_{MISU}	Input Register Setup time	0.073	1.007	0.086	0.956	ns
T_{MIHD}	Input Register Hold time	0.456	0.618	0.536	0.730	ns
$T_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	1.229	2.100	1.446	2.241	ns
$T_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.205	0.334	0.241	0.396	ns
$T_{MARSTREM}$	Asynchronous Reset Removal time	–0.456	–0.456	–0.536	–0.536	ns
$T_{MARSTREC}$	Asynchronous Reset Recovery time	0.601	0.601	0.707	0.707	ns
T_{MICQ}	Input Register Clock to Output delay	3.171	3.171	3.731	3.731	ns
$T_{MCDIN2Q}$	CDIN to Output delay	2.852	2.852	3.355	3.355	ns

The following table lists the mathblock with input and output in bypass mode in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 15-4. Mathblock with Input and Output in Bypass Mode

		Speed Grade –1		Speed Grade STD		
Parameter	**Description**	**SET Filter OFF**	**SET Filter ON**	**SET Filter OFF**	**SET Filter ON**	**Units**
T_{MIQ}	Input to output delay	2.912	2.912	3.426	3.426	ns
$T_{MCDIN2Q}$	CDIN to output delay	2.040	2.040	2.400	2.400	ns

16. I/O Delay Block Characteristics

The following table lists the I/O programmable delay block timing characteristics in worst-case military conditions, when T_J = 125 °C and V_{DD} = 1.14V.

Table 16-1. I/O Programmable Delay Block Timing Characteristics

Delay Step	DDR IO Speed Grade –1	DDR IO Speed Grade STD	MSIO IO Speed Grade –1	MSIO IO Speed Grade STD	MSIOD IO Speed Grade –1	MSIOD IO Speed Grade STD	Units
0	1.194	1.404	0.837	0.984	0.828	0.975	ns
1	1.344	1.581	0.979	1.152	0.971	1.142	ns
2	1.443	1.697	1.088	1.280	1.081	1.271	ns
3	1.593	1.874	1.235	1.453	1.224	1.440	ns
4	1.669	1.964	1.295	1.523	1.288	1.515	ns
5	1.819	2.140	1.442	1.696	1.431	1.684	ns
6	1.919	2.257	1.549	1.822	1.541	1.813	ns
7	2.069	2.434	1.693	1.992	1.685	1.982	ns
8	2.099	2.469	1.739	2.046	1.729	2.034	ns
9	2.249	2.646	1.881	2.213	1.873	2.203	ns
10	2.348	2.762	1.993	2.344	1.983	2.333	ns
11	2.498	2.939	2.136	2.512	2.126	2.501	ns
12	2.575	3.029	2.200	2.588	2.189	2.576	ns
13	2.725	3.206	2.342	2.755	2.333	2.744	ns
14	2.824	3.322	2.454	2.886	2.443	2.873	ns
15	2.974	3.499	2.598	3.056	2.587	3.043	ns
16	2.967	3.490	2.596	3.053	2.582	3.039	ns
17	3.117	3.667	2.738	3.221	2.725	3.205	ns
18	3.216	3.783	2.848	3.350	2.836	3.336	ns
19	3.366	3.960	2.992	3.520	2.979	3.504	ns
20	3.443	4.050	3.054	3.593	3.042	3.579	ns
21	3.593	4.227	3.199	3.763	3.185	3.747	ns
22	3.692	4.344	3.310	3.894	3.296	3.877	ns
23	3.842	4.520	3.455	4.064	3.438	4.045	ns
24	3.872	4.555	3.498	4.115	3.483	4.097	ns
25	4.022	4.731	3.642	4.285	3.627	4.267	ns

.....continued

Delay Step	DDR IO Speed Grade –1	DDR IO Speed Grade STD	MSIO IO Speed Grade –1	MSIO IO Speed Grade STD	MSIOD IO Speed Grade –1	MSIOD IO Speed Grade STD	Units
26	4.121	4.848	3.753	4.415	3.737	4.396	ns
27	4.272	5.025	3.896	4.584	3.880	4.564	ns
28	4.347	5.114	3.959	4.657	3.944	4.639	ns
29	4.498	5.291	4.103	4.826	4.086	4.807	ns
30	4.596	5.406	4.212	4.955	4.198	4.938	ns
31	4.747	5.584	4.357	5.125	4.340	5.105	ns
32	4.709	5.539	4.328	5.091	4.309	5.070	ns
33	4.859	5.716	4.472	5.261	4.452	5.238	ns
34	4.958	5.833	4.581	5.389	4.563	5.368	ns
35	5.108	6.010	4.725	5.559	4.706	5.536	ns
36	5.184	6.099	4.787	5.632	4.770	5.611	ns
37	5.335	6.276	4.933	5.803	4.913	5.779	ns
38	5.434	6.392	5.042	5.932	5.023	5.909	ns
39	5.584	6.569	5.187	6.102	5.166	6.078	ns
40	5.614	6.604	5.230	6.152	5.211	6.131	ns
41	5.764	6.781	5.375	6.323	5.354	6.299	ns
42	5.863	6.898	5.484	6.451	5.465	6.429	ns
43	6.013	7.074	5.630	6.623	5.610	6.600	ns
44	6.089	7.163	5.690	6.694	5.671	6.672	ns
45	6.240	7.340	5.838	6.867	5.815	6.841	ns
46	6.339	7.457	5.947	6.996	5.925	6.971	ns
47	6.489	7.634	6.093	7.167	6.069	7.139	ns
48	6.481	7.624	6.088	7.162	6.064	7.134	ns
49	6.632	7.801	6.235	7.335	6.207	7.302	ns
50	6.731	7.918	6.343	7.462	6.318	7.433	ns
51	6.880	8.094	6.487	7.631	6.462	7.602	ns
52	6.956	8.183	6.549	7.704	6.524	7.674	ns
53	7.107	8.361	6.694	7.875	6.667	7.843	ns
54	7.207	8.478	6.805	8.005	6.778	7.974	ns

.....continued

Delay Step	DDR IO Speed Grade –1	DDR IO Speed Grade STD	MSIO IO Speed Grade –1	MSIO IO Speed Grade STD	MSIOD IO Speed Grade –1	MSIOD IO Speed Grade STD	Units
55	7.357	8.655	6.949	8.174	6.922	8.143	ns
56	7.387	8.690	6.994	8.227	6.965	8.193	ns
57	7.537	8.866	7.139	8.398	7.108	8.362	ns
58	7.636	8.983	7.246	8.524	7.220	8.494	ns
59	7.786	9.160	7.392	8.696	7.365	8.664	ns
60	7.862	9.249	7.454	8.768	7.426	8.735	ns
61	8.012	9.426	7.598	8.939	7.569	8.904	ns
62	8.112	9.542	7.708	9.068	7.681	9.036	ns
63	8.262	9.719	7.852	9.237	7.825	9.205	ns

17. SerDes Electrical and Timing Characteristics

The RTG4 FPGAs have up to four hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block. Worst-case military conditions: T_J = 125 °C and V_{DD} = 1.14V. The SerDes can also be used for XAUI and generic EPCS interfaces. For more information about SerDes electrical and timing AC and DC characteristics, see the CR0028: RTG4 FPGA Characterization Report for XAUI and the CR0031: RTG4 PCIe Characterization Report.

Table 17-1. Transmitter Parameters

Parameter	Description	Min	Typ	Max	Units
V_{TXCM}	Output common mode voltage	—	—	20	mV
$T_{RISE-TIME}$	Tx rise time (20%–80%)	0.125	—	—	UI
$T_{FALL-TIME}$	Tx fall time (20%–80%)	0.125	—	—	UI
R_{OUT}	Differential output impedance	80	—	120	Ω
T_{LLSKEW}	Lane-to-lane Tx skew within a SerDes block	—	—	500 ps + 2 UI	ps
$RL_{TX-DIFF}$	Return loss differential mode	—	—	–10	dB
RL_{TX-CM}	Return loss common mode	—	—	–6	dB
$T_{RESET-LOCK}$	Transmit PLL lock time from reset	—	—	10	µs
$F_{SPLL-VCO}$[1]	SPLL VCO frequency range	500	—	1000	MHz
$F_{TXPLL-VCO}$ [1]	Tx PLL VCO frequency range	2000	—	5000	MHz
F_{TXRate}	Transmitter serial data rate	1.0	—	F_{MAXCvR}[2]	Gbps

Notes:

1. Follow valid frequency range setting in the Libero SoC software.
2. For F_{MAXCvR}, see Table 17-9.

Note: See protocol-specific tables Table 17-3 and Table 17-8 for PCIe Gen1, XAUI, and SRIO additional characteristics.

Table 17-2. Receiver Parameters

Parameter	Description	Min	Typ	Max	Units
V_{RXCM}	Input common mode voltage (AC coupled)	—	—	150	mV
R_{IN}	Differential input termination	80	100	120	Ω
R_{EXT}	External calibration resistor	1188	1,200	1212	Ω
$T_{CDRRESET-Lock}$	CDR relock time from reset	—	—	15	µs
CID[1]	CID limit	—	—	200	UI
$V_{RXIDLEDET}$	Electrical Idle detect threshold (differential peak-to-peak)	65	—	75	mV
F_{RXRate}	Receiver serial data rate	1.0	—	F_{MAXCvR}[2]	Gbps

Notes:

1. AC-coupled, BER = e^{-12}
2. For F_{MAXCvR}, see Table 17-9.

Note: See the protocol-specific tables for PCIe Gen1, XAUI, and SRIO additional characteristics.

Table 17-3. Transmitter (PCIE Gen1)

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing	0.8	—	1.2	V
TJ (1E-12)	Total jitter	—	—	0.25	UI

Note: PCIe compliance pattern used for jitter.

Table 17-4. Receiver (PCIE Gen1)

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Differential input peak-to-peak sensitivity	0.238		1.2	V
RX-JTOL	Receiver jitter tolerance	0.4	—	—	UI
RLRX-DIFF	Return loss differential mode	—	—	–10	dB
RLRX-CM	Return loss common mode	—	—	–6	dB

Notes:

- With add-in card, as specified in the *PCI Express CEM Rev 2.0*.
- PCIe compliance pattern used for JTOL.
- BER error criteria for JTOL is 10^{-12}.

Table 17-5. SRIO Transmitter

Parameter	Description	Condition	Min	Max	Units
$T_{SRIO-RISE-TIME}$	Rise time	20% to 80%	60	—	ps
$T_{SRIO-FALL-TIME}$	Fall time	80% to 20%	60	—	ps
$V_{TX-SRIO-VOD}$	Output amplitude	Short reach	0.5	1	V
$TJ_{TX-SRIO}$	Total transmit jitter	Far end	—	0.65	UI

Note: CJPAT pattern is used.

Table 17-6. SRIO Receiver

Parameter	Description	Condition	Min	Max	Units
$JTOL_{RX-SRIO}$	Receive jitter tolerance	10^{-12} BER	0.65		Ulp-p
$RL_{RX-SRIO-DIFF}$	Return loss differential mode	—	—	–8	dB
$RL_{RX-SRIO-CM}$	Return loss differential mode	—	—	–6	dB

Note: CJPAT pattern is used for JTOL.

Table 17-7. XAUI Transmitter

Parameter	Description	Condition	Min	Max	Units
$T_{XAUI-RISE-TIME}$	Rise time	20% to 80%	60	130	ps
$T_{XAUI-FALL-TIME}$	Fall time	80% to 20%	60	130	ps
$V_{TX-XAUI-VOD}$	Output amplitude	Short reach	0.2	1.2	V
$TJ_{TX-XAUI}$	Total transmit jitter	Far end	—	0.55	UI
$DJ_{TX-XAUI}$	Deterministic jitter	Far end	—	0.37	UI

Note: CJPAT pattern is used.

Table 17-8. XAUI Receiver

Parameter	Description	Condition	Min	Max	Units
$JTOL_{RX-XAUI}$	Receive jitter tolerance	10^{-12} BER	0.65	—	UIp-p
$RL_{RX-XAUI-DIFF}$	Return loss differential mode	—	—	–10[1]	dB
$RL_{RX-XAUI-CM}$	Return loss differential mode	—	—	–6[2]	dB

Notes:
1. With regard to 100Ω.
2. With regard to 25Ω.

Note: CJPAT pattern is used for JTOL.

Table 17-9. SerDes Protocol Compliance

Protocol	Maximum Data Rate (F_{MAXCVR})	Speed Grade –1	Speed Grade STD
PCIe Gen 1	2.5 Gbps	Yes	Yes
Generic EPCS	3.125 Gbps	Yes	No
Generic EPCS	2.5 Gbps	Yes	Yes
SRIO	3.125 Gbps	Yes	No
SRIO	2.5 Gbps	Yes	Yes
XAUI	3.125 (x4 lanes)	Yes	No

Note: For more information, see the UG0567: RTG4 FPGA High-Speed Serial Interfaces User Guide.

Table 17-10. SerDes Reference Clock AC Specifications

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	—	160	MHz
TRISE	Reference Clock Rise Time	0.6	—	4	V/ns
TFALL	Reference Clock Fall Time	0.6	—	4	V/ns
TCYC	Reference Clock Duty Cycle	40	—	60	%
MmREFCLK[1]	Reference Clock Mismatch	–300	—	300	ppm

.....continued					
Symbols	**Description**	**Min**	**Typ**	**Max**	**Units**
SSCref	Reference Spread Spectrum Clock	0	—	5000	ppm

Note:

1. MmREFCLK is the ppm difference between REFCLKs in systems using independent reference clocks.

Table 17-11. Worst-Case SerDes Transmit Jitter Per REFCLK I/O Standard

	LVPECL[1]			LVDS33[1]			LVDS25, HCSL, LVCMOS25
T_J Range (°C)	–55 to 125	25 to 125	–55 to 125	–55 to 125	25 to 125	–55 to 125	–55 to 125
Worst Case Total Transmit Jitter (ps)	360	80	107	360	80	107	100
VICM[2] (V)	0.6 – 1.8	0.6 – 1.8	0.6 – 1.8[3]	0.6 – 1.8	0.6 – 1.8	0.6 – 1.8[3]	See tables: • LVCMOS 2.5 V DC Voltage Specification • LVDS25 DC Voltage Specification (Applicable to MSIO, MSIOD Banks, and SerDes REFCLK Input) • HCSL DC Voltage Specification (Applicable to SerDes REFCLK only)
VID[2, 5] (V)	0.6 – 2.4	0.6 – 2.4	0.6 – 2.4[3]	0.5 – 2.4	0.5 – 2.4	0.6 – 2.4[3]	
Restriction	None[4]	Restricted Operating Temp. Range	VID ≥ VICM	None[4]	Restricted Operating Temp. Range	VID ≥ VICM	

Notes:

1. For the lowest possible jitter on SerDes TX outputs running at 3.125 Gbps across the full Mil-Temp range, use LVDS25 differential inputs for the SerDes REFCLK receiver with `SERDES_VDDI` set to 2.5 V and design the interface to meet a minimum V_{ICM} of 600 mV.
2. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4$ V and $V_{ICM} – (V_{ID}/2) > –0.3$ V.
3. $V_{ID} \geq V_{ICM}$
4. If no measures are taken, such as limiting operating temperature range, or meeting $V_{ID} \geq V_{ICM}$ relationship, then the SerDes will still start-up at –55 °C to 25 °C range, but the maximum total transmit jitter could exceed the TX jitter limits of the serial protocol in use until T_J rises to ≥25 °C.
5. Refer to Figure 4-4 for more information on V_{ID}.

For additional worst-case jitter specifications, see Table 17-12.

Table 17-12. RTG4 Global Network—Max Period Jitter

	Global Net Jitter (Peak-to-Peak)			Unit
% FF Used (of Total FFs in Device)[1, 2]	**15%**	**25%**	**50%**	**%**
Average Toggle Rate[4]	**30%**	**30%**	**30%**	**%**
Effective FF Toggle Percentage[3]	**4.5%**	**7.5%**	**15.0%**	**%**
–1	±200	±250	±400	ps
–1	400	500	800	ps
STD	±300	±400	±650	ps
STD	600	800	1300	ps

Notes:

1. % Flip-Flop (FF) used is defined as the percentage of total device FFs (out of 151,824 total) that are switching in a given clock domain.
2. The 50% FF used per clock domain is only shown to illustrate the impact of high utilization on a global clock net's jitter. Typical designs are expected to have less than 25% FF used per clock domain (as defined in the preceeding note).
3. Effective FF toggle percentage is the product of % FF used and average toggle rate. In the table above, jitter is specified for an average toggle rate of 30%. To determine jitter for a given combination, multiply FF used and average toggle rate then use linear interpolation as shown in Figure 17-1.
4. Measured jitter is generated at varying % FF used levels with a switching rate of 30%.
5. For a clock from an input buffer (except 3.3V differential inputs) feeding a global network, use jitter value as specified in Table 17-12.
6. For a clock from an LVDS33/LVPECL input buffer feeding a global network, use maximum jitter of Table 17-12 or Table 13-3.
7. For a PLL reference clock from input buffer, output of PLL feeding a global net, use maximum jitter of Table 17-12 or Table 13-2.
8. For a PLL reference clock from global net, output of PLL feeding a global net, use maximum jitter of Table 17-12 or Table 13-2.
9. For a PLL reference clock from global, output of PLL feeding output buffer, use maximum jitter of Table 17-12 or Table 13-2.
10. All measurements were taken by observing the clock from the FPGA output pin.
11. For further details, see UG0586: RTG4 FPGA Clocking Resources User Guide (section Global Net Clock Jitter).

- **Example 1:** If % FF used is 18% and the average toggle rate is 25%, the effective toggle percentage is 4.5%. The corresponding peak-to-peak jitter is 400 ps (–1) and 600 ps (–STD).
- **Example 2:** If % FF used is 50% and the average toggle rate is 20%, the effective toggle percentage is 10%. The corresponding peak-to-peak jitter can be determined by performing linear interpolation among the 3 data points as shown in Figure 17-1. The resulting peak-to-peak jitter in this case would be 605 ps (–1) and 966 ps (–STD)

Figure 17-1. Peak-to-Peak Jitter vs Effective Toggle Percentage

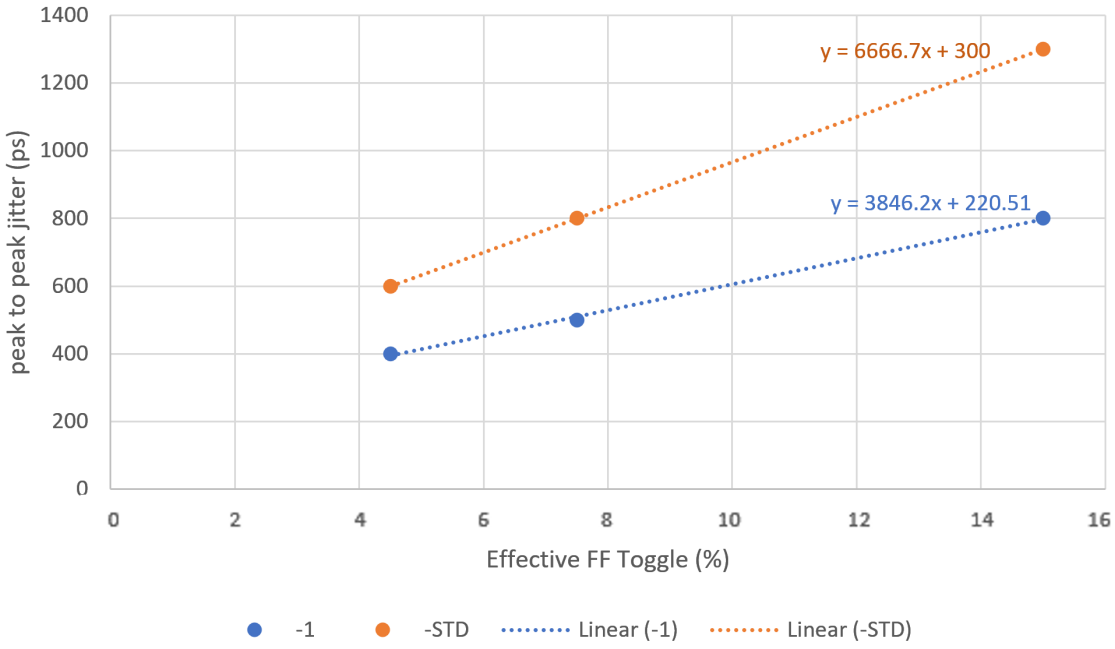


Table 17-13. SerDes Reference Clock Phase Noise

Parameter	Phase Noise	Data Rate	TxRefClk	Max	Units
$F_{TxRefPN}$	10 KHz	2.5 Gbps	125 MHz	–118	dBc/Hz
	100 KHz	2.5 Gbps	125 MHz	–117	dBc/Hz
	1 MHz	2.5 Gbps	125 MHz	–140	dBc/Hz
	10 KHz	3.125 Gbps	156.25 MHz	–117	dBc/Hz
	100 KHz	3.125 Gbps	156.25 MHz	–125	dBc/Hz
	1 MHz	3.125 Gbps	156.25 MHz	–142	dBc/Hz

Note: The phase noise requirements must be met to achieve jitter specifications in worst-case military conditions. If the desired reference clock frequency (TxRefClk) is not listed, the phase noise requirements should be adjusted by 20 × log10 (TxRefClk/156.25 MHz).

Table 17-14. HCSL DC Voltage Specification (Applicable to SerDes REFCLK only)

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
VI	DC input voltage	0	—	2.625	V
HCSL Differential Voltage Specification					
VICM[1]	With on-die termination (Rt)	0.05	—	1.5	V
	With external differential termination (Rt)	0.05	—	2.2	V

.....continued					
Symbols	**Parameters**	**Min**	**Typ**	**Max**	**Units**
VID[1, 2, 3]	Input differential voltage	200	—	1100	mV

Notes:

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4$ V and $V_{ICM} – (V_{ID}/2) > –0.3$V.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas the same 2.5 mA current produces only 250 mV across the 100Ω termination.
3. V_{ID} = | VinP – VinN |

The SerDes REFCLK input also supports LVDS25 and LVDS33 standards. For DC specification, see Table 4-69 and Table 4-73.

Table 17-15. HCSL AC Specifications (Applicable to SerDes REFCLK only)

Symbols	Parameters	Min	Typ	Max	Units
HCSL Maximum AC Switching Speed					
Fmax	Maximum data rate	—	—	350	Mbps
HCSL Impedance Specifications					
Rt	On-die termination resistance	90	100	150	Ω
	External 100Ω differential termination[1]	95	100	105	Ω
	External 200Ω differential termination[1, 2]	190	200	210	Ω

Notes:

1. When the external termination is being used, ODT must be disabled using the Libero SoC.
2. A 200Ω differential termination effectively doubles the differential voltage for a given drive current compared to a 100Ω termination. For example, a 2.5 mA current produces 500 mV of differential voltage across the 200Ω termination, whereas the same 2.5 mA current produces only 250 mV across the 100Ω termination.

18. SpaceWire Clock and Data Recovery

Table 18-1. SpaceWire Clock and Data Recovery Characteristics

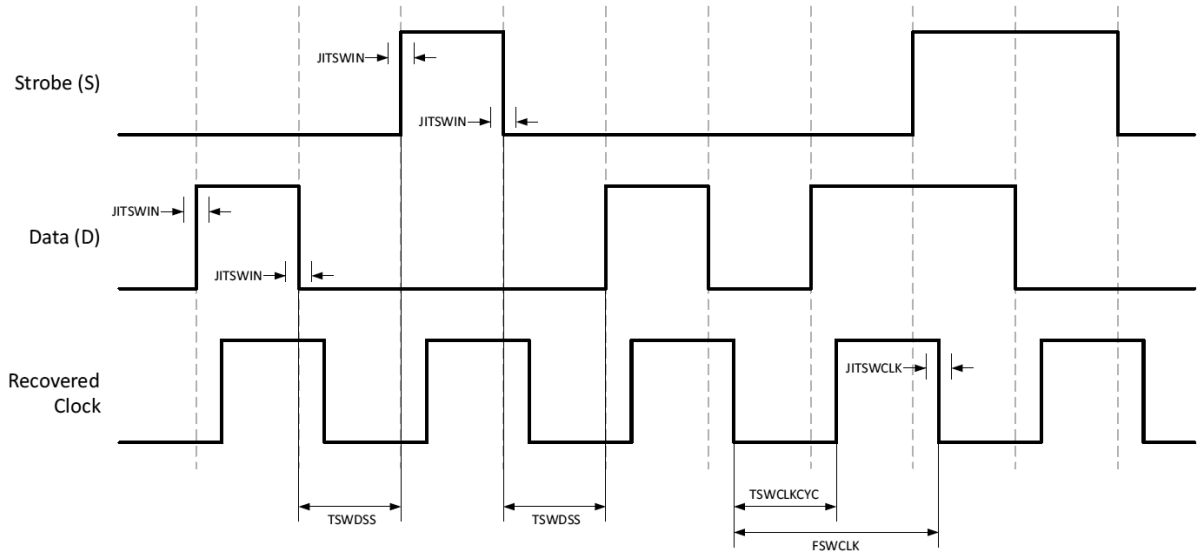
Symbol	Description	Conditions	Min	Typ	Max (–1)	Max (STD)	Units
FSWCLK	Recovered clock frequency	Bank: MSIO/MSIOD SET Mitigation: OFF No. of available channels: 14	1	—	100	90	MHz
		Bank: DDRIO SET Mitigation: OFF No. of available channels: 2	1	—	66	58	MHz
		Bank: MSIO/MSIOD SET Mitigation: ON No. of available channels: 14	1	—	75	66	MHz
		Bank: DDRIO SET Mitigation: ON No. of available channels: 2	1	—	66	58	MHz
DSW	Recovered data rate	Bank: MSIO/MSIOD SET Mitigation: OFF No. of available channels: 14	2	—	200	180	Mbps
		Bank: DDRIO SET Mitigation: OFF No. of available channels: 2	2	—	132	116	Mbps
		Bank: MSIO/MSIOD SET Mitigation: ON No. of available channels: 14	2	—	150	132	Mbps
		Bank: DDRIO SET Mitigation: ON No. of available channels: 2	2	—	132	116	Mbps
TSWCLKCYC	Recovered clock duty cycle	—	—	50	—	—	%
TSWDSS[3]	Rx input data to strobe separation	—	—	500 × (1/FSWCLK)	—	—	ns
JITSWIN[1]	Jitter tolerance on Data or Strobe inputs	—	—	—	200	200	ps
JITSWCLK[2]	Recovered Clock Jitter	Period Jitter (peak to peak)	—	200	500	500	ps

.....continued							
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max (–1)**	**Max (STD)**	**Units**
	Supported Receiver I/O Standards	LVTTL	See the 4.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification section for AC/DC specifications.				
		LVDS	See the 4.8.1 LVDS section for AC/DC specifications.				

Notes:

1. Input Jitter Tolerance (JITSWIN) includes jitter on strobe and data inputs, and any deviation of strobe and data from their ideal timing. Deviation from this specification degrades timing performance and may require compensation using the programmable delay cell available in the I/O For more information, see AC444: Implementing SpaceWire Clock and Data Recovery in RTG4 FPGA Application Note.
2. Represents Recovered Clock jitter when Strobe and Data Input jitter are negligible (<15 ps RMS). As the SpaceWire clock recovery circuit does not include a jitter filtering mechanism, additional jitter on the Strobe and Data inputs is passed to the recovered clock, in addition to the inherent jitter of the recovery circuit itself. Therefore, the input jitter on the Strobe and Data inputs should be minimized as much as possible. Assuming that the input jitter follows a Gaussian distribution around the ideal input edge, the following formula can be used to calculate the impact of the input jitter for a given system: Effective Recovered Clock jitter = (0.5 × Data Input jitter) + (0.5 × Strobe Input jitter) + JITSWCLK The Recovered Clock jitter represents a jitter window around the ideal recovered clock edge position, and therefore, can be used with SmartTime Static Timing Analysis as ±(0.5 × Effective Recovered Clock jitter).
3. The unit for the referenced FSWCLK is MHz.

Figure 18-1. Spacewire Timing Diagram



19. Temperature Sensing Diode

The following table lists the temperature diode maximum current.

Table 19-1. Temperature Diode Maximum Current

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{diode}	Diode current	—	—	—	10	mA

The following table lists two ways of calculating temperature sensing diode accuracy based on sample data obtained during characterization.

Table 19-2. Temperature Sensing Diode—Sample Data 1 and Calculation

Temperature forced on package	VBE when I_{diode} = 200 µA (V)	'm' calculated using –55 °C and 100 °C	T0 calculated at –55 °C	T_J calculated using m and T0	Accuracy (Actual – Calculated)
–55 °C	0.895	–748.79	615.17	–55.00 °C	0.00 °C
–40 °C	0.875			–40.02 °C	0.02 °C
0 °C	0.824			–1.84 °C	1.84 °C
25 °C	0.792			22.13 °C	2.87 °C
85 °C	0.710			83.53 °C	1.47 °C
100 °C	0.688			100.00 °C	0.00 °C
125 °C	0.653			126.21 °C	–1.21 °C

Table 19-3. Temperature Sensing Diode—Sample Data 2 and Calculation

Temperature forced on package	VBE when I_{diode} = 200 µA (V)	'm' calculated using 0 °C and 125 °C	T0 calculated at 0 °C	T_J calculated using m and T0	Accuracy (Actual – Calculated)
–55 °C	0.895	–730.99	602.34	–51.90 °C	–3.10 °C
–40 °C	0.875			–37.28 °C	–2.72 °C
0 °C	0.824			0.00 °C	0.00 °C
25 °C	0.792			23.39 °C	1.61 °C
85 °C	0.710			83.33 °C	1.67 °C
100 °C	0.688			99.42 °C	0.58 °C
125 °C	0.653			125.00 °C	0.00 °C

20. Revision History

Revision	Date	Description
B	09/2021	• Updated RT4G150 FCG/FC1657 device status to “Production” (SAR 120390). • Updated list of RTG4 FPGA Technical Briefs and Pin Descriptions. • Corrected units from “Mbps” to “MHz” in Table 4-2. Maximum I/O Frequency Summary for Worst-Case Military Conditions. • Updated Table 1-3. Operating Limits with in-flight programming information (SAR 120023) and table notes with RTG4 µPROM read cycle endurance (SAR 111814). • Clarified full amplitude range for V_{ID} in: – Note 3 under Table 4-69. LVDS25 DC Voltage Specification (Applicable to MSIO, MSIOD Banks, and SerDes REFCLK Input) (SAR 117013). – Note 5 under Table 4-73. LVDS33 DC Voltage Specification (Applicable to MSIO Banks and SerDes REFCLK Only) (SAR 119167). – Note 5 under Table 17-11. Worst-Case SerDes Transmit Jitter Per REFCLK I/O Standard (SAR 119167). • Added “DEVRST_N pulse width” information to Table 11-1. DEVRST_N Characteristics (SAR 110457 and SAR 118784). • Added “Loop Bandwidth” information and note 3 to Table 13-1. RTG4 FPGAs CCC/PLL Specification (SAR 87429). • Updated “Max Output Clock Jitter (Peak-to-Peak Period Jitter)” column (SAR 116796) and added note (SAR 118045) in: – Table 13-2. Fabric PLL Output Clock Jitter Specification – Table 13-3. Maximum MSIO Input Buffer Jitter Added to Input Clocks Directly Driving Globals. • Updated Max APB Clock Frequency to 53.75 MHz in Table 14-3. APB Configuration Interface Timing Characteristics (SAR 118080). • Updated Table 17-12. RTG4 Global Network—Max Period Jitter along with table notes, examples, and graph (SAR 117259). • Added footnote 3 to clarify the unit for TSWDSS in Table 18-1. SpaceWire Clock and Data Recovery Characteristics (SAR 120388).
A	09/2020	Following is the summary of changes. • The document was updated as per Microchip standards. • Document ID was changed from DS0131 to DS00003669A. • Added FCG/FC1657 package to Table 1. • Added references in the 2 Technical Briefs and Pin Descriptions section. • Added FCG/FC1657 package to the 1.1.3 Thermal Characteristics section. • Updated table title of Table 4-2. Replaced I/O Frequency with I/O Data Rate. • Added miminmum data values which were incorrectly placed in the Conditions column of Table 4-6. • Added clear Figure 11-1.

.....continued

Revision	Date	Description
7.0	07/2020	Following is a summary of changes. • Corrected HSTL15 to SSTL18 in Table 4-55. • Added table note 3 to Table 4-69. • Added table note 5 to Table 4-73. • Added Note to Table 5-2. • Added "+ (1.45 x Input Jitter)" to Table 13-2. • Corrected units from µs to ms in rows TVDD2OUT through TVDD2POR in Table 10-1. • Added Table 14-3. • Removed protocol-specific parameters from Table 17-1 and Table 17-2. • Added Table 17-3 and Table 17-4. • Added Table 17-5 and Table 17-6. • Added Table 17-7 and Table 17-8. • Added SRIO parameters to Table 17-9. • Added Table 17-12.
6.0	08/2019	Following is a summary of changes. • Table 1 was updated and note was added. • Recommended Operating Conditions was updated with a note. • Operating Limits table and notes were updated. • Power-Up Sequence section was updated with references. • Table 1-5 was updated with Θ_{JA} information and table notes. • Table 2-2 was updated with IDC Low Power parameter. • Table 4-73 note was updated. • Table 4-74 note was updated. • Table 4-99 was updated with a note. • Table 13-1 was updated with PLL_ARST_N information. • Table 17-1 was updated with rows for SPLL VCO frequency range and Tx PLL VCO frequency range. • Table 17-9 was updated with XAUI information. • Table 17-13 was added. • Table 19-1 was added.

Revision	Date	Description
5.0	08/2018	Following is the summary of changes. • Information about RTG4 device status was updated. • Information about maximum input buffer jitter was added. • Differential Input signaling waveform diagram was added. • Information about RAM1K18 - Dual-Port Mode for Depth x Width Configuration 1Kx18 was updated. • Information about fabric PLL output clock jitter specification was added. • A footnote about input leakage current of VREF was added. • Information about FPGA operating limits was updated. • Information about receiver parameters was updated. • A footnote about AC transient limit of VDD and VDDI was added. • Timing diagram of Spacewire characteristics was added. • Information about tristate leakage current (IOZ) was added. • Information about combinatorial cell propagation delays was updated. • Replaced ramp rate with ramp time for DEVRST_N characteristics. • Information about JTAG AC timing was added. • DEVRSTN to functional timing waveform diagram was updated.
4.0	07/2018	Following is the summary of changes. • Information about worst-case SerDes transmit jitter per REFCLK I/O standard was added. • Information about LVDS33 AC and DC voltage specification was updated to clarify these specifications are applicable to MSIO Banks and SerDes REFCLK only. • A footnote is added for VID in the LVDS33 DC Voltage Specification (Applicable to MSIO Banks and SerDes REFCLK Only) table. • A footnote is added for VID in the LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks and SerDes REFCLK Only) table. • Tables were updated to state that non-pipelined ECC mode is not supported with SET Filter OFF.
3.0	11/2017	Following is the summary of changes. • Information about AC FPGA core supply voltage was added. • Information about IDC was added as a footnote. • Updated I/O buffer tristate timing figure. • Information about VIH max specification for I/O standards was updated. • Information about DC input differential voltage (VID) was updated. • Information about RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx12, and 2Kx9 was removed from section FPGA Fabric Large SRAM (LSRAM). • Information about MSIO HCSL Fmax was added. • Information about DC supply voltage for LVDS25 and LVDS33 differential I/O Banks was added. • Updated section Power-Up and Power-Down Sequence. • Information about stand-alone verify was added as a note to FPGA Operating Limits table.

Revision	Date	Description
3.0	11/2017	• Information about Clock conditioning circuitry output frequency fOUT_CCC was updated. • Information about VOH and VOL is updated in LVCMOS 5V DC output voltage and transmitter drive strength specifications. • Information about Reference Clock Mismatch (MmREFCLK) is added as a footnote to SerDes Reference Clock AC Specifications table. • Information about limitation associated with DDRIO when used for SpaceWire was added. • Reference of CR0028: RTG4 FPGA Characterization Report for XAUI and CR0031: RTG4 PCIe Characterization Report was added to section SerDes Electrical and Timing AC and DC Characteristics. • Information about I/O programmable delay block timing characteristics was added. • Information about SLE, DDR, I/O, and MATH interface register data was updated. • Information about LVDS25 VID specification was updated. Footnotes are added for VICM and VID in the Mini-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) • The Fmax of LVPECL and LVDS33 is updated. • Information about LPDDR/LVCMOS speed was corrected. • Information about programming current was added. • Information about Quiescent Supply Current was updated. • Information about package thermal resistance for LG1657 and CQFP352 devices was added and for CCGA1657 was updated. • Information about SerDes I/O absolute maximum voltage was added. • Information about power supply grouping requirements was added as a note to Recommended Operating Conditions table. • Removed reference to RT4G075 device from this document. • A table and a figure are added for high temperature data retention. • In differential I/O, MSIO is updated for LVPECL (input only) and LVDS 3 V. • HSTL 5V DC Output Voltage Specification is updated for IOH at VOH and IOL at VOL. • Values and a footnote are updated for LVDS25 DC Differential Voltage Specification in the LVDS25 DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only). • Values and a footnote are updated for LVDS25 Impedance Specification in the LVDS25 AC Specifications (Applicable to MSIO and MSIOD Banks Only). • A footnote is added for VICM in the LVDS33 DC Voltage Specification (Applicable to MSIO Banks Only) table. • A footnote is added for VICM in the B-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) table.

Revision	Date	Description
3.0	11/2017	• A footnote is added for VICM and VID in the M-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) table. • Footnotes are added for VICM and VID in the RSDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) table. • Footnotes are added for VICM and VID in the RSDS AC Specifications (Applicable to MSIO and MSIOD Banks Only) table. • Footnotes are added for VICM and VID in the Mini-LVDS DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) table. • Footnotes are added for Rt in the Mini-LVDS AC Specifications (Applicable to MSIO and MSIOD Banks Only) table. • A footnote is added for VICM and VID in the LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only) table. • A note is added for Input Jitter Tolerance in the SpaceWire Clock and Data Recovery Characteristics table. • The Temperature Sensing Diode section is added. • Values of Maximum DEVRST_N to Functional Time are updated for TDEVRST2GRST and TVDD2POR. • Values are updated for Rt and footnotes are added in the HCSL AC Specifications (Applicable to SerDes REFCLK only) table. • The Power-Up and Power-Down Sequence section is updated for SERDES_x_Lyz_VDDAIO Requirements. • Values about Input Data Register Propagation Delays, Output/Enable Data Register Propagation Delays, Input DDR Propagation Delays, Output DDR Propagation Delays, and Register Delays are updated. • Information about FPGA operating limits was updated. • Information about Input capacitance was updated. • Information about I/O Weak Pull-Up/Pull-Down Resistance Values for DDRIO, MSIO, and MSIOD Banks was updated (SAR 75909). • Updated minimum parameter values for IOH at VOH, and IOL at VOL. • Information about LVDS25 DC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) was updated. • Information about LVDS25 AC Voltage Specification (Applicable to MSIO and MSIOD Banks Only) was updated. • Information about LVDS33 DC Voltage Specification (Applicable to MSIO Banks Only) and LVDS33 AC Voltage Specification (Applicable to MSIO Banks Only) was added. • Information about LVDS33 Receiver Characteristics was updated. • Information about B-LVDS AC and DC Voltage Specification was updated. • Information about B-LVDS AC Switching Characteristics for Receiver was updated. • Information about M-LVDS AC and DC Voltage Specification was updated. • Information about M-LVDS AC Switching Characteristics for Receiver was updated. • Information about RSDS AC and DC Voltage Specification was updated. • Information about Mini-LVDS AC and DC Voltage Specification was updated. • Information about LVPECL DC Voltage Specification was updated.

Revision	Date	Description
3.0	11/2017	• Updated TWESU, TWEHD and F Max parameters. • Information about Spacewire Clock and Data Recovery Characteristics was updated. • Information about CCC/PLL Specification was updated. • Information about Electrical Characteristics of the 50 MHz RC Oscillator was updated. • Information about Live Probe was added. • Information about Power-up to Functional Times was added. • Information about DEVRST_N to Functional Times was added. • Information about DEVRST_N Characteristics was updated. • Information about System Controller SPI Characteristics was updated. • Information about SerDes Electrical and Timing AC and DC Characteristics was updated. • Information about SerDes Protocol Compliance was added.
2.0		Updated section Power-Up and Power-Down Sequence.
1.0		This was the initial release of the document.

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