

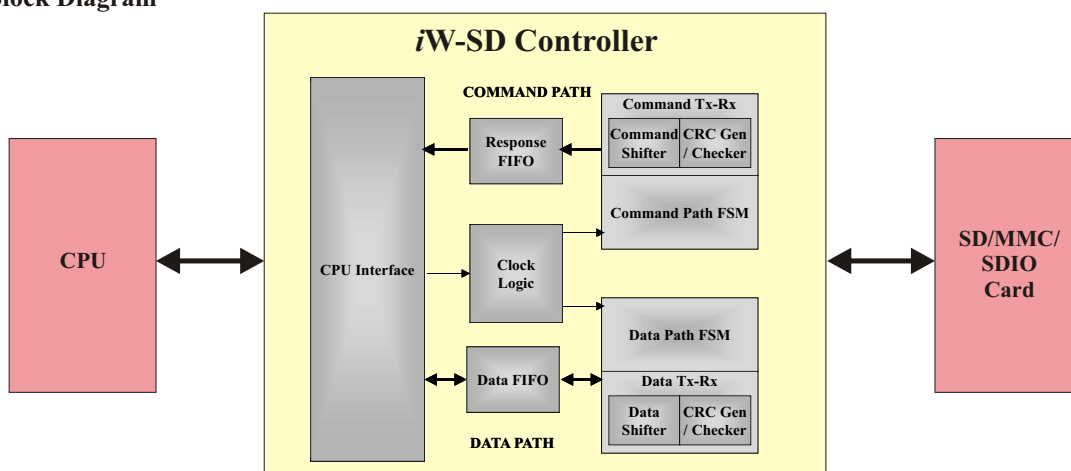
Overview

iW-SD Controller is an interface between any 8-bit processor and the SD/ MMC/ SDIO card. The interface towards the SD card is realized by the SD protocol implemented in the controller. The main blocks in the controller are CPU interface, command path state machine, command transmitter/ receiver, data path state machine, data transmit/receive and clock logic.

Features

- ❖ 1-bit/4-bit modes of SD, MMC and SDIO supported
- ❖ 8-bit Generic CPU interface
- ❖ Both DMA and Interrupt mode is supported for Data transfer
- ❖ Command buffers to store command index and argument
- ❖ Any byte size transfers supported. Sector size can be set from 1 byte to 2048 bytes
- ❖ CRC generation / checking supported for both command and data transactions
- ❖ Compliant with SDIO specification version 1.1
- ❖ Compliant with SD specification version 1.1
- ❖ Compliant with MMC specification version 2.0
- ❖ Using the SD/SDIO/MMC communication protocol, one SDIO or SD or MMC card is supported
- ❖ Card Detection / Removal support
- ❖ Write protect using mechanical switch
- ❖ Interrupts for errors

Block Diagram



Resource Utilization Summary

Bus Interface	Actel Family	Device	Tiles	Core Utilization	I/O Cells	RAM Utilization	Frequency	Power
SD1.1/ SDIO 1.1/ MMC2.0	ProASIC3	A3P600	3449	24.95%	57	37.50%	20 MHz	75.112 mW
	IGLOO	AGL600	3570	25.82%	57	37.50%	20 MHz	73.149 mW

Note : The above values are for 32-bit generic CPU interface.

Core Benefits

- ❖ Eases SOC integration
- ❖ Configurable for ease of use

Core Application

- ❖ Used as Host controller for SD, MMC and SDIO cards

Deliverables

- ❖ Technical Specification
- ❖ RTL Verilog Synthesizable Code
- ❖ Comprehensive Test Environment
- ❖ Technical Support and Maintenance

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