

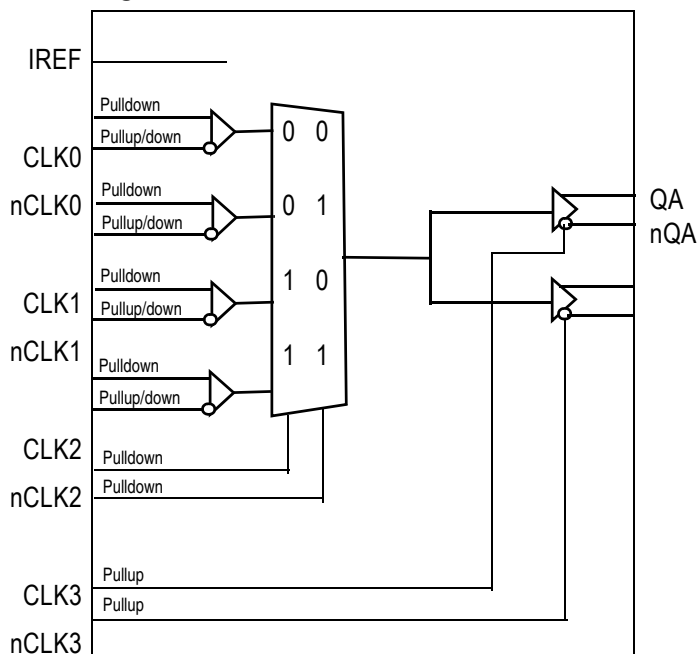
## General Description

The 831742I is a high-performance, differential HCSL clock/data multiplexer and fanout buffer. The device is designed for the multiplexing and fanout of high-frequency clock and data signals. The device has four differential, selectable clock/data inputs. The selected input signal is distributed to two low-skew differential HCSL outputs. Each input pair accepts HCSL, LVDS and LVPECL levels. The 831742I is characterized to operate from a 3.3V power supply. Guaranteed input, output-to-output and part-to-part skew characteristics make the 831742I ideal for those clock and data distribution applications demanding well-defined performance and repeatability. The 831742I supports the clock multiplexing and distribution of PCI Express (2.5 Gb/s), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) clock signals.

## Features

- 4:2 differential clock/data multiplexer with fanout
- Four selectable, differential input pairs
- Each differential input pair can accept the following levels: HCSL, LVDS and LVPECL
- Two differential HCSL output pairs
- Maximum input/output clock frequency: 700MHz
- Maximum input/output data rate: 1400Mb/s (NRZ)
- LVCMOS interface levels for all control inputs
- PCI Express (2.5Gb/s), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) clock jitter compliant
- Input skew: 110ps max
- Part-to-part skew: 225ps max
- Full 3.3V supply voltage
- Available in lead-free (RoHS 6)
- -40°C to 85°C ambient operating temperature

## Block Diagram



## Pin Assignment

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| GND             | 1  | 24 | SEL1            |
| CLK0            | 2  | 23 | IREF            |
| nCLK0           | 3  | 22 | SEL0            |
| V <sub>DD</sub> | 4  | 21 | V <sub>DD</sub> |
| CLK1            | 5  | 20 | nQB             |
| nCLK1           | 6  | 19 | QB              |
| CLK2            | 7  | 18 | nQA             |
| nCLK2           | 8  | 17 | QA              |
| GND             | 9  | 16 | V <sub>DD</sub> |
| CLK3            | 10 | 15 | GND             |
| nCLK3           | 11 | 14 | nOEB            |
| V <sub>DD</sub> | 12 | 13 | nOEA            |

**831742AGI**

**24-Lead TSSOP**

**4.4mm x 7.8mm x 0.925mm package body**

**G Package**

**Top View**

**Table 1. Pin Descriptions**

| Number        | Name       | Type   |                 | Description   |
|---------------|------------|--------|-----------------|---|
| 1, 9, 15      | GND        | Power  |                 | Power supply ground.  |
| 2             | CLK0       | Input  | Pulldown        | Non-inverting clock/data input.   |
| 3             | nCLK0      | Input  | Pulldown/Pullup | Inverting differential clock/data input. $V_{DD}/2$ default when left floating.   |
| 4, 12, 16, 21 | $V_{DD}$   | Power  |                 | Positive power supply.  |
| 5             | CLK1       | Input  | Pulldown        | Non-inverting clock/data input.   |
| 6             | nCLK1      | Input  | Pulldown/Pullup | Inverting differential clock/data input. $V_{DD}/2$ default when left floating.   |
| 7             | CLK2       | Input  | Pulldown        | Non-inverting clock/data input.   |
| 8             | nCLK2      | Input  | Pulldown/Pullup | Inverting differential clock/data input. $V_{DD}/2$ default when left floating.   |
| 10            | CLK3       | Input  | Pulldown        | Non-inverting clock/data input.   |
| 11            | nCLK3      | Input  | Pulldown/Pullup | Inverting differential clock/data input. $V_{DD}/2$ default when left floating.   |
| 13            | nOEA       | Input  | Pullup          | Output enable for the QA output. See Table 3A for function. LVCMOS/LVTTL interface levels.  |
| 14            | nOEB       | Input  | Pullup          | Output enable for the QB output. See Table 3B for function. LVCMOS/LVTTL interface levels.  |
| 17, 18        | QA, nQA    | Output |                 | Differential output pair. HCSL interface levels.  |
| 19, 20        | QB, nQB    | Output |                 | Differential output pair. HCSL interface levels.  |
| 22, 24        | SEL0, SEL1 | Input  | Pulldown        | Differential clock/data Input select. See Table 3C for function. LVCMOS/LVTTL interface levels.   |
| 23            | IREF       | Input  |                 | An external fixed precision resistor ( $475\Omega$ ) from this pin to ground provides a reference current used for the differential current-mode QX, nQX outputs. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol         | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units     |
|----------------|-------------------------|-----------------|---------|---------|---------|-----------|
| $C_{IN}$       | Input Capacitance       |                 |         | 4       |         | pF        |
| $R_{PULLUP}$   | Input Pullup Resistor   |                 |         | 51      |         | $k\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor |                 |         | 51      |         | $k\Omega$ |

## Function Tables

**Table 3A. nOEA Configuration Table**

| Input       |  | Operation                                    |
|-------------|--|--|
| nOEA        |  |  |
| 0           |  | Output QA, nQA is enabled.                   |
| 1 (default) |  | Output QA, nQA is in a high-impedance state. |

NOTE: nOEA is an asynchronous control.

**Table 3B. nOEB Configuration Table**

| Input       |  | Operation                                    |
|-------------|--|--|
| nOEB        |  |  |
| 0           |  | Output QB, nQB is enabled.                   |
| 1 (default) |  | Output QB, nQB is in a high-impedance state. |

NOTE: nOEB is an asynchronous control.

**Table 3C. SELx Configuration Table**

| Input       |             | Selected    |
|-------------|-------------|-------------|
| SEL1        | SEL0        |             |
| 0 (default) | 0 (default) | CLK0, nCLK0 |
| 0           | 1           | CLK1, nCLK1 |
| 1           | 0           | CLK2, nCLK2 |
| 1           | 1           | CLK3, nCLK3 |

NOTE: SEL1 and SEL0 are asynchronous controls

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                   |
|--|--------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                     |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 87.8°C/W (0 mps)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter               | Test Conditions  | Minimum | Typical | Maximum | Units |
|----------|-------------------------|------------------|---------|---------|---------|-------|
| $V_{DD}$ | Positive Supply Voltage |                  | 3.0     | 3.3     | 3.6     | V     |
| $I_{DD}$ | Power Supply Current    | Outputs Unloaded |         |         | 26      | mA    |

**Table 4B. LVCMOS/LVTTL Input DC Characteristics,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter          | Test Conditions | Minimum                         | Typical | Maximum        | Units   |
|----------|--------------------|-----------------|---------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                 | 2                               |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                 | -0.3                            |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | nOEA, nOEB      | $V_{DD} = V_{IN} = 3.6V$        |         | 5              | $\mu A$ |
|          |                    | SEL0, SEL1      | $V_{DD} = V_{IN} = 3.6V$        |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | nOEA, nOEB      | $V_{DD} = 3.6V$ , $V_{IN} = 0V$ | -150    |                | $\mu A$ |
|          |                    | SEL0, SEL1      | $V_{DD} = 3.6V$ , $V_{IN} = 0V$ | -5      |                | $\mu A$ |

**Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter                            | Test Conditions                                    | Minimum                         | Typical | Maximum         | Units   |
|-----------|--------------------------------------|--|---------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | CLK0, nCLK0; CLK1, nCLK1; CLK2, nCLK2; CLK3, nCLK3 | $V_{DD} = V_{IN} = 3.6V$        |         | 150             | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | CLK[0:3]   | $V_{DD} = 3.6V$ , $V_{IN} = 0V$ | -5      |                 | $\mu A$ |
|           |                                      | nCLK[0:3]  | $V_{DD} = 3.6V$ , $V_{IN} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Voltage; NOTE 1         |  | 0.15                            |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |  | 0.5                             |         | $V_{DD} - 0.85$ | V       |

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .

## AC Electrical Characteristics

**Table 5A. PCI Express Jitter Specifications,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

| Symbol                                | Parameter                                  | Test Conditions  | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---------------------------------------|--|--|---------|---------|---------|-----------------------------|-------|
| $t_j$<br>(PCIe Gen 1)                 | Phase Jitter<br>Peak-to-Peak;<br>NOTE 1, 4 | $f = 100MHz$ , 100MHz Input<br>Evaluation Band: 0Hz - Nyquist<br>(clock frequency/2) |         | 10      | 21      | 86                          | ps    |
| $t_{REFCLK\_HF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter RMS;<br>NOTE 2, 4             | $f = 100MHz$ , 100MHz Input<br>High Band: 1.5MHz - Nyquist<br>(clock frequency/2)    |         | 1       | 2.5     | 3.1                         | ps    |
| $t_{REFCLK\_LF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter RMS;<br>NOTE 2, 4             | $f = 100MHz$ , 100MHz Input<br>Low Band: 10kHz - 1.5MHz                              |         | 0.05    | 0.2     | 3.0                         | ps    |
| $t_{REFCLK\_RMS}$<br>(PCIe Gen 3)     | Phase Jitter RMS;<br>NOTE 3, 4             | $f = 100MHz$ , 100MHz Input<br>Evaluation Band: 0Hz - Nyquist<br>(clock frequency/2) |         | 0.2     | 0.8     | 0.8                         | ps    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. Measurements performed with a PCI Express compliant input source. For additional information, refer to the *PCI Express Application Note section* in the datasheet.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of  $10^6$  clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

**Table 5B. HCSL AC Characteristics,  $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol             | Parameter  | Test Conditions    | Minimum | Typical | Maximum | Units |
|--------------------|--|--------------------|---------|---------|---------|-------|
| $f_{OUT}$          | Output Frequency   |                    |         |         | 700     | MHz   |
| $t_{PD}$           | Propagation Delay; NOTE 1                                    |                    | 1.5     | 2       | 2.5     | ns    |
| $t_{sk(o)}$        | Output Skew; NOTE 16   | Across All Outputs |         | 3       | 15      | ps    |
| $t_{sk(i)}$        | Input Skew; NOTE 13  | Any Input to Q/nQ  |         | 30      | 110     | ps    |
| $t_{sk(pp)}$       | Part-to-Part Skew; NOTE 14, 15                               |                    |         |         | 225     | ps    |
| $MUX_{ISOL}$       | Mux Isolation  | $f = 100MHz$       |         | 40      |         | dB    |
| Rising Edge Rate   | Rising Edge Rate; NOTE 2, 3                                  | $f = 100MHz$       | 0.6     |         | 4       | V/ns  |
| Falling Edge Rate  | Falling Edge Rate; NOTE 2, 3                                 | $f = 100MHz$       | 0.6     |         | 4       | V/ns  |
| $V_{RB}$           | Ringback Voltage; NOTE 2, 4                                  | $f = 100MHz$       | -100    |         | 100     | mV    |
| $V_{MAX}$          | Absolute Max Output Voltage; NOTE 5, 6                       | $f = 100MHz$       |         |         | 1150    | mV    |
| $V_{MIN}$          | Absolute Min Output Voltage; NOTE 5, 7                       | $f = 100MHz$       | -300    |         |         | mV    |
| $V_{CROSS}$        | Absolute Crossing Voltage; NOTE 5, 8, 9                      | $f = 100MHz$       | 250     |         | 550     | mV    |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all edges; NOTE 5, 8, 10 | $f = 100MHz$       |         |         | 140     | mV    |
| odc                | Output Duty Cycle; NOTE 11                                   | $f \leq 200MHz$    | 48      | 50      | 52      | %     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the differential input cross point to the differential output crossing point.

NOTE 2: Measurement taken from differential waveform.

NOTE 3: Measurement from -150mV to +150mV on the differential waveform (derived from QX minus nQX). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 4:  $T_{STABLE}$  is the time the differential clock must maintain a minimum  $\pm 150mV$  differential voltage after rising/falling edges before it is allowed to drop back into the  $V_{RB} = \pm 100$  differential range. See Parameter Measurement Information Section.

NOTE 5: Measurement taken from single-ended waveform.

NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of QX equals the falling edge of nQX.

See Parameter Measurement Information Section

NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 10: Defined as the total variation of all crossing voltage of rising QX and falling nQX. This is the maximum allowed variance in the  $V_{CROSS}$  for any particular system. See Parameter Measurement Information Section.

NOTE 11: Input duty cycle must be 50%.

NOTE 12: Matching applies to rising edge rate for QX and falling edge rate for nQX. It is measured using a  $\pm 75mV$  window centered on the median crosspoint where QX meets nQX falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of QX should be compared to the fall edge rate of nQX, the maximum allowed difference should not exceed 20% of the slowest edge rate.

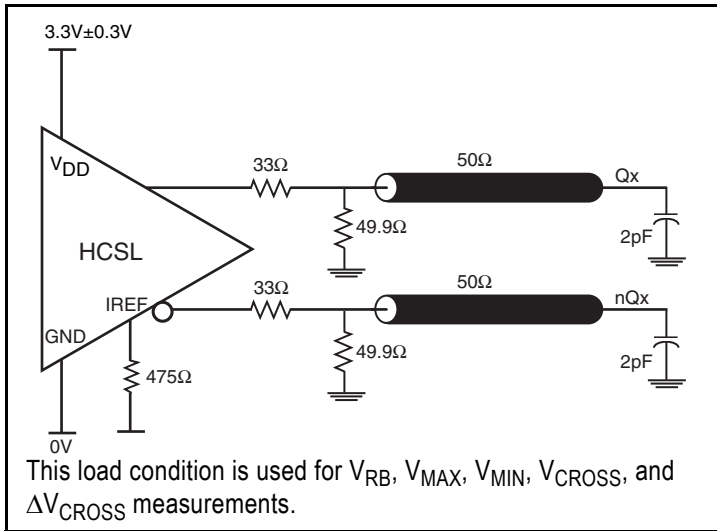
NOTE 13: Defined as skew between input paths on the same device, using the same input signal levels, measured at one specific output at the differential cross points.

NOTE 14: This parameter is defined in accordance with JEDEC Standard 65.

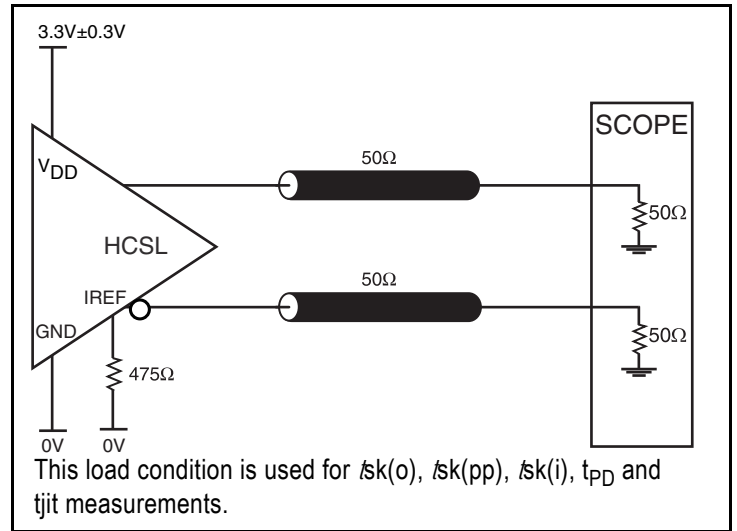
NOTE 15: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 16: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

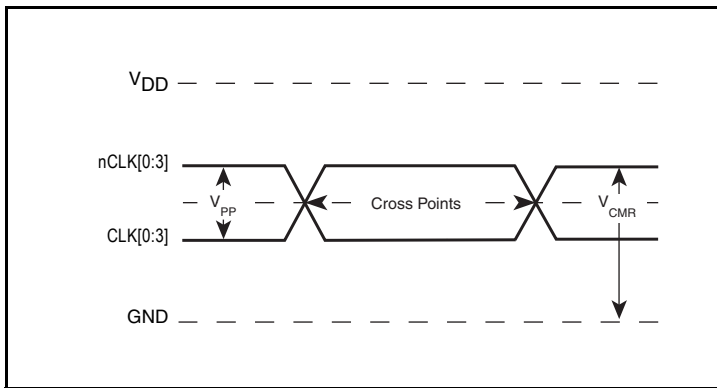
## Parameter Measurement Information



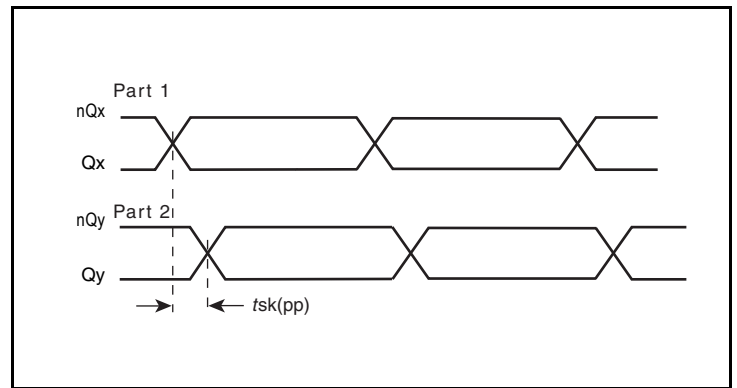
3.3V HCSL Output Load AC Test Circuit



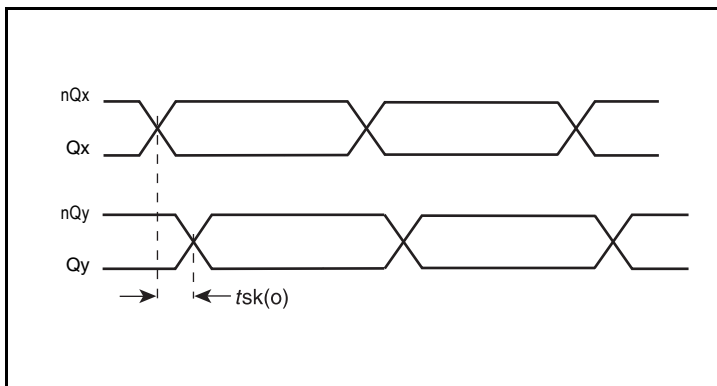
3.3V HCSL Output Load AC Test Circuit



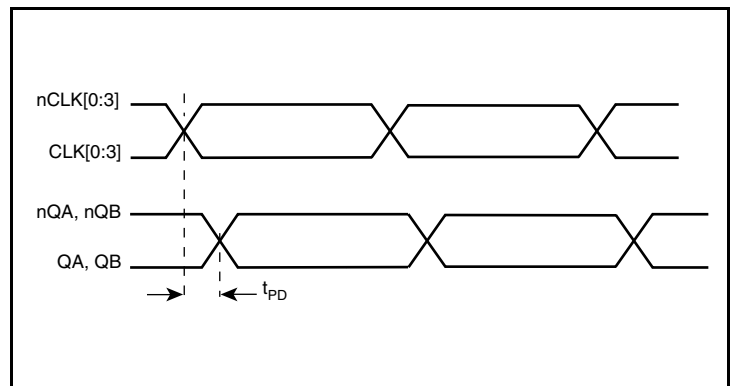
Differential Input Level



Part-to-Part Skew

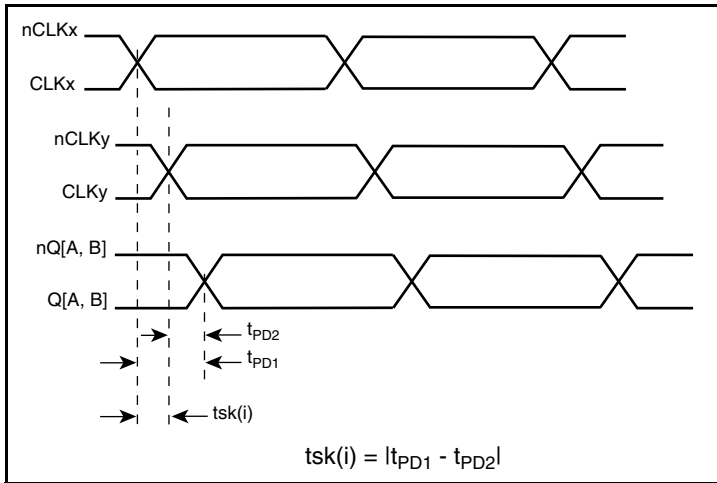
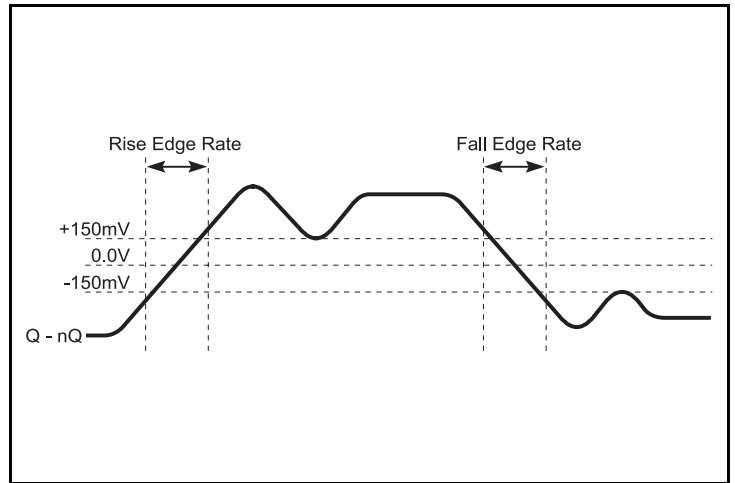
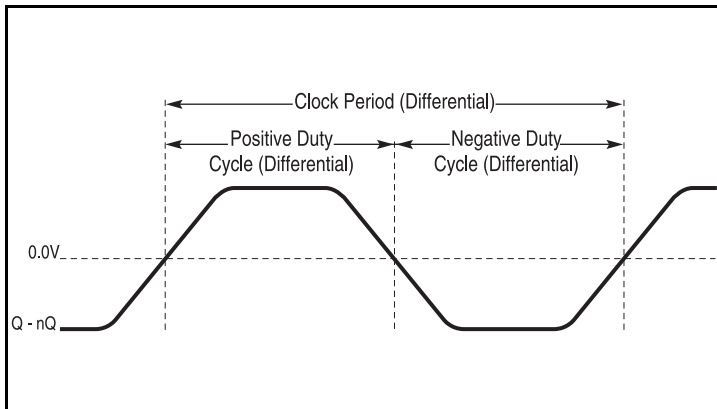
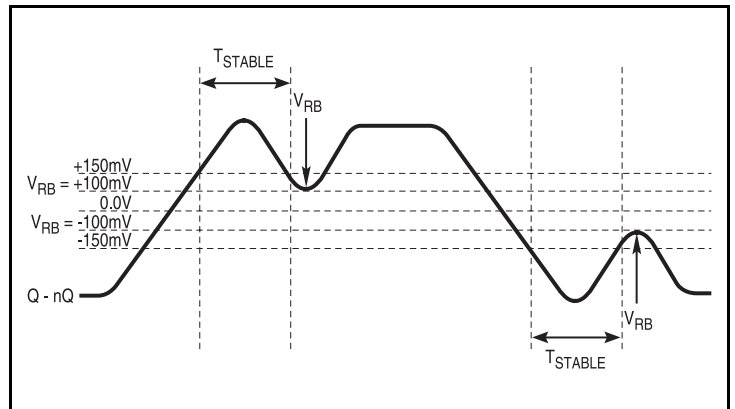
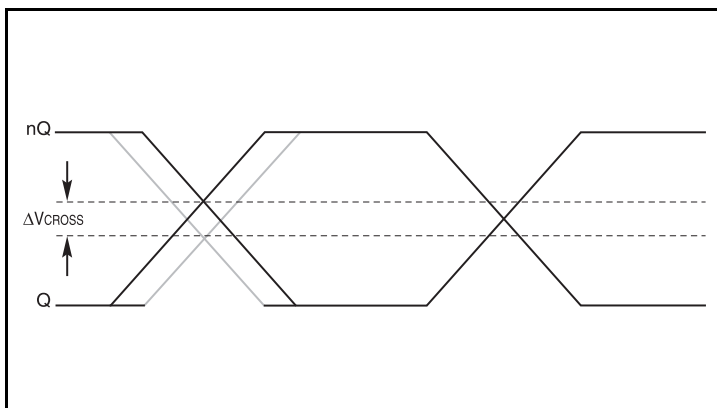
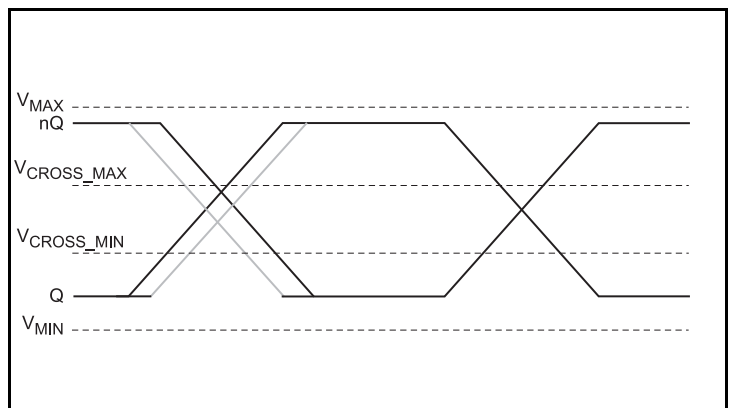


Output Skew



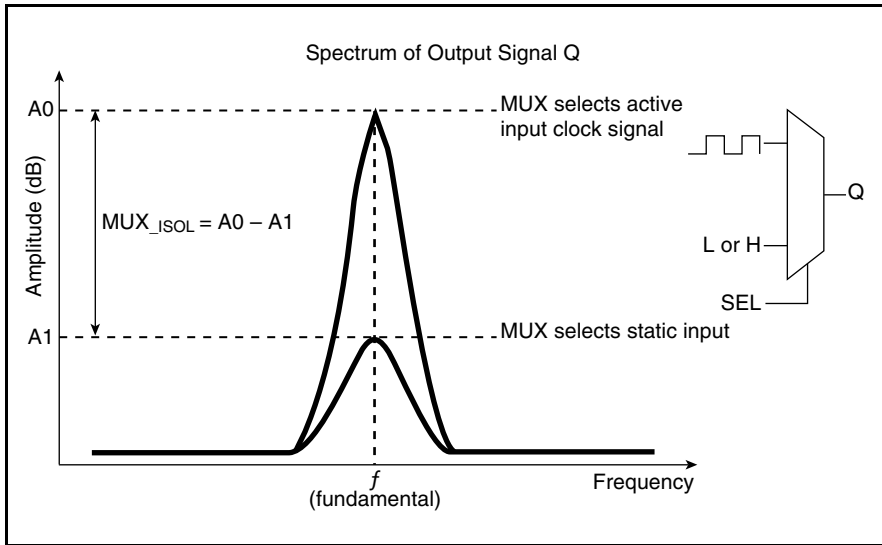
Propagation Delay

## Parameter Measurement Information, continued


**Input Skew**

**Differential Measurement Points for Rise/Fall Edge Rate**

**Differential Measurement Points for Duty Cycle/Period**

**Differential Measurement Points for Ringback**

**Single-ended Measurement Points for Delta Cross Point**

**Single-ended Measurement Points for Absolute Cross Point/Swing**



## Parameter Measurement Information, continued



**MUX Isolation**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullup or pulldown; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

##### CLK/nCLK Inputs

For applications not requiring the use of the all differential inputs, any CLK/nCLK input can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from CLK to ground.

#### Outputs:

##### Differential Outputs

The unused differential output can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ , R1 and R2 value should be adjusted to set  $V_1$  at  $1.25\text{V}$ . The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission

line impedance. For most  $50\Omega$  applications, R3 and R4 can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVC MOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3\text{V}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

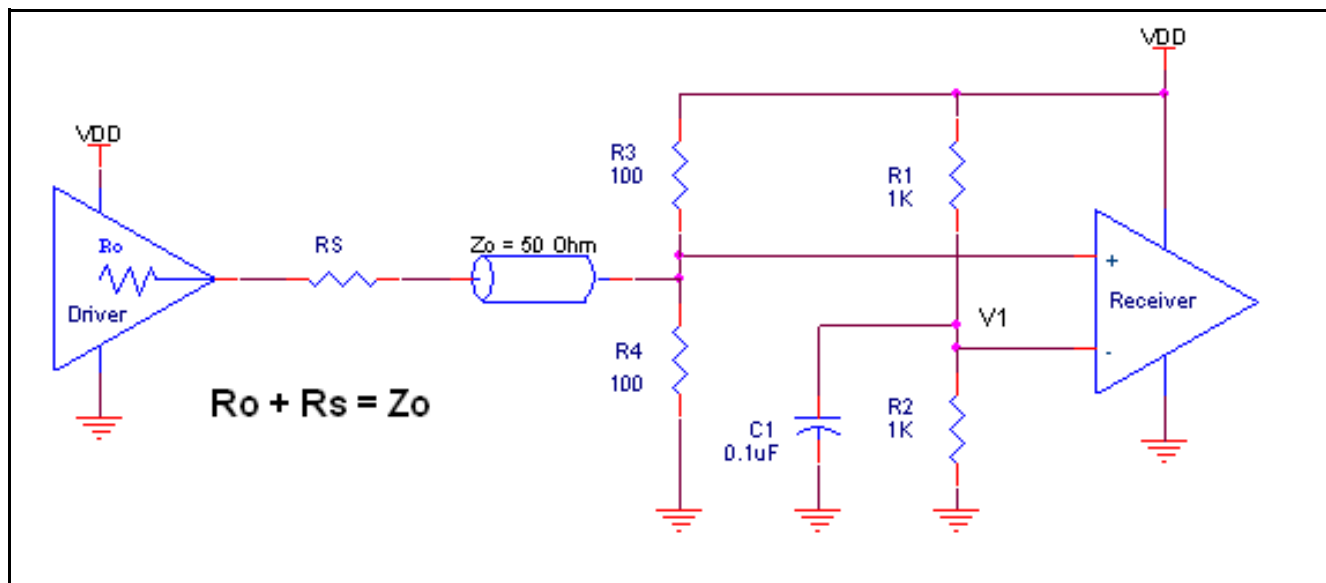
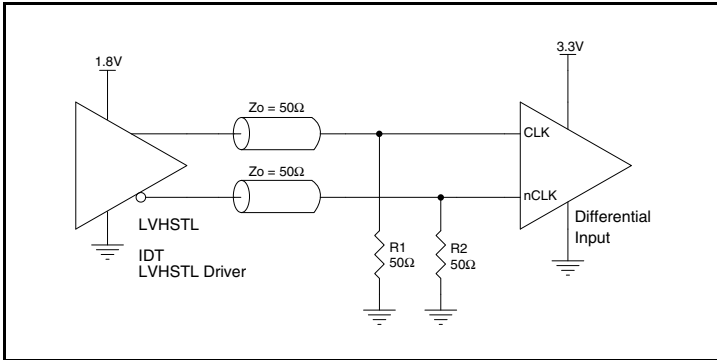


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

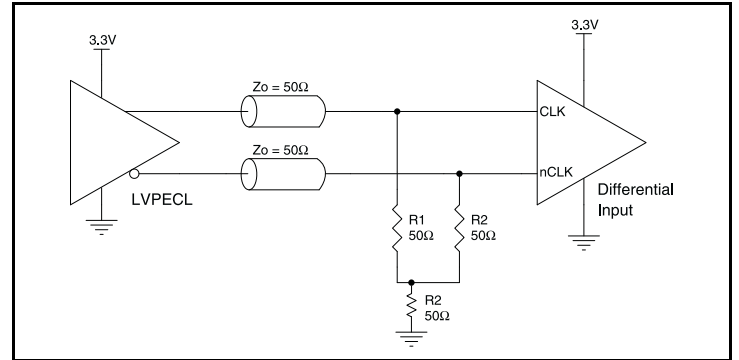
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the

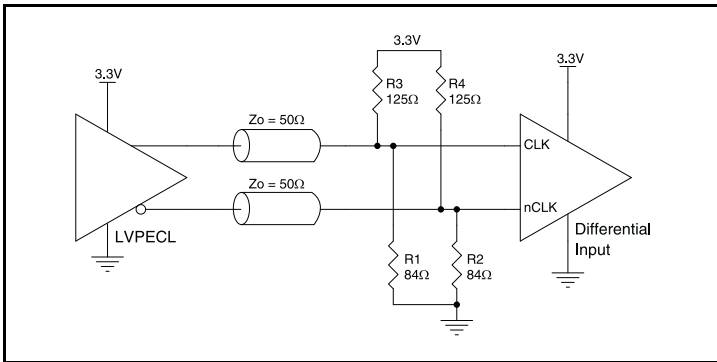
vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



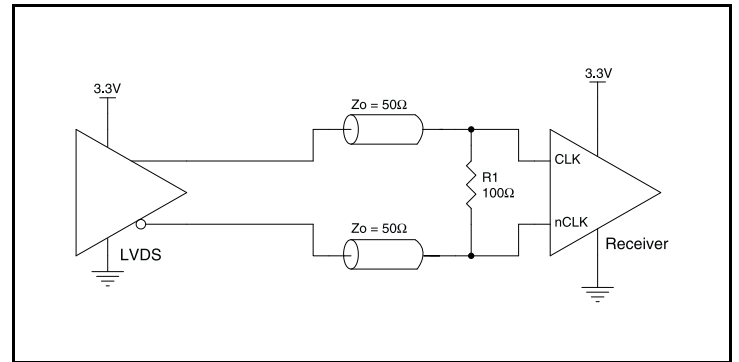
**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter HiPerClocks LVHSTL Driver**



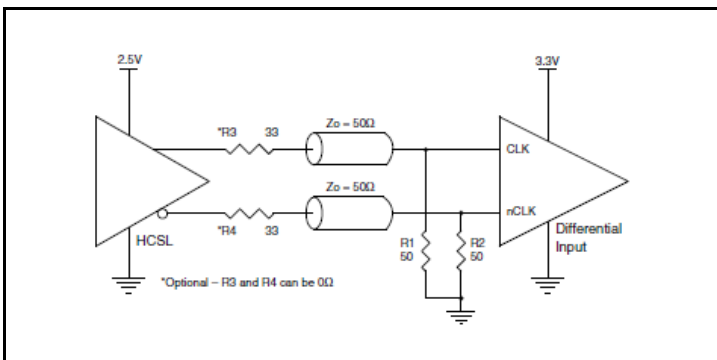
**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

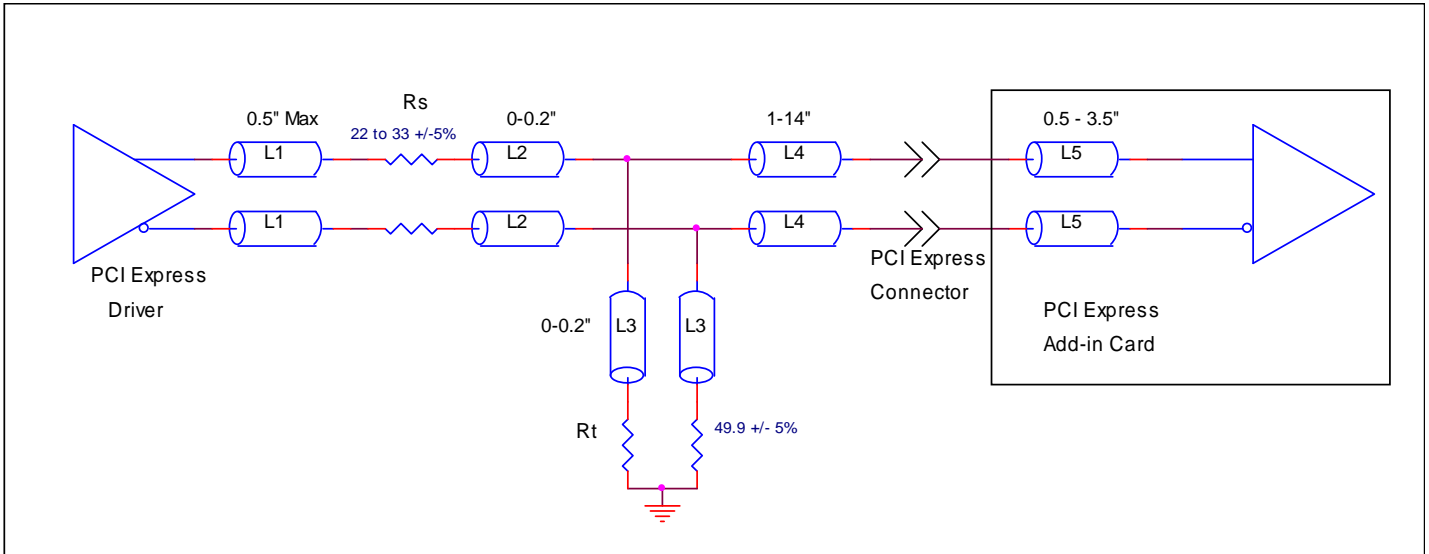


**Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

### Recommended Termination

Figure 3A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

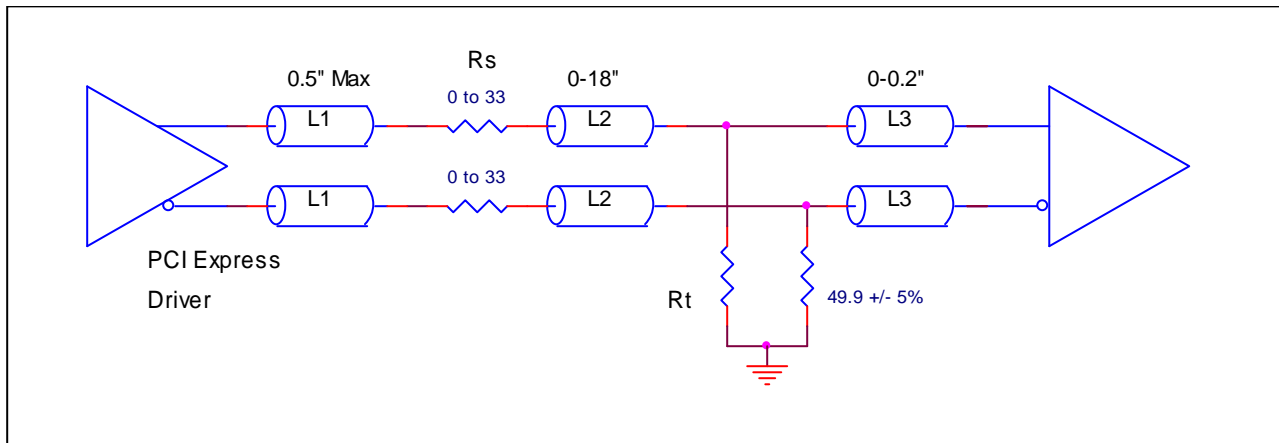
All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 3A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

Figure 3B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 3B. Recommended Termination (where a point-to-point connection can be used)**

### PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

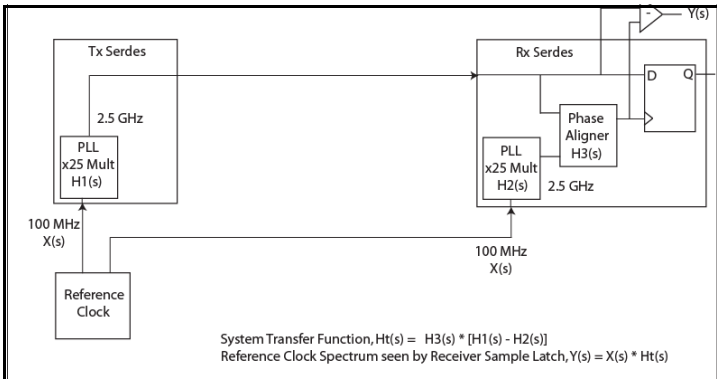
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

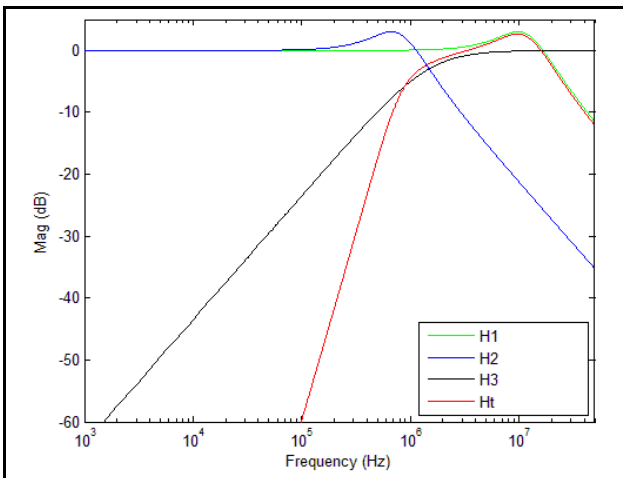
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on  $X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$ .



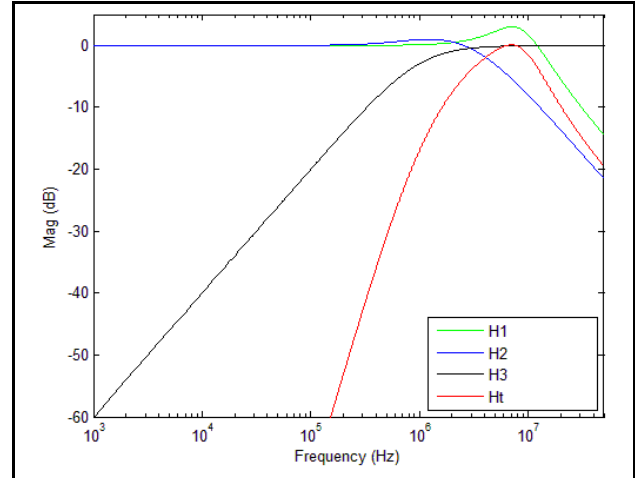
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

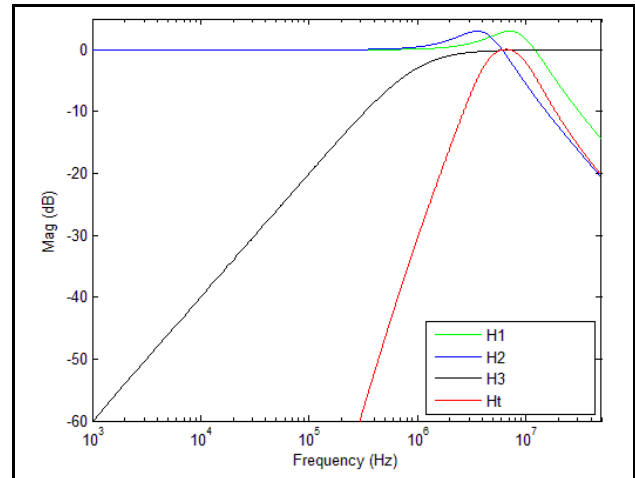


PCI Express Gen 1 Magnitude of Transfer Function

For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



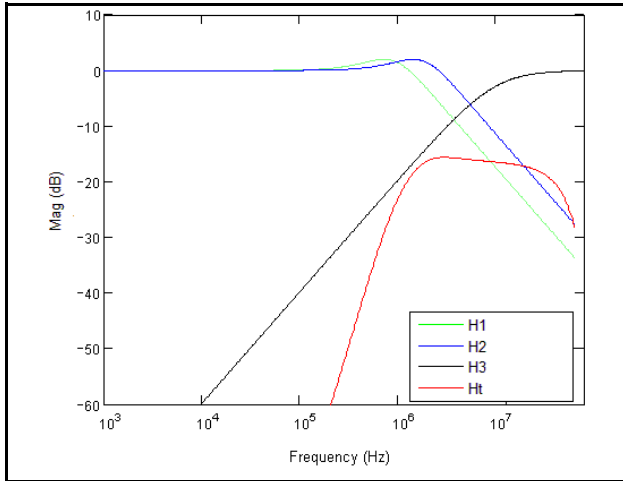
PCI Express Gen 2A Magnitude of Transfer Function



PCI Express Gen 2B Magnitude of Transfer Function

## PCI Express Application Note continued.

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



### PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

## Power Considerations

This section provides information on power dissipation and junction temperature for the 831742I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 831742I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 0.3V = 3.6V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.6V * 26mA = 93.6mW$
- Power (outputs)<sub>MAX</sub> = **46.8mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 46.8mW = 93.6mW$

**Total Power**<sub>MAX</sub> =  $93.6mW + 93.6mW = 187.2mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 87.8°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.187W * 87.8^\circ C/W = 101.4^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

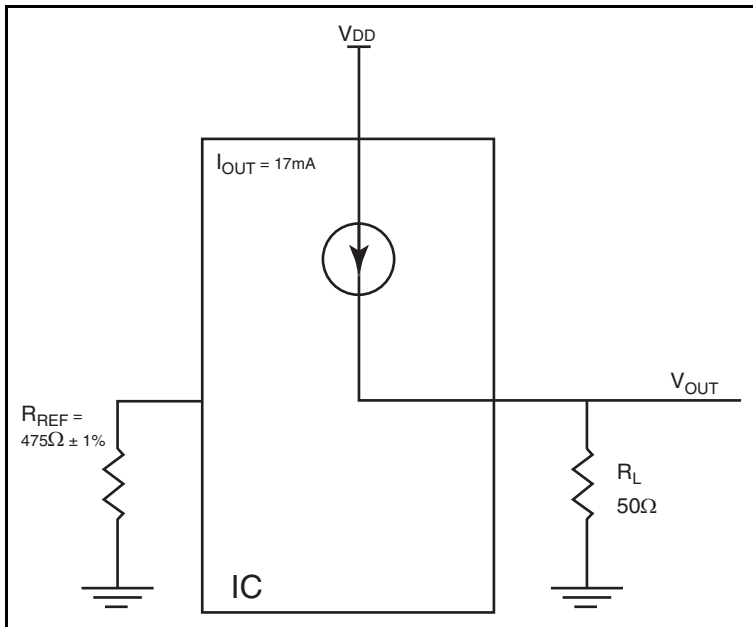
**Table 6. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, Forced Convection**

| Meters per Second                           | $\theta_{JA}$ vs. Air Flow |          |          |
|---|----------------------------|----------|----------|
|   | 0                          | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 87.8°C/W                   | 83.5°C/W | 81.3°C/W |

### 3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when  $V_{DD\_MAX}$ .

$$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT},$$

$$\text{since } V_{OUT} = I_{OUT} * R_L$$

$$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$$

$$= (3.6V - 17mA * 50\Omega) * 17mA$$

Total Power Dissipation per output pair = **46.8mW**



## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 87.8°C/W | 83.5°C/W | 81.3°C/W |

## Transistor Count

The transistor count for the 831742I is: 765

## Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

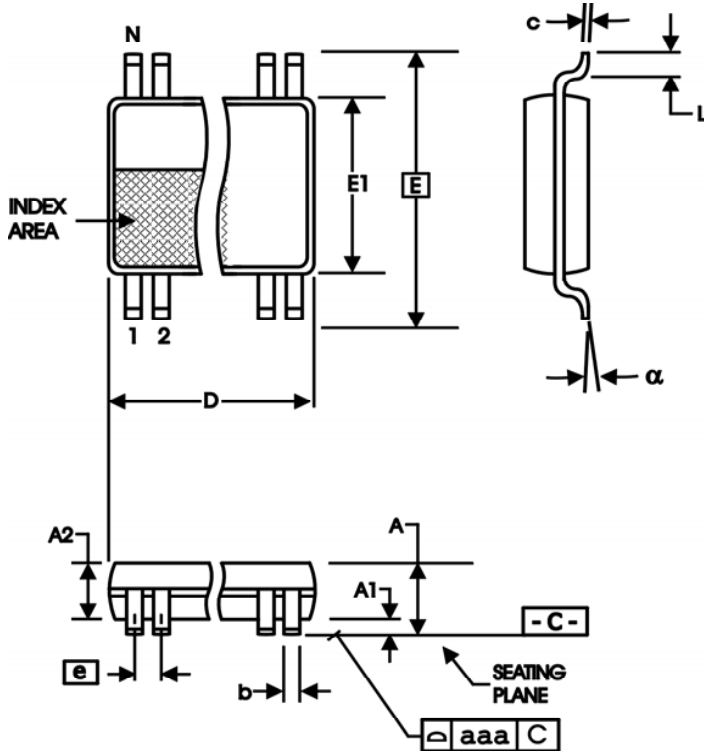


Table 8. Package Dimensions

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 24         |         |
| A                             |            | 1.20    |
| A1                            | 0.5        | 0.15    |
| A2                            | 0.80       | 1.05    |
| b                             | 0.19       | 0.30    |
| c                             | 0.09       | 0.20    |
| D                             | 7.70       | 7.90    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.45       | 0.75    |
| $\alpha$                      | 0°         | 8°      |
| aaa                           |            | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

**Table 9. Ordering Information**

| <b>Part/Order Number</b> | <b>Marking</b> | <b>Package</b>            | <b>Shipping Packaging</b> | <b>Temperature</b> |
|--------------------------|----------------|---------------------------|---------------------------|--------------------|
| 831742AGILF              | ICS831742AGIL  | "Lead-Free" 24 Lead TSSOP | Tube                      | -40°C to 85°C      |
| 831742AGILFT             | ICS831742AGIL  | "Lead-Free" 24 Lead TSSOP | Tape & Reel               | -40°C to 85°C      |

## Revision History

1

| Revision Date | Description of Change   |
|---------------|---|
| April 5, 2016 | <ul style="list-style-type: none"><li>▪ Removed ICS from part numbers where needed.</li><li>▪ Ordering Information - Deleted LF note below table.</li><li>▪ Updated data sheet header and footer.</li></ul> |



Corporate Headquarters  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

Sales  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
[www.IDT.com/go/sales](http://www.IDT.com/go/sales)

Tech Support  
[www.idt.com/go/support](http://www.idt.com/go/support)

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners.

For datasheet type definitions and a glossary of common terms, visit [www.idt.com/go/glossary](http://www.idt.com/go/glossary).

Copyright ©2016 Integrated Device Technology, Inc. All rights reserved.