



# HIGH-SPEED 3.3V 64/32K x 8 SYNCHRONOUS DUAL-PORT STATIC RAM

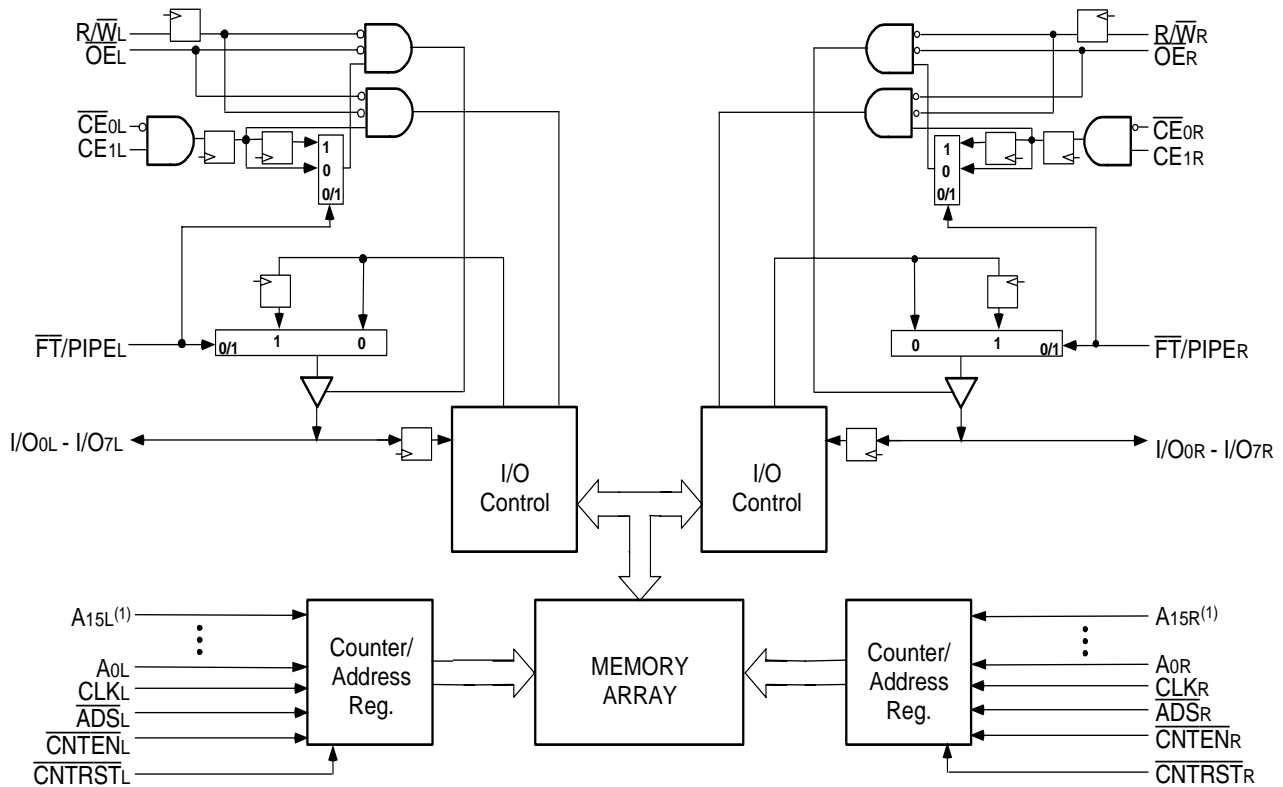
IDT70V9089/79S/L

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

## Features:

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
  - Commercial: 6.5/7.5/9/12/15ns (max.)
  - Industrial: 12ns (max.)
- ◆ Low-power operation
  - IDT70V9089/79S  
Active: 429mW (typ.)  
Standby: 3.3mW (typ.)
  - IDT70V9089/79L  
Active: 429mW (typ.)  
Standby: 1.32mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either port via the FT/PIPE pin
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 4ns setup to clock and 1ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 6.5ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 10ns cycle time, 100MHz operation in the Pipelined output mode
- ◆ LVTTTL-compatible, single 3.3V ( $\pm 0.3V$ ) power supply
- ◆ Industrial temperature range ( $-40^{\circ}C$  to  $+85^{\circ}C$ ) is available for selected speeds
- ◆ Available in a 100 pin Thin Quad Flatpack (TQFP) package
- ◆ Green parts available, see ordering information

## Functional Block Diagram



3750 drw 01

### NOTE:

1. A15x is a NC for IDT70V9079.

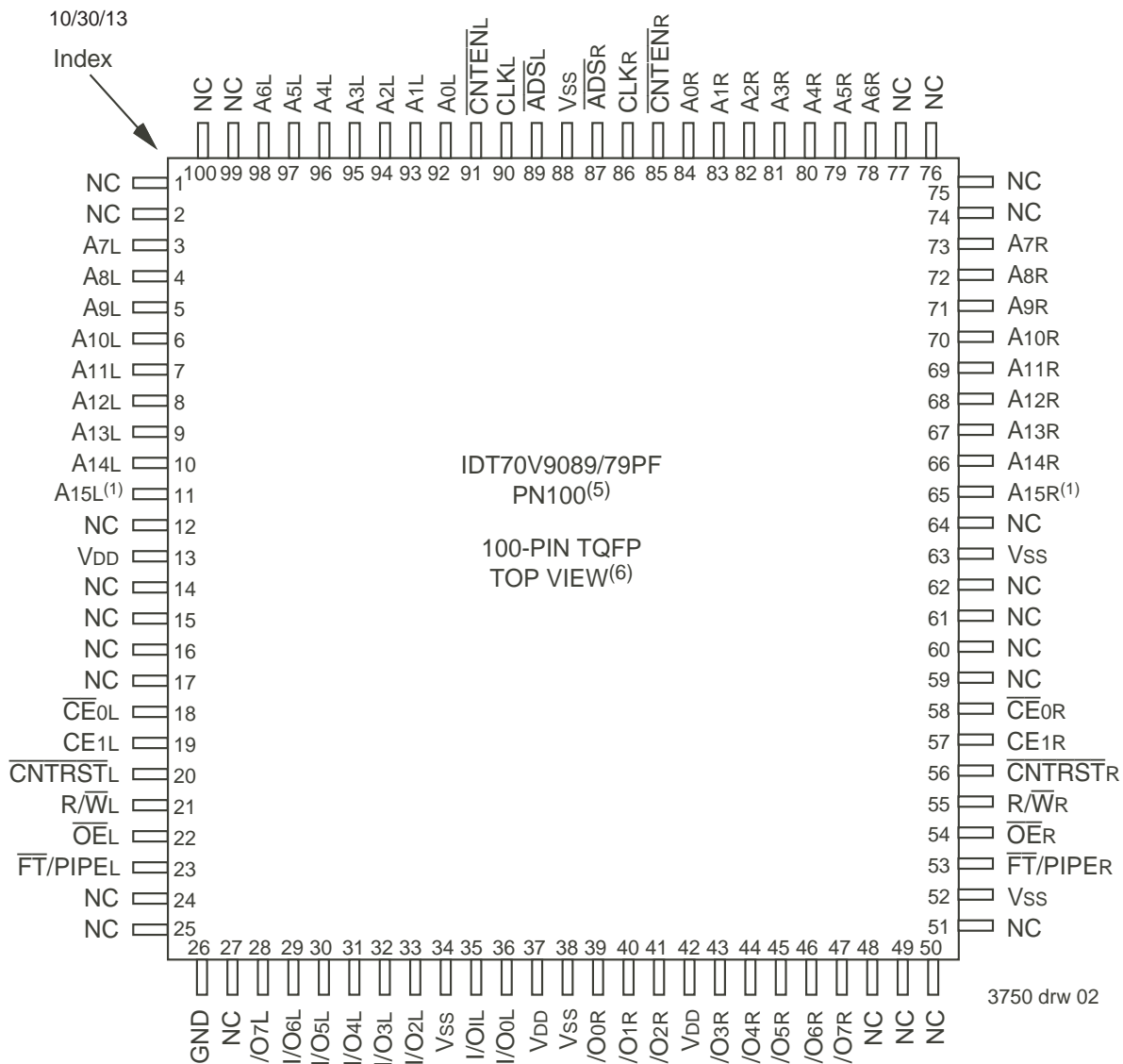
FEBRUARY 2018

## Description:

The IDT70V9089/79 is a high-speed 64/32K x 8 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70V9089/79 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by  $\overline{CE}_0$  and  $CE_1$ , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 429mW of power.

## Pin Configurations<sup>(2,3,4)</sup>



### NOTES:

1. A15x is a NC for IDT70V9079.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

| Left Port               | Right Port              | Names                 |
|-------------------------|-------------------------|-----------------------|
| $\overline{CE}0L, CE1L$ | $\overline{CE}0R, CE1R$ | Chip Enables          |
| $R/\overline{WL}$       | $R/\overline{WR}$       | Read/Write Enable     |
| $\overline{OE}L$        | $\overline{OE}R$        | Output Enable         |
| $A0L - A15L^{(1)}$      | $A0R - A15R^{(1)}$      | Address               |
| $I/O0L - I/O7L$         | $I/O0R - I/O7R$         | Data Input/Output     |
| $CLKL$                  | $CLKR$                  | Clock                 |
| $\overline{ADSL}$       | $\overline{ADSR}$       | Address Strobe        |
| $\overline{CNTENL}$     | $\overline{CNTENR}$     | Counter Enable        |
| $\overline{CNTRSTL}$    | $\overline{CNTRSTR}$    | Counter Reset         |
| $\overline{FT}/PIPEL$   | $\overline{FT}/PIPER$   | Flow-Through/Pipeline |
| $V_{DD}$                |                         | Power (3.3V)          |
| $V_{SS}$                |                         | Ground (0V)           |

3750 tbl 01

### NOTE:

- $A15x$  is a NC for IDT70V9079.
- $\overline{LB}$  and  $\overline{UB}$  are single buffered regardless of state of  $\overline{FT}/PIPE$ .
- $\overline{CE}0$  and  $CE1$  are single buffered when  $\overline{FT}/PIPE = V_{IL}$ ,  $\overline{CE}0$  and  $CE1$  are double buffered when  $\overline{FT}/PIPE = V_{IH}$ , i.e. the signals take two cycles to deselect.

## Truth Table I—Read/Write and Enable Control<sup>(1,2,3)</sup>

| $\overline{OE}$ | CLK | $\overline{CE}0$ | $CE1$ | $R/\overline{W}$ | I/O <sub>0-7</sub>  | Mode                    |
|-----------------|-----|------------------|-------|------------------|---------------------|-------------------------|
| X               | ↑   | H                | X     | X                | High-Z              | Deselected - Power Down |
| X               | ↑   | X                | L     | X                | High-Z              | Deselected - Power Down |
| X               | ↑   | L                | H     | L                | DATA <sub>IN</sub>  | Write                   |
| L               | ↑   | L                | H     | H                | DATA <sub>OUT</sub> | Read                    |
| H               | X   | L                | H     | X                | High-Z              | Outputs Disabled        |

3750 tbl 02

### NOTES:

- "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
- $\overline{ADSL}$ ,  $\overline{CNTEN}$ ,  $\overline{CNTRST}$  = X.
- $\overline{OE}$  is an asynchronous input signal.

## Truth Table II—Address Counter Control<sup>(1,2,3)</sup>

| External Address | Previous Internal Address | Internal Address Used | CLK | $\overline{ADSL}$ | $\overline{CNTEN}$ | $\overline{CNTRST}$ | I/O <sup>(3)</sup> | MODE  |
|------------------|---------------------------|-----------------------|-----|-------------------|--------------------|---------------------|--------------------|---|
| $A_n$            | X                         | $A_n$                 | ↑   | $L^{(4)}$         | X                  | H                   | $D_{I/O}(n)$       | External Address Used   |
| X                | $A_n$                     | $A_n + 1$             | ↑   | H                 | $L^{(5)}$          | H                   | $D_{I/O}(n+1)$     | Counter Enabled—Internal Address generation                   |
| X                | $A_n + 1$                 | $A_n + 1$             | ↑   | H                 | H                  | H                   | $D_{I/O}(n+1)$     | External Address Blocked—Counter disabled ( $A_n + 1$ reused) |
| X                | X                         | $A_0$                 | ↑   | X                 | X                  | $L^{(4)}$           | $D_{I/O}(0)$       | Counter Reset to Address 0                                    |

3750 tbl 03

### NOTES:

- "H" =  $V_{IH}$ , "L" =  $V_{IL}$ , "X" = Don't Care.
- $\overline{CE}0$  and  $\overline{OE} = V_{IL}$ ;  $CE1$  and  $R/\overline{W} = V_{IH}$ .
- Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- $\overline{ADSL}$  and  $\overline{CNTRST}$  are independent of all other signals including  $\overline{CE}0$  and  $CE1$ .
- The address counter advances if  $\overline{CNTEN} = V_{IL}$  on the rising edge of CLK, regardless of all other signals including  $\overline{CE}0$  and  $CE1$ .

### Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

| Grade      | Ambient Temperature | GND | V <sub>DD</sub> |
|------------|---------------------|-----|-----------------|
| Commercial | 0°C to +70°C        | 0V  | 3.3V ± 0.3V     |
| Industrial | -40°C to +85°C      | 0V  | 3.3V ± 0.3V     |

3750 tbl 04

**NOTES:**

1. This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

### Recommended DC Operating Conditions

| Symbol          | Parameter          | Min.                | Typ. | Max.                                  | Unit |
|-----------------|--------------------|---------------------|------|---------------------------------------|------|
| V <sub>DD</sub> | Supply Voltage     | 3.0                 | 3.3  | 3.6                                   | V    |
| V <sub>SS</sub> | Ground             | 0                   | 0    | 0                                     | V    |
| V <sub>IH</sub> | Input High Voltage | 2.2                 | —    | V <sub>DD</sub> + 0.3V <sup>(1)</sup> | V    |
| V <sub>IL</sub> | Input Low Voltage  | -0.3 <sup>(2)</sup> | —    | 0.8                                   | V    |

3750 tbl 05

**NOTES:**

1. V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V.
2. V<sub>IL</sub> ≥ -1.5V for pulse width less than 10ns.

### Absolute Maximum Ratings<sup>(1)</sup>

| Symbol                           | Rating                               | Commercial & Industrial | Unit |
|----------------------------------|--------------------------------------|-------------------------|------|
| V <sub>TERM</sub> <sup>(2)</sup> | Terminal Voltage with Respect to GND | -0.5 to +4.6            | V    |
| T <sub>BIAS</sub>                | Temperature Under Bias               | -55 to +125             | °C   |
| T <sub>STG</sub>                 | Storage Temperature                  | -65 to +150             | °C   |
| T <sub>JN</sub>                  | Junction Temperature                 | +150                    | °C   |
| I <sub>OUT</sub>                 | DC Output Current                    | 50                      | mA   |

3750 tbl 06

**NOTES:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 0.3V.
3. Ambient Temperature Under Bias. Chip Deselected.

### Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol                          | Parameter <sup>(1)</sup> | Conditions <sup>(2)</sup> | Max. | Unit |
|---------------------------------|--------------------------|---------------------------|------|------|
| C <sub>IN</sub>                 | Input Capacitance        | V <sub>IN</sub> = 3dV     | 9    | pF   |
| C <sub>OUT</sub> <sup>(3)</sup> | Output Capacitance       | V <sub>OUT</sub> = 3dV    | 10   | pF   |

3750 tbl 07

**NOTES:**

1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
3. C<sub>OUT</sub> also references C<sub>I/O</sub>.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 3.3V \pm 0.3V$ )

| Symbol     | Parameter                            | Test Conditions   | 70V9089/79S |      | 70V9089/79L |      | Unit    |
|------------|--------------------------------------|---|-------------|------|-------------|------|---------|
|            |                                      |   | Min.        | Max. | Min.        | Max. |         |
| $ I_{Li} $ | Input Leakage Current <sup>(1)</sup> | $V_{DD} = 3.3V, V_{IN} = 0V$ to $V_{DD}$                                | —           | 10   | —           | 5    | $\mu A$ |
| $ I_{Lo} $ | Output Leakage Current               | $\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}, V_{OUT} = 0V$ to $V_{DD}$ | —           | 10   | —           | 5    | $\mu A$ |
| $V_{OL}$   | Output Low Voltage                   | $I_{OL} = +4mA$   | —           | 0.4  | —           | 0.4  | V       |
| $V_{OH}$   | Output High Voltage                  | $I_{OH} = -4mA$   | 2.4         | —    | 2.4         | —    | V       |

**NOTE:**

1. At  $V_{DD} \leq 2.0V$  input leakages are undefined.

3750 tbl 08

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(6)</sup> ( $V_{DD} = 3.3V \pm 0.3V$ )

| Symbol   | Parameter   | Test Condition   | Version | 70V9089/79X6<br>Com'l Only |      | 70V9089/79X7<br>Com'l Only |      | 70V9089/79X9<br>Com'l Only |      | Unit |    |
|----------|---|--|---------|----------------------------|------|----------------------------|------|----------------------------|------|------|----|
|          |   |  |         | Typ. <sup>(4)</sup>        | Max. | Typ. <sup>(4)</sup>        | Max. | Typ. <sup>(4)</sup>        | Max. |      |    |
| $I_{CC}$ | Dynamic Operating Current<br>(Both Ports Active)            | $\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$<br>Outputs Disabled<br>$f = f_{MAX}^{(1)}$  | COM'L   | S                          | 220  | 395                        | 200  | 335                        | 180  | 260  | mA |
|          |   |  |         | L                          | 220  | 350                        | 200  | 290                        | 180  | 225  |    |
| ISB1     | Standby Current<br>(Both Ports - TTL<br>Level Inputs)       | $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$<br>$f = f_{MAX}^{(1)}$  | COM'L   | S                          | 70   | 145                        | 60   | 115                        | 50   | 75   | mA |
|          |   |  |         | L                          | 70   | 130                        | 60   | 100                        | 50   | 65   |    |
| ISB2     | Standby Current<br>(One Port - TTL<br>Level Inputs)         | $\overline{CE}^{*A} = V_{IL}$ and<br>$\overline{CE}^{*B} = V_{IH}^{(3)}$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(1)}$   | COM'L   | S                          | 150  | 280                        | 130  | 240                        | 110  | 170  | mA |
|          |   |  |         | L                          | 150  | 250                        | 130  | 210                        | 110  | 150  |    |
| ISB3     | Full Standby Current<br>(Both Ports -<br>CMOS Level Inputs) | Both Ports $\overline{CE}_R$ and<br>$\overline{CE}_L \geq V_{DD} - 0.2V$<br>$V_{IN} \geq V_{DD} - 0.2V$ or<br>$V_{IN} \leq 0.2V, f = 0^{(2)}$  | COM'L   | S                          | 1.0  | 5                          | 1.0  | 5                          | 1.0  | 5    | mA |
|          |   |  |         | L                          | 0.4  | 3                          | 0.4  | 3                          | 0.4  | 3    |    |
| ISB4     | Full Standby Current<br>(One Port -<br>CMOS Level Inputs)   | $\overline{CE}^{*A} \leq 0.2V$ and<br>$\overline{CE}^{*B} \geq V_{DD} - 0.2V^{(6)}$<br>$V_{IN} \geq V_{DD} - 0.2V$ or<br>$V_{IN} \leq 0.2V$ , Active Port<br>Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L   | S                          | 140  | 270                        | 120  | 230                        | 100  | 160  | mA |
|          |   |  |         | L                          | 140  | 240                        | 120  | 200                        | 100  | 140  |    |
|          |   |  | IND     | S                          | —    | —                          | —    | —                          | —    |      |    |
|          |   |  |         | L                          | —    | —                          | —    | —                          | —    |      |    |

3750 tbl 09a

**NOTES:**

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cvc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V, TA = 25^\circ C$  for Typ, and are not production tested.  $I_{CC DC}(f=0) = 90mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DD} - 0.2V$   
 $\overline{CE}_X \geq V_{DD} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DD} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
 "X" represents "L" for left port or "R" for right port.
- 'X' in part number indicates power rating (S or L).

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(6)</sup> ( $V_{DD} = 3.3V \pm 0.3V$ )(Cont'd)

| Symbol           | Parameter   | Test Condition   | Version | 70V9089/79X12<br>Com'l & Ind |      | 70V9089/79X15<br>Com'l Only |      | Unit |    |
|------------------|---|--|---------|------------------------------|------|-----------------------------|------|------|----|
|                  |   |  |         | Typ. <sup>(4)</sup>          | Max. | Typ. <sup>(4)</sup>         | Max. |      |    |
| I <sub>CC</sub>  | Dynamic Operating Current<br>(Both Ports Active)            | $\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$<br>Outputs Disabled<br>$f = f_{MAX}^{(1)}$  | COM'L   | S                            | 150  | 240                         | 130  | 220  | mA |
|                  |   |  |         | L                            | 150  | 215                         | 130  | 185  |    |
|                  |   |  | IND     | S                            | —    | —                           | —    | —    |    |
|                  |   |  |         | L                            | 150  | 215                         | —    | —    |    |
| I <sub>SB1</sub> | Standby Current<br>(Both Ports - TTL<br>Level Inputs)       | $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$<br>$f = f_{MAX}^{(1)}$  | COM'L   | S                            | 40   | 65                          | 30   | 55   | mA |
|                  |   |  |         | L                            | 40   | 60                          | 30   | 35   |    |
|                  |   |  | IND     | S                            | —    | —                           | —    | —    |    |
|                  |   |  |         | L                            | 40   | 60                          | —    | —    |    |
| I <sub>SB2</sub> | Standby Current<br>(One Port - TTL<br>Level Inputs)         | $\overline{CE}^{*A} = V_{IL}$ and<br>$\overline{CE}^{*B} = V_{IH}^{(3)}$<br>Active Port Outputs Disabled,<br>$f = f_{MAX}^{(1)}$   | COM'L   | S                            | 100  | 160                         | 90   | 150  | mA |
|                  |   |  |         | L                            | 100  | 140                         | 90   | 130  |    |
|                  |   |  | IND     | S                            | —    | —                           | —    | —    |    |
|                  |   |  |         | L                            | 100  | 150                         | —    | —    |    |
| I <sub>SB3</sub> | Full Standby Current<br>(Both Ports -<br>CMOS Level Inputs) | Both Ports $\overline{CE}_R$ and<br>$\overline{CE}_L \geq V_{DD} - 0.2V$<br>$V_{IN} \geq V_{DD} - 0.2V$ or<br>$V_{IN} \leq 0.2V, f = 0^{(2)}$  | COM'L   | S                            | 1.0  | 5                           | 1.0  | 5    | mA |
|                  |   |  |         | L                            | 0.4  | 3                           | 0.4  | 3    |    |
|                  |   |  | IND     | S                            | —    | —                           | —    | —    |    |
|                  |   |  |         | L                            | 0.4  | 3                           | —    | —    |    |
| I <sub>SB4</sub> | Full Standby Current<br>(One Port -<br>CMOS Level Inputs)   | $\overline{CE}^{*A} \leq 0.2V$ and<br>$\overline{CE}^{*B} \geq V_{DD} - 0.2V^{(5)}$<br>$V_{IN} \geq V_{DD} - 0.2V$ or<br>$V_{IN} \leq 0.2V$ , Active Port<br>Outputs Disabled, $f = f_{MAX}^{(1)}$ | COM'L   | S                            | 90   | 150                         | 80   | 140  | mA |
|                  |   |  |         | L                            | 90   | 130                         | 80   | 120  |    |
|                  |   |  | IND     | S                            | —    | —                           | —    | —    |    |
|                  |   |  |         | L                            | 90   | 140                         | —    | —    |    |

3750 tbl 09b

NOTES:

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{cyc}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $I_{CC DC}(f=0) = 90mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DD} - 0.2V$   
 $\overline{CE}_X \geq V_{DD} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DD} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
 "X" represents "L" for left port or "R" for right port.
- 'X' in part number indicates power rating (S or L).

## AC Test Conditions

|                               |                   |
|-------------------------------|-------------------|
| Input Pulse Levels            | GND to 3.0V       |
| Input Rise/Fall Times         | 3ns Max.          |
| Input Timing Reference Levels | 1.5V              |
| Output Reference Levels       | 1.5V              |
| Output Load                   | Figures 1,2 and 3 |

3750 tbl 10

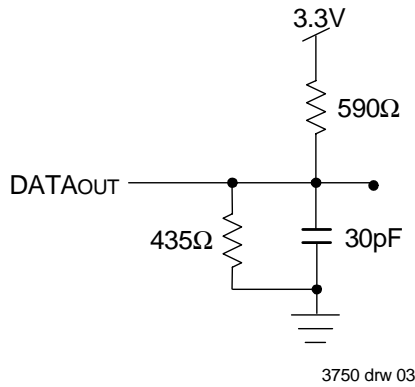


Figure 1. AC Output Test load.

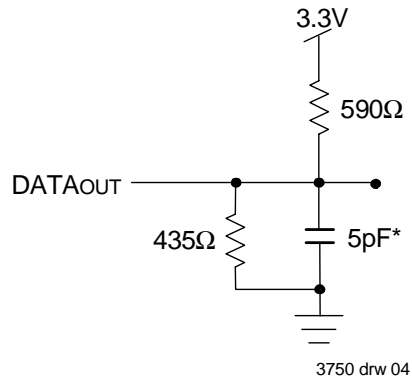


Figure 2. Output Test Load  
(For t<sub>CKLZ</sub>, t<sub>CKHZ</sub>, t<sub>OLZ</sub>, and t<sub>OHZ</sub>).  
\*Including scope and jig.

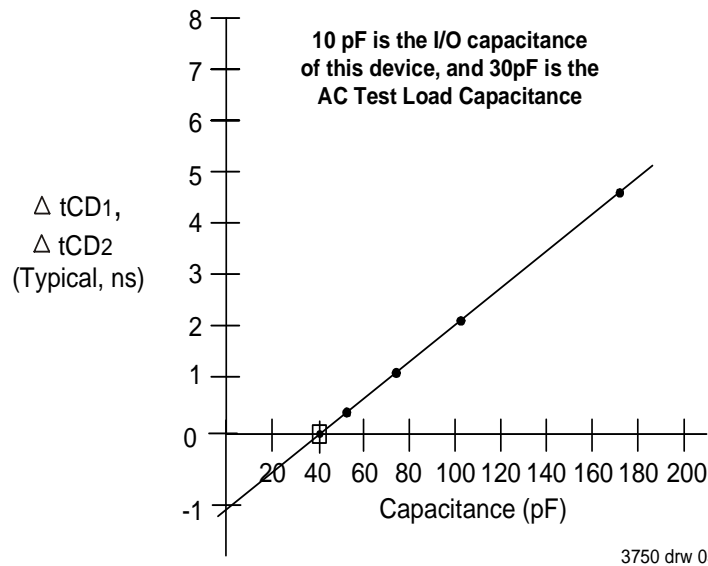


Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(3,4)</sup> ( $V_{DD} = 3.3V \pm 0.3$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

| Symbol                    | Parameter   | 70V9089/79X6 Com'l Only |      | 70V9089/79X7 Com'l Only |      | 70V9089/79X9 Com'l Only |      | Unit |
|---------------------------|---|-------------------------|------|-------------------------|------|-------------------------|------|------|
|                           |   | Min.                    | Max. | Min.                    | Max. | Min.                    | Max. |      |
| t <sub>CYC1</sub>         | Clock Cycle Time (Flow-Through) <sup>(2)</sup>    | 19                      | —    | 22                      | —    | 25                      | —    | ns   |
| t <sub>CYC2</sub>         | Clock Cycle Time (Pipelined) <sup>(2)</sup>       | 10                      | —    | 12                      | —    | 15                      | —    | ns   |
| t <sub>CH1</sub>          | Clock High Time (Flow-Through) <sup>(2)</sup>     | 6.5                     | —    | 7.5                     | —    | 12                      | —    | ns   |
| t <sub>CL1</sub>          | Clock Low Time (Flow-Through) <sup>(2)</sup>      | 6.5                     | —    | 7.5                     | —    | 12                      | —    | ns   |
| t <sub>CH2</sub>          | Clock High Time (Pipelined) <sup>(2)</sup>        | 4                       | —    | 5                       | —    | 6                       | —    | ns   |
| t <sub>CL2</sub>          | Clock Low Time (Pipelined) <sup>(2)</sup>         | 4                       | —    | 5                       | —    | 6                       | —    | ns   |
| t <sub>R</sub>            | Clock Rise Time                                   | —                       | 3    | —                       | 3    | —                       | 3    | ns   |
| t <sub>F</sub>            | Clock Fall Time                                   | —                       | 3    | —                       | 3    | —                       | 3    | ns   |
| t <sub>SA</sub>           | Address Setup Time                                | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HA</sub>           | Address Hold Time                                 | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SC</sub>           | Chip Enable Setup Time                            | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HC</sub>           | Chip Enable Hold Time                             | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SW</sub>           | R/W Setup Time                                    | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HW</sub>           | R/W Hold Time                                     | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SD</sub>           | Input Data Setup Time                             | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HD</sub>           | Input Data Hold Time                              | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SAD</sub>          | $\overline{ADS}$ Setup Time                       | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HAD</sub>          | $\overline{ADS}$ Hold Time                        | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SCN</sub>          | $\overline{CNTEN}$ Setup Time                     | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HCN</sub>          | $\overline{CNTEN}$ Hold Time                      | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>SRST</sub>         | $\overline{CNTRST}$ Setup Time                    | 3.5                     | —    | 4                       | —    | 4                       | —    | ns   |
| t <sub>HRST</sub>         | $\overline{CNTRST}$ Hold Time                     | 0                       | —    | 0                       | —    | 1                       | —    | ns   |
| t <sub>OE</sub>           | Output Enable to Data Valid                       | —                       | 6.5  | —                       | 7.5  | —                       | 9    | ns   |
| t <sub>OLZ</sub>          | Output Enable to Output Low-Z <sup>(1)</sup>      | 2                       | —    | 2                       | —    | 2                       | —    | ns   |
| t <sub>OHZ</sub>          | Output Enable to Output High-Z <sup>(1)</sup>     | 1                       | 7    | 1                       | 7    | 1                       | 7    | ns   |
| t <sub>CD1</sub>          | Clock to Data Valid (Flow-Through) <sup>(2)</sup> | —                       | 15   | —                       | 18   | —                       | 20   | ns   |
| t <sub>CD2</sub>          | Clock to Data Valid (Pipelined) <sup>(2)</sup>    | —                       | 6.5  | —                       | 7.5  | —                       | 9    | ns   |
| t <sub>DC</sub>           | Data Output Hold After Clock High                 | 2                       | —    | 2                       | —    | 2                       | —    | ns   |
| t <sub>CKHZ</sub>         | Clock High to Output High-Z <sup>(1)</sup>        | 2                       | 9    | 2                       | 9    | 2                       | 9    | ns   |
| t <sub>CKLZ</sub>         | Clock High to Output Low-Z <sup>(1)</sup>         | 2                       | —    | 2                       | —    | 2                       | —    | ns   |
| <b>Port-to-Port Delay</b> |   |                         |      |                         |      |                         |      |      |
| t <sub>CWDD</sub>         | Write Port Clock High to Read Data Delay          | —                       | 24   | —                       | 28   | —                       | 35   | ns   |
| t <sub>CCS</sub>          | Clock-to-Clock Setup Time                         | —                       | 9    | —                       | 10   | —                       | 15   | ns   |

3750 tbl 11a

### NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both left and right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
4. 'X' in part number indicates power rating (S or L).



## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(3,4)</sup> ( $V_{DD} = 3.3V \pm 0.3$ )

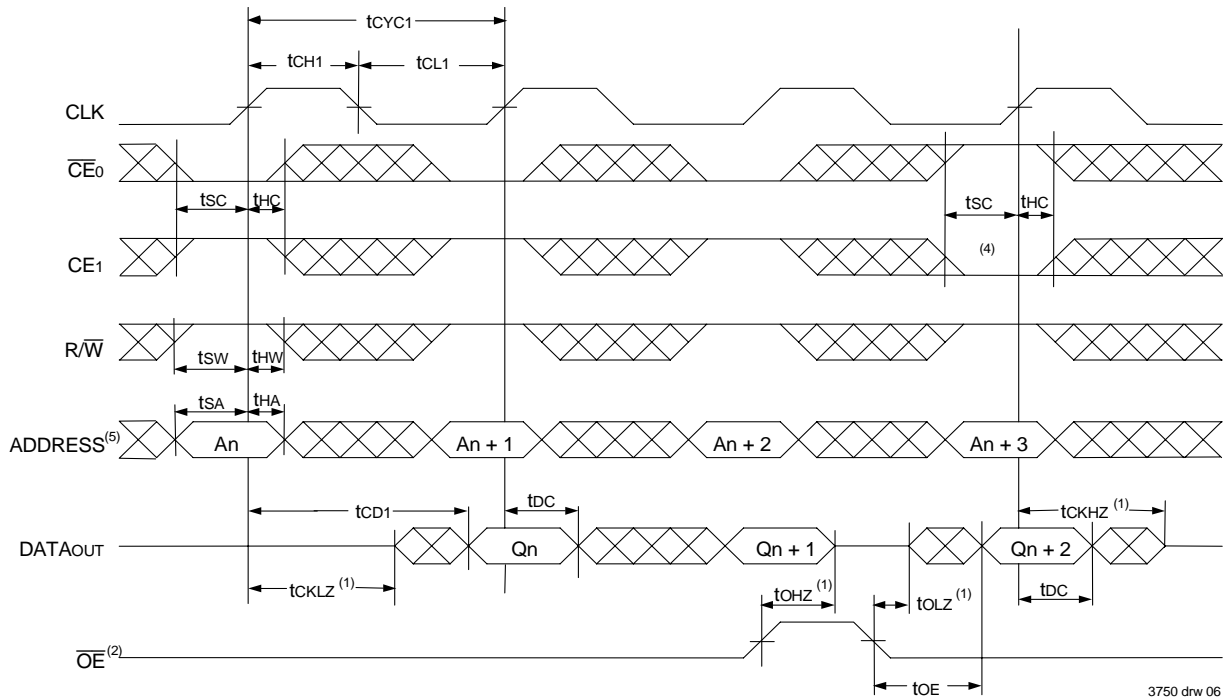
| Symbol                    | Parameter   | 70V9089/79X12<br>Com'l & Ind |      | 70V908979X15<br>Com'l Only |      | Unit |
|---------------------------|---|------------------------------|------|----------------------------|------|------|
|                           |   | Min.                         | Max. | Min.                       | Max. |      |
| t <sub>CYC1</sub>         | Clock Cycle Time (Flow-Through) <sup>(2)</sup>    | 30                           | —    | 35                         | —    | ns   |
| t <sub>CYC2</sub>         | Clock Cycle Time (Pipelined) <sup>(2)</sup>       | 20                           | —    | 25                         | —    | ns   |
| t <sub>CH1</sub>          | Clock High Time (Flow-Through) <sup>(2)</sup>     | 12                           | —    | 12                         | —    | ns   |
| t <sub>CL1</sub>          | Clock Low Time (Flow-Through) <sup>(2)</sup>      | 12                           | —    | 12                         | —    | ns   |
| t <sub>CH2</sub>          | Clock High Time (Pipelined) <sup>(2)</sup>        | 8                            | —    | 10                         | —    | ns   |
| t <sub>CL2</sub>          | Clock Low Time (Pipelined) <sup>(2)</sup>         | 8                            | —    | 10                         | —    | ns   |
| t <sub>R</sub>            | Clock Rise Time                                   | —                            | 3    | —                          | 3    | ns   |
| t <sub>F</sub>            | Clock Fall Time                                   | —                            | 3    | —                          | 3    | ns   |
| t <sub>SA</sub>           | Address Setup Time                                | 4                            | —    | 4                          | —    | ns   |
| t <sub>HA</sub>           | Address Hold Time                                 | 1                            | —    | 1                          | —    | ns   |
| t <sub>SC</sub>           | Chip Enable Setup Time                            | 4                            | —    | 4                          | —    | ns   |
| t <sub>HC</sub>           | Chip Enable Hold Time                             | 1                            | —    | 1                          | —    | ns   |
| t <sub>SW</sub>           | R/W Setup Time                                    | 4                            | —    | 4                          | —    | ns   |
| t <sub>HW</sub>           | R/W Hold Time                                     | 1                            | —    | 1                          | —    | ns   |
| t <sub>SD</sub>           | Input Data Setup Time                             | 4                            | —    | 4                          | —    | ns   |
| t <sub>HD</sub>           | Input Data Hold Time                              | 1                            | —    | 1                          | —    | ns   |
| t <sub>SAD</sub>          | $\overline{ADS}$ Setup Time                       | 4                            | —    | 4                          | —    | ns   |
| t <sub>HAD</sub>          | $\overline{ADS}$ Hold Time                        | 1                            | —    | 1                          | —    | ns   |
| t <sub>SCN</sub>          | $\overline{CNTEN}$ Setup Time                     | 4                            | —    | 4                          | —    | ns   |
| t <sub>HCN</sub>          | $\overline{CNTEN}$ Hold Time                      | 1                            | —    | 1                          | —    | ns   |
| t <sub>SRST</sub>         | $\overline{CNTRST}$ Setup Time                    | 4                            | —    | 4                          | —    | ns   |
| t <sub>HRST</sub>         | $\overline{CNTRST}$ Hold Time                     | 1                            | —    | 1                          | —    | ns   |
| t <sub>OE</sub>           | Output Enable to Data Valid                       | —                            | 12   | —                          | 15   | ns   |
| t <sub>OLZ</sub>          | Output Enable to Output Low-Z <sup>(1)</sup>      | 2                            | —    | 2                          | —    | ns   |
| t <sub>OHZ</sub>          | Output Enable to Output High-Z <sup>(1)</sup>     | 1                            | 7    | 1                          | 7    | ns   |
| t <sub>CD1</sub>          | Clock to Data Valid (Flow-Through) <sup>(2)</sup> | —                            | 25   | —                          | 30   | ns   |
| t <sub>CD2</sub>          | Clock to Data Valid (Pipelined) <sup>(2)</sup>    | —                            | 12   | —                          | 15   | ns   |
| t <sub>DC</sub>           | Data Output Hold After Clock High                 | 2                            | —    | 2                          | —    | ns   |
| t <sub>CKHZ</sub>         | Clock High to Output High-Z <sup>(1)</sup>        | 2                            | 9    | 2                          | 9    | ns   |
| t <sub>CKLZ</sub>         | Clock High to Output Low-Z <sup>(1)</sup>         | 2                            | —    | 2                          | —    | ns   |
| <b>Port-to-Port Delay</b> |   |                              |      |                            |      |      |
| t <sub>CWDD</sub>         | Write Port Clock High to Read Data Delay          | —                            | 40   | —                          | 50   | ns   |
| t <sub>CCS</sub>          | Clock-to-Clock Setup Time                         | —                            | 15   | —                          | 20   | ns   |

3750 tbl 11b

### NOTES:

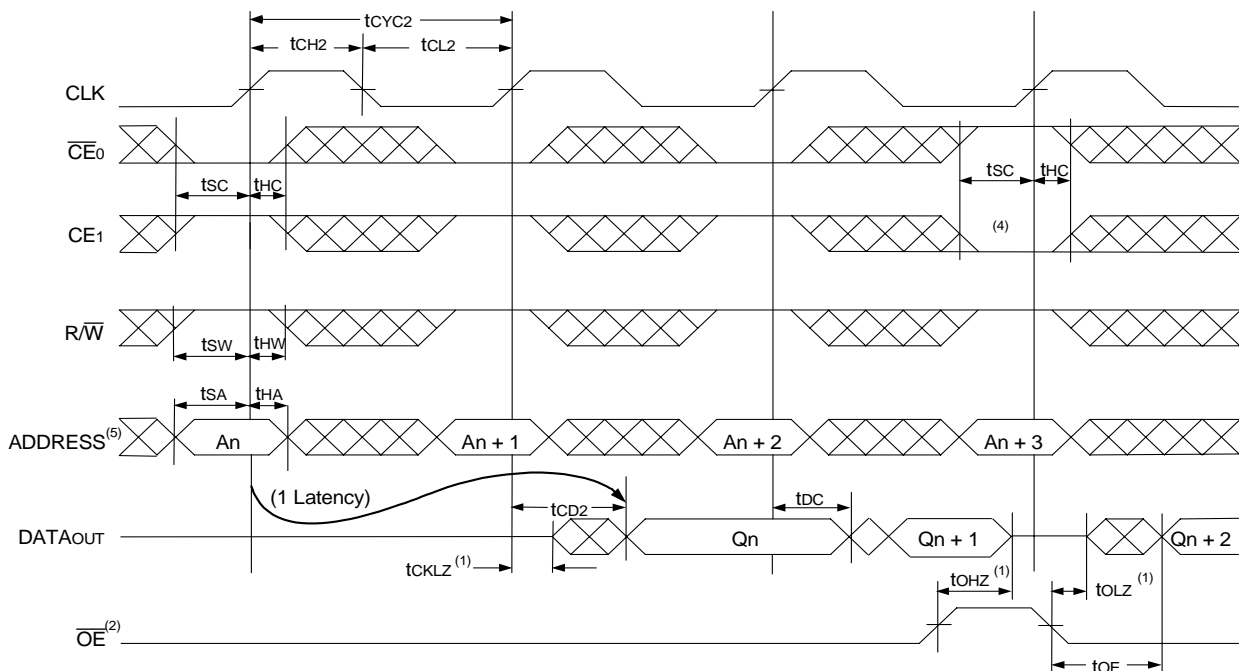
- Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
- The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both left and right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPE$ .  $\overline{FT}/PIPE$  should be treated as a DC signal, i.e. steady state during operation.
- 'X' in part number indicates power rating (S or L).

### Timing Waveform of Read Cycle for Flow-Through Output ( $\overline{FT}/\text{PIPE}^{\text{X}} = V_{IL}$ )<sup>(3,6)</sup>



3750 drw 06

### Timing Waveform of Read Cycle for Pipelined Output ( $\overline{FT}/\text{PIPE}^{\text{X}} = V_{IH}$ )<sup>(3,6)</sup>

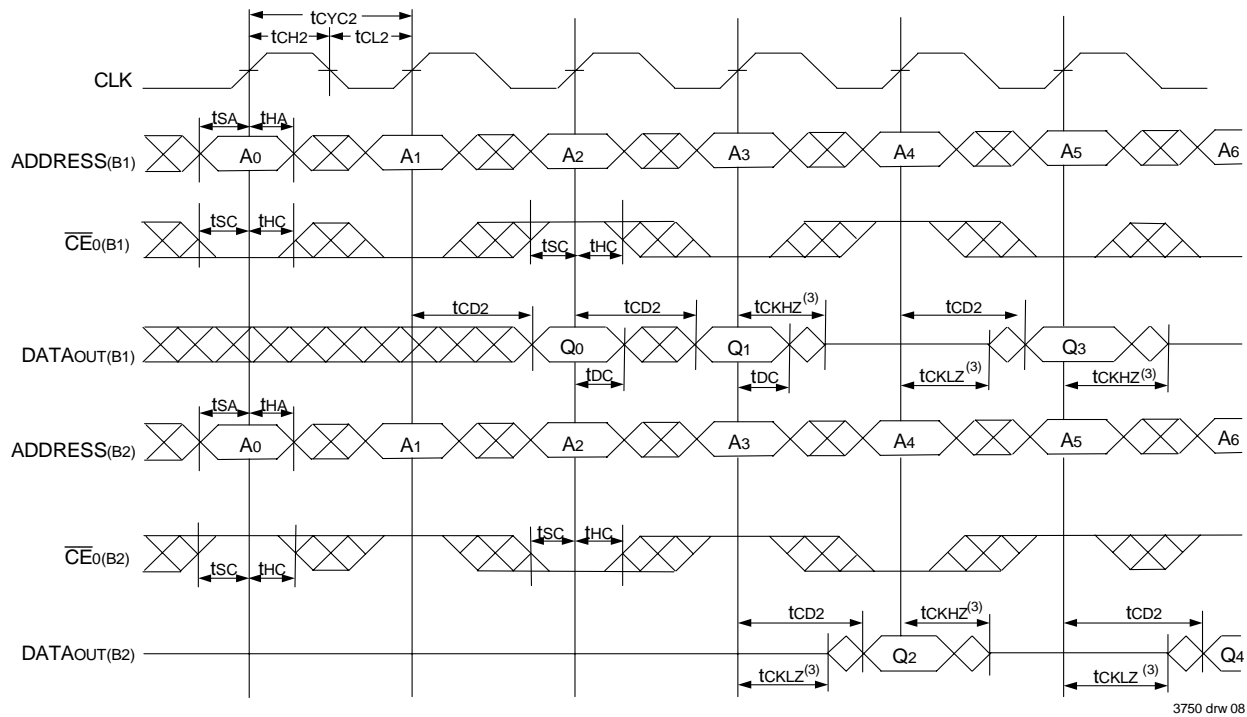


3750 drw 07

**NOTES:**

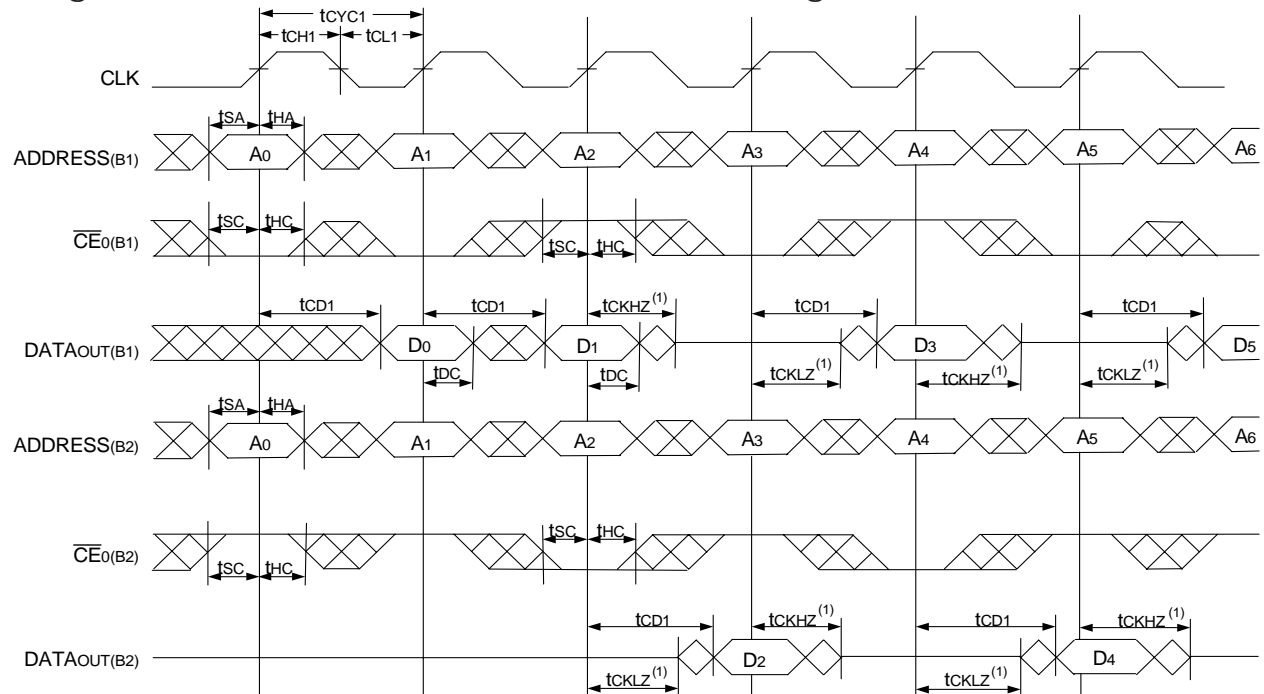
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3.  $\overline{ADS} = V_{IL}$  and  $\overline{CNTRST} = V_{IH}$ .
4. The output is disabled (High-impedance state) by  $\overline{CE0} = V_{IH}$  or  $CE1 = V_{IL}$  following the next rising edge of clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. "x" denotes Left or Right port. The diagram is with respect to that port.

### Timing Waveform of a Bank Select Pipelined Read<sup>(1,2)</sup>



3750 drw 08

### Timing Waveform of a Bank Select Flow-Through Read<sup>(6)</sup>

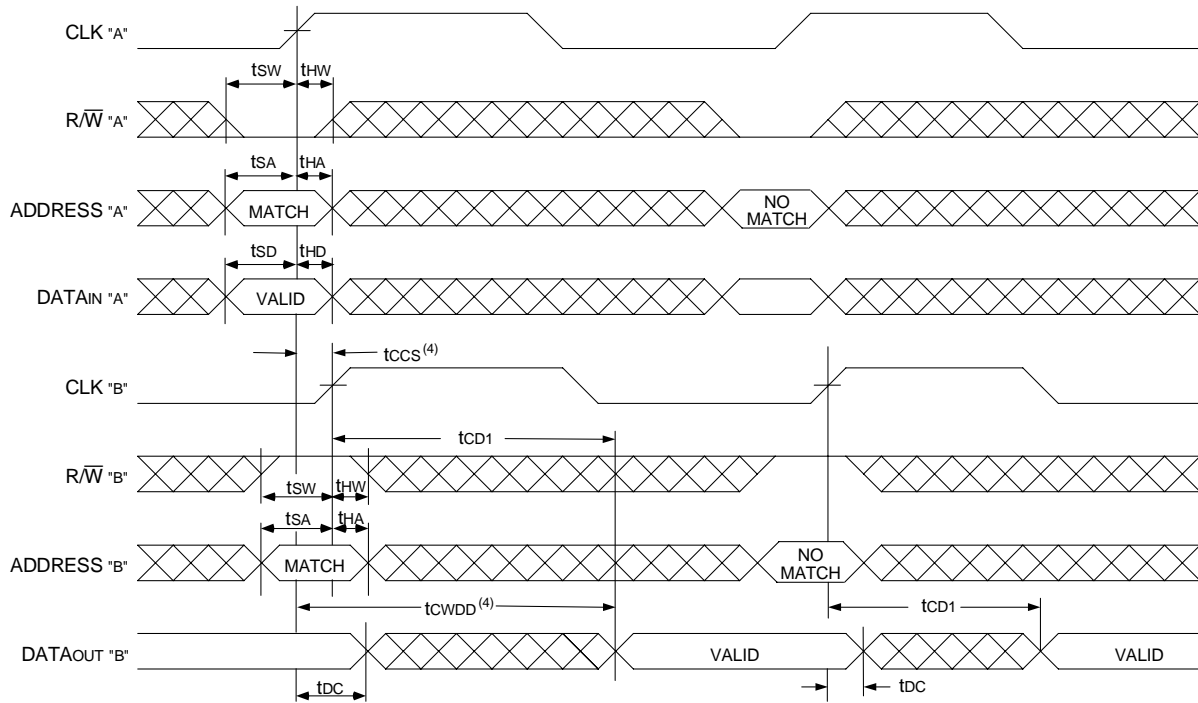


3750 drw 08a

**NOTES:**

1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70V9089/79 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2.  $\overline{OE}$  and  $\overline{ADS} = V_{IL}$ ; CE1(B1), CE1(B2), R/W and CNTRST =  $V_{IH}$ .
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4.  $\overline{CE0}$  and  $\overline{ADS} = V_{IL}$ ; CE1 and CNTRST =  $V_{IH}$ .
5.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
6. If  $t_{CCS} \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $tc_{WDD}$ . If  $t_{CCS} >$  maximum specified, then data from right port READ is not valid until  $t_{CCS} + t_{CD1}$ .  $tc_{WDD}$  does not apply in this case.

## Timing Waveform Port-to-Port Flow-Through Read<sup>(1,2,3,5)</sup>

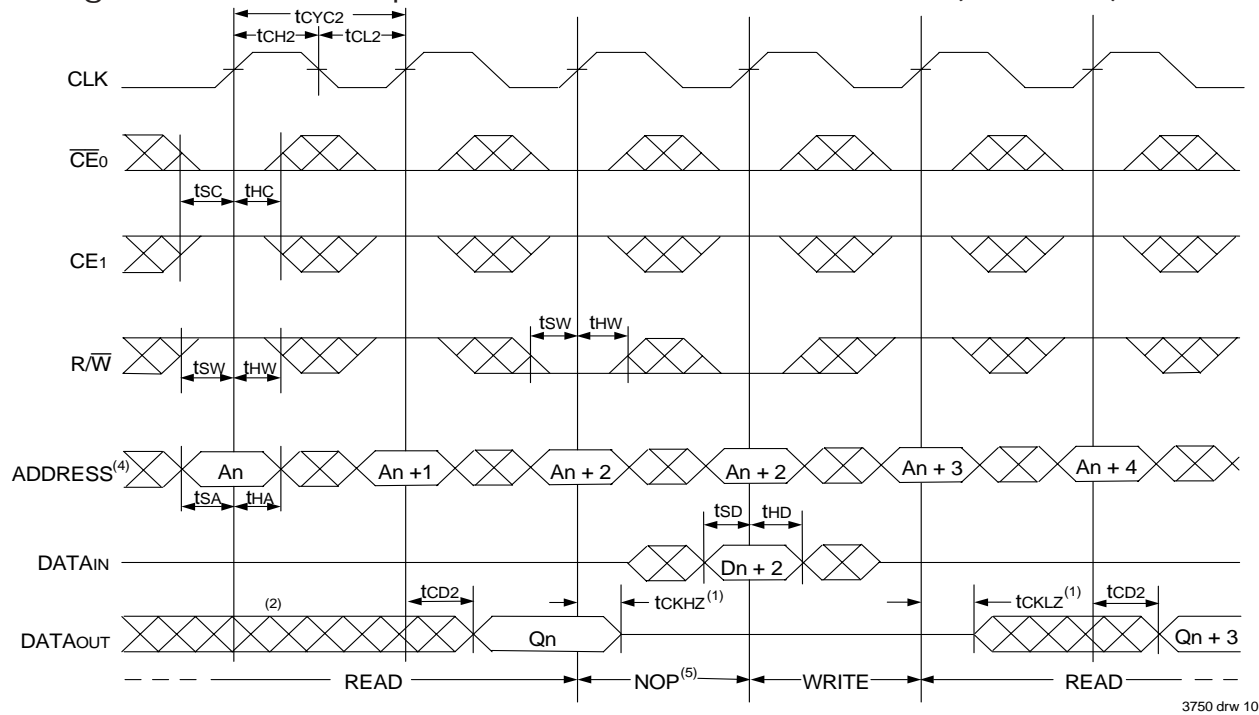


3750 drw 09

### NOTES:

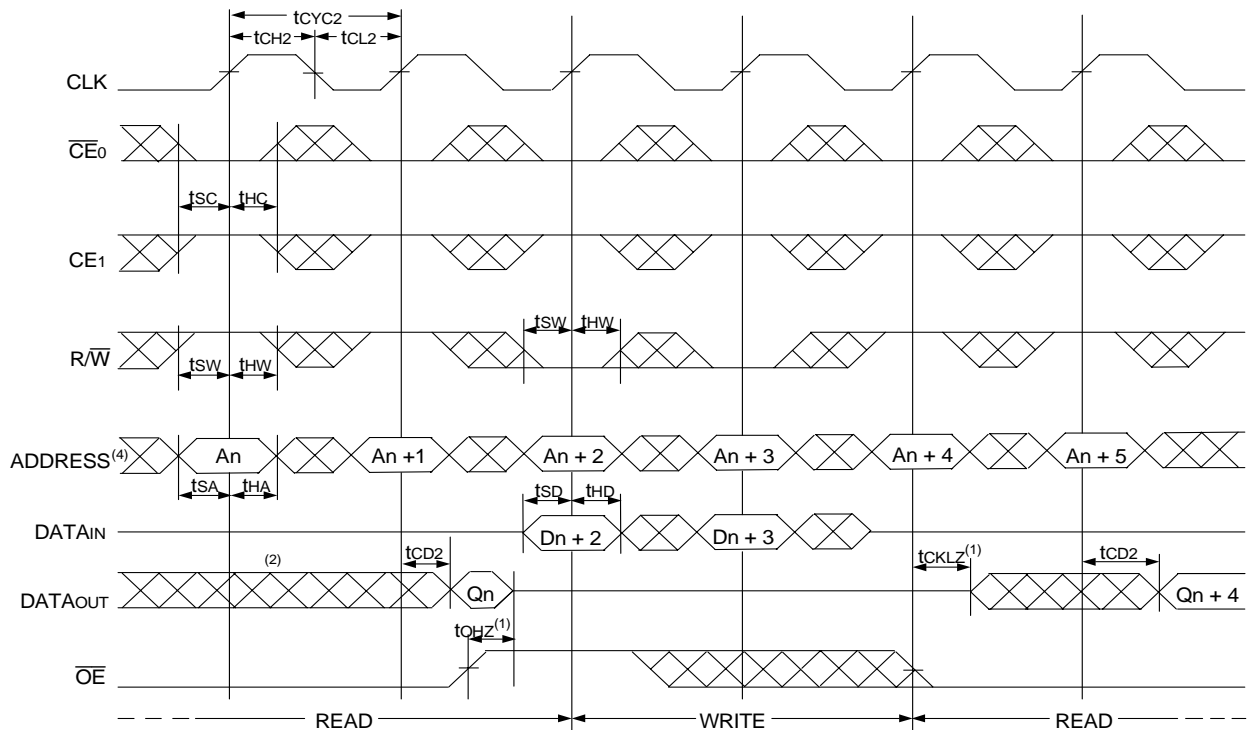
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{CE_0}$  and  $\overline{ADS} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST} = V_{IH}$ .
3.  $\overline{OE} = V_{IL}$  for the Port "B", which is being read from.  $\overline{OE} = V_{IH}$  for the Port "A", which is being written to.
4. If  $t_{ccs} \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $t_{cwb}$ .  
If  $t_{ccs} >$  maximum specified, then data from right port READ is not valid until  $t_{ccs} + t_{cd1}$ .  $t_{cwwd}$  does not apply in this case.
5. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>



3750 drw 10

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(3)</sup>

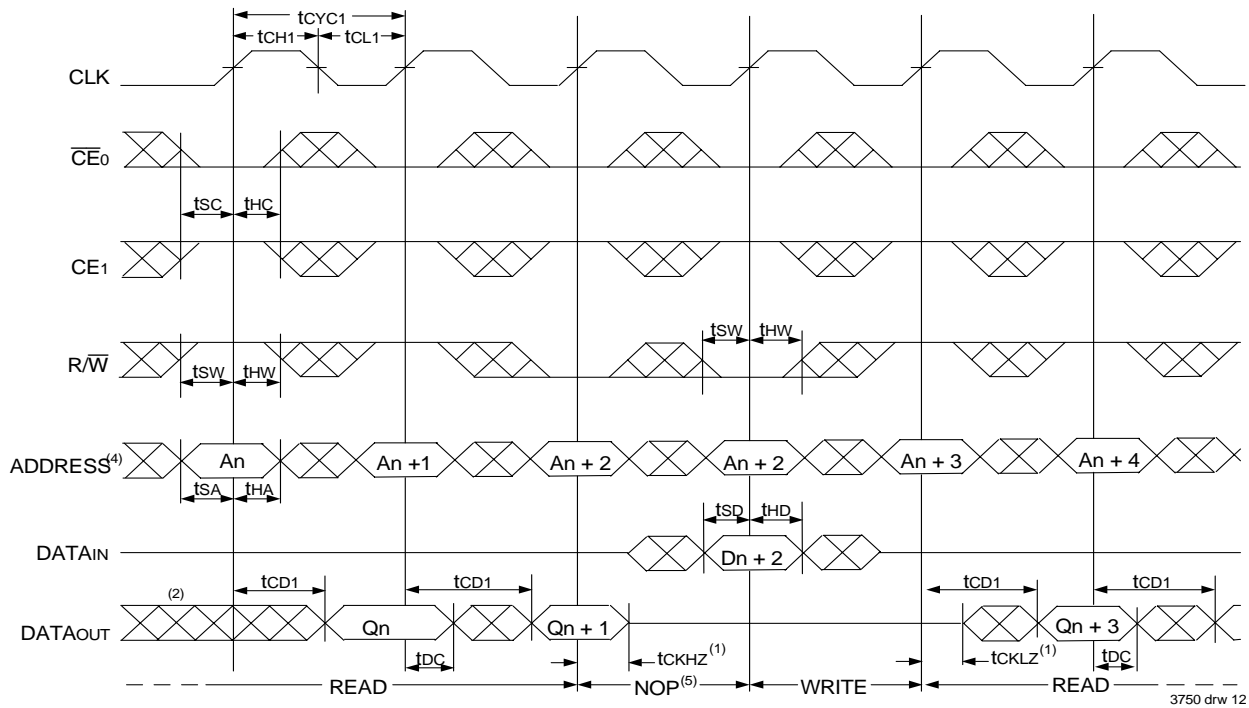


3750 drw 11

**NOTES:**

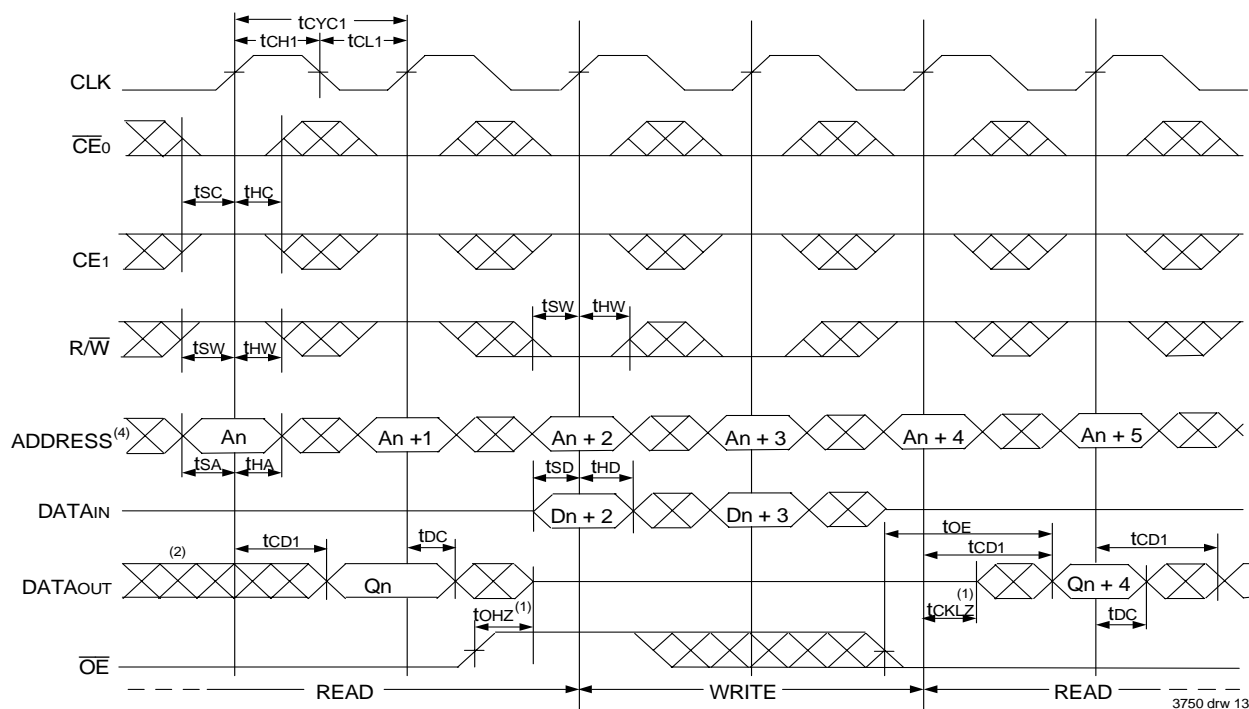
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$  and  $\overline{ADS} = V_{IL}$ ;  $CE_1$  and  $CNTRST = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>



3750 drw 12

Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$  Controlled)<sup>(3)</sup>

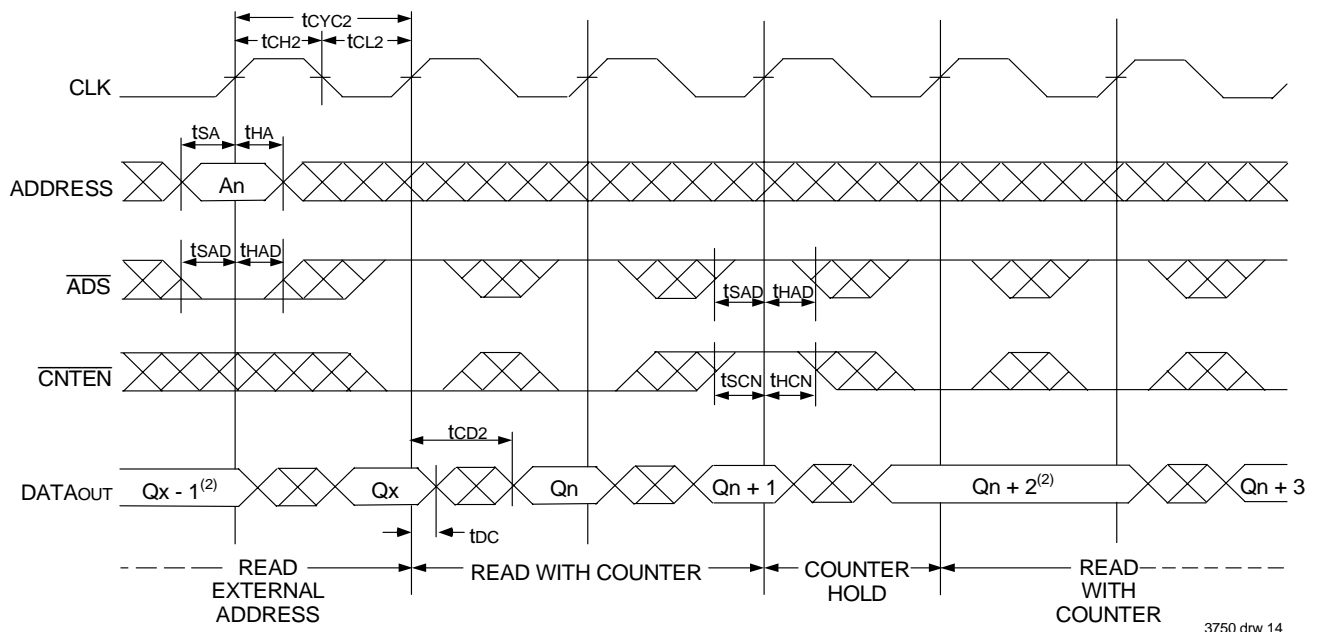


3750 drw 13

NOTES:

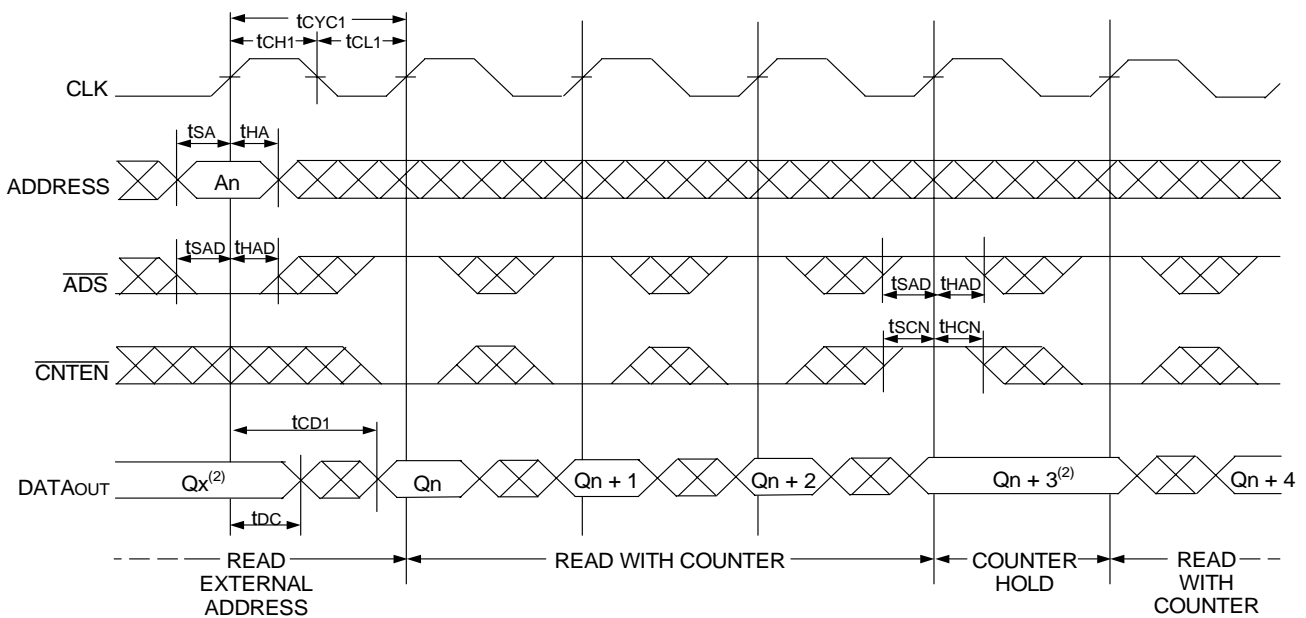
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE0}$  and  $\overline{ADS} = V_{IL}$ ;  $CE1$  and  $CNTRST = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

### Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



3750 drw 14

### Timing Waveform of Flow-Through Counter Read with Address Counter Advance<sup>(1)</sup>

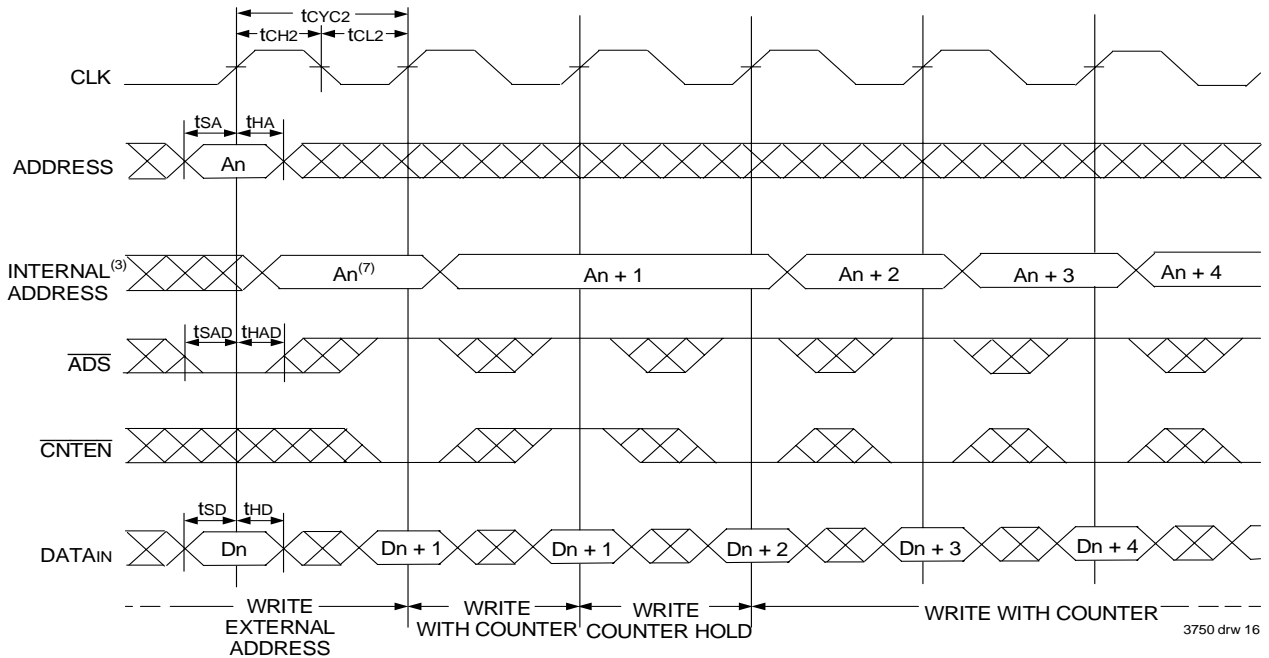


3750 drw 15

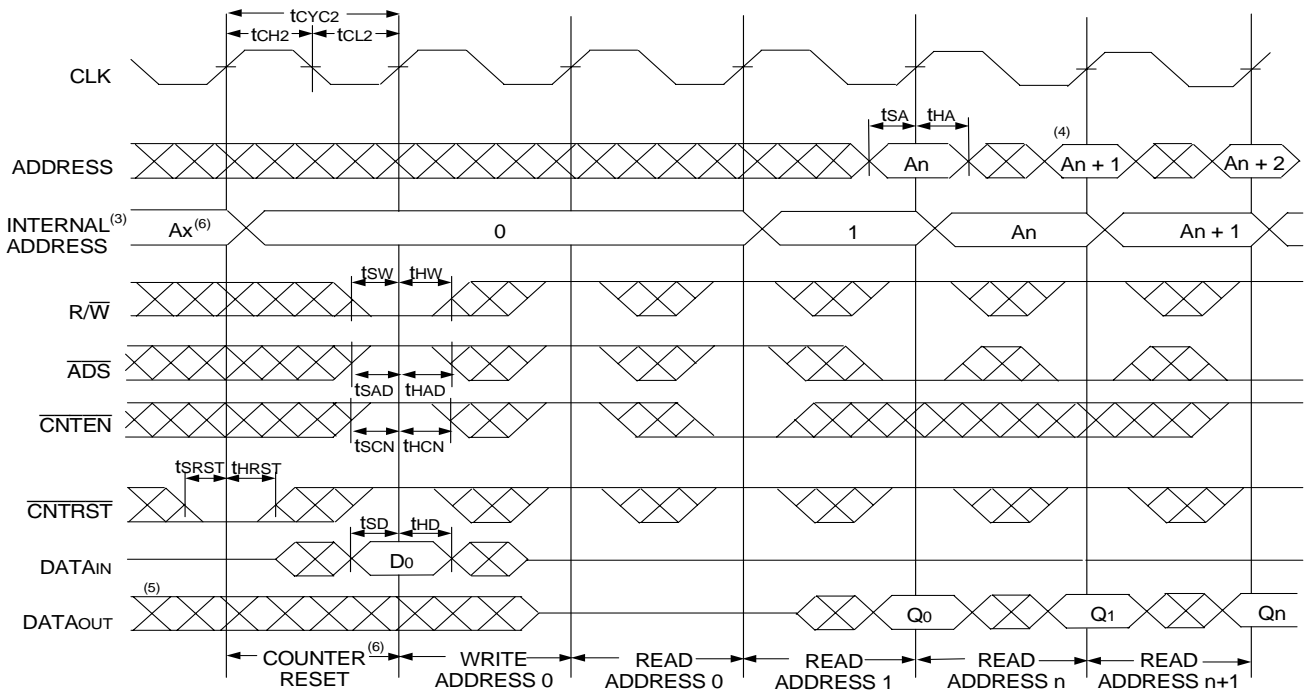
**NOTES:**

1.  $\overline{CE}_0$  and  $\overline{OE} = V_{IL}$ ;  $CE_1$ ,  $R/\overline{W}$ , and  $\overline{CNT\overline{RST}} = V_{IH}$ .
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)<sup>(1)</sup>



## Timing Waveform of Counter Reset (Pipelined Outputs)<sup>(2)</sup>



**NOTES:**

1.  $\overline{CE}_0$  and  $\overline{R/W} = V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST} = V_{IH}$ .
2.  $\overline{CE}_0 = V_{IL}$ ;  $CE_1 = V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset. ADDR0 will be accessed. Extra cycles are shown here simply for clarification.
7.  $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' address is written to during this cycle.



## Functional Description

The IDT70V9089/79 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the counter registers for fast interleaved memory applications.

A HIGH on  $\overline{CE_0}$  or a LOW on  $CE_1$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V9089/79's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with  $\overline{CE_0}$  LOW and  $CE_1$  HIGH to re-activate the outputs.

## Depth and Width Expansion

The IDT70V9089/79 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V9089/79 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 16-bit or wider applications.

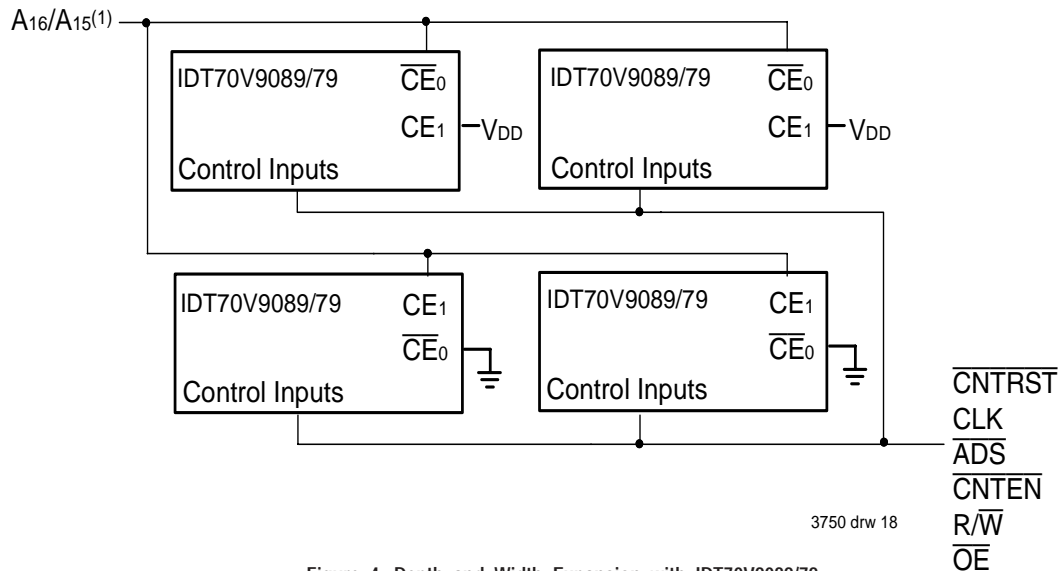
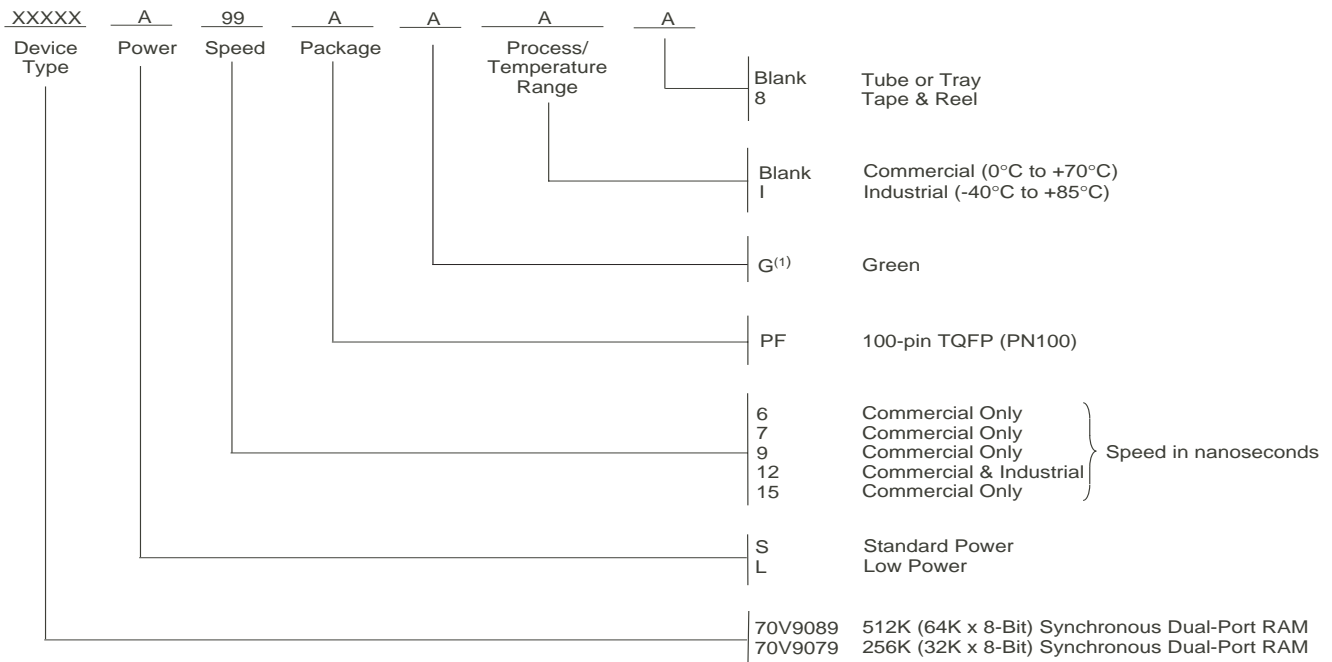


Figure 4. Depth and Width Expansion with IDT70V9089/79

**NOTE:**

1. A16 is for IDT70V9089. A15 is for IDT70V9079.

## Ordering Information



**NOTE:**

- Green parts available. For specific speeds, packages and powers contact your sales office.  
**LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02**

## Ordering Information for Flow-through Devices

| Old Flow-through Part | New Combined Part |
|-----------------------|-------------------|
| 70V908S/L25           | 70V9089S/L12      |
| 70V908S/L30           | 70V9089S/L15      |

3750 tbi 12

| Old Flow-through Part | New Combined Part |
|-----------------------|-------------------|
| 70V907S/L25           | 70V9079S/L12      |
| 70V907S/L30           | 70V9079S/L15      |

3750 tbi 13

## IDT Clock Solution for IDT70V9089/79 Dual-Port

| IDT Dual-Port Part Number | Dual-Port I/O Specifications |        | Clock Specifications |                              |                   |                  | IDT PLL Clock Device | IDT Non-PLL Clock Device                               |
|---------------------------|------------------------------|--------|----------------------|------------------------------|-------------------|------------------|----------------------|--|
|                           | Voltage                      | I/O    | Input Capacitance    | Input Duty Cycle Requirement | Maximum Frequency | Jitter Tolerance |                      |  |
| 70V9089/79                | 3.3                          | LVTTTL | 9pF                  | 40%                          | 100               | 150ps            | 2305<br>2308<br>2309 | 49FCT3805<br>49FCT3805D/E<br>74FCT3807<br>74FCT3807D/E |

3750 tbi 14

## Datasheet Document History

- 01/18/99:
- Initiated datasheet document history
  - Converted to new format
  - Cosmetic and typographical corrections
  - Added additional notes to pin configurations
  - Added Depth and Width Expansion section.

## Datasheet Document History (con't.)

|           |                  |   |
|-----------|------------------|---|
| 06/11/99: | Page 3           | Deleted note 6 for Table II   |
| 11/12/99: |                  | Replaced IDT logo   |
| 03/31/00: |                  | Combined Pipelined 70V9089 family and Flow-through 70V908 family offerings into one data sheet<br>Changed $\pm 200\text{mV}$ in waveform notes to $0\text{mV}$<br>Added corresponding part chart with ordering information        |
| 01/10/01: | Page 3<br>Page 4 | Changed information in Truth Table II<br>Increased storage temperature parameters<br>Clarified $T_A$ parameter  |
|           | Page 5           | DC Electrical parameters—changed wording from "open" to "disabled"<br>Removed Preliminary Status  |
| 01/15/04: |                  | Consolidated multiple devices into one datasheet<br>Changed naming conventions from $V_{CC}$ to $V_{DD}$ and from GND to $V_{SS}$<br>Removed I-temp footnote from tables  |
|           | Page 2           | Added date revision to pin configuration  |
|           | Page 4           | Added Junction Temperature to Absolute Maximum Ratings Table<br>Added Ambient Temperature footnote  |
|           | Page 5           | Added I-temp numbers for 9ns speed to the DC Electrical Characteristics Table<br>Added 6ns & 7ns speeds DC power numbers to the DC Electrical Characteristics Table   |
|           | Page 7           | Added I-temp for 9ns speed to AC Electrical Characteristics Table<br>Added 6ns & 7ns speeds AC timing numbers to the AC Electrical Characteristics Table  |
|           | Page 16          | Added 6ns & 7ns speeds grade and 9ns I-temp to ordering information<br>Added IDT Clock Solution Table   |
|           | Pages 1 & 17     | Replaced © IDT logo with ™ new logo   |
| 05/11/04: | Pages 1 & 19     | Added 7ns speed grade to ordering information   |
|           | Page 5           | Added 7ns speed DC power numbers to the DC Electrical Characteristics Table   |
|           | Page 8           | Added 7ns speed AC timing numbers to the AC Electrical Characteristics Table  |
| 12/01/05: | Page 1           | Added green parts availability to features  |
|           | Page 18          | Added green indicator to ordering information   |
| 01/19/09: | Page 18          | Removed "IDT" from orderable part number  |
| 07/26/10: | Page 8           | In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range values located in the table, the commercial $T_A$ header note has been removed                                     |
|           | Pages 10-14      | In order to correct the footnotes of timing diagrams, $\overline{\text{CNTEN}}$ has been removed to reconcile the footnotes with the $\overline{\text{CNTEN}}$ logic definition found in Truth Table II - Address Counter Control |
| 07/15/14: | Page 1           | Replaced Industrial 9ns with 12ns. Replaced Low Power Operation Standby from 600mW (typ) to 1.32mW (typ) in the Features  |
|           | Page 2           | Corrected some text typos   |
|           | Page 5           | Removed the 9ns Industrial temp power values for the S & L offering in the DC Elec Chars table  |
|           | Page 6           | Added the 12ns Industrial temp power value for the L offering in the DC Elec Chars table  |
|           | Pages 8 & 9      | Updated the column headings of the AC Elec Chars table to indicate the Commercial and Industrial speed grade offerings  |
|           | Page 18          | Updated all the Commercial and Industrial speed grade offerings and added Tape & Reel to Ordering Information   |
|           | Page 2 & 18      | The label PN100-1 changed to PN100 to match the standard package code   |
|           | Page 18          | Corrected Old Flow-through Part number in table 13 to 70V907S/L25 & L3  |
| 02/20/18: |                  | Product Discontinuation Notice - PDN# SP-17-02<br>Last time buy expires June 15, 2018   |



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
www.idt.com

**for Tech Support:**  
408-284-2794  
DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.