

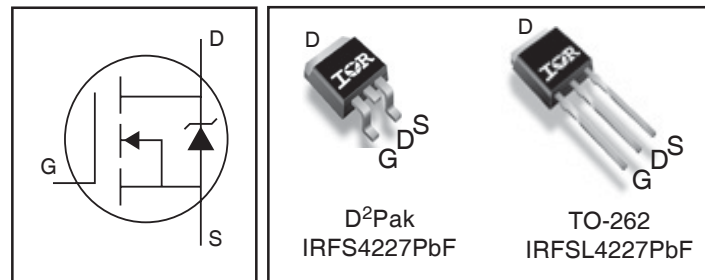
**PDP SWITCH**

**IRFS4227PbF**  
**IRFSL4227PbF**

**Features**

- Advanced Process Technology
- Key Parameters Optimized for PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $E_{PULSE}$  Rating to Reduce Power Dissipation in PDP Sustain, Energy Recovery and Pass Switch Applications
- Low  $Q_G$  for Fast Response
- High Repetitive Peak Current Capability for Reliable Operation
- Short Fall & Rise Times for Fast Switching
- 175°C Operating Junction Temperature for Improved Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability

Key Parameters		
$V_{DS}$ max	200	V
$V_{DS}$ (Avalanche) typ.	240	V
$R_{DS(ON)}$ typ. @ 10V	22	mΩ
$I_{RP}$ max @ $T_C = 100^\circ\text{C}$	130	A
$T_J$ max	175	°C



G	D	S
Gate	Drain	Source

**Description**

This HEXFET® Power MOSFET is specifically designed for Sustain, Energy Recovery & Pass switch applications in Plasma Display Panels. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area and low  $E_{PULSE}$  rating. Additional features of this MOSFET are 175°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	±30	V
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	62	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	44	
$I_{DM}$	Pulsed Drain Current ①	260	
$I_{RP}$ @ $T_C = 100^\circ\text{C}$	Repetitive Peak Current ⑤	130	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
$P_D$ @ $T_C = 100^\circ\text{C}$	Power Dissipation	190	
	Linear Derating Factor	2.2	W/°C
$T_J$	Operating Junction and	-40 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature for 10 seconds	300	
	Mounting Torque, 6-32 or M3 Screw	10lbf·in (1.1N·m)	N

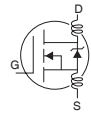
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	0.45*	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted) D²Pak ⑥	—	40	

\*  $R_{\theta JC}$  (end of life) for D²Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	170	—	mV/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	22	26	m $\Omega$	$V_{GS} = 10V, I_D = 46A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-13	—	mV/ $^\circ\text{C}$	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V$
		—	—	200	$\mu A$	$V_{DS} = 200V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	49	—	—	S	$V_{DS} = 25V, I_D = 46A$
$Q_g$	Total Gate Charge	—	70	98	nC	$V_{DD} = 100V, I_D = 46A, V_{GS} = 10V$ ③
$Q_{gd}$	Gate-to-Drain Charge	—	23	—	nC	
$t_{d(on)}$	Turn-On Delay Time	—	33	—	ns	$V_{DD} = 100V, V_{GS} = 10V$ ③ $I_D = 46A$ $R_G = 2.5\Omega$ See Fig. 22
$t_r$	Rise Time	—	20	—		
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		
$t_f$	Fall Time	—	31	—		
$t_{st}$	Shoot Through Blocking Time	100	—	—	ns	$V_{DD} = 160V, V_{GS} = 15V, R_G = 4.7\Omega$
$E_{PULSE}$	Energy per Pulse	—	570	—	$\mu J$	$L = 220\text{nH}, C = 0.4\mu F, V_{GS} = 15V$ $V_{DS} = 160V, R_G = 4.7\Omega, T_J = 25^\circ\text{C}$
		—	910	—		$L = 220\text{nH}, C = 0.4\mu F, V_{GS} = 15V$ $V_{DS} = 160V, R_G = 4.7\Omega, T_J = 100^\circ\text{C}$
$C_{iss}$	Input Capacitance	—	4600	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	460	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	91	—		$f = 1.0\text{MHz},$
$C_{oss\ eff.}$	Effective Output Capacitance	—	360	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 160V$
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		

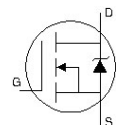


## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	140	mJ
$E_{AR}$	Repetitive Avalanche Energy ①	—	46	mJ
$V_{DS(Avalanche)}$	Repetitive Avalanche Voltage ①	240	—	V
$I_{AS}$	Avalanche Current ②	—	37	A

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	62	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	260		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 46A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}, I_F = 46A, V_{DD} = 50V$
$Q_{rr}$	Reverse Recovery Charge	—	430	640	nC	$di/dt = 100A/\mu s$ ③



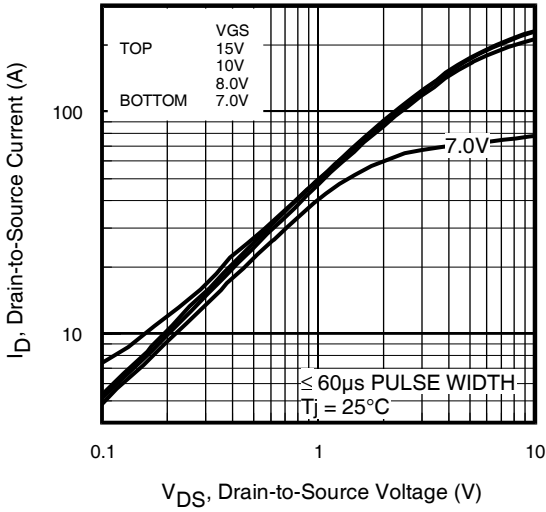


Fig 1. Typical Output Characteristics

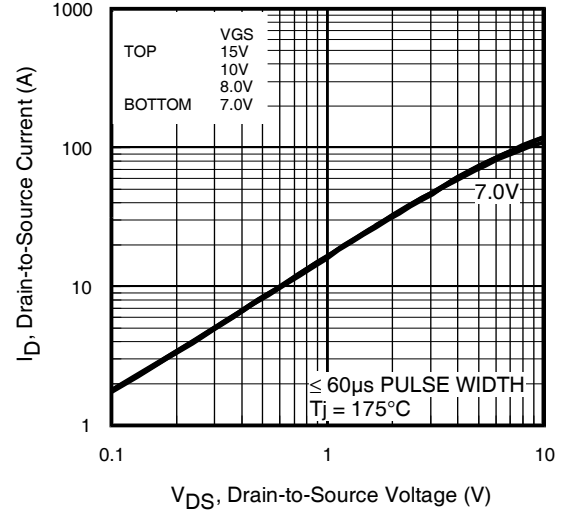


Fig 2. Typical Output Characteristics

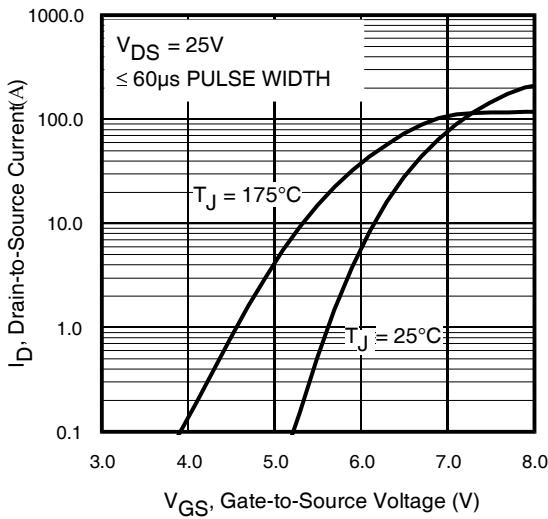


Fig 3. Typical Transfer Characteristics

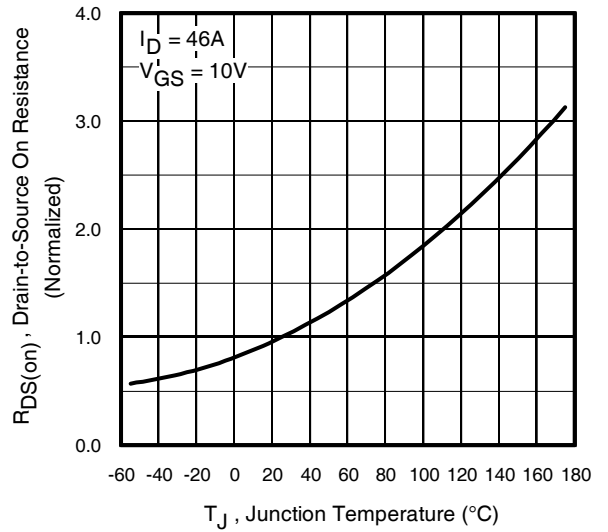


Fig 4. Normalized On-Resistance vs. Temperature

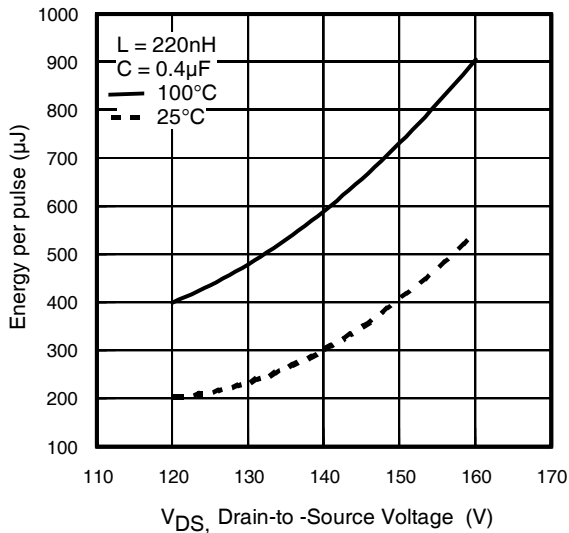


Fig 5. Typical  $E_{PULSE}$  vs. Drain-to-Source Voltage

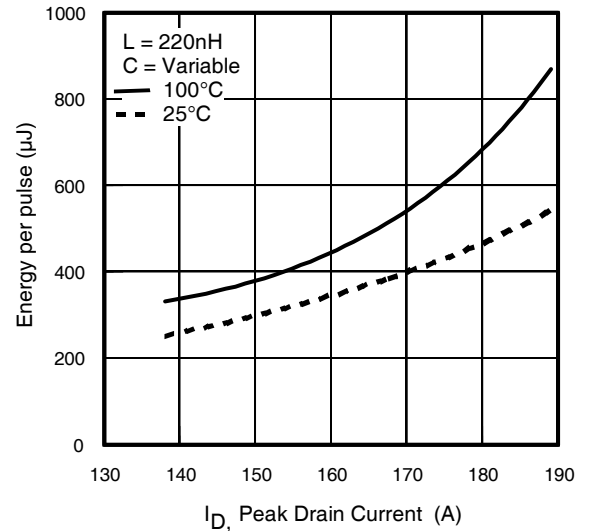
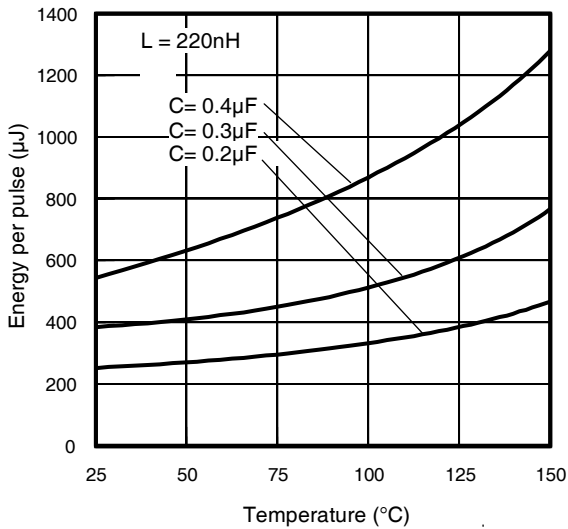
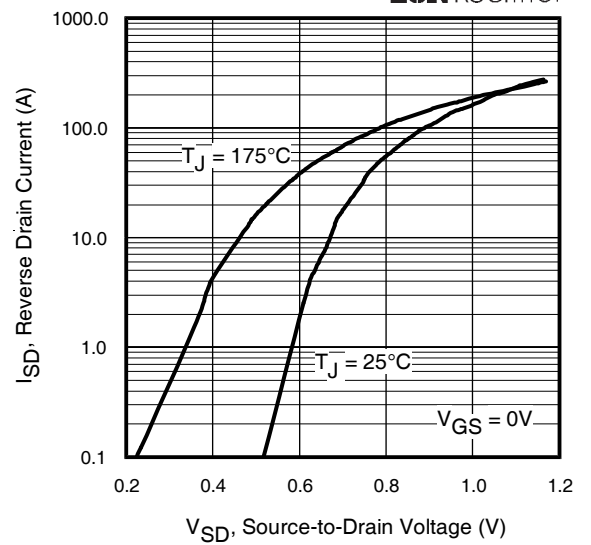


Fig 6. Typical  $E_{PULSE}$  vs. Drain Current

# IRFS/SL4227PbF



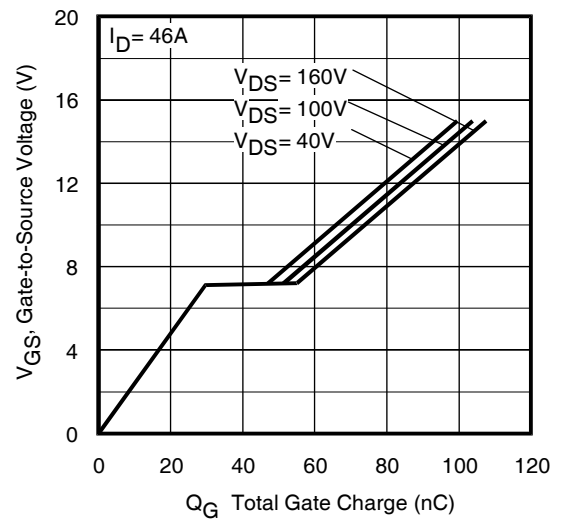
**Fig 7.** Typical  $E_{\text{PULSE}}$  vs. Temperature



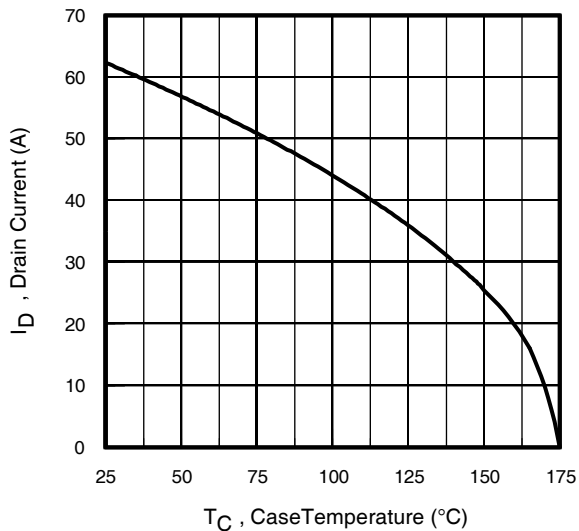
**Fig 8.** Typical Source-Drain Diode Forward Voltage



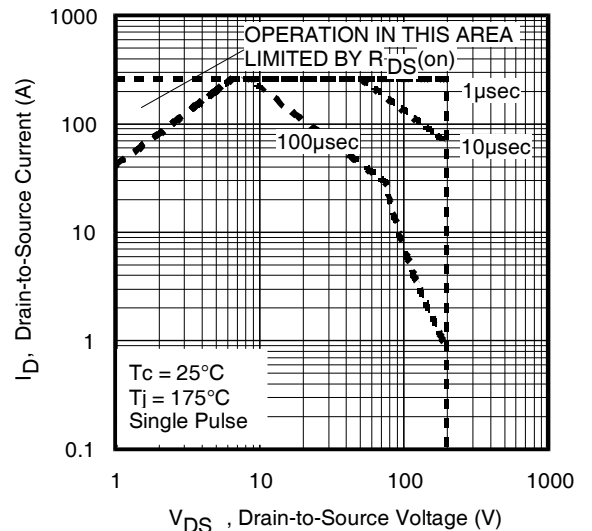
**Fig 9.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



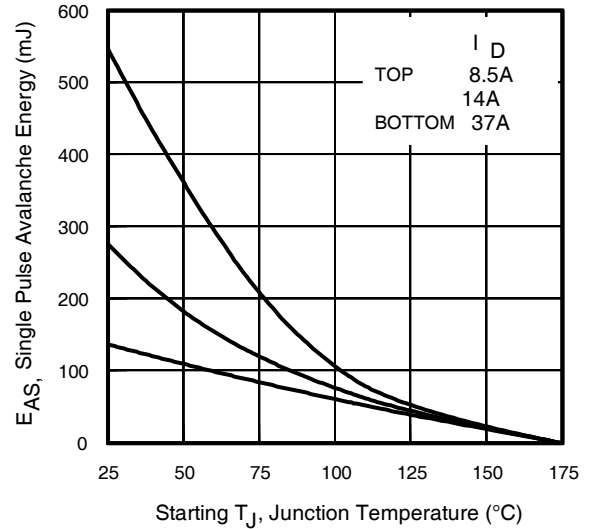
**Fig 11.** Maximum Drain Current vs. Case Temperature



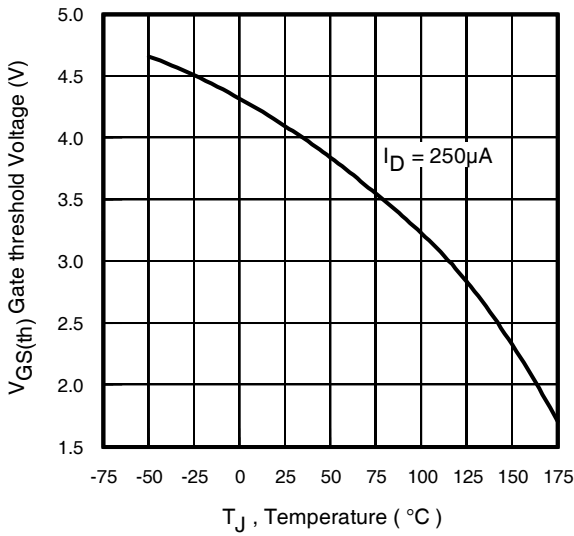
**Fig 12.** Maximum Safe Operating Area



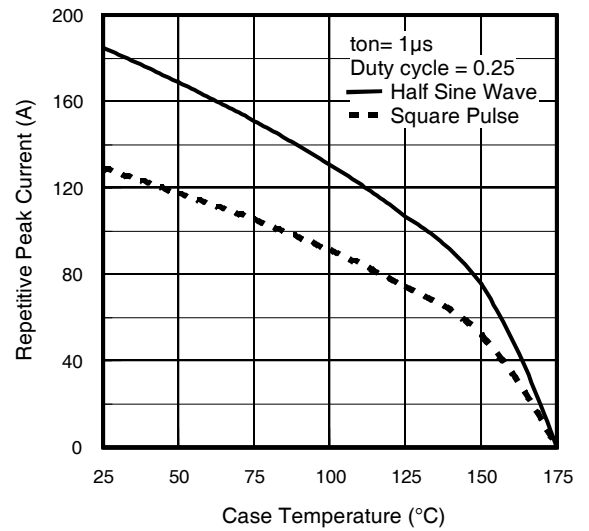
**Fig 13.** On-Resistance Vs. Gate Voltage



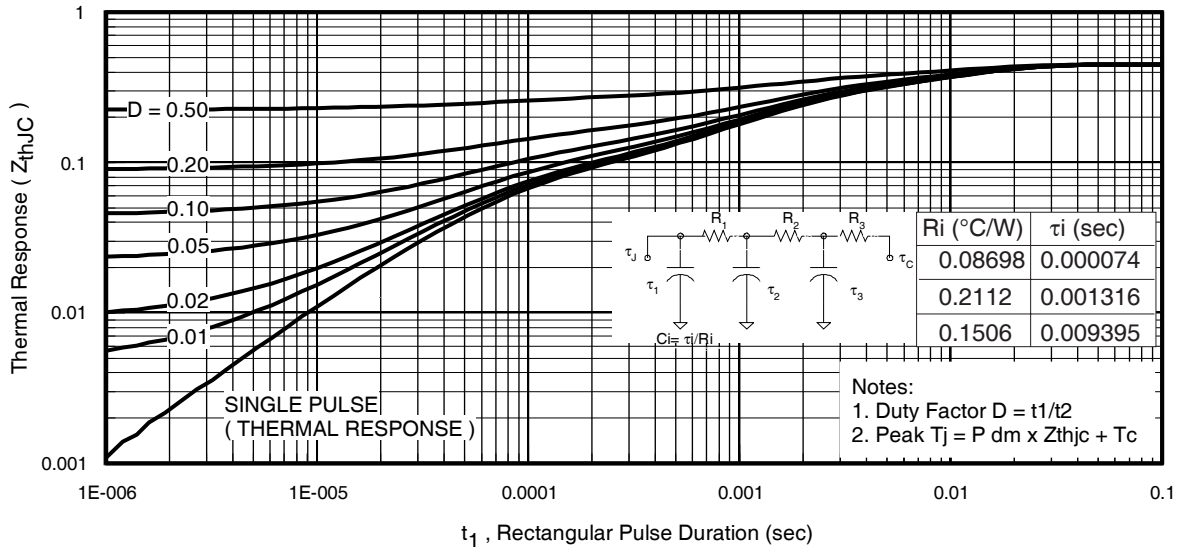
**Fig 14.** Maximum Avalanche Energy Vs. Temperature



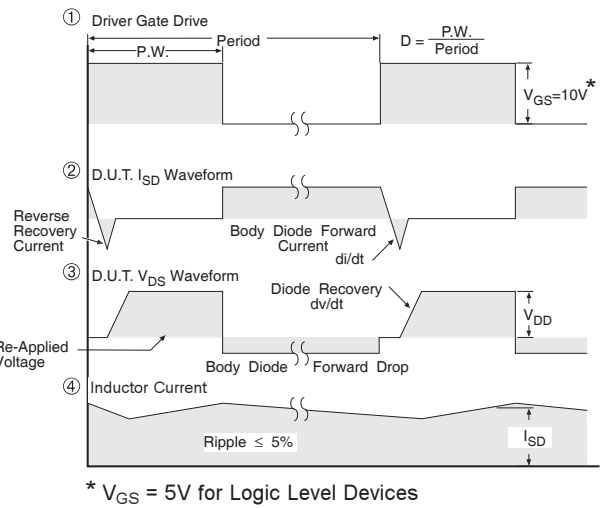
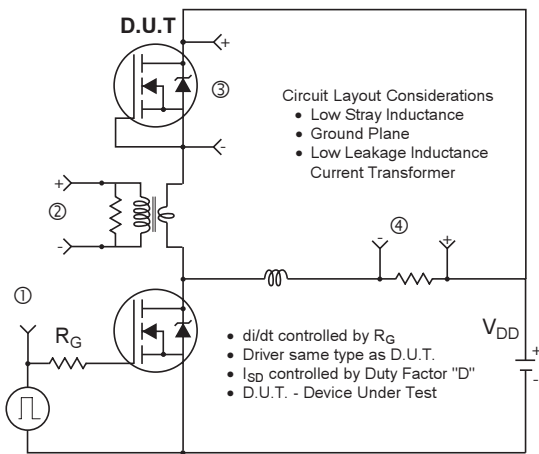
**Fig 15.** Threshold Voltage vs. Temperature



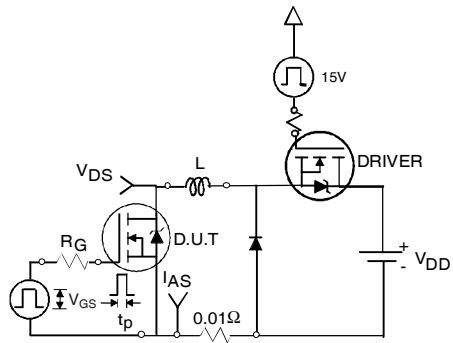
**Fig 16.** Typical Repetitive peak Current vs. Case temperature



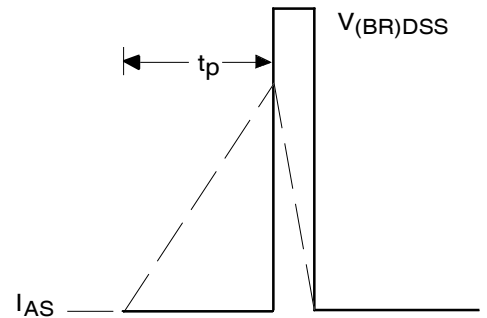
**Fig 17.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



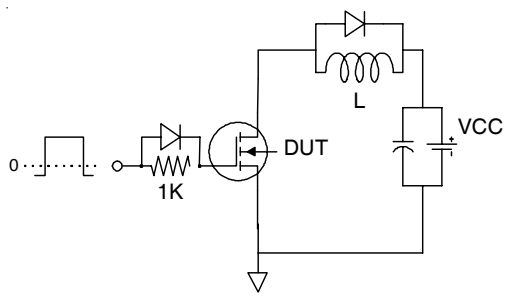
**Fig 18.** Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs



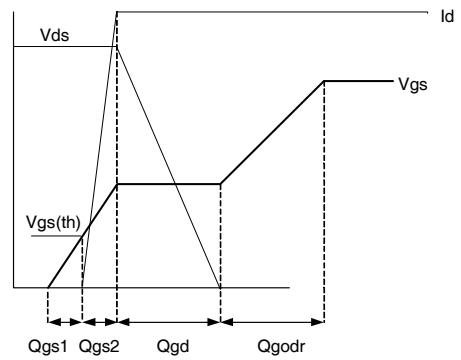
**Fig 19a.** Unclamped Inductive Test Circuit



**Fig 19b.** Unclamped Inductive Waveforms



**Fig 20a.** Gate Charge Test Circuit



**Fig 20b.** Gate Charge Waveform

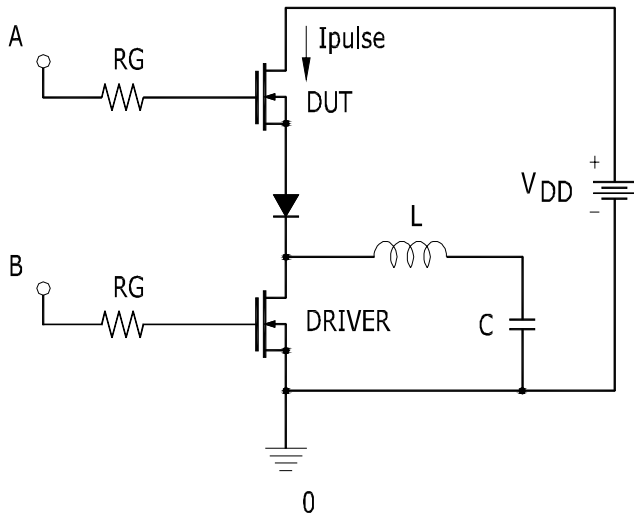


Fig 21a.  $t_{st}$  and  $E_{PULSE}$  Test Circuit

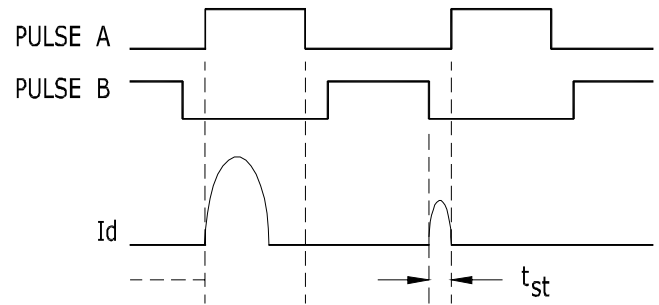


Fig 21b.  $t_{st}$  Test Waveforms

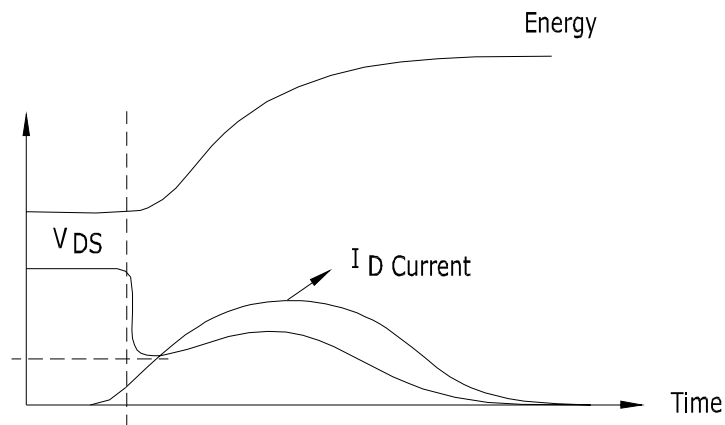


Fig 21c.  $E_{PULSE}$  Test Waveforms

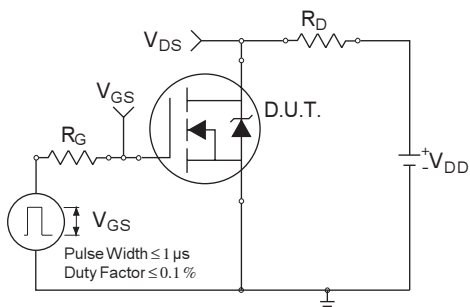


Fig 22a. Switching Time Test Circuit

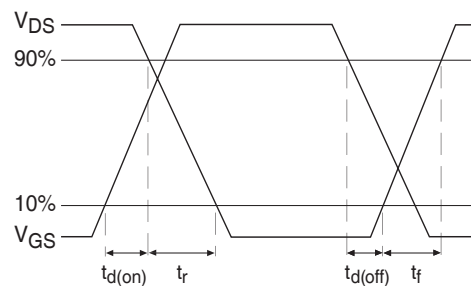
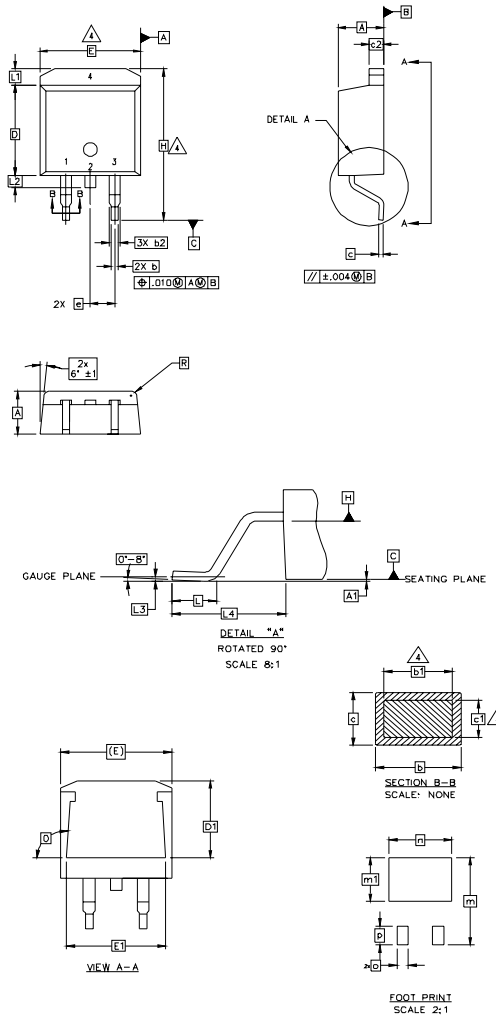


Fig 22b. Switching Time Waveforms

## D<sup>2</sup>Pak Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYM BOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
theta	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

#### IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

#### DIODES

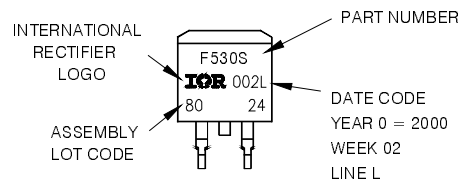
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

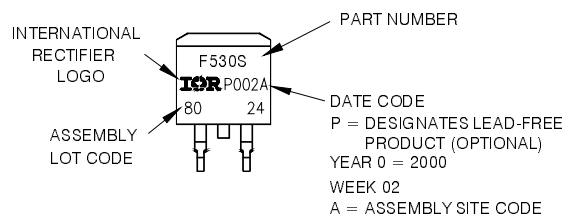
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE 'L'

Note: 'P' in assembly line  
position indicates 'Lead-Free'



OR

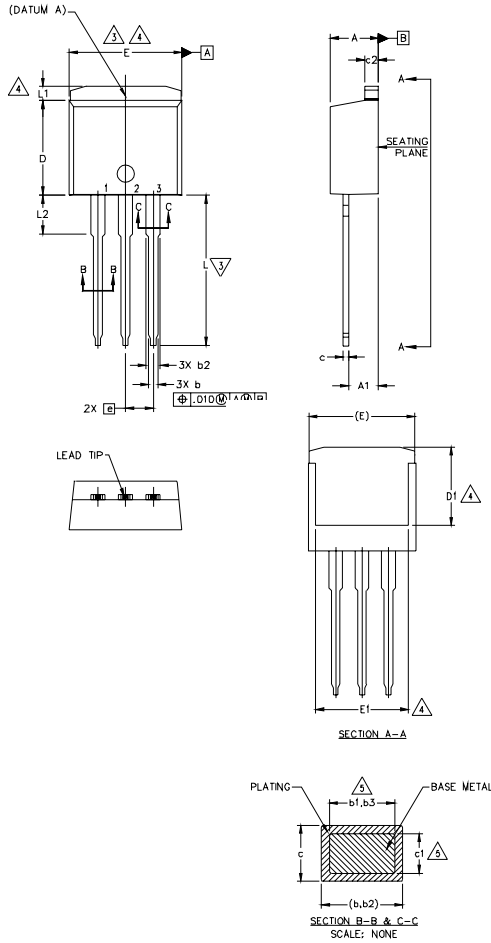


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	4
L1	-	1.65	-	.065	
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

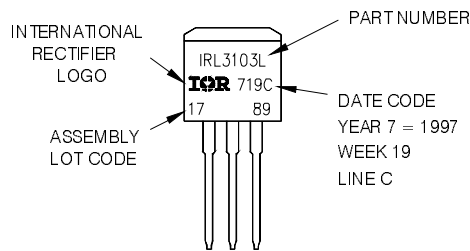
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

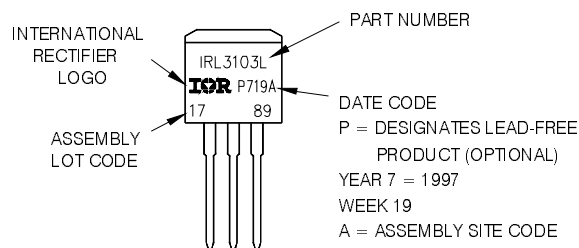
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE 'C'

Note: "P" in assembly line position indicates "Lead - Free"

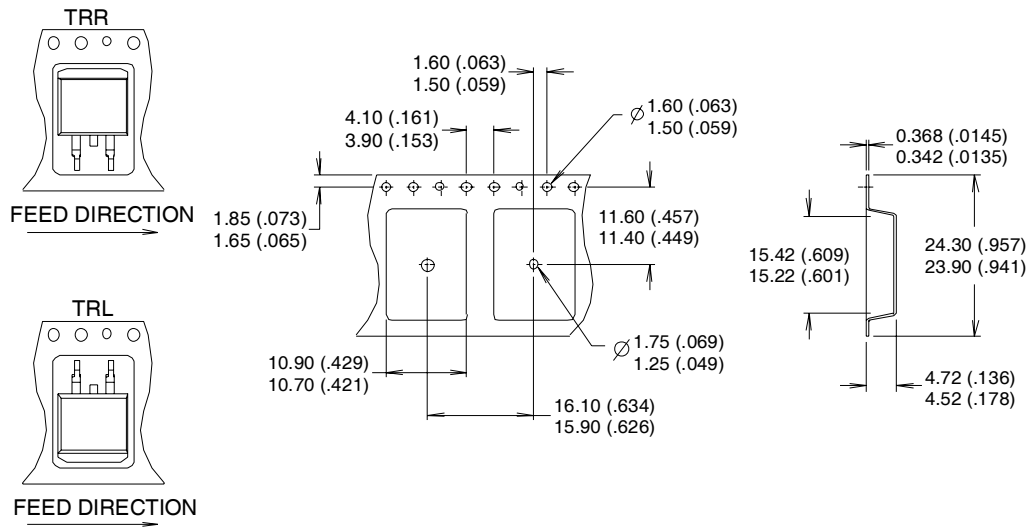


OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## D<sup>2</sup>Pak Tape & Reel Information



- NOTES:
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.2\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 37\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ Half sine wave with duty cycle = 0.25,  $t_{on} = 1\mu\text{sec}$ .
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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